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23 March 1959

HARVEST Memory Configuration Report

This report summarizes a study on the various problems concerning the memory to be used on the HARVEST System.

The original decision on HARVEST memory was to order two boxes of high speed memory (2,048 words), and two boxes of medium speed memory (32,768) to be delivered with the HARVEST System. Additional funds (4 million dollars) were programmed in the fiscal year 1961 budget to provide for doubling this memory capacity. A number of changes have occurred since that time which can greatly affect our original decision. They are:

1. A reduction in the rate of the high speed memory from .5 microseconds to approximately .75 microseconds per repeated access.

2. A.E.C.'s probable decision to order all medium speed memory. This would leave NSA as sole purchaser of high speed memory. IBM has indicated that there is no company interest in this development.

3. Maintenance problems are predicted for high speed memory.

4. We will have a problem in justifying additional memory in FY 1961 if NSA's budget continues to tighten.

5. IBM's ability to produce and install additional medium speed memory with the delivery of the HARVEST System.

The above prompted an investigation into the feasibility of replacing the high speed memory with medium speed memory. A summation of the various memory configurations follows. The times were based on a HARVEST memory bus assumption, made by ANEQ-1, with a synchronized slot time of .25 microseconds, and no memory conflicts. The average random access times were computed on a stream length of 8 characters.

	CONFIGURATION 1	CONFIGURATION 2	
	4 Boxes 2.25 microseconds	2 Boxes .75 microseconds	2 Boxes 2.25 microseconds
Number of words	65,536	2,048	32,768
Single access	1.5 microseconds	1.25 microseconds	1.5 microseconds
Repeated access	2.25	.75	2.25
Average time for Sequential access	.563	.375	1.125
Average time for Random access	1.0	.48	1.43
Average time for Count in memory	1.0	.636	1.43
Average time for Existence in memory	1.0	.636	1.43

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A definition of single access for medium speed memory is where sucessive accesses to a memory box occur at an interval exceeding the memory rate. On high-speed memory, the single access time is used for the first reference following an idle interval of 1.25 microseconds.

Repetitive access time is used when sucessive references to the same memory box occur at an interval less than the memory rate. On some problems this can be eliminated by duplication of the memory area into all boxes. This approach is made much easier when memory can be spared. By duplicating and using the memory distributor, sequential accessing may be performed.

The stream unit is capable of a .25 microsecond byte rate (8 bits) on a logic unit operation involving two input streams and one output stream. The source of the input data and the storage of the output is normally in medium speed memory. The size of high speed memory limits its use for data streams. The following table indicates the possible byte rate, assuming stream register memory conflicts only, for the memory configurations under consideration.

Character Representation	Byte Rates 4 Boxes 2.25 FASTEST	AVERAGE	Byte Rates 2 Boxes 2.25 FASTEST	AVERAGE
8 Bits	.30 microseconds	.39 microseconds	.42 microsec.	.46 microsec.
6 Bits	.23 microseconds	.29 microseconds	.32 microsec.	.35 microsec.
4 Bits	.15 microseconds	.19 microseconds	.21 microsec.	.23 microsec.
1 Bit	.04 microseconds	.05 microseconds	.05 microsec.	.06 microsec.

The fastest rate can be obtained when the programmer controls the starting address of each stream.

A comparison of the two memory configurations can be made based on an 8 hour shift of a HARVEST System having two boxes of fast memory and 4 boxes of medium speed memory.

A new memory configuration is brought in at this time, because it contains the best features of both configurations under question. This allows a fixed base from which to measure the other two configurations.

We will assume that a typical operation shift would break down as follows:

1. 10% Basic computer mode.
2. 50% Stream logic operation (sorting, differencing etc.)
3. 30% Sequential table look up (wired rotor, etc.)
4. 5% Random table look up (decode, etc.)
5. 5% Count or existence look up (frequency dist.)

The processing times for this workload are as follows:

	2 FAST - 4 MEDIUM	2 FAST - 2 MEDIUM	Ø FAST - 4 MEDIUM
Basic Computer	.80	.90	.80
Logic OP	4.00	4.72	4.00
Sequential Lookup	2.40	2.40	3.36
Random Lookup	.40	.57	.40
Count	.40	.40	.63
	8.00 Hours	8.99 Hours	9.19 Hours

If the fast memory repeated access time exceeds .75 microseconds and has to be made a 1 microsecond access, the times above for the first two cases would stay constant, while the Ø-4 case would be reduced to 8.53.

The count in memory feature is not on medium speed memory. This requirement would require some reengineering, but could be added without changing the 2.25 rate.

There are other immeasurable factors that affect the above evaluation. The access time to HARVEST indexing levels slows down streaming when the indexing levels are stored in medium speed memory. Memory conflicts due to input-output functions occur twice as often when only two boxes of medium speed memory are available.

This study points out that the two configurations are approximately equal in speed. However, the Ø fast-4 medium configuration would give us 30,720 additional words of memory. The medium speed memory is a commercial item minus the special memory features. This is an indication of the reliability that can be expected. There is an indication of a speed improvement in medium speed memory (2.0 microseconds) while fast memory seems to be heading in the opposite direction.

Further references and abstracts are included here to complete the study.

HARVEST Status Memo # 2 1 March 1959

FAST MEMORY

The Fast Memory program has been under review with the intent of formulating a more intensive effort. The new program is in terms of having both Fast Memory units tested and available by March, 1960. This program was discussed in detail with Mr. F. Dunham and will not be repeated here. It is sufficiently compact that the next reporting period (March, April) should be of considerable interest.

SUPPLEMENTARY MEMORY BUS

A memory bus design suitable for HARVEST presents two fundamental problems not found in the Basic system alone. The first arises because the cycle times of Basic and HARVEST are different, i.e. 200 and 250 millimicroseconds respectively. In turn the memory bus must be run at one or the other of the two rates, or else the two rates might be made equal.

This latter possibility is unlikely because Basic should not be slowed down on the one hand and HARVEST cannot be speeded up, on the other hand without increasing stream segmentation to a point there most adjustments become impossible. Present thinking is in terms of a bus system run at the HARVEST rate, with checking done in series with the bus operation rather then the re-entrant method employed in Basic. (Ref. Harvest File Memo #12, Appendix #2.) Some time will be lost in establishing synchronism between arithmetic mode operations and the bus, though the look-ahead mechanism may compensate wholly or in part.

The second problem concerns the treatment of Fast Memory, for which the delays inherent in the geneal bus seem too great. Present thinking is in terms of a direct connection between Fast Memory and the Table Reference Unit, with the general bus entering in a less direct way to preserve the common addressability of all memory.

It should be noted that bus delay does not affect the rate of Fast Memory, only the individual access time. The need for minimum bus delay depends very much on the relative weight given to multiple look-up operations.

The Sigma memory bus is described in Sigma Computer memo #20.

The following ANEQ memo is by the project engineer assigned to HARVEST memory. See attached memo (copy).

The following actions are recommended in order to resolve the question on high speed memory:

1) Request ANEQ-1 to perform an engineering evaluation study, based on the recently completed feasibility to determine the answers to the following:

   a. Ability to produce on schedule.
   b. Reliability of components to be used in construction.
   c. Maintenance considerations.
   d. Speed.

2) MPRO discussion of the problem.

3) MPRO - ANEQ discussion on contract problems and results of engineering evaluation. This should be scheduled for the first week of April.

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MPRO-03