15 October 1959

HARVEST PROGRAMMING

The following statements are presented either to clarify a point, or record a change in specifications:

1. Gate configuration 1, 3, 4 is illeagal.

2. The byte mask on R will not effect the bytes read out from SACC and SCTR. The programmer must supply the R indexing.

3. The match operations are:

   0 No op
   1 Swallow both LU inputs and insert match
   2 Swallow connected byte
   3 Swallow all connected inputs
   4 Swallow both Lu inputs and insert match, KB = 1

4. Match units W, X, Y and Z will have a span bit.

5. The Memory distributor bit will cause address shifting and accessing to two fast Memories or four Large Memories. The Bus will access the memory frame that is available. The Memory distributor counter has been removed.

6. The coding for the control byte on the STIR hybrid instruction depends on the internal character coding used. If the character set on page 7.28 of the Sigma Manual is accepted, the 2-3 bit (01) of character D (delete) will stand for the take option, and the 2-3 bits (10) of character R (replace) will stand for the replace option. Bits (00) will stand for insert.

7. All Index Flags will be monitored during advance and run out adjustments.

8. When the last byte from a reading level causes a reset adjustment, the index flag stimulus on that level can not be inhibited. All other flags occuring during the execution of the reset adjustment will be inhibited.

9. If, during the execution of a run out adjustment, a stimulus of higher priority occurs the run out adjustment is suspended and control is transferred to the higher priority adjustment. Adjustments in the half word to the right of the run out will be lost. Lower priority adjustments will be saved and executed at the completion of the run out of the higher priority adjustment. If the run out appears in the first half word of a chain, and interrupt occurs, the second half word is also lost.

10. The offset is applied to the R address prior to moving data on the SQNL hybrid. An N value of Ø indicates no data. If possible, an offset value of Ø will not cause a data fetch on Q or R. Level 1 indexing will appear as follows when offsets ≠ Ø are present: N/O = 1, Large N.

11. SCTR is no longer addressable via P indexing. It is now on the logic unit slide. It may be used as an input to T by opening gates 7 and 6. The low order 8 bits are sent to T.

12. The special byte causing an adjustment will be processed prior to adjustment in some cases. An example of this would be when F_1P initiates the adjustment "add SCTR to TBA". The special byte would form its address with the contents of TBA prior to addition. In short, any sink will process the byte at 1S3 prior to adjustments on that sink.

13. Valid byte and gating is monitored prior to allowing an adjustment stimulus to occur. This insures the result from the special byte causing the stimulus is at 1S3 prior to the execution of adjustments.

14. When a single stream is gated to the logic unit the alternate stream is interpreted as zero. When resuming a stream after changing to a single stream gating configuration, the first byte submitted from the other stream could be anything.

15. During run out no logic unit signals occur.

16. The run out and match only bits are ignored on nested levels.

17. The runout, match only, read, priorities are as follows:

a) runout or match only always precede read
b) P stream runs out prior to Q
c) match only may occur simultaneously with a runout match or another match only.

The gate may be closed if a stream is only running out or matching.

18. The TBA dictates which memory is to be used during a table lookup operation. A lookup address outside the bounds of the memory in use causes an error type interrupt. When TAM mode 001 is used the interrupt is inhibited.

19. The memories will not wraparound.

20. The debug scan will send the 3000 maintenance indicators to memory. Some method of entering thru the basic exchange will be used. The programmer must supply the locate instruction and control word.

21. Flags may be "ANDED" on chaining. They occur at different times normally.

22. The adjustment validity checker can be justified for its ability to prove machine performance. The HAP I and II should also test these conditions.

23. The and tag on the adjustment half word causes the following reaction conditions:

a) sequential stimuli one and two causes 6 reactions.
b) stimulus two only, causes stimulus two reactions.
c) stimulus one only, no reaction.
d) one adjustment cycle is used on the half and.

24. EOG can not come from MSL. Index flags causing EOG must be on a reading level.

25. The ØØ case on K will be considered cell size 8.

26. Flag 3 will be used for all collating hybrid breakpoints. EOG will be used for all table lookup hybrid breakpoints..

27. CC = Ø will always cause a stop. This signal is never inhibited.

28. Gates 9 and 11 have been added to the SILS hybrid instruction.

29. Gates 10 and 12 have been added to the SQNL hybrid instruction.

30. R is not reset to Ø on RC mode Ø. Skip space in R adjustment or a half word store will leave junk in R. This prohibits the use of R for formatting records for printing when RC= Ø.

31. Level 1 Q/R on the SILS hybrid instruction will have a SR value of 1. This allows transfer of the address to Q/R without taking a level 2 increment when N is large and EOG is a match.

32. Triangular indexing should not be used on 2nd level or higher level reading levels. The parameters are not stored and the next iteration after EOL would have the original N value.

33. P, Q indexing parameters are always fetched. SP, SQ data is always fetched. Care must be taken in setting up, so that invalid conditions don't occur.

34. The MD bit will have no effect when TAM sets the T unit to form addresses only.

35. The R unit stores at EOL_1.

36. The following functions were deleated 7 October 1959. They presented engineering problems, either due to space, speed or implementation:

a) U Adjustments: reset, repeat, match only.
b) T Adjustment: Reference TBA-1 and Increment.
c) Adjustment Stimuli: SCTR steps, EOG.
d) Hybrid Instruction: SMLU
e) Logic Unit Options: parallel double 4 bit addition, carry propagate, gate 7 KLM outputs.
f) Functions in base computer: Half word Transmit, Spray, Indirect Addressing using HARVEST Index units.

Joseph E. O'Hara

JOSEPH E. O'HARA
MPRO-03