Generating Voltage Drop Aware Current Budgets for RC Power Grids

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***Abstract*—Efficient verification of the chip power distribution network is a critical task in modern chip design. It should be done early in the design process where adjustments can be most easily incorporated. As an alternative to simulation based methods, vectorless verification is a class of techniques that requires user-specified current constraints (budgets), and checks if the corresponding worst-case voltage drops at all grid nodes are below user-specified thresholds. However, obtaining/specifying the current constraints remains a burdensome task for users. Recent literature has addressed the constraints generation problem by proposing the *inverse* problem: for a given grid, we would like to *generate* circuit current constraints which, if adhered to by the underlying logic, would guarantee grid safety. In this paper, we adopt the same framework. We develop an efficient algorithm for constraints generation that targets a key grid quality metric namely the uniformity of temperature distribution across the die area.**

I. Introduction

The rising demand for low-voltage integrated circuits (ICs) design has made the power and ground networks susceptible to the flow of large switching currents, causing excessive supply voltage variations that put both circuit performance and reliability at risk. A well-designed chip power/ground network should deliver well-regulated voltages at all grid nodes in order to guarantee correct logic functionality at the intended design speed. Therefore, efficient verification of power grids is a necessity in modern chip design. We will use the term *power grid* to refer to either the power or ground distribution networks.

Today, power grid verification is done using simulation-based methods. These methods determine the voltage drop at every node by simulating the grid over a large set of current waveforms in order to cover most typical scenarios and guarantee power grid integrity. A major drawback of these methods is that they do not allow early verification as they rely on the complete knowledge of the circuit design. As an alternative to simulation-based methods, the authors in [1] proposed a verification scheme, referred to as a *vectorless* approach, that deals with circuit uncertainty in the form of *current constraints* or *current budgets*. This information may be available at an early stage of the design and thus allows for early verification of the grid. Under such framework, the grid is said to be *safe* if it satisfies the voltage drop requirements at all grid nodes under all possible transient current waveforms that satisfy user-specified current constraints. These methods require the user to obtain/specify the current constraints which remains a burdensome task and a hurdle to adoption of the vectorless approach.

Instead of the traditional *vectorless* approach that expects the users to provide current constraints that would be used to check if the grid is safe (what one might call the *forward* problem), the authors in [2] proposed the *inverse* problem: given a grid and the allowed voltage drop thresholds at all grid nodes, we would like to *generate* circuit current constraints which, if satisfied by the underlying circuitry, would guarantee grid safety. Furthermore, the authors developed two constraints generation algorithms targeting key grid quality metrics such as: the peak power dissipation a grid can safely support and the uniformity of current distribution across the die area. In [3], the authors presented a different formulation of the same algorithms as in [2] achieving a significant speedup along with a third algorithm that combines the above two design objectives. However, the proposed algorithms are not scalable for typical grids. In this paper, we propose a novel algorithm for targeting the uniformity of current distribution. We then provide a comparison between the proposed algorithm and the uniform current distribution approach developed in [2] and [3].

II. Power Grid Model

Consider an RC model of the power grid, where each branch is represented by a resistor and where there exists a capacitor from every node to ground. Some nodes have ideal current sources (to ground) representing the currents drawn by the logic circuits tied to the grid at these nodes, while other nodes may be connected to ideal voltage sources representing the connection to the external voltage supply V_{dd}. Let the power grid consist of n non-V_{dd} nodes out of which $m \leq n$ nodes are connected to ideal current sources. Without loss of generality, suppose that nodes attached to current sources are numbered $1, \ldots, m$, where $m \leq n$. Let $H = [I_m \quad 0]^T$ be an $n \times m$ matrix where I_m is the m-dimensional identity matrix, and let $i_s(t) = Hi(t)$. Nodal Analysis [4] can be used to construct the system model [1] for the power grid:

$$Gv(t) + C\dot{v}(t) = i_s(t) \tag{1}$$

where $v(t)$ is the $n \times 1$ vector of time-varying voltage drops (difference between V_{dd} and true node voltages); C is the $n \times n$ *diagonal* non-negative capacitance matrix, which is non-singular because every node is attached to a capacitor; G is the $n \times n$ conductance matrix, which is known to be symmetric and *irreducibly diagonally dominant* $\mathcal{M}$-matrix so that G is non-singular and $G^{-1} > 0$ [2].

Using a finite-difference approximation for the derivative, such as a Backward Euler numerical integration scheme $\dot{v}(t) \approx (v(t) - v(t - \Delta t))/\Delta t$, the grid system model (1) leads to:

$$v(t) = A^{-1}Bv(t - \Delta t) + A^{-1}i_s(t) \tag{2}$$

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where $B = C/\Delta t$ is an $n \times n$ diagonal matrix with $b_{ii} > 0$, $\forall i$, and $A = G + B$. Just like G, A can be shown to be non-singular with $A^{-1} > 0$ [2]. Let $M = A^{-1} > 0$ and define the $n \times m$ matrix $M' = MH > 0$.

Finally, we assume that a certain number of grid nodes $d \leq n$ are required to satisfy some user-provided *voltage drop threshold specifications*, captured in the $d \times 1$ vector $V_{th} \geq 0$. These would typically be nodes at the lower metal layers, where the chip circuitry is connected. Let P be a $d \times n$ matrix consisting of 0 and 1 elements only, specifying (with a 1 entry) the nodes that are subject to voltage threshold specification. Note that $P \geq 0$ and P has exactly one 1 entry in every row, otherwise 0s, and that no column of P has more than one 1.

III. Preliminaries

In this section, we will review the terminology and major theoretical results that were introduced in [2] and are crucial to our work.

A. Safe Containers

The following definition introduces the notion of a *container* for a vector of current waveforms, which will help us to express constraints that guarantee grid safety.

Definition 1. (Container) *Let $t \in \mathbb{R}$, let $i(t) \in \mathbb{R}^m$ be a bounded function of time, and let $\mathcal{F} \subset \mathbb{R}^m$ be a closed subset of $\mathbb{R}^m$. If $i(t) \in \mathcal{F}$, $\forall t \in \mathbb{R}$, then we say that $\mathcal{F}$ contains $i(t)$, represented by the shorthand $i(t) \subset \mathcal{F}$, and we refer to $\mathcal{F}$ as a container of $i(t)$.*

Definition 2. (Safe Grid) *A grid is said to be* safe *for a given $i(t)$, defined $\forall t \in \mathbb{R}$, if the resulting $Pv(t) \leq V_{th}$, $\forall t \in \mathbb{R}$.*

To check if a power grid is safe, one would typically be interested in the worst-case voltage drop at some grid node k, at some time point $\tau \in \mathbb{R}$, over a wide range of possible current waveforms. Using the above notation, and given a container $\mathcal{F}$ that contains a wide range of current waveforms that are of interest, we can express this as $\max_{i(t) \subset \mathcal{F}}(v_k(\tau))$. Clearly, because $\mathcal{F}$ is the same irrespective of time, and applies at all time points $t \in \mathbb{R}$, then this worst-case voltage drop must be time-invariant, independent of the chosen time point τ. Therefore, one way to check node safety is to compute the worst-case voltage drop attained by each component of $v(t)$, denoted as $v^*(\mathcal{F}) = \operatorname{emax}_{i(t) \subset \mathcal{F}}(v(\tau))$ where the "$\operatorname{emax}(\cdot)$" notation denotes *element-wise* maximization, as in [2]. In [5], the authors derived an exact expression for the worst-case voltage drop $v^*(\mathcal{F})$ that requires an infinite sum of $\operatorname{emax}(\cdot)$ operations. Thus, relying on $v^*(\mathcal{F})$ is prohibitively expensive and so we will use an upper-bound on $v^*(\mathcal{F})$ based on the following.

Definition 3. *For any $\mathcal{F} \subset \mathbb{R}^m$, define:*

$$\overline{v}(\mathcal{F}) \triangleq G^{-1} A \operatorname*{emax}_{I \in \mathcal{F}} (M'I) \tag{3}$$

where $I \in \mathbb{R}^m$ is a vector of artificial variables, with units of current, that is used to carry out the $\operatorname{emax}(\cdot)$ operation, with the convention that $\operatorname{emax}_{I \in \mathcal{F}} (M'I) = 0$, if $\mathcal{F} = \phi$.

In [5], the authors have derived the following upper-bound on $v^*(\mathcal{F})$:

$$v^*(\mathcal{F}) \leq \overline{v}(\mathcal{F}) \tag{4}$$

Furthermore, in [5], the authors investigate the accuracy of this upper-bound which was found to be quite good (recent tests show a maximum error of 4mV on a 5K node grid).

Definition 4. (Safe Container) *For a given container $\mathcal{F}$, we say that $\mathcal{F}$ is* safe *if $P\overline{v}(\mathcal{F}) \leq V_{th}$.*

Thus, we are interested to discover a container $\mathcal{F}$ for which $P\overline{v}(\mathcal{F}) \leq V_{th}$, so that $Pv^*(\mathcal{F}) \leq V_{th}$ and the grid is safe. A safe container $\mathcal{F}$ can be expressed as a set of constraints on the circuit currents that load the grid, thereby providing a set of linear constraints that are sufficient to guarantee grid safety.

B. Maximal Containers

Let $u \in \mathbb{R}^n$ and define the sets $\mathcal{U}$, $\mathcal{F}(u)$, and $\mathcal{S}$ as follows:

$$\mathcal{U} \triangleq \{u \in \mathbb{R}^n : u \geq 0, Pu \leq V_{th}\} \tag{5}$$

$$\mathcal{F}(u) \triangleq \{I \in \mathbb{R}^m : I \geq 0,\ M'I \leq MGu\} \tag{6}$$

$$\mathcal{S} \triangleq \{\mathcal{F}(u) : u \in \mathcal{U}\} \tag{7}$$

Because $i(t) \geq 0$ is already assumed in our grid model, it is enough to consider only containers of the form (6), due to the following *necessary and sufficient condition*.

Lemma 1. [2] *A container $\mathcal{J} \subset \mathbb{R}^m_+$ is safe if and only if it is a member of $\mathcal{S}$ or a subset of a member of $\mathcal{S}$.*

The importance of the above lemma is two-fold: 1) $\mathcal{F}(u)$ is safe for any $u \in \mathcal{U}$ and 2) all interesting safe containers $\mathcal{J}$ may be found as either specific $\mathcal{F}(u)$ for some $u \in \mathcal{U}$, or as subsets of such $\mathcal{F}(u)$. Note that, if $\mathcal{J} \subseteq \mathcal{F}(u)$, for some $u \in \mathcal{U}$, with $\mathcal{J} \neq \mathcal{F}(u)$, then clearly $\mathcal{F}(u)$ is a better choice than $\mathcal{J}$. Choosing $\mathcal{J}$ would be unnecessarily limiting, while $\mathcal{F}(u)$ would allow more flexibility in the circuit loading currents. Therefore, it is enough to consider *only* containers of the form $\mathcal{F}(u)$ with $u \in \mathcal{U}$.

Going further, if $\mathcal{F}(u_1) \subseteq \mathcal{F}(u_2)$ with $\mathcal{F}(u_1) \neq \mathcal{F}(u_2)$, then clearly $\mathcal{F}(u_2)$ is a better choice than $\mathcal{F}(u_1)$. Thus, in a sense, the "larger" the container, the better. Therefore, we are interested in safe containers that are not fully contained in any other safe container. We refer to such containers as *maximal*.

IV. Algorithms

In this section, we present an algorithm that targets the uniformity of current distribution across the die area. This algorithm will lead us to find a specific safe maximal container. An algorithm that targets the same design objective was developed in [2] and [3]. As we will see in Section V, our proposed algorithm achieves a significant runtime advantage over [2] and [3].

A. Uniform Current Distribution

The design team may be interested in a grid that safely supports a uniform current distribution across the die, so as to allow a placement that provides a uniform temperature distribution. We can generate constraints that allow that objective by searching for a safe maximal container $\mathcal{F}(u)$ that contains the hypercube in current space that has the largest volume, or the largest edge length L. We will develop a method (10) which, when applied to the simple grid in Fig. 1, generates the container $\mathcal{F}(u_l)$ shown in Fig. 1, where $u_l = [27\ 43\ 36\ 38]^T$ (units of mV). The method proposed

in [2] and [3] generates the container $\mathcal{F}(u_s)$ shown in Fig. 1, where $u_s = [26\ 43\ 36\ 37]^T$ (units of mV). Notice that both containers allow similar current distribution between $i_1(t)$ and $i_2(t)$ and thus provide similar features for the design team.

Let $C(L) \subset \mathbb{R}^m$ denote the hypercube with edge length L, i.e. $C(L) = \{I : 0 \leq I \leq L\mathbb{1}_m\}$, where $\mathbb{1}_m$ is an $m \times 1$ vector whose every entry is 1. We are interested in a non-empty $\mathcal{F}(u)$ such that $C(L) \subseteq \mathcal{F}(u)$. Let $\eta = M'\mathbb{1}_m \geq 0$, because $M' \geq 0$. In the following lemma, we will derive a necessary and sufficient algebraic condition for which $C(L) \subseteq \mathcal{F}(u)$ - this will be useful to solve (8).

Lemma 2. *For any $L \geq 0$ and $u \in \mathbb{R}^n$, $C(L) \subseteq \mathcal{F}(u)$ if and only if $L\eta \leq MGu$.*

Proof: To prove the "if direction," let $I \in C(L)$, i.e. $0 \leq I \leq L\mathbb{1}_m$, so that $0 \leq M'I \leq LM'\mathbb{1}_m = L\eta$, due to $M' > 0$. Therefore, we have $M'I \leq L\eta \leq MGu$ and $I \geq 0$, so that $I \in \mathcal{F}(u)$. Conversely, let $I = L\mathbb{1}_m$ and notice that $I \in C(L)$, so that $I \in \mathcal{F}(u)$. Therefore, $M'I = LM'\mathbb{1}_m = L\eta \leq MGu$, and the proof is complete. ■

For any $u \in \mathcal{U}$, we define $l(u)$ to be the largest $L \geq 0$ for which $C(L) \subseteq \mathcal{F}(u)$, or equivalently, for which $L\eta \leq MGu$ is satisfied, so that:

$$l(u) \triangleq \max_{C(L) \subseteq \mathcal{F}(u)} (L) = \max_{0 \leq L\eta \leq MGu} (L) \tag{8}$$

and we define L^* to be the largest $l(u)$ achievable over all possible $u \in \mathcal{U}$, i.e.:

$$L^* \triangleq \max_{u \in \mathcal{U}} (l(u)) \tag{9}$$

Let u_l be a vector at which the above maximization attains its maximum. In other words, $u_l \in \mathcal{U}$ is such that $l(u_l) = L^*$ and $C(L^*) \subseteq \mathcal{F}(u_l)$. In general, u_l may not be unique. We can express the combined (8) and (9) as the following linear program (LP):

$$\begin{aligned} L^* = \quad & \text{Maximize} && L \\ & \text{subject to} && \begin{array}{ll} L\eta \leq MGu, & Pu \leq V_{th}, \\ L \geq 0, & u \geq 0 \end{array} \end{aligned} \tag{10}$$

Let $\mathcal{T}$ be the feasible region of the LP (10):

$$\mathcal{T} \triangleq \{(L, u) : L \geq 0, u \geq 0, L\eta \leq MGu, Pu \leq V_{th}\} \tag{11}$$

so that, from the above, we have:

$$L^* = \max_{(L,u) \in \mathcal{T}} (L) \tag{12}$$

Notice that, $(0, 0) \in \mathcal{T}$ so that $\mathcal{T}$ is not empty and L^* and u_l are well-defined. Also, for every $(L, u) \in \mathcal{T}$, we have $L\eta \leq MGu$ and $L \geq 0$. Because $\eta \geq 0$, it follows that $0 \leq L\eta \leq MGu$ so that u is *feasible* [2] meaning that the container $\mathcal{F}(u_l) = \{I \in \mathbb{R}^m : I \geq 0, M'I \leq MGu_l\} \neq \phi$. Therefore, $\mathcal{F}(u_l)$ provides the desired current constraints:

$$\begin{aligned} i(t) \geq 0, \quad \forall t \in \mathbb{R} \\ M'i(t) \leq MGu_l, \quad \forall t \in \mathbb{R} \end{aligned}$$

It can be shown that $\mathcal{F}(u_l)$ is maximal[1].

The importance of the following lemma is two-fold. First, it simplifies the LP (10) into (18) achieving a significant speedup. Second, it shows that, after solving for u_l, the resulting $\mathcal{F}(u_l)$ can be represented using only m rows of $M'I \leq MGu_l$, based on a lemma proved in [3].

[1]The proof is omitted due to lack of space.

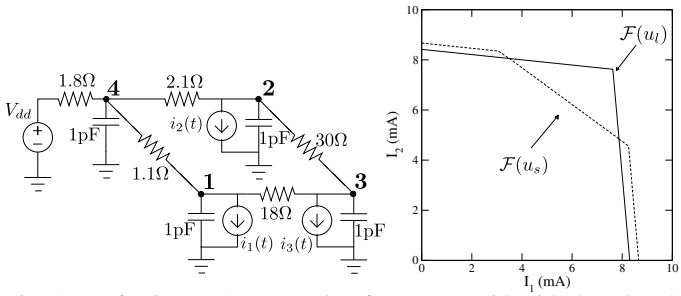

Fig. 1: (Left Figure) An example of a power grid with 4 nodes, 3 current sources, and $V_{th} = [88\ 45\ 36\ 83]^T$ (units of mV). (Right Figure) An example of $\mathcal{F}(u_s)$ and $\mathcal{F}(u_l)$.

Lemma 3. *Let $u^* = L^*G^{-1}H\mathbb{1}_m$, then $u^* \in \mathcal{U}$ and $l(u^*) = L^*$.*

Proof: Recall that $\eta \geq 0$ and $L^* \geq 0$, so that $L^*\eta \geq 0$. Moreover, because $C(L^*) \subseteq \mathcal{F}(u_l)$, we have:

$$0 \leq L^*\eta = L^*MH\mathbb{1}_m \leq MGu_l \tag{13}$$

where we used the fact that $\eta = M'\mathbb{1}_m = MH\mathbb{1}_m$ and the final step due to Lemma 2. Notice that $G^{-1}A = G^{-1}(G + B) = I_n + G^{-1}B \geq 0$, because $I_n \geq 0$, $G^{-1} \geq 0$, and $B \geq 0$. Multiplying (13) with $G^{-1}A \geq 0$, we get:

$$0 \leq L^*G^{-1}H\mathbb{1}_m \leq u_l \tag{14}$$

Therefore, we have $0 \leq u^* = L^*G^{-1}H\mathbb{1}_m \leq u_l$, so that $Pu^* \leq Pu_l \leq V_{th}$, because $P \geq 0$ and the final step is due to $u_l \in \mathcal{U}$. It follows that $u^* \in \mathcal{U}$. Moreover, we have that $MGu^* = L^*MH\mathbb{1}_m = L^*\eta$, from which $C(L^*) \subseteq \mathcal{F}(u^*)$, due to Lemma 2, so that $l(u^*) = L^*$, due to (8), and the proof is complete. ■

Recall that u_l is defined to be any vector $u \in \mathcal{U}$ such that $l(u) = L^*$. Therefore, using Lemma 3, we can let $u_l = L^*G^{-1}H\mathbb{1}_m$. Define the set $\mathcal{T}'$ as follows:

$$\mathcal{T}' \triangleq \{(L, u) : L \geq 0, u \geq 0, Pu \leq V_{th}, u = LG^{-1}H\mathbb{1}_m\} \tag{15}$$

Notice that, for any $(L, u) \in \mathcal{T}'$, we have $u = LG^{-1}H\mathbb{1}_m$, so that $MGu = LM'\mathbb{1}_m = L\eta$ which, combined with $L \geq 0$, $u \geq 0$, and $Pu \leq V_{th}$, gives $(L, u) \in \mathcal{T}$. Therefore, we have $\mathcal{T}' \subseteq \mathcal{T}$. Also, because $(L^*, u_l) \in \mathcal{T}'$, then $L^* = \max_{(L,u) \in \mathcal{T}'} (L)$, which can be found using the LP:

$$\begin{aligned} L^* = \quad & \text{Maximize} && L \\ & \text{subject to} && \begin{array}{ll} u = LG^{-1}H\mathbb{1}_m, & Pu \leq V_{th}, \\ L \geq 0, & u \geq 0 \end{array} \end{aligned} \tag{16}$$

Let $G = \begin{bmatrix} G_1 \\ G_2 \end{bmatrix}$, where G_1 and G_2 are $m \times n$ and $(n-m) \times n$ matrices, respectively. Recall that $H = [I_m\ 0]^T$, so that for every $(L, u) \in \mathcal{T}'$, we have:

$$Gu = \begin{bmatrix} G_1u \\ G_2u \end{bmatrix} = LH\mathbb{1}_m = L\begin{bmatrix} \mathbb{1}_m \\ 0 \end{bmatrix} \tag{17}$$

from which, $G_1u = L\mathbb{1}_m$ and $G_2u = 0$. Using (17), we can rewrite (16) as:

$$\begin{aligned} L^* = \quad & \text{Maximize} && L \\ & \text{subject to} && \begin{array}{ll} G_1u = L\mathbb{1}_m, & G_2u = 0, \\ Pu \leq V_{th}, & L, u \geq 0 \end{array} \end{aligned} \tag{18}$$

TABLE I: Comparison of the two approaches

Power Grid			Uniform Current Distribution: Sphere Approach (from [2] and [3])			Uniform Current Distribution: Cube Approach		
Name	Nodes	Current Sources	$P(u_s)$ in mW	$\rho(u_s)$ in μA	Total Time	$P(u_l)$ in mW	$l(u_l)$ in μA	Total Time
G1	312K	19K	35.23	2.03	22.67 min	36.80	1.89	50 sec
G2	449K	28K	50.10	1.61	46.47 min	41.60	1.48	1.7 min
G3	1M	63K	116.19	1.94	3.66 hrs	114.10	1.81	4.6 min
G4	1.7M	111K	205.21	1.84	13.93 hrs	184.40	1.64	10.9 min
G5	2.4M	151K	269.76	1.48	25.27 hrs	207.30	1.37	22.5 min
G6	2.7M	174K	319.34	2.03	33.45 hrs	336.40	1.93	21.2 min

where $\mathbb{1}_m$ is an $m \times 1$ vector whose every entry is 1. The LP in (18) has a remarkable simplification over (10) for two reasons: 1) $I_n - MB = I_n - M(A-G) = MG$ which means that MG is a dense matrix, because I_n and B are diagonal matrices and M is a dense matrix, so that the constraints of (10) are dense whereas the constraints of (18) are sparse, and 2) it does not require the computation of $\eta = M'\mathbb{1}_m$ which, because $M' \geq 0$, requires an LU-factorization of A and a forward/backward substitution.

Let $w = \begin{bmatrix} w^{(1)} \\ w^{(2)} \end{bmatrix} = MGu_l$, where $w^{(1)}$ and $w^{(2)}$ are $m \times 1$ and $(n-m) \times 1$ vectors, respectively. Also, let $M' = \begin{bmatrix} M_1 \\ M_2 \end{bmatrix}$, where M_1 and M_2 are $m \times m$ and $(n-m) \times m$ matrices, respectively. Because $u_l = LG^{-1}H\mathbb{1}_m$, then $Gu_l = LH\mathbb{1}_m \geq 0$. Hence, it can be shown that $M_1 I \leq w^{(1)} \iff M'I \leq w$ [3], i.e. $r'_j I \leq r_j G u_l$ is redundant, $\forall j \in \{m+1, \ldots, n\}$, where r'_j and r_j denote the jth rows of M' and M, respectively. This being said, the container $\mathcal{F}(u_l)$ can be expressed as $\mathcal{F}(u_l) = \{I \in \mathbb{R}^m : I \geq 0, r'_j I \leq r_j G u_l, \ \forall j \in \{1, \ldots, m\}\}$ which provides the desired current constraints:

$$i(t) \geq 0, \quad \forall t \in \mathbb{R}$$
$$r'_j i(t) \leq r_j G u_l, \quad \forall j \in \{1, \ldots, m\}, \quad \forall t \in \mathbb{R}$$

V. Results

The above algorithm (18) and the algorithm presented in [2] and [3] targeting uniform current distribution have been implemented using C++. The maximizations were performed using the Mosek optimization package [6]. We conducted tests on a set of power grids with a 1.1 V supply voltage that were generated based on user specifications, including grid dimensions, metal layers, pitch and width per layer, and C4 and current source distributions, consistent with 65nm technology. All results were obtained using a 3.4 GHz Linux machine with 32 GB of RAM.

The CPU time for solving (18) is given in column 9 of Table I. Furthermore, we include the CPU time for solving the uniform current distribution algorithm presented in [3] in column 6 of Table I. The LP (18) achieves 57X speedup on average compared to the uniform current distribution approach presented in [3].

In Table I, we present the results of the two approaches in columns 4, 5, 7, and 8. We compare both approaches based on the peak power dissipation and the uniformity of current distribution allowed under the resulting containers $\mathcal{F}(u_s)$ and $\mathcal{F}(u_l)$, where $\mathcal{F}(u_s)$ is the container resulting from the approach presented in [2] and [3]. Denote by $P(u) \triangleq V_{dd} \times \max_{I \in \mathcal{F}(u)} \left(\sum_{j=1}^{m} I_j \right)$ the peak power dissipation allowed under $\mathcal{F}(u)$. We computed the peak power dissipation achievable under both containers, which are $P(u_s)$ and $P(u_l)$. For instance, on a 449K node grid, the peak power dissipation achievable under $\mathcal{F}(u_s)$ and $\mathcal{F}(u_l)$ is 50.1 mW and 46.47 mW, respectively. Also, we computed the maximum radius of the hypersphere that has its part in the first quadrant in $\mathbb{R}^m$ inscribed in $\mathcal{F}(u_s)$ and the largest current edge for which the hypercube is contained in $\mathcal{F}(u_l)$, which are $\rho(u_s)$ and $l(u_l)$. Note that $\rho(u_s)$ and $l(u_l)$ represent the uniformity of the current distribution across the die area that each container can allow. For example, on a 449K node grid, the maximum radius hypersphere that has its part in the first quadrant inscribed in $\mathcal{F}(u_s)$ and largest current edge for which the hypercube in the first quadrant is contained in $\mathcal{F}(u_l)$ is 1.61 μA and 1.48 μA, respectively. The results show that $P(u_s) \approx P(u_l)$ and $\rho(u_s) \approx l(u_l)$ on all grids. Thus, both $\mathcal{F}(u_s)$ and $\mathcal{F}(u_l)$ provide similar features. Therefore, the the uniform current distribution approach presented in this paper is superior as it achieves a huge speedup compared to that presented in [3].

VI. Conclusion

Efficient and early verification of the power grid is a critical step in modern chip design. Typical methods for power grid verification include simulation-based and vector-less approaches, both of which have serious shortcomings. Recent literature has addressed the problem of generating circuit current constraints that ensure power grid safety. We adopted the same framework and developed a new constraints generation algorithm that target a key quality metric of the grid: the uniformity of the power spread across the die. We then compare our approach with that presented in [2] and [3]. Both approaches provide similar current distribution features. On the other hand, the approach presented in this paper has a huge runtime advantage ($\sim$ 57X speedup).

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