Battery-less Tri-band-Radio Neuro-monitor and Responsive Neurostimulator for Diagnostics and Treatment of Neurological Disorders

Hossein Kassiri, *Student Member, IEEE*, Arezu Bagheri, *Student Member, IEEE*, Nima Soltani, *Student Member, IEEE*, Karim Abdelhalim, Hamed Mazhab Jafari, M. Tariqus Salam, *Member, IEEE*, Jose Luis Perez Velazquez, and Roman Genov, *Senior Member, IEEE*

***Abstract*—A 0.13 μm CMOS system on a chip (SoC) for 64 channel neuroelectrical monitoring and responsive neurostimulation is presented. The direct-coupled chopper-stabilized neural recording front end rejects up to ±50 mV input dc offset using an in-channel digitally assisted feedback loop. It yields a compact 0.018 mm^2 integration area and 4.2 μVrms integrated input-referred noise over 1 Hz to 1 kHz frequency range. A multiplying specific absorption rate (SAR) ADC in each channel calibrates channel-to-channel gain mismatch. A multicore low-power DSP performs synchrony-based neurological event detection and triggers a subset of 64 programmable current-mode stimulators for subsequent neuromodulation. Triple-band FSK/ultra-wideband (UWB) wireless transmitters communicate to receivers located at 10 cm to 10 m distance from the SoC with data rates from 1.2 to 45 Mbps. An inductive link that operates at 1.5 MHz, provides power and is also used to communicate commands to an on-chip ASK receiver. The chip occupies 16 mm^2 while consuming 2.17 and 5.8 mW with UWB and FSK transmitters, respectively. Efficacy of the SoC is assessed using a rat model of temporal lobe epilepsy characterized by spontaneous seizures. It exhibits an average seizure detection sensitivity and specificity of 87% and 95%, respectively, with over 78% of all seizures aborted.**

***Index Terms*—Analog multiplication, batteryless implant, brain monitoring, chronic *in vivo* experiments, closed loop, closed-loop system on a chip (SoC), dc-coupled front end, diagnostics, digital calibration, digitally assisted feedback, epileptic seizure detection, implantable wireless SoC, inductive powering, interactable, multiband radio, multiplying ADC (MADC), neural recording, neural stimulation, phase synchronization, SoC.**

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H. Kassiri, N. Soltani, M. T. Salam, and R. Genov are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: hkassiri@eecg.utoronto.ca).

A. Bagheri and H. M. Jafari are with Semtech Inc., Toronto, ON M5J 2M4, Canada.

K. Abdelhalim is with Broadcom Inc., Irvine, CA 92617 USA.

J. L. Perez Velazquez is with the Brain and Behavior Programme and Division of Neurology, Hospital for Sick Children, University of Toronto, Toronto, ON M5G 1X8, Canada.

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I. Introduction

MONITORING and treatment of neurological disorders using a microelectronic brain implant has been investigated as a promising alternative for patients who are refractory to current pharmacological solutions [1]–[9]. Ideally, this requires the implanted system to record neural activity at high spatial resolution, process recorded signals, and, in some cases, trigger responsive action to control an undesired neurological event. Recently, several implementations have been reported for multisite brain-activity monitoring [11]–[15], some with signal processing and closed-loop neurostimulation [5], [8], [10], [16]. These advances, alongside the growth in our understanding of the human brain make such implants, a promising treatment alternative for neurological disorders such as epilepsy.

A general block diagram of a wireless closed-loop neurostimulator brain implant is shown in Fig. 1. This figure also shows an envisioned implantation configuration of the system on a chip (SoC) in the proximity of a human brain where it is connected to an array of electrocorticography (ECoG) or depth electrodes. The system communicates diagnostic data to an external module (e.g., a computer) through a wireless link and receives power and configuration commands through an inductive link. To monitor high spatial resolution brain activity, the SoC must integrate many (>16) low-noise neural recording channels to collect data from a large population of neurons. The overall size and power consumption should be minimized to follow the safety guidelines [17], [18].

This paper presents a 16 mm^2 0.13 μm CMOS SoC. The chip has 64 dc-coupled neural recording channels, each with a digitally assisted dc-offset cancellation feedback. Chopper stabilization is employed in each neural amplifier to suppress its flicker noise. Channel-to-channel gain mismatch is removed by utilizing a multiplying ADC (MADC), included in each channel, in a digital calibration loop. A multicore digital processor shared between all the channels is used to carry out signal feature extraction and epileptic seizure detection. The chip also has 64 programmable biphasic current-mode stimulators that are triggered by the on-chip digital processor upon detection of a neurological event, to modulate brain activity. Three wireless transmitters are included in the design, which enable communication of diagnostic data to a wide range of distances over three different bands of frequency. The chip is powered wirelessly using a magnetic inductive link, with energy signals that are

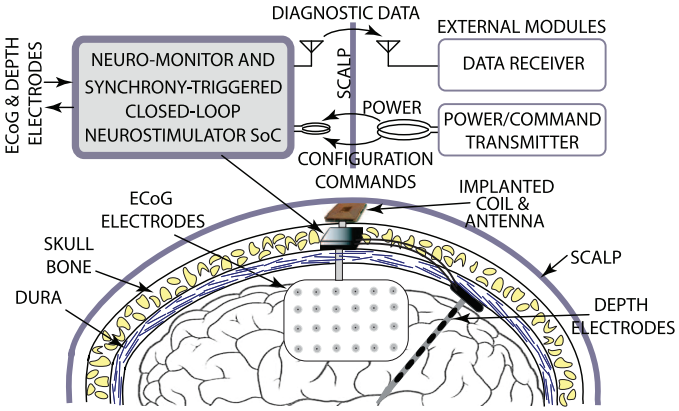

Fig. 1. Block diagram of a wireless closed-loop neurostimulator. An envisioned implanting configuration is also depicted.

amplitude shift keyed to communicate configuration commands to the chip. The chip is validated *in vivo* on four freely moving rats and offline on three human patients. This paper extends on an earlier report of the principle and demonstration in [16], and offers a more detailed analysis of the design and additional experimental results characterizing the circuit implementation and *in vivo* validation.

Compared to the previous generation of our responsive neurostimulation system published in [5], the recording channel is replaced with a new dc-coupled front-end design which resulted in smaller area per channel. Each channel is also chopper stabilized, resulting in lower flicker noise. In terms of system-level differences, multiband FSK/ultra-wideband (UWB) wireless transmitters are added in this work, enabling versatile data communication, both in terms of range and data rate. Also, the presented design includes wireless power and command receiving circuitry, which allows for powering the SoC inductively. In terms of application-level novelties, the presented system is validated *in vivo* in a 500 h chronic treatment of a rat model of temporal-lobe epilepsy.

This paper is organized as follows. Section II summarizes different design challenges of an implantable wireless neurostimulator that must be considered. Section III discusses the VLSI architecture of the neurostimulator SoC. Section IV presents the circuit implementation of the key functional blocks in the SoC. Section V presents electrical experimental results from individual blocks as well as the full system. Section VI presents *in vivo* online animal epilepsy seizure detection and treatment results and offline human epilepsy seizure detection results. Section VII discusses resource utilization and comparison with the state of the art.

II. Design Considerations

Design of a low-noise front end for recording small-amplitude neural signals (10 μV to 1 mV) that have frequency content in sub-Hz to 5 kHz [21] band creates various challenges. The task becomes more difficult at the lower frequencies where the flicker noise is dominant. Techniques such as large input device sizing [19], correlated double sampling [20], and chopping [22] are utilized to reduce the input-referred noise. Large input device sizing significantly limits the channel count. Correlated double sampling partially removes the low-frequency content of the signal at the input of the opamp which includes the offset and the flicker noise. On the other hand, chopper stabilization filters the flicker noise after upmodulating it to a higher frequency [27]. Despite being a very effective technique for flicker noise reduction, chopping has limitations in neural amplifiers. It has been shown that when chopping is applied to a conventional neural amplifier with ac-coupled inputs, it results in noise multiplication and input impedance reduction [22]. This necessitates the use of large input capacitors and the addition of an impedance boosting loop [23]. To avoid this overhead, the chopping technique can alternatively be used either at the folding node of a folded-cascode amplifier [31] which does not remove the flicker noise of the input transistors or with a dc-coupled amplifier [22].

Removing dc offset at the input of the recording amplifier is another challenge in the design of neural interface front ends. The offset is generated due to chemical reactions between brain cells and electrodes and can saturate the amplifier. Conventionally, this is done by adding ac-coupling capacitors between the electrode and the amplifier [5]–[8], [14], [15]. These capacitors increase channel area significantly as they must be larger than 10 pF to ensure high closed-loop gain and small-frequency high-pass pole at the same time [14], [30]. Such large input capacitors reduce the input impedance and consequently degrade the common-mode rejection ratio (CMRR). Also, as mentioned, ac coupling prevents use of noise reduction techniques at the input.

Recently, dc-coupled front-end amplifiers with an offset-removal feedback were proposed as a solution to the issues described above. In [29], an analog feedback loop is used to sense and cancel the dc offset. However, the opamp in the feedback increases the power consumption significantly, and its open-loop gain variation results in a varying high-pass pole. Differential difference amplifier topology is also utilized to remove the dc offset [33]. Despite being effective in dc offset removal, it can only be used for systems with a small number of channels as it requires use of large off-chip passive components in each channel to achieve the low-frequency high-pass pole. A fully digital implementation of the feedback loop for offset cancellation causes very small additional area and power consumption and allows for adjusting the high-pass pole with high accuracy. A digital feedback implementation is reported in [1] that adds/removes parallel transistors to/from the input differential pair for the input dc offset correction. Changing the number of parallel input transistors modifies the input device noise and leads to offset-dependent noise performance. Thus, the feedback implementation must be modified to achieve offset-independent noise performance.

An open-loop configuration with channel-to-channel gain variations is an important disadvantage of dc-coupled neural amplifiers. The change in the channel gain is due to temperature, supply voltage, and process variations [1], [22]. As a result, the signal amplitude and phase information of different channels cannot be directly compared to each other. Consequently, without channel-to-channel gain-mismatch removal, any multivariate signal processing done

among different channels will have a significant error. To solve this issue, the gain of all channels must be set to a nominal value using a calibration block implemented with minimum power and silicon overhead.

To detect neurological disorders, digital signal processing is done on the recorded signals. The detection for most cases should be done within a few microseconds after an event occurrence, which emphasizes necessity of an on-chip signal processing unit. Several on-chip processors implemented in neural monitoring SoCs have been reported in which spectral information such as magnitude and energy in each band is extracted from recorded signals [24], [25]. Depending on the application, various detection algorithms ranging from simple thresholding to advanced machine-learning-based methods [8], [38] are applied to the extracted information to detect different neurological events. For an accurate detection, the signal processing unit is required to extract both magnitude and phase information of neural signals for each channel as well as variations of these parameters among different channels. This yields information on neural activity in each region of the brain along with correlated activities among different regions.

Responsive neurostimulation is done upon detection of a neurological event to modulate undesired brain activity. For effective neuromodulation, many-site electrical stimulation triggered by the detection algorithm is required. For these stimulators, pulse amplitude, frequency, and duty cycle should be programmable for each channel independently to allow for versatile neuromodulation. In [8], an SVM-based detection algorithm is implemented on-chip to perform epileptic seizure detection. However, only one stimulation channel with the maximum current amplitude of 30 μA is available on the chip. In [6], 64 6 bit current-mode stimulating channels are reported with maximum amplitude of only 135 μA and 2 bits shared between all channels (i.e., only four independent channels).

A high-data-rate power-efficient wireless data transmitter is required for the SoC to communicate recorded neural information to a computer for display and/or further processing. Depending on the application, the receiver is typically located at 1 cm to 10 m from the implant. The choice of a specific application determines what data rate is required for the wireless link. Some narrow-band transmitters are reported to transmit data to as far as a few meters [8], [14], [26]. However, they typically have high power consumption and a limited data transfer rate of up to 2 Mbps. Recently, short-range (<1 m) UWB transmitters have been used, as they exhibit a much higher data rate while consuming less power [5], [36]. For a versatile wireless communication that covers a wide range of data rates and transmission distances for various applications, multiple transmitters with different data modulation schemes, transmission range, and frequency of operation must be included in the design of the SoC.

For a chronically implantable system, power and configuration commands should also ideally be provided wirelessly. Conventional chronically implanted batteries have the disadvantage of making the system heavy and bulky [13], [28]. An inductive powering system enables the use of a smaller rechargeable battery or in some cases removes the requirement for a battery altogether. The inductive link should have a reasonable range (on the order of centimeters) while keeping specific absorption rate (SAR) below the safety-permitted limit [34].

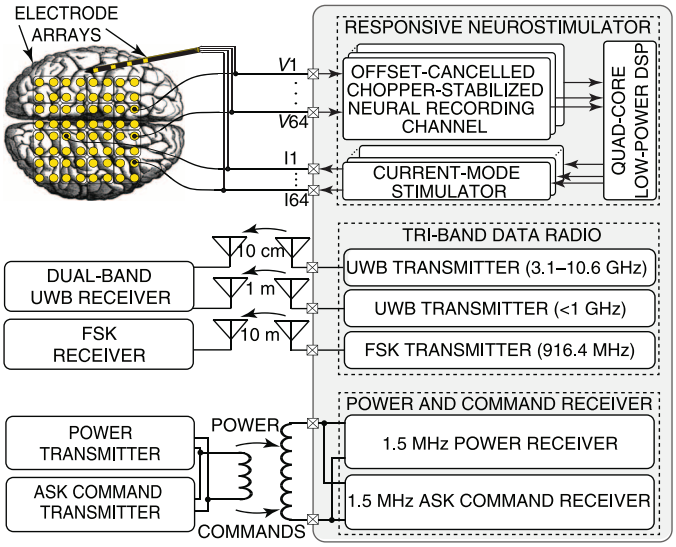

Fig. 2. Simplified functional diagram of the presented neurostimulator SoC and peripheral blocks.

III. System VLSI Architecture

A simplified functional diagram of the neurostimulator SoC is shown in Fig. 2. An array of intracranially implanted ECoG and depth electroencephalogram (EEG) electrodes connects to the 64 channels available on the chip for voltage recording and current stimulation. The recording front end in each channel is dc coupled to one data electrode and the reference electrode (not shown in Fig. 2 for simplicity). It utilizes chopper stabilization for low-frequency noise suppression. The direct-coupled configuration allows for removal of large dc-blocking capacitors that are conventionally used in each channel [3], [5], [6], [11], [13]–[15].

The amplified EEG signal is digitized using an ADC and is fed to an on-chip multicore CORDIC-based signal processing unit that is shared among all channels, to calculate magnitude, phase, and phase derivative of each recorded signal as well as phase synchrony among them. Upon early detection of an upcoming seizure, the on-chip processor triggers a programmable biphasic current-mode stimulation pulse train generated by a subset of 64 stimulators with a spatiotemporal profile specifically chosen for a given subject (a rodent or a human patient).

The chip is also equipped with three wireless transmitters with a different bandwidth, data rate, and range of transmission to communicate the raw recorded EEG signal or the processor's output. The 3.1–10.6 GHz UWB short-range transmitter communicates to an on-skin wearable receiver. The under 1 GHz UWB mid-range transmitter communicates to a handheld receiver, and the 915 MHz FSK long-range transmitter communicates to an indoor stationary receiver. The whole chip is powered wirelessly using a cellular inductive link operating at 1.5 MHz. The same inductive link is utilized for sending configuration commands and clock signals to the chip.

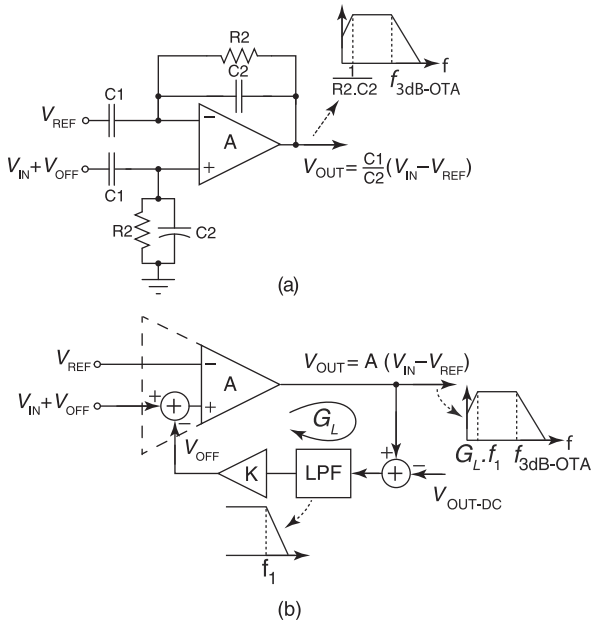

Fig. 3. Two types of input dc offset removal circuits. (a) AC-coupled closed-loop architecture. (b) DC-coupled open-loop architecture.

IV. VLSI Circuit Implementation

A. Neural Recording

1) DC-Coupled Recording Front End: Fig. 3(a) shows an ac-coupled closed-loop single-ended neural amplifier. Different variations of such topology have been used in several works such as [11], [14], and [15]. In this topology, the voltage gain is set by C_1/C_2 ratio, where C_1 and C_2 are the input decoupling and feedback capacitors, respectively. Also, the lower 3 dB bandwidth of the amplifier is set by $\frac{1}{C_2\times R_2}$, and the decoupling capacitor is placed at the input to block the dc offset voltage. To prevent any significant signal loss in lower frequencies where majority of epilepsy-related brain activities occur (δ (<4 Hz), θ (4–7 Hz), α (8–15 Hz), and β (16–31 Hz) bands), the lower 3 dB bandwidth of the amplifier should be set to a maximum of 1 Hz. To meet this condition, while maintaining a reasonably high voltage gain, and also to keep C_1 in a reasonable range for on-chip implementation, C_2 is typically chosen to be in the order of 100 fF, which forces R_2 to have a very large value ($>$100 GΩ).

Even with above considerations, C_1 is typically $>$10 pF, making it the most significant silicon area consumer on the chip considering that it is repeated twice in every channel. In addition, on-chip realization of a $>$100 GΩ resistor is another design challenge in the ac-coupled closed-loop topology. Due to area constrains, passive implementation is impossible for such large resistors. Therefore, multiple active pseudoresistor implementations are proposed in the literature [11], [14], [30] which despite their high-resistance, often suffer from nonlinear performance when a high-swing signal is applied across them (discussed in detail in [30]).

In addition to area, poor noise performance is another drawback of ac-coupled neural amplifiers. This is because conventional noise reduction methods such as chopper stabilization cannot be used in this topology as it introduces new problems with input impedance. Chopping switches can either be inserted in front of the input decoupling capacitors or after them. If placed in front of the capacitors as suggested in [12], they will reduce input impedance of the amplifier and consequently degrade quality of signal recording. If placed after the capacitors [3], [6], they form a switched capacitor with the input parasitic capacitance of the amplifier. The equivalent resistance of this SC-circuit shapes the OTA thermal noise with $1/f$ characteristics when referred to the input and consequently increases flicker noise considerably.

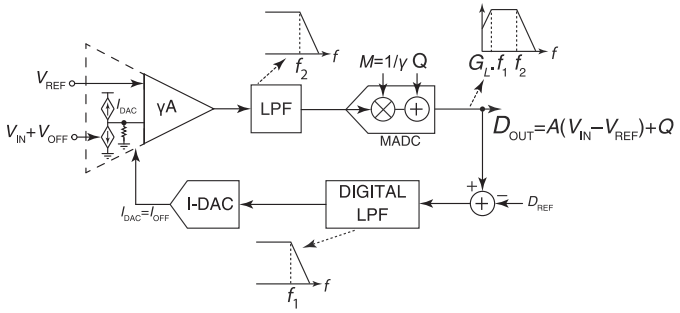

Fig. 4. Simplified block diagram of the presented open-loop dc-coupled front end with digital feedback and gain calibration.

Based on the above discussion, removing input decoupling capacitor seems to be solving several problems at once. However, the input dc offset that is now directly connected to the amplifier could result in output saturation. A substitute for input capacitors with minimum overhead area and power is required to remove this offset. Several solutions are suggested in the literature such as differential difference amplifiers [7], [35], which are very effective in removing input dc offset but result in excessive area overhead or additional off-chip passive components. A capacitive-T topology is suggested in [32], which slightly reduces the channel area in cost of significant noise performance degradation. In [2], the authors suggest using the electrode capacitance together with a huge resistive component to realize a high-pass pole. This technique removes the input decoupling capacitor and results in saving significant silicon area but fails to control the high-pass pole accurately.

Another option is to implement the front end in a way that is shown in Fig. 3(b). Here, the idea is to compare the amplifier's output dc level with a reference value and feed the average of the difference (error) to the input. Such a loop realizes a low-pass transfer characteristics in the feedback path, which translates into a high-pass transfer function in the feed-forward path. In this method, the neural front-end performance depends on where the feedback is applied and how it is implemented which is discussed in Section IV-A.2.

2) Digitally Assisted Feedback: Fig. 4 shows the simplified block diagram of the proposed dc-coupled neural front end with a digitally assisted feedback loop for dc offset cancellation. As shown, output of the amplifier is fed to a MADC. The multiplying capability of the ADC is only used when there is a channel-to-channel gain mismatch (gain mismatch is shown by a coefficient γ in Fig. 4). The digital output of the ADC is then compared with a reference number that represents the

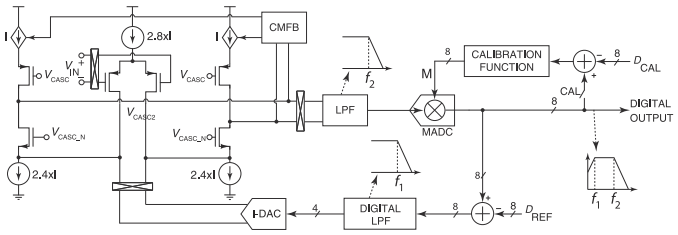

Fig. 5. Simplified circuit diagram of the chopper-stabilized neural recording front end with digitally assisted offset cancellation and digital gain-mismatch calibration.

midrange voltage at the ADC input. The difference is integrated using a digital low-pass filter and then sent to a current-steering DAC that adjusts the biasing of the amplifier to cancel the input offset. Since the output of the ADC is used for dc offset cancellation, sharing it among multiple amplifiers [22] would cause an over 100 ms delay in order for the output to stabilize after switching from one channel to another. This delay is mainly due to the fact that the input dc offset varies among different channels, and its compensation is done gradually due to the long-time constant of the digital low-pass filter in the feedback path. Every time the ADC is switched from one channel to another, the loop should operate for some time so that the digital LPF has integrated enough data points to compensate for the offset completely. During this settling time, the recorded brain signals would not be fully meaningful until the offset-cancellation loop is settled. As a result, a dedicated ADC is placed inside each channel to address the issue.

The low-pass filter in the feedback is implemented digitally, which results in very small area and power overhead while providing a very well-controlled bandwidth. This is important as the digital LPF cutoff frequency f_1 causes a high-pass pole in the feed-forward path equal to $G_L \times f_1$, where G_L denotes the loop gain. As a result, by adjusting f_1 using filter's coefficients, an undesired lower frequency range of the input (including dc) is blocked. As mentioned, the output of the integrator is then fed to a 4 bit current DAC to apply appropriate corrections to the biasing of the input amplifier and consequently cancel the input dc offset.

Fig. 5 shows the circuit schematic of the neural front end in more detail. As shown, the low-noise amplifier uses a differential folded-cascode topology. As the decoupling capacitors are removed, the input dc offset could result in an imbalance in the differential pair that leads to amplifier output saturation. In [1], authors cancel the imbalance caused by the input dc offset using a digitally assisted feedback that adds/removes parallel transistors to/from the input differential pair. This method prevents amplifier saturation in cost of tuning input differential pair device size that leads to input-referred noise variations. In other words, the noise performance becomes offset dependent, forcing the designer to size the input pair for the worst case (highest offset) and results in a significant unnecessary overdesign for smaller offset values.

We propose a feedback loop that applies a dc current to the folding node of the folded-cascode amplifier [22]. As shown in Fig. 5, the ADC output is compared with a reference value and the difference is averaged using a digital low-pass filter. The result is the error caused by the input dc offset that should be removed by injecting current to the folding node of the folded-cascode amplifier. The injected feedback current is set by a current DAC and is adjusted in accordance to the amount of dc offset. Using this method, the imbalance is cancelled while noise and other performance characteristics of the front end remain intact.

3) Chopper Stabilization: As shown in Fig. 5, chopper stabilization is used at the input to reduce the input-referred noise of the neural front end. Thanks to the dc-coupled inputs, there is no need for an extra complex auxiliary circuit such as impedance boosting block at the input. A set of chopping switches is the only additional components that should be added in the feedback injection node (folding node of the amplifier). This is because the input dc offset is upconverted after the input chopper and the offset-cancellation feedback should also be upconverted to ensure the two signals are always out of phase, or in other words, feedback is always negative.

4) Gain Calibration: As input decoupling capacitors are removed, open-loop configuration is chosen for the front-end gain-stage implementation. Unlike the closed-loop configuration, open-loop voltage gain is not very well controlled and changes with process, supply, and temperature variations. This results in a considerable channel-to-channel gain mismatch that leads to significant error in signal processing results and consequently less accurate seizure detection.

An MADC in conjunction with a calibration feedback loop is used to set the total gain of the front end (amplifier + ADC) to a constant value for all of the channels. Fig. 5 illustrates how the gain calibration loop and the MADC are connected with the rest of the recording front end. Since the SoC is designed to be implanted in the patient body, temperature variations are expected to be very small, making the process and supply variations more important factors. The SoC goes to the calibration mode only after long periods of recording. Once in the calibration mode, the same input is applied to all of the channels (the input is generated using an off-chip DAC that is controlled by an on-board FPGA), and their digital output is compared to a reference 8 bit number that represents digital translation of the input amplitude multiplied by the desired gain. An off-chip calibration module implemented on FPGA calculates new coefficients for the MADC to make the digital output of all channels equal to the reference.

Fig. 6 shows the simplified block diagram of the multiplying SAR ADC. The multiplication is performed in the sampling phase and requires an overhead of only three logic gates per bit [14]. When multiplying is not required, the MADC operates as a normal SAR ADC. However, when it is in the multiplying mode, the SAR digital controller selects a subset of capacitor bank based on the 8 bit coefficient set by the calibration function. These capacitors will be the only ones connected to the input voltage during the sampling phase, and the rest will be connected to the ground. Using this strategy, input voltage is multiplied by a number between zero and one that can be adjusted with 8 bits of resolution.

5) Closed-Loop Neurostimulation: The digital output of the neural recording channels is fed to an on-chip custom-made CORDIC-based digital processor that calculates magnitude,

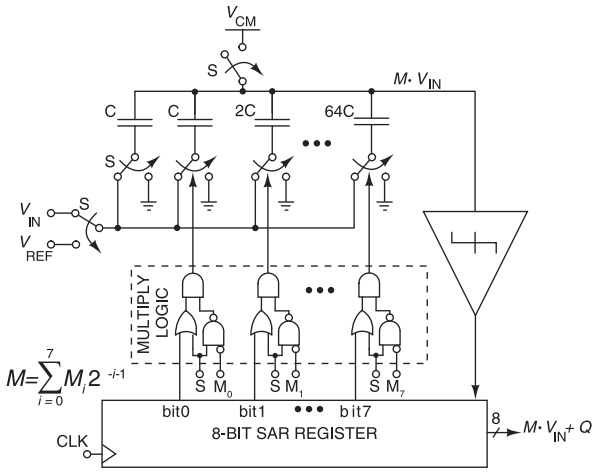

Fig. 6. Simplified block diagram of the MADC utilized for gain mismatch calibration (Q is quantization noise).

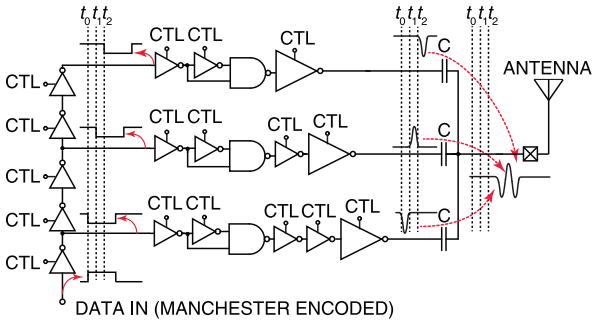

Fig. 7. Circuit schematic of the UWB transmitters with a tunable bandwidth. CTL controls the output pulse bandwidth by controlling the delay of each inverter cell.

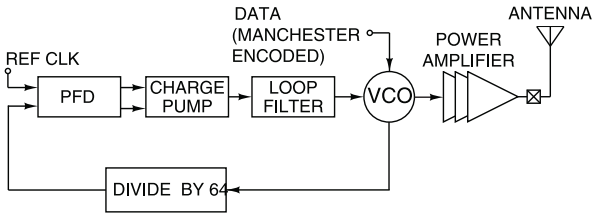

Fig. 8. Simplified block diagram of the FSK transmitter operating at 916.4 MHz.

phase, and phase derivative of signals from each channel as well as phase synchrony between channels. The phase synchrony is used for early detection of epilepsy seizure onset [43]. To abort a seizure, the digital processor triggers a subset of current-mode neural stimulators upon detection. The current-mode neurostimulator in each channel (originally presented in [5]) is capable of providing biphasic current pulses to the brain with programmable amplitude (0.01–1 mA), duty cycle, and frequency. The choice of stimulation parameters and stimulation pattern came from one of our earlier studies on *in vitro* [44] and *in vivo* [45] which demonstrated that early stimulation at seizure onset could prevent a seizure. The stimulation current and pulsewidth were chosen according to safety considerations [46] (three times lower than the maximum deliverable charge per phase [13]). The seizure formation was effectively aborted using low-frequency stimulation by means of the neural inhibition mechanism [47], which could be similar to that of antiepileptic drugs [48]. The total impedance seen from the circuit output was measured and ensured to be below 1 kΩ prior to running experiments with closed-loop stimulation. This impedance is controllable by electrode size, material, and roughness.

B. Wireless Transmitters

Three wireless transmitters are designed and implemented on-chip to cover a wide range of applications. The first and second are both UWB transmitters with a difference in their operating frequency, data rate, and range of transmission. The UWB transmitter circuit schematic is shown in Fig. 7. UWB pulse bandwidth is controlled by tuning the delay of current-starved inverters using a control voltage. The first transmitter operates in the 3.1–10.6 GHz range and has the highest data rate (45 Mb/s) measured at 10 cm which is the smallest range among three. The transmitter communicates to an on-skin receiver located very close to the implant. Due to its high data rate, it can be turned off for a long period of time and transmit buffered data using a few bursts. The second transmitter operates in $<$1 GHz range and has a maximum of 10 Mb/s data rate measured at 1 m. This transmitter is designed to communicate neural data at a reasonably high data rate to a hand-held receiver located at a maximum of 1 m distance from the implant.

The third transmitter which is shown in Fig. 8 utilizes a Manchester-encoded FSK modulation scheme with carrier frequency at 916.4 MHz. It benefits from a closed-loop PLL that prevents carrier frequency drift and allows avoiding an off-chip passive component for tuning. The transmitter has a 1.5 Mb/s data-rate (for both data and address bits) measured at maximum of 10 m which results in a 1.5 kS/s data rate for neural data of each channel when all 64 channels are used, and higher data rate when fewer number of channels are used. The 10 m range of this transmitter connects the SoC to a stationary receiver connected to a computer in the room.

C. Inductive Power and Command Telemetry

To enable *in vivo* experiments with a freely moving animal, the SoC has to be wire free. Since batteries increase total weight of the system significantly, an inductive link is designed to provide energy. The link operates at 1.5 MHz and provides up to 30 mW at a 15 cm range [40]. The operating frequency is chosen as it provides much higher magnetic field compared to high MHz frequencies (e.g., $>$100 MHz) and also unlike kHz range, does not require lossy and heavy ferrite cores for the receiver. The same inductive link is used to send commands to the the SoC. These commands include configuration of SoC's mode of operation, stimulation pulse-train properties (frequency, duty cycle, and amplitude), and recording bandwidth.

1) Coil Design: For both transmitting and receiving coils, planar spiral PCBs are used for implementation. The receiver is sized 2 cm $\times$ 2 cm with eight layers (104 turns in total) which results in 176 μH. The copper thickness on the PCB is set to

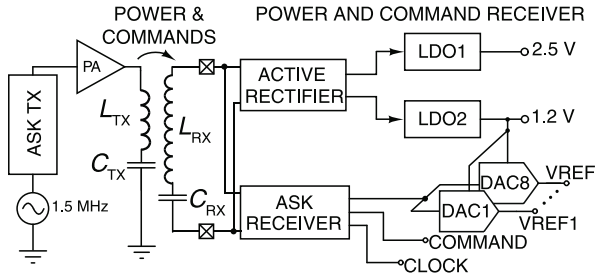

Fig. 9. Simplified block diagram of the inductive powering system and the command receiver.

yield highest possible quality factor for the coils, thus a higher power transfer efficiency.

An inductive surface sits under the nonconductive animal cage for power transmission. Unlike the receiver coil, there is no constraint for the transmitting coil size other than being large enough to cover any possible location of the SoC mounted on top of the animal's head. To reduce magnetic field intensity significantly, a multicoil architecture is chosen over a single coil. This makes the experiment environment safer for both the technician and the animal under test. Our experimental results also show much higher coupling coefficient at closer distances for the multicoil implementation. The transmit coils are arranged in two 2×4 overlapping arrays of PCB coils each sized at 11 cm $\times$ 11 cm making the total area of 45 cm $\times$ 26 cm for the inductive floor. The arrays of inductor coils are offset by 50% of the coil pitch in both x and y dimensions to eliminate magnetic field dead zones.

2) On-Chip Receiver: The received energy wave is rectified and regulated on-chip to provide supply voltage for different blocks of the SoC. As shown in Fig. 9, two supply voltages of 1.2 and 2.5 V are generated for recording and stimulation blocks, respectively. In addition, eight 8 bit DACs are implemented on-chip to provide different biasing voltages. An ASK receiver is implemented on-chip to receive the commands that are also sent through the inductive link for chip configuration. These commands shape the recording bandwidth and set the desired gain, stimulation pulse duty cycle and amplitude, and assign digital inputs to the DACs that are used to generate bias voltages.

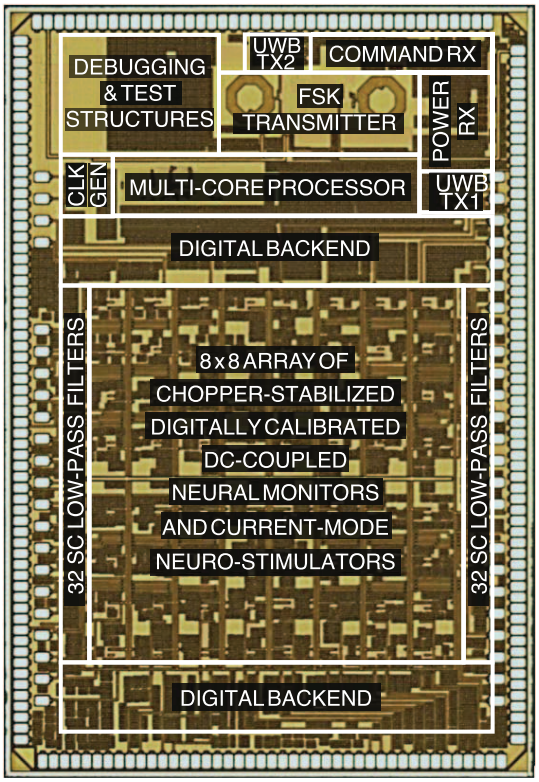

Fig. 10. Micrograph of the SoC with major blocks labeled.

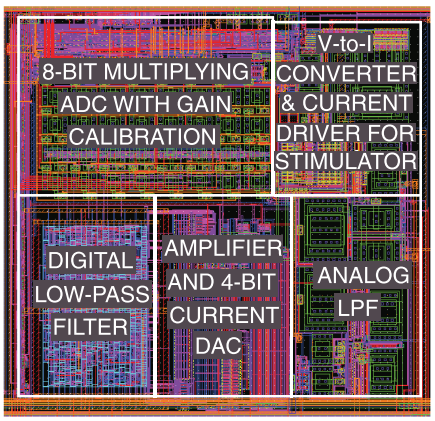

Fig. 11. Floor plan of the neural recording/stimulation channel.

V. Experimental Results

Fig. 10 shows the micrograph of the neurostimulator SoC. The chip is designed and fabricated in a 0.13 μm CMOS technology and is 4.8×3.3 mm^2. It has two power supplies of 1.2 V for neural recording and 3.3 V (2.5 V, when powered wirelessly) for current-mode stimulation. The floor plan of each channel is shown in Fig. 11. As illustrated, each channel houses a recording amplifier, a digitally assisted feedback, a MADC, a low-pass filter, and a current-mode stimulator as well as 22 bit memory that stores multiplication coefficients and stimulation signal properties.

A. Analog Front End

Fig. 12(a) shows the amplitude response of the front-end amplifier from sub-Hz frequencies up to MHz range. The 5 bit coefficient of the feedback digital LPF λ can adjust the lower 3 dB frequency from 1 to 220 Hz. The midband gain is measured to be over 51 dB for all the channels. The experimentally measured CMRR at 30 and 900 Hz is 69.2 and 64.1 dB, respectively. The frequency response of multiple channels was measured on-chip, on different dies. The voltage gain spreads between 51.1 and 53 dB, and the low-pass filter corner frequency varies from 9.5 to 11 kHz.

Fig. 12(b) shows the experimentally measured FFT of the front-end output with 130 Hz input frequency sampled at 7.2 kS/s. The SFDR and ENOB of the ADC are measured to be 56.5 dB and 6.7 bits, respectively. THD was measured to be lower than -50 dB for input peak-to-peak amplitudes up to 1 mV which is the nominal higher limit of neural signals. Fig. 12(c) shows the experimentally measured input-referred

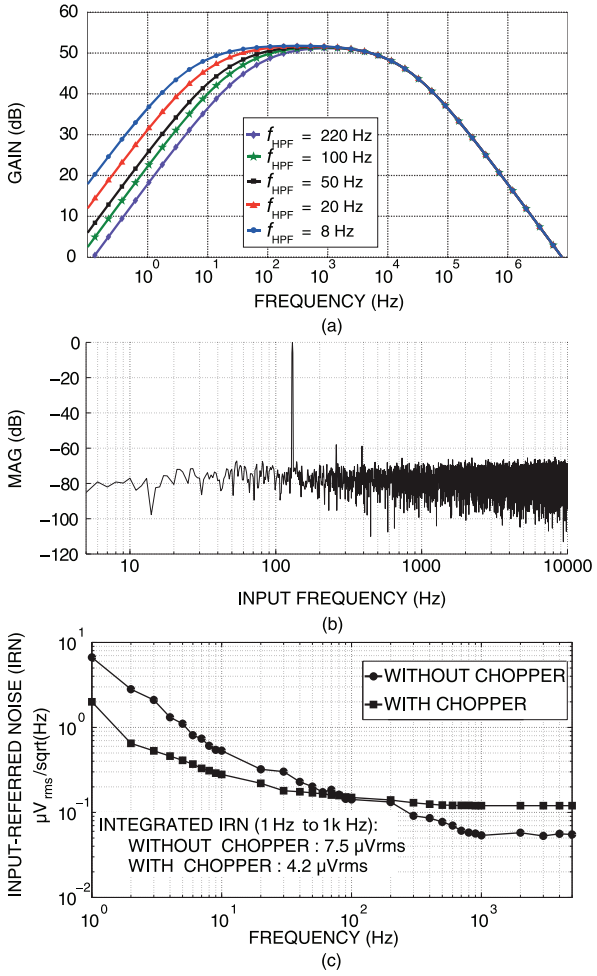

Fig. 12. Experimentally measured results for the analog front end. (a) Transfer characteristics spectrum of the recording front end with digitally adjustable high-pass pole. (b) Power spectral density of the ADC with 130 Hz input at full scale. (c) Input-referred noise with and without chopper stabilization.

noise with and without chopper stabilization. As shown, the integrated input-referred noise is measured to be 7.5 and 4.2 μV_{rms} before and after adding chopping switches, respectively.

The MOSFET switches used for chopping result in an increase in input noise current mainly due to charge injection and clock feed-through effects. When used with high-impedance biopotential electrodes, this current noise is converted into voltage, which will then add to the amplifiers total IRN. As shown in [41], this noise has a white power spectral density and is linearly proportional to the chopping frequency. In this design, we sized switches to minimize both charge injection and CFT, and also chopped the input signal at the lowest possible frequency to minimize the mentioned current noise. However, as shown in Fig. 12(c), the white baseline of IRN is increased after chopping. This has not affected the system performance significantly due to the mentioned precautions that were taken as well as using low-impedance recording electrodes.

Fig. 13(a) shows the experimentally measured CMRR and PSRR of the front-end amplifier for different input dc offset voltages. Both parameters stay higher than 50 dB for the entire

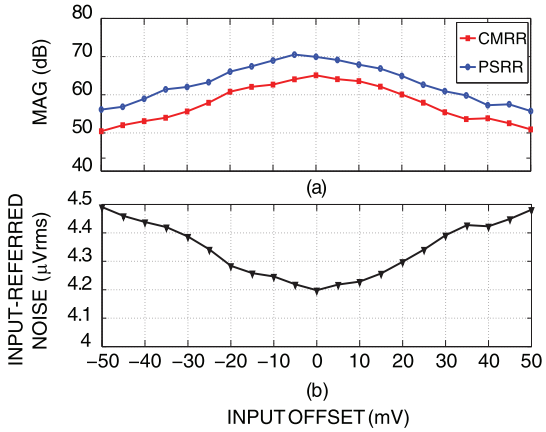

Fig. 13. Experimentally measured (a) analog front-end CMRR and PSRR versus input dc offset and (b) input-referred noise (integrated from 1 Hz to 1 kHz) versus input dc offset.

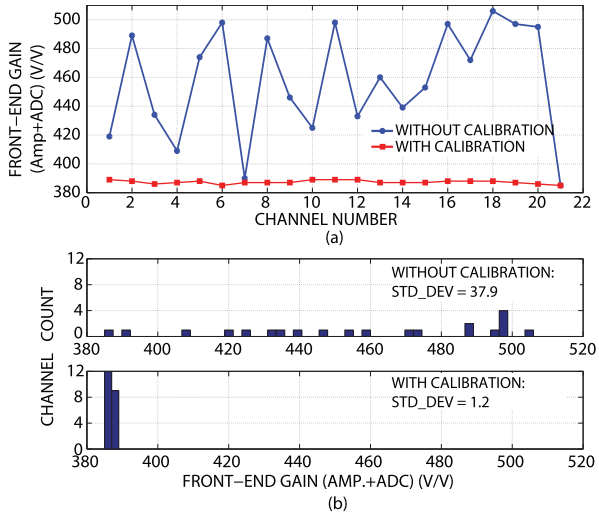

Fig. 14. Experimentally measured (a) voltage gain values for several channels before and after gain-mismatch calibration and (b) histogram of gain value distribution before and after calibration.

range of input offset values. Also they both have their maximum very close to zero dc offset which shows minimized mismatch of differential amplifier. Input-referred noise is also measured for different offset values and is shown in Fig. 13(b). As illustrated, IRN stays below 4.5 μV_{rms} for the entire range.

Fig. 14(a) shows gain variations for different channels before and after calibration. As illustrated in this figure, the measured open-loop voltage gain changes from 385 to 508 before calibration and 385 to 389 afterward. The voltage gain distribution is also demonstrated in Fig. 14(b) where it has standard deviation of 37.9 and 1.2 before and after calibration, respectively, exhibiting an over 30× improvement.

The current-mode stimulator is also tested to generate various biphasic pulse shapes with different amplitudes, frequencies, and duty cycles. For the electrodes that are used for neurostimulation, a typical resistive impedance of 1 kΩ is assumed which has allowed us to stimulate peak-to-peak amplitude of up to 2 mA using the 3.3 V voltage compliance. The high voltage compliance is achieved by using thick-oxide

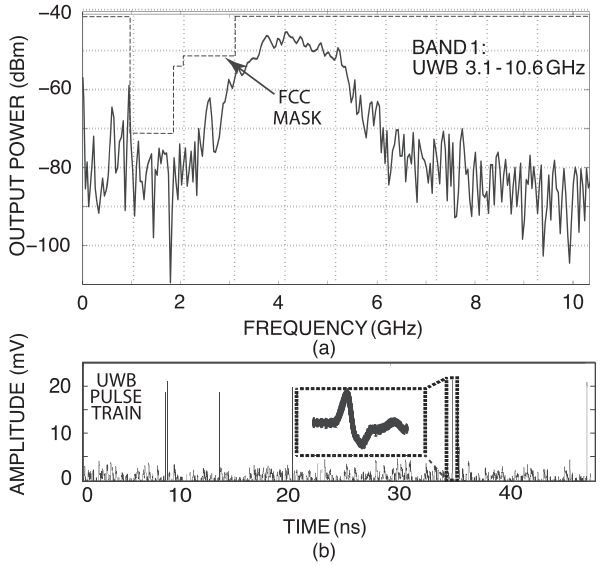

Fig. 15. Experimentally measured (a) output spectrum of the pulse for the first UWB transmitter (BAND1: 3.1–10.6 GHz) and (b) example of a transmitted pulse train.

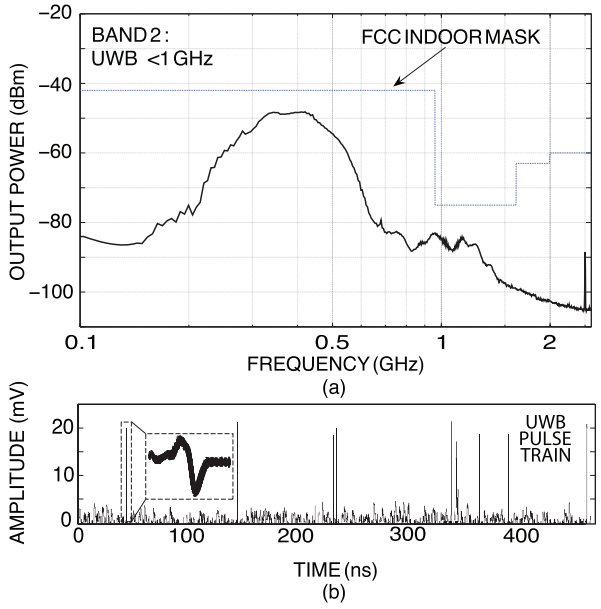

Fig. 16. Experimentally measured (a) output spectrum of the pulse for the second UWB transmitter (BAND2: <1 GHz) and (b) example of a transmitted pulse train.

devices in the current-mode stimulator circuit. Compared to the state of the art summarized in Table II, our voltage compliance is the second largest published.

B. Wireless Transmitters

Three wireless transmitters were tested experimentally with receivers located in different distances from the SoC. For the FSK radio, the receiver was the RFM 868–960 MHz TRC103 transceiver. The transmitter used a quarter-wave 915 MHz antenna and the receiver used a half-wave 915 MHz antenna, both connected through SMA connections. The UWB pulses

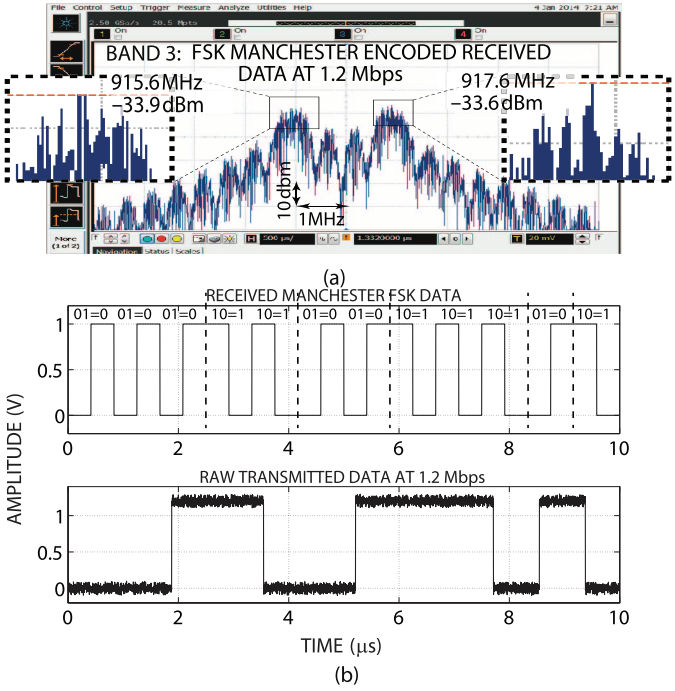

Fig. 17. Experimentally measured (a) spectrum of the FSK transmitter and (b) example of transmitted and received Manchester-encoded data at 1.2 Mbps using FSK modulation.

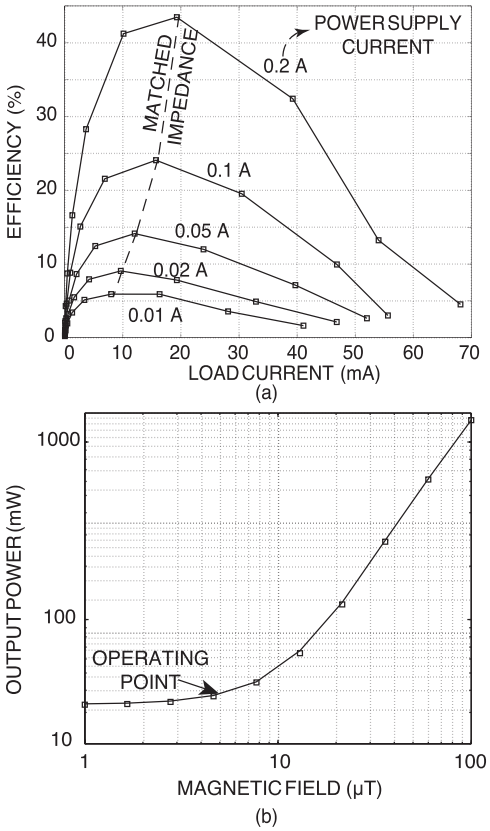

Fig. 18. Experimentally measured results for inductive link: (a) power transfer efficiency and (b) output power versus magnetic field.

are measured using custom-built UWB antennas (10 cm and 1 m spacing between the transmitter and receiver) and a custom-built receiver board.

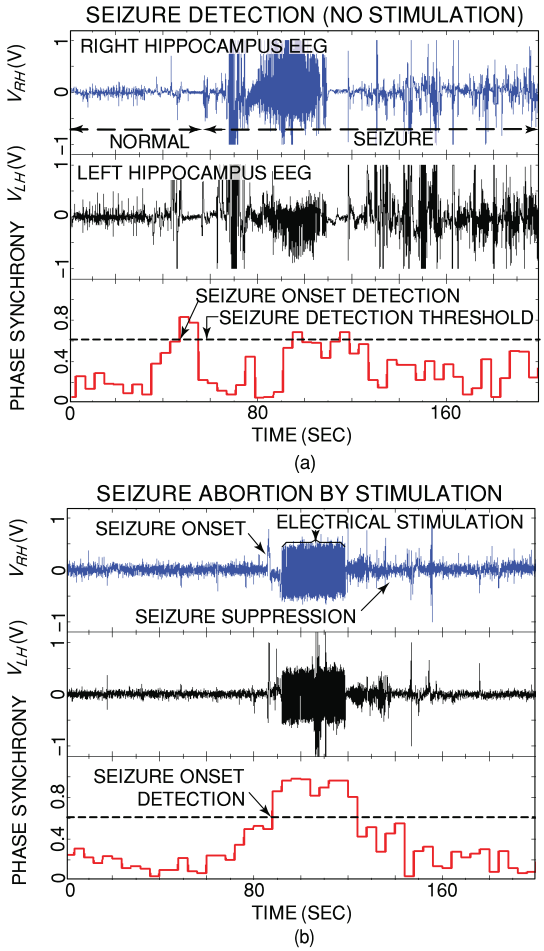

Fig. 19. Experimentally measured seizure detection and control results. (a) Example of seizure detection for the nontreatment group of rats. (b) Example of a seizure abortion for the treatment group of rats.

Fig. 15(a) shows the frequency spectrum and sample received pulses for the first UWB transmitter operating in the 3.1–10.6 GHz band. The experimental measurements show a maximum of data rate of 45 Mbps at 10 cm that promises a high-throughput link for short-distance communications to a wearable on-skin receiver. Fig. 16 shows the same result for the second UWB transmitter that operates under 1 GHz range and has a maximum data rate of 10 Mbps measured at a distance of 1 m. Fig. 17(a) shows the frequency spectrum of the Manchester-encoded FSK transmitter measured at the receiver with the highest measured data rate of 1.2 Mbps. Also Fig. 17(b) shows the pulse train for a sample sent and received using the Manchester-encoded FSK modulation. To avoid excessive power dissipation that could cause tissue damage, the three radios are not turned on simultaneously. The wireless transmitters are turned on depending on the application and proximity of the receiver (on skin, hand held, or stationary). In the worst case, when all three transmitters have to be ON, the total power consumption will be 6 mW, which is still within the power budget allocated to the inductive link.

C. Inductive Power and Command Telemetry

Fig. 18(a) shows experimentally measured power transfer efficiency for various currents consumed by the load. The ideal loading condition is when the system consumes approximately 15 mA, at which point the input impedance of the active rectifier is matched to the output impedance of the receiver coil. Fig. 18(b) depicts the power received at different intensities of the magnetic field at the receiver. Due to the significantly increased quality factor, the stacked configuration results in more power harvested from the transmitted magnetic field as compared to a conventional single-layer coil, for the same field intensity. Based on the experimental measurements, the variations of the field intensity are 13% from the nominal value of

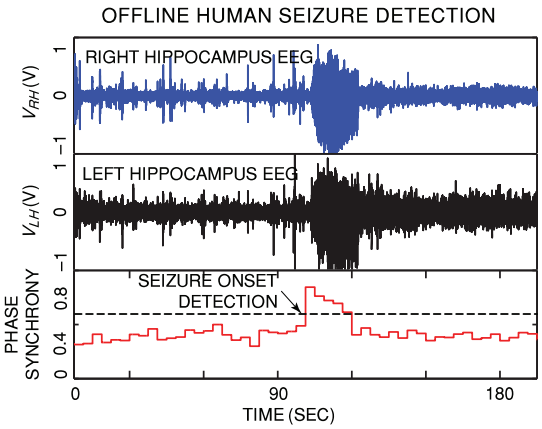

Fig. 20. Example of offline early seizure detection in a human patient.

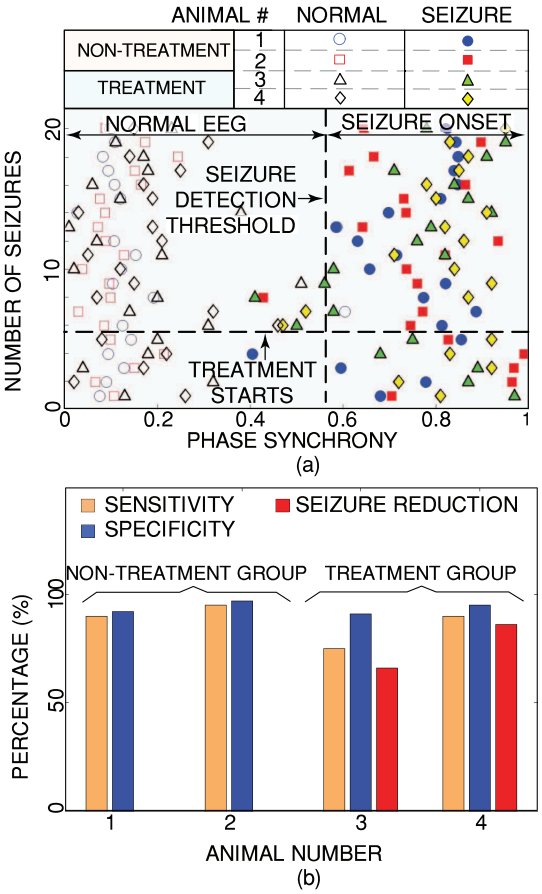

Fig. 21. (a) Statistical analysis for the *in vivo* experiments. (b) Seizure detection sensitivity, specificity, and seizure reduction rate of the epileptic rats in *in vivo* experiments.

TABLE I
SUMMARY OF THE EXPERIMENTAL RESULTS

System:			
Technology		IBM 0.13 μm	
Supply voltage (Rec.)		1.2 V	
Supply voltage (Stim.)		2.5/3.3 V	
Die dimensions		4.8 mm × 3.3 mm	
Area per channel		300 μm × 300 μm	
No. of recording channels		64	
No. of stimulation channels		64	
Power dissipation (Rec.)		2.17(UWB)/5.8(FSK) mW	
Power dissipation (Stim.)		1.14 mW	
Recording channel:			
Gain		51.5–51.8 dB	
Input-ref . noise (1 Hz–1k Hz)			
Without chopper		7.5 μV	
With chopper		4.2 μV	
LNA NEF		6.9	
CMRR		65 dB	
THD at 130 Hz		0.8%	
ADC SNDR		44.5	
ADC SFDR		59.5	
ADC ENOB		7.1 bits	
Power diss. (LNA + ADC)		9.1 μW	
Number of FIR filters		64	
Neural stimulation:			
Type		Biphasic current	
Current range		10 μA–1.0 mA	
DAC resolution		8 bits	
Duty cycle resolution		4 bits	
Wirless TX:	BAND1	BAND2	BAND3
Modulation	UWB	UWB	FSK
Freq. band	3.1–10.6 GHz	< 1 GHz	916.4 MHz
Data rate	45 Mbps	10 Mbps	1.2 Mbps
Range	10 cm	1 m	10 m
Power diss.	100 μW	100 μW	3.7 mW
Wirless power:			
Receiver coil:			
Type		8-layer flexible	
Size		2 cm x 2 cm	
No. of turns		104	
Inductance		176 μH	
Coil separation		15 cm	
Power transfer efficiency		40%	
Frequency		1.5 MHz	
No. of voltage levels		10	

6 μT. The multilayer receiver coil is measured to have high-quality factor of 24 despite the small size resulting in an overall wireless power transfer efficiency of 40%.

The RX coil receives a signal with the amplitude limited to 3 V. The rectifier outputs a noisy dc signal at 2.9 V with a 70 mV ripple, which is fed to two LDOs on the chip. The outputs of LDOs are steady 2.5 and 1.2 V dc, both with less than 5 mV ripple at all time, which is acceptable considering the PSRR values shown in Fig. 13(a). These voltages are used as reference inputs to the 8 output 8 bit voltage DAC, to generate biasing voltage on the chip.

VI. EXPERIMENTAL VALIDATION

An on-chip-calculated phase-synchrony indicator is used for early detection of epilepsy seizures. The phase synchrony is calculated between pairs of channels, and seizure is detected using thresholding. Upon detection, a programmable pulse train is triggered to a subset of current-mode stimulation channels for seizure abortion.

A. In Vivo Early Seizure Detection and Control

The efficacy of the responsive neurostimulator at aborting ictal events was assessed in a 500 h chronic treatment of a rodent model of temporal lobe epilepsy. For this purpose, kainic acid was injected intraperitoneally into four Wistar rats to induce the appearance of recurrent spontaneous temporal lobe seizures 1–2 months after the injection. At this point, rats underwent craniotomy with general anesthesia and microelectrodes were implanted into the hippocampus. Following the implantation and recovery period, the rats were connected to the presented system for the spontaneous recurrent electrographic seizure recordings and automatic seizure detection. As well,

rats were connected to a commercial recording system and were video monitored for the clinically associated behaviors during seizure activity (e.g., convulsions). Thus, seizures were classified according to electrographic and behavioral features for 24 h a day, 7 days a week.

For every subject, EEG was collected for 1 h and seizures were labeled by a professional epileptologist. The labeled data are used to set the threshold for the specific subject, and the chip is programmed with the offline-calculated threshold. This threshold is then used for long-term (>1 month) online seizure detection and abortion.

The rats were divided into two groups: 1) nontreatment group and 2) treatment group. In the nontreatment group (two rats), seizures were monitored and labeled (seizure start and stop time recorded) and the seizure frequency per hour was determined. In the treatment group (two rats), initially seizures were also monitored and labeled; later the stimulators on the SoC were activated to inject automatically triggered biphasic current pulses to suppress an upcoming seizure. Fig. 19(a) shows phase synchrony indicator [PLV (phase locking value)] in the nontreatment group during a detected seizure where it is increased rapidly to over 0.6 at the seizure onset. Fig. 19(b) shows an example of seizure onset detection and subsequent seizure suppression with self-triggered stimulation in treatment group.

Fig. 19(a) shows the sudden appearance of the typical neural discharges following low-voltage fast activity recording at the seizure onset and later an increase in frequency and amplitude of the neural signals during the seizure period. Fig. 19(b) illustrates an initiation of a pulse-train current-mode stimulation upon detection of the discharge and low-voltage fast activity (seizure onset) and disruption of the frequency and amplitude growth. The feedback electrical stimulation consists of a burst of square-wave biphasic current pulses of 150 μA, pulse width 100 μs, frequency 5 Hz, and duration 5 s triggered by the real-time synchrony analysis in response to the seizure precursor detection. Following the stimulation, neurons generate 5 Hz rhythms similar to the stimulation pattern, which prevents them from initiating epileptic high-frequency seizure activity. Once the neural stimulation is started, the recording and signal processing blocks of the SoC are disabled (otherwise, the SoCs amplifiers are saturated), and a benchtop amplifier is used to analyze the results.

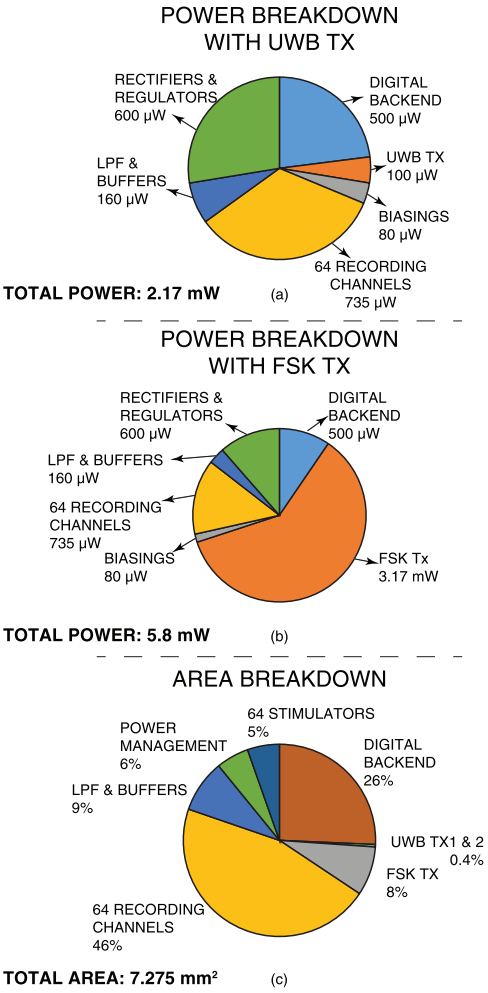

Fig. 22. Power breakdown of the integrated circuit operating in two modes: (a) with the UWB transmitters and (b) with the FSK transmitter. (c) Area breakdown of the IC.

B. *Offline Early Seizure Detection in Humans*

Fig. 20 shows an example of offline early seizure detection in human ECoG data from a University of Toronto epileptic patient. Eight hours of ECoG data was collected from three patients including a total of 12 seizures. These were fed to the SoC, and its detection performance was evaluated. As shown, the seizure is detected prior to its clinical onset (high-amplitude activity in the recording) using the on-chip synchrony-based algorithm.

C. *Statistical Analysis*

Fig. 21(a) demonstrates the SoC's seizure onset detection performance. As shown, treatment was started once the number of seizures per day was higher than 6. Also this figure shows the seizure onset detection performance that is evaluated online, using intracranial EEG signals recorded by the SoC from four animals, two in the nontreatment group and two in the treatment group. The detection performance was characterized by calculating detection sensitivity, false-positive rate, and false-negative rates. After PLV calculation, it was observed that normal EEG signals had an average PLV in the range of 0.3–0.7. However, the PLV increased rapidly up to 0.8 at seizure onset and gradually decreased to under 0.5 during the seizure.

To evaluate overall performance of the SoC in terms of seizure detection and abortion, sensitivity and specificity of detection were defined as: sensitivity: the ratio of TP to TP + FN. Specificity: the ratio of TN to TN + FP where true positive (TP) is the number of discharge events following the detection of the putative discharge precursor; false positive (FP) is when a discharge event does not follow the detection of the discharge precursor; true negatives (TN) are the absence of discharge activity correctly identified as nondischarge; and false negatives (FN) are the discharges that occurs without detection of the discharge precursor.

TABLE II
STATE-OF-THE-ART NEURAL RECORDING AND/OR STIMULATION SOCS

Spec.	[9] JSSC'13 Yoo	[36] ISSCC'08 Yuce	[6] JSSC'10 Flynn	[37] JSSC'12 Meng	[5] JSSC'13 Genov	[3] TBCAS'10 Ghovanloo	[8] JSSC'14 Wu	[26] ISSCC'14 Rabaey	This work	
Targeted Application	Eye blink detection	Snail EEG recording	Rat EEG recording	Monkey EEG recording	Epileptic seizure detection and control	Rodent EEG monitoring	Epileptic seizure detection and control	Rat EEG recording	Epileptic seizure detection and control	
Tech. (μm)	0.18	0.35	0.35	0.13	0.13	0.5	0.18	0.065	0.13	
Area (mm)	25	65	2.7	12	12	16.4	13.47	5.76	16	
Supply (V)	1.8	3.3	1.8	1.2	1.2	3	1.8	0.5	1.2/2.5	
Power diss. (mW)	N/R	6	0.09	6.5	1.4	7.05	2.8	0.225	2.17	
Power/Ch (μW)	66	11	9	68	10	75	6.71	2.3	9.1	
Neural front-end										
Area (mm^2)	0.7	0.3	0.1	0.26	0.09	0.1	0.5	0.025	0.018	
Gain (dB)	50–70	57–60	40	56	54–60	68–78	59.3	46	51.5	
Bandwidth (Hz)	0.5–100	0.1–20k	16–5.3k	1–10k	1–5k	0.1– 8k	0.1–7k	1–250	1–5k	
Noise (μVrms)	0.91	4.9	5.24	14	4.7	9.3	5.23	1.43	7.5/4.2	
Noise BW (Hz)	0.5–100	N/R	1–8k	1–100	10–5k	1–10k	0.5–7k	1–500	1–1k	
# of rec. channels	8	128	8	96	64	32	8	64	64	
Chopper count	8	0	0	0	64	0	0	0	64	
Signal processing	YES	YES	YES	NO	YES	NO	YES	NO	YES	
Closed-loop	NO	NO	NO*	NO	YES	NO	YES	NO	YES	
Detection Method	SVM	–	–	–	Ampl/phase synchrony	–	Entropy /spectrum	–	Phase derivative	
Neural stimulation	NO	NO	YES	NO	YES	NO	YES	NO	YES	
# of Stim. channels	0	0	64	0	64	0	1	0	64	
Current range (μA)	–	–	3–135	–	10–1200	–	30	–	10–1000	
Wireless power	NO	NO	NO	NO	NO	YES	YES	YES	YES	
Receiver coil										
Type	–	–	–	–	–	1-layer	Wire-wound	1-layer flex	8–layer flex	
Size/area (cm^2)	–	–	–	–	–	4.5	5.72	0.42	4	
# of turns	–	–	–	–	–	2	4	1	104	
Inductance (μH)	–	–	–	–	–	0.41	N/R	N/R	176	
Coil separation (cm)	–	–	–	–	–	<12	N/R	1.6	<15	
Power efficiency	–	–	–	–	–	N/R	N/R	N/R	40%	
Frequency (MHz)	–	–	–	–	–	13.56	13.56	300	1.5	
# of voltage levels	–	–	–	–	–	N/R	3	2	10	
Wireless comm.	NO	YES	NO	NO	YES	YES	YES	YES	Band1	Band2 Band3
Modulation	–	UWB	–	–	UWB	FSK	OOK	OOK	UWB	UWB FSK
Frequency (Hz)	–	3.1–10.6G	–	–	3.1–10.6G	915M	401M	300M	3.1–10.6 G	<1 G 916.4 M
In-vivo results	YES	NO	NO	NO	YES	NO	YES	YES		YES
Sensitivity (%)	71.4–88	–	–	–	–	–	92			88–96
Specificity (%)	N/R	–	–	–	–	–	–	–		89–97
Seizure reduction (%)	–	–	–	–	–	–	–	–		78
Advanced detection (s)	N/R	–	–	–	–	–	–	–		25–45

–: not applicable.
N/R: not reported.
*: off-chip.

The average sensitivity and specificity of the detection are 87% and 95%, respectively. The average false-positive and false-negative frequencies are 0.52 and 0.33 times per hour, respectively. Seizure frequency has been reduced on average by over 78% in the treatment group compared to the nontreatment group, as shown in Fig. 21(b).

VII. DISCUSSION

A. Resource Utilization

A summary of experimental measurement results is shown in Table I. Also Fig. 22(a) and (b) shows the power breakdown of the chip when operating with UWB and FSK transmitters, respectively. The SoC dissipates 2.17 mW when operating with UWB transmitters and 5.8 mW with the FSK transmitter. Also the feed-forward path of the SoC which includes analog front end and digital back end consumes 1.32 mW for 64 channels resulting in 21 μW per channel. When operating in stimulation mode, the SoC dissipates 1.14 mW or 18 μW per channel, from a 2.5 V supply. With cost of 30% more power consumption, the supply voltage can be increased to 3.3 V for higher stimulation headroom when the SoC is not inductively powered. Since the SoC goes to the stimulation mode for less than 1% of the experiment time, this increase affects total power consumption insignificantly.

Fig. 22(c) shows the area breakdown of the chip (excluding routings, IO pads, and decoupling capacitors for supplies). The total area occupied by 64 recording and stimulation channels together with the digital back end, wireless transmitters, and power management circuits is 7.275 mm^2. Sixty-four recording front ends have the biggest quota with 46% followed by the digital back end (FIR filters and on-chip processor). The 64 stimulators are added to the chip with very small area overhead of 5% since they share some blocks such as DAC and 12 bit memory (for duty-cycle control) with the recording circuitry.

B. Comparison to the State of the Art

A comparison with other neural monitoring and/or neurostimulation SoCs is given in Table II. This work demonstrates the highest degree of integration among recently published state-of-the-art SoCs by combining 64 recording channels with digital offset-cancellation feedback loop and chopper stabilization, 64 current-mode stimulation channels, 64 multiplying SAR ADCs, a multicore DSP unit, three wireless transmitters, and wireless power and command receivers. It also has the smallest front-end area and benefits from the most versatile wireless data transmission. The extensive *in vivo* validation of the work with statistical data analysis is also unique among published works. The "seizure onset" is defined as the time when the amplitude of the electrographic recording in the paroxysm becomes greater than twice the standard deviation of the baseline activity. The "advanced seizure detection time" mentioned in Table II is defined as the time between the detection of the seizure precursor and the seizure onset.

C. In Vivo Results

We note that in our study, we detect an increased value of the synchrony index rather than the typical decreased reported in other studies [13], [15], [43] because the time window used to average the phase differences to compute the synchrony index was longer (4 s), which precluded the observation of the sharp decrease previously found in this animal model that requires a <1 s averaging.

VIII. Conclusion

A CMOS fully wireless closed-loop neurostimulation SoC is presented. The 16 mm^2 die integrates 64 differential direct-coupled chopper-stabilized recording amplifiers with in-channel digital offset cancellation feedback, 64 in-channel MADCs, multicore digital signal processing unit, triple-band FSK/UWB wireless transmitters, active rectifiers, regulators, and DACs for inductive power receiving, ASK demodulator for command receiving, and 64 in-channel synchrony-triggered current-mode stimulators for abortion of undesired neurological events. Gain mismatch is calibrated using the on-chip MADCs and off-chip calibration loop.

The SoC is implemented in IBM 0.13 μm technology and dissipates 2.17 and 5.8 mW with UWB and FSK transmitters, respectively. It is validated in a chronic *in vivo* epilepsy monitoring and treatment for multiple rodents and demonstrates average seizure detection sensitivity and specificity of 87% and 95%, respectively, with 78% seizure frequency reduction.

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Hossein Kassiri (S'10) received the B.Sc. degree from the University of Tehran, Tehran, Iran, in 2008, the M.A.Sc. degree from McMaster University, Hamilton, ON, Canada, in 2010, and the Ph.D. degree (focused on the design, development, and validation of wireless and battery-less neural recording and stimulation systems, and their application in monitoring and treatment of neurological disorders) from the University of Toronto, Toronto, ON, Canada, in 2015, all in electrical and computer engineering.

From January to May 2012, he worked as an Electronic Design Consultant with Treata Smart Solutions, Toronto, ON, Canada, for the development of a low-power localization module to help Alzheimer's disease patients. He is currently working as the CTO of the BrainCom Technologies, Toronto, ON, Canada, a company he co-founded in September 2015, specialized in implantable brain–computer interfaces.

He has been the recipient of Ontario Brain Institute (OBI) Entrepreneurship Award in 2015, Heffernan Commercialization Award in 2014, University of Toronto Early Stage Technology Award in 2014, and the CMC Brian L. Barge Award for Excellence in Microsystems Integration in 2012.

Arezu Bagheri (S'11) received the B.Sc. degree in electrical and computer engineering from the University of Tehran, Tehran, Iran, and the M.A.Sc. degree in electrical and computer engineering (focused on dc-coupled digitally assisted neural recording amplifiers with high integration density) from the University of Toronto, Toronto, ON, Canada, in 2009 and 2013, respectively.

She was a Research Assistant with the Intelligent Sensory Microsystem Laboratory, University of Toronto. She is currently with Semtech Snowbush IP, Toronto, ON, Canada, where she focuses on mixed-signal circuit design for high-speed wireline communication systems. Her research interests include analog- and mixed-signal-integrated circuit design.

Ms. Bagheri was the recipient of the Ontario Graduate Scholarship in 2011.

Nima Soltani (S'12) received the B.Eng. and M.A.Sc. (focused on ultralow-power RF circuits for passive microsystems, and RF power transmission) degrees in electrical engineering from Ryerson University, Toronto, ON, Canada, in 2007 and 2010, respectively. He is currently working toward the Ph.D. degree (focusing on inductively powered implantable brain chemistry monitoring systems) at the University of Toronto, Toronto, ON, Canada.

From 2010 to 2011, he worked with Solace Power Inc., Mount Pearl, NL, Canada, on the development of the first electrical induction system for medium-range wireless power transfer. He is a Co-Founder of BrainCom Inc., Toronto, ON, Canada, specializing in the development of wearable and implantable platforms for high-resolution brain signal processing and acquisition.

Karim Abdelhalim received the B.Eng. and M.A.Sc. degrees in electrical engineering from Carleton University, Ottawa, ON, Canada, in 2005 and 2007, respectively, and the Ph.D. degree in electrical and computer engineering (focused on wireless neural recording and stimulation SoCs and their application in monitoring and treatment of intractable epilepsy) from the University of Toronto, Toronto, ON, Canada, in 2013.

From 2011 to 2015, he was a Senior Staff Scientist with Broadcom Corporation, Irvine, CA, USA, where he was involved in the design of mixed-signal ICs for 10/100/1G-BASE-T Ethernet applications and 100BASE-T1 and 1000BASE-T1 automotive Ethernet applications. From July 2010 to October 2010, he also worked as an Intern in mixed-signal design engineering with Broadcom Corporation. Since 2015, he has been a Senior Staff Analog IC Design Engineer with Inphi Corporation, Irvine, CA, USA, where his main focus is on ultra high-speed transceivers for optical applications.

Hamed Mazhab Jafari received the B.Eng. and M.A.Sc. (focused on low-power UWB CMOS front ends and UWB antennas) degrees in electrical engineering from McMaster University, Hamilton, ON, Canada, in 2004 and 2006, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2013, where he is currently working toward the Ph.D. degree in CMOS DNA analysis SoC.

He has held Internship positions with Kapik Integration, Toronto, ON, Canada, where he worked on low-power mixed-signal circuits. Since 2011, he has been with Snowbush IP, Toronto, ON, Canada, where he focuses on the research and development of next-generation high-speed wireline communication systems.

M. Tariqus Salam (M'09) received the B.Sc. degree in electrical and electronics engineering from Islamic University of Technology (IUT), Dhaka, Bangladesh, in 2003, the M.A.Sc. degree in electrical and computer engineering from Concordia University, Montreal, QC, Canada, in 2007, and the Ph.D. degree in electrical engineering from Polytechnique, University of Montréal, Montreal, QC, Canada, in 2012.

He is currently a Postdoctoral Fellow with the University of Toronto, Toronto, ON, Canada, where he works with the Neuroscience Division of Toronto Western Hospital. His research interests include low-power circuit design, brain–machine interface, and mental disease diagnosis and therapy.

Jose Luis Perez Velazquez was born in Zaragoza, Spain. He received the Licenciado degree in chemistry (biochemistry) from the University of Zaragoza, Zaragoza, Spain, and Complutense University of Madrid, Madrid, Spain, and the Ph.D. degree in molecular physiology and biophysics from Baylor College of Medicine, Houston, TX, USA, in 1992.

He was homologated to Doctorate in Chemistry by the Spanish Ministry of Culture in 1997. Currently, he is an Associate Scientist with the Neuroscience and Mental Programme and the Brain and Behaviour Center at the Hospital For Sick Children, Toronto, ON, Canada, and Associate Professor with the University of Toronto, Toronto, ON, Canada.

Roman Genov (S'96–M'02–SM'11) received the B.S. degree in electrical engineering from Rochester Institute of Technology, Rochester, NY, USA, in 1996, and the M.S.E. and Ph.D. degrees in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, USA, in 1998 and 2003, respectively.

He held engineering positions with Atmel Corporation, Columbia, MD, USA, in 1995, and Xerox Corporation, Rochester, NY, USA, in 1996. He was a Visiting Researcher at the Laboratory of Intelligent Systems, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1998, and at the Center for Biological and Computational Learning, Massachusetts Institute of Technology, Cambridge, MA, USA, in 1999. He is currently a Professor with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is a Member of Electronics Group and Biomedical Engineering Group and the Director of Intelligent Sensory Microsystems Laboratory. His research interests include primarily in analog-integrated circuits and systems for energy-constrained biological, medical, and consumer sensory applications, such as implantable, wearable, or disposable sensory microsystems, energy-efficient sensory signal processors, and wireless sensors, including brain–chip interfaces, neurostimulators, image sensors, optical and electro-chemical DNA microarrays, and other biosensors.

Dr. Genov was a Technical Program Co-Chair at the IEEE Biomedical Circuits and Systems Conference. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS and IEEE SIGNAL PROCESSING LETTERS. He is currently an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and a member of IEEE International Solid-State Circuits Conference International Program Committee serving in Imagers, MEMS, Medical, and Displays (IMMD) Subcommittee. He was the corecipient of the Best Paper Award of the IEEE Biomedical Circuits and Systems Conference, Best Student Paper Award of the IEEE International Symposium on Circuits and Systems, the Best Paper Award of the IEEE Circuits and Systems Society Sensory Systems Technical Committee, Brian L. Barge Award for Excellence in Microsystems Integration, MEMSCAP Microsystems Design Award, DALSA Corporation Award for Excellence in Microsystems Innovation, and Canadian Institutes of Health Research Next-Generation Award.