320-Channel Active Probe for High-Resolution Neuromonitoring and Responsive Neurostimulation

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Abstract—We present a 320-channel active probe for high-spatial-resolution neuromonitoring and responsive neurostimulation. The probe comprises an integrated circuit (IC) cell array bonded to the back side of a pitch-matched microelectrode array. The IC enables up to 256-site neural recording and 64-site neural stimulation at the spatial resolution of 400 μm and 200 μm, respectively. It is suitable for direct integration with electrode arrays with the shank pitch of integer multiples of 200 μm. In the presented configuration, the IC is bonded with a 8×8 400 μm-pitch Utah electrode array (UEA) and up to additional 192 recording channels are used for peripheral neuromonitoring. The 0.35 μm CMOS circuit array has a total die size of 3.5 mm $\times$ 3.65 mm. Each stimulator channel employs a current memory for simultaneous multi-site neurostimulation, outputs 20 μA–250 μA square or arbitrary waveform current, occupies 0.02 mm^2, and dissipates 2.76 μW quiescent power. Each fully differential recording channel has two stages of amplification and filtering and an 8-bit single-slope ADC, occupies 0.035 mm^2, and consumes 51.9 μW. The neural probe has been experimentally validated in epileptic seizure propagation studies in a mouse hippocampal slice *in vitro* and in responsive neurostimulation for seizure suppression in an acute epilepsy rat model *in vivo*.

Index Terms—Brain, CMOS, extracellular recording, hippocampus, implantable, intractable epilepsy, multichannel neural recording, multichannel neural stimulation, neural amplifier, very large scale integration (VLSI).

I. INTRODUCTION

ADAPTIVE neural stimulators with closed-loop feedback are a promising new technology in neurology and neural engineering. It has been shown that applying a stimulus in response to a neural event can be useful in treating neurological disorders such as intractable epilepsy [1]. A system that acquires neural activity, processes the data and, upon detection of a certain neural behaviour, responds with a stimulus of a certain type,
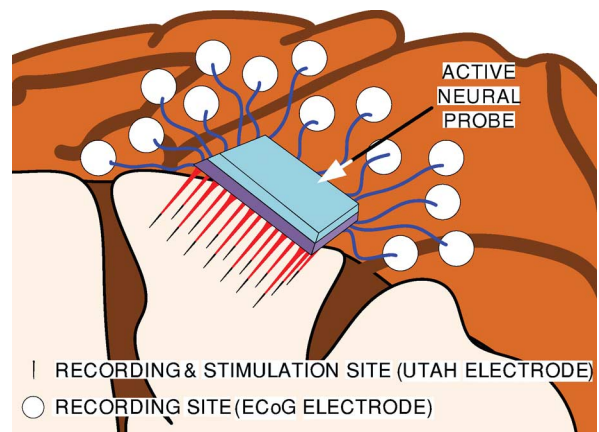
Fig. 1. Envisioned bidirectional active neural probe.

can be utilized in the treatment of such neurological disorders. Responsive electrical stimulation on 1 to 8 channels is already being evaluated for epilepsy treatment but with limited efficacy—less than 13% of patients are rendered seizure-free [2].

This drawback necessitates extensive studies on animal epilepsy models to improve our understanding of epilepsy and its treatment strategies. Massively-parallel bidirectional integrated neural interfaces have a potential to improve our understanding of neurological disorders such as intractable epilepsy, and meliorate therapy development. There is currently a need to monitor spatial propagation of neurophysiological indicators of a pathological brain state such as an epileptic seizure at a fine spatial resolution [3] and to deliver an optimum spatio-temporal neurostimulation pattern [4]. A compact implantable system that can perform both real-time neuromonitoring and neurostimulation makes such studies possible.

Fig. 1 shows the envisioned active probe for neuromonitoring and responsive neural stimulation for epilepsy treatment studies in rodent seizure models (e.g., guinea pigs, rats). The integrated circuit (chip) interfaces with the brain through two types of electrodes. Utah electrode array (UEA) is connected to (a total of 64) on-chip recording and stimulation channels and is implanted in the epileptogenic zone. Additional on-chip recording channels (up to 192) are connected to ECoG (electrocorticography) electrodes, implanted subdurally in adjacent regions for wider and sparser spatial monitoring. Intracranial EEG signals are monitored continuously at the UEA shank tips and on the ECoG electrodes. Stimulation is applied to the epileptogenic zone in response to a seizure onset detection.

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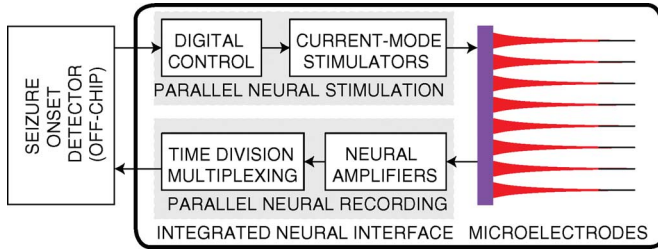IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS

Fig. 2. A block diagram of the active probe for multichannel responsive neural stimulation.

The block diagram of the active probe is outlined in Fig. 2. It consists of the neural stimulators, the recording channels and the microelectrode array. An off-chip seizure detector closes the loop as needed for on-line seizure control studies in rodents. This paper extends upon the work presented in [5] and focuses on the system-level design and validation of the active probe in animal studies.

The rest of this paper is organized as follows. Section II presents neural recording and stimulation system design specifications and the existing bidirectional integrated neural interfaces. Section III describes the system architecture of the bidirectional active probe. Section IV presents the circuit implementation of the neural stimulator. Section V describes the recording channel with the in-channel ADC. Section VI contains the summary of the experimental characteristics of the active probe.

II. REVIEW OF INTEGRATED NEURAL INTERFACES

The high density of neurons in neurobiological tissue requires a large number of electrodes to obtain the most accurate representation of neural activity (e.g., to monitor spatial propagation of a seizure), and provide better control over the location of the stimulation sites [6]. When integrating a large number of recording and stimulation channels on a single chip, low power dissipation becomes a major constraint. Power density must be limited 0.8 mW/mm^2 [7], [8] to prevent tissue damage (and to provide a longer battery life for implantable systems). Also, a small form factor is required to ensure minimal tissue damage and tissue displacement during implantation [9]. Intrinsic circuit noise is often traded for low power and high density of integration.

A. Neural Stimulator Design Specifications

Neural stimulation arrays have been developed for various applications such as for use in cochlear and retinal prostheses [10]–[12]. Neural stimulation is typically performed by one of the following two approaches.

Voltage-mode stimulation establishes current flow by controlling the voltage between two electrodes. Voltage-mode stimulation has the advantage of higher energy efficiency [13]. Its main drawback is the lack of control over the charge delivered to the tissue due to variability of the tissue impedance. Tissue impedance varies from a nominal value of 10 kΩ to as high as a few MΩ due to cellular reactions [14]. Also, as the electrode tissue interface has a capacitive component, the instantaneous current between electrodes is not well controlled.

Current-mode stimulation establishes a well-controlled current between a pair of electrodes. Current-mode stimulation offers direct control over the charge delivered to the tissue due to the linear relationship between charge and current. Currents in the range of 10 μA–1 mA are sufficient to invoke a neural response [15]. Higher voltage compliance of current-mode neural stimulators allows the current driver to supply a wider range of currents to a given load. Maximizing the output impedance allows the current driver to maintain well-controlled current under variable load conditions. Current-mode neural stimulators often contain a digital-to-analog converter (DAC) to control the output current amplitude. Some designs use current-mode DACs as the output stage of the stimulator [12], [16], [17]; others use a voltage-mode DAC interfaced with a voltage-to-current converter circuit [18].

Safety is a major concern in the design of implantable neural stimulators. Adverse chemical reactions such as electrolysis, pH changes and tissue and electrode damage can occur whenever the tissue is exposed to prolonged DC currents, or if charge accumulation takes place in the tissue. It is essential to provide accurate control over the charge delivered and retracted, to and from the tissue, respectively. Various approaches for charge balancing have been used towards this goal as summarized in [19]. High accuracy and linearity of the current driver are thus important design considerations.

B. Neural Monitor Design Specifications

The amplitude of extracellular neural action potentials and LFPs (local field potentials) varies approximately between 20 μV and 500 μV, with abnormal neural signals (e.g., during a seizure) being as large as several millivolts [20], [21]. Action potentials and abnormal neural signals occupy the frequency band of 100 Hz–6 kHz (and by some estimates up to 10 kHz) and the amplitude of the signal is 50–500 μV [6]. The local field potentials (LFPs) have spectral content ranging from 0.1 Hz to 500 Hz [22] and their amplitude varies from hundreds of microvolts to several millivolts [23].

A neural recording channel should detect and amplify these low-amplitude signals, while keeping the input-referred noise of the channel below the background noise at the recording site, which is typically 5–10 μV [6]. Substrate noise, such as that due to the digital circuits on the same chip, can degrade the quality of the recorded signal. Also, 60 Hz noise from power lines and other types of common-mode noise have an adverse effect on the signal. A fully differential circuit architecture helps achieve a high common-mode rejection ratio (CMRR). DC offset and drift are common at the electrode site and can get as large as 1 V [6], [20]. An AC-coupled front-end circuit eliminates such phenomena.

C. Summary of Novel Contributions

The state of the art in the area of integrated neural interfaces design is presented throughout this paper where various components of neural interfaces are introduced, such as neural stimulator circuits in Section IV and neural recording circuits in Section V. A summary of the state of the art is given in Section VI (particularly Tables V, VI, and VII). Compared to the state of

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the art, the presented design includes the following key novel contributions.

At the circuit level, a neurostimulator current driver is introduced that yields both accurate charge balancing and high packing density. This is achieved by employing an in-channel current-mode sample-and-hold circuit that eliminates non-linearity inherent to neurostimulators employing in-channel voltage-mode sample-and-hold circuits or DACs [18], and avoids excessive integration area needed for neurostimulators with in-channel current-mode DACs [16], as detailed in Section IV-C. High output impedance is achieved without a significant area penalty by time-multiplexed reuse of the sample-and-hold circuit OTA for regulating the cascoded output current source.

At the very large scale integration (VLSI) architecture level, a system-on-chip for adaptive neurostimulation is introduced. It includes both a large number of neural stimulation channels (256) and a large number of neural recording channels (64). The former is needed for studying electrophysiological activity propagation in the brain, such as that of epileptic seizures, on a fine spatial scale (e.g., so-called microdomains [3]). The latter is required for studying optimum spatio-temporal neurostimulation patterns for neuromodulation and neural control [4], in applications such as intractable epilepsy treatment. The truly simultaneous nature of multi-site neurostimulation and that of multi-site neural recording is also an important aspect of this design. The former eliminates unwanted parasitic currents due to timing mismatches as needed for accurate time-aligned spatial neurostimulation pattern generation. The latter enables time-lag-free spatial neural data monitoring (e.g., for subsequent timing-sensitive epileptic seizure detection based on site-to-site neural signal phase synchrony computation).

At the microsystem integration level, we present a small-form-factor active probe with an iridium-oxide-tipped Utah electrode array bonded directly onto a CMOS die. To our knowledge, this is the first such implementation of a bidirectional active probe—that is it has both neurostimulation and neuromonitoring capabilities, time-multiplexed through the same electrode array.

At the application level, we experimentally validate such an assembled microsystem in a seizure propagation study in a mouse epilepsy model *in vitro*, in order to locate the area where a seizure initiates. The neural signals are truly-simultaneously sampled with 400 μm spatial resolution. Also, we provide key experimental evidence that on-line closed-loop neurostimulation using the presented bidirectional integrated neural interface IC and a seizure-predicting computer-in-the-loop is effective in controlling seizures in a rat epilepsy model.

III. ACTIVE PROBE SYSTEM ARCHITECTURE AND INTEGRATION WITH UTAH ELECTRODE ARRAY

We present a 0.35 μm CMOS bidirectional neural recording and stimulation active probe with 64 current-mode neural stimulation channels, and 256 fully-differential neural recording channels, each with an in-channel ADC. The stimulation mode is programmable and the stimulator current driver can provide square or arbitrary waveforms by means of an analog memory.
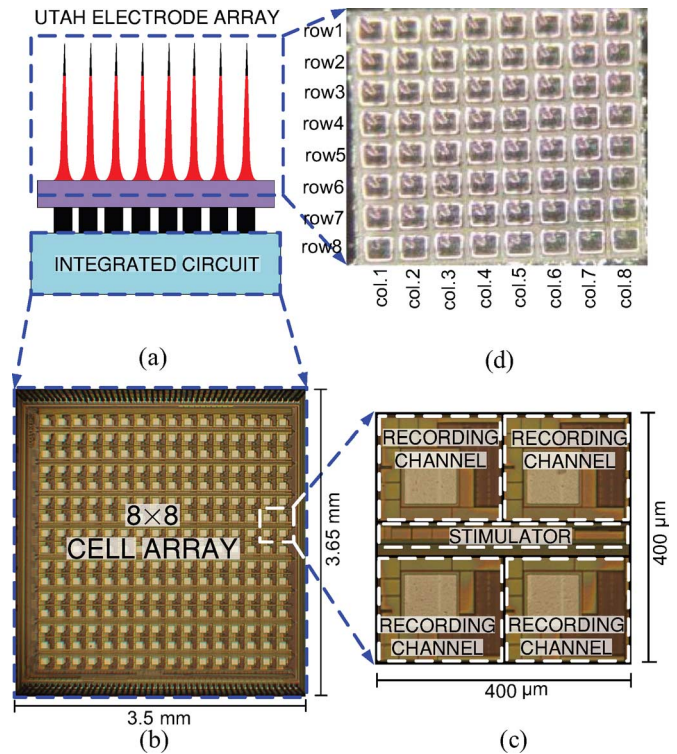

Fig. 3. Bidirectional active neural probe. (a) Cross-sectional view of the active probe including the Utah electrode array. (b) Micrograph of the integrated 64-channel neural stimulation and 256-channel neural recording interface implemented in a 0.35 μm CMOS technology. (c) Closeup view of a cell in the 8×8 cell array comprising one stimulation channel and four recording channels. (d) Photograph of the 8×8 Utah electrode array bonded directly onto the CMOS die in (b).

The memory in every stimulator allows for simultaneous stimulation on all active channels, which can not be achieved with conventional time multiplexing. The stimulators occupy only 0.02 mm^2 per channel. This is achieved by re-using the OTA in the stimulator in two different configurations, and sharing a single DAC (off-chip). These techniques also result in low quiescent power consumption of 2.76 μW per stimulator. The recording channel is fully differential, occupying an area of 0.035 mm^2 and consuming 51.9 μW. The sampling and quantization is performed simultaneously on all channels.

This design includes hybrid integration with a UEA with custom iridium oxide-coated tips, as needed for neural stimulation with a low electrode interface impedance. The Utah electrode array is bonded onto the integrated circuit (IC), as illustrated in Fig. 3(a), using a method reported by us in [24]. Fig. 3(b) shows the prototype fabricated in a standard 0.35 μm double-poly CMOS technology. The 3.5 mm $\times$ 3.65 mm die consists of an array of 16×16 neural recording channels organized on a 200 μm-pitch grid and interleaved with an array of 8×8 neural stimulator channels. Fig. 3(c) shows the closeup view of a tiled cell comprising one stimulator channel and four recording channels.

Bonding pads for the tissue I/O signals are also arranged on the same grid. Each bonding pad is connected to a recording channel input. One of every four pads is connected to a neural stimulator channel output. This results in a 400 μm pitch of stimulation electrodes. This pitch is chosen to match that of
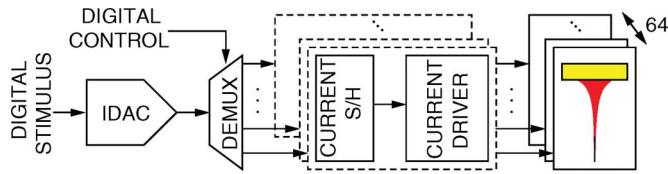
Fig. 4. Architecture of the current-mode neural stimulator with an in-channel sample-and-hold circuit and a single DAC.

the Utah electrode array (UEA) for direct bonding of the microelectrode array onto the CMOS die as shown in Fig. 3(d). The stimulation channels time-share 64 UEA shanks with 64 recording channels. The remaining 192 recording channels are available for connection to additional off-chip electrodes such as ECoG microgrids for greater spatial coverage of the brain cortex (Fig. 1) [25]. The integrated neural interface connects to a desktop computer-based seizure onset detector for analyzing intracranial EEG recordings in real time, which triggers the stimulators upon detection of a seizure.

IV. NEURAL STIMULATOR

A. Stimulator VLSI Architecture

Current-mode stimulation was chosen for the control it provides over the charge delivered to the tissue. The VLSI architecture of the neurostimulator is shown in Fig. 4. The choice of the stimulator architecture was dictated by the low area, low power, high output impedance and accurate charge balancing design constraints. A single current-mode DAC loads analog currents into up to 64 in-channel current-mode sample-and-hold circuits. The stimulators are individually addressable and any subset of them can be enabled or disabled. The output currents of enabled drivers are well-matched, as the same current-mode DAC is used to deliver the current being sampled.

The enabled stimulators are also capable of truly simultaneous stimulation without time-multiplexing. Truly simultaneous multi-site neurostimulation enables precise control of spatial stimulation pattern timing, as needed to modulate an expected neural response. The incorporation of an analog memory (current-output sample-and-hold circuit) in each current driver has two additional benefits. First, it saves on area because the DAC can be placed outside of the cell and shared by all the channels. Second, simultaneous stimulation prevents unwanted current flow due to timing mismatches.

The neural stimulator output stage is designed to supply a monophasic, biphasic or arbitrary-waveform current to the tissue with impedance Z_L. Monophasic stimulation applies a positive pulse with a certain amplitude and duration to the tissue. Biphasic stimulation applies a positive pulse followed by a negative pulse to the tissue such that the areas under the two pulses are equal, which ensures the charge applied to the tissue is refracted. Arbitrary-waveform neurostimulation is provided by storing the desired waveform in the form of an analog current samples sequences in the analog memory, one sample at a time, and delivering it over multiple cycles.

The neural stimulator can be configured in either monopolar or bipolar configuration. Monopolar stimulation is performed
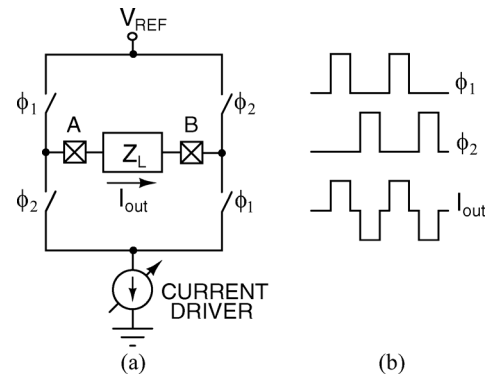

Fig. 5. (a) A general implementation of bipolar biphasic neurostimulation. (b) A corresponding output waveform.

by a single active electrode and a reference electrode. Bipolar stimulation is performed by two active electrodes placed close to each other, as needed for local stimulation.

Fig. 5 illustrates the bipolar biphasic stimulation configuration. Each electrode site that is connected to a stimulator can be connected either to the current driver or a reference voltage. During the anodic phase, ϕ_1 is high and the current is flowing from site A to site B. During the cathodic phase, ϕ_2 is high and current is flowing from site B to site A. The amplitude and duration of the current pulses during the two phases need not be the same. However, the area under the anodic and cathodic phases of the current waveform should be equal in order to satisfy the charge balance requirement. The stimulator is fully programmable and the amplitude and duration of each pulse can be set independently. The voltage transitions on the electrodes during switching is of little consequence as the tissue is not connected to the ground in the bipolar configuration. A key challenge is to generate accurate currents for varying tissue impedances in order to ensure proper charge balancing.

B. Existing Current Driver Circuits

There are several approaches to set the output current of a stimulation current driver. One way is shown in Fig. 6(a) [26]. A current-mode DAC is used to set the current which is then copied through a current mirror to the output. The output impedance of this topology is of the order of r_o of the output transistor. This design suffers from high power consumption, which can be reduced by moving the DAC to the output path, as shown in Fig. 6(b) [11].

It is desirable to increase the output impedance of the current driver to reduce the sensitivity of the output current to the load impedance variations. Introducing another transistor to the output path with an active feedback significantly increases the output impedance of the current driver, as demonstrated in Fig. 6(c). The output current is set by the voltage-mode DAC that drives the gate of transistor M_1. If V_b is sufficiently small, transistor M_1 will be biased in the triode region and used as a voltage-controlled resistor [18]. This technique increases the output impedance significantly. The linearity of the transistor in triode region is compromised by the effect of mobility degradation, making the drain current not linear with the overdrive voltage. The compensation circuit introduced in [18] increases

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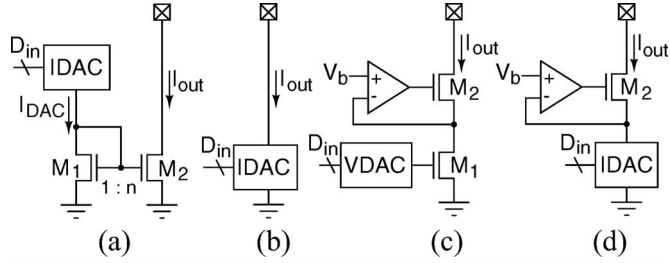

Fig. 6. Existing current driver designs. (a) Current-mode DAC with current mirror. (b) Current-mode DAC used in the output path. (c) Adding active feedback to increase output impedance of the current driver. (d) Improving linearity by using current-mode DAC.

the power consumption of the stimulator. One way to reduce the nonlinearity is to reintroduce the current-mode DAC to the output current path, as shown in Fig. 6(d) [16].

None of the designs described above incorporate memory in the stimulator which means that truly simultaneous stimulation cannot be performed on several channels. Another disadvantage is the necessity to include a DAC with every stimulator circuit, which increases the area and often power dissipation of the stimulator.

C. Current Driver

The current driver overcomes the above-mentioned problems by storing the stimulation current and stimulating through the same path, without requiring a DAC in every stimulator circuit. This provides an advantage in terms of accurate current copying, small area and low power consumption.

The current driver circuit is illustrated in Fig. 7(a). The programmable stimulator consists of three major blocks: digital memory, digital control and a high output impedance current driver. The driver operates in two phases: setup phase and active phase. During the setup phase, the stimulation sites are sequentially addressed, the analog input current is sampled by the analog memory, and the digital memory is programmed with a 2-bit code which represents the state the output stage of the stimulator will be in during the active phase. During the active phase the stored currents are held and simultaneously delivered to the tissue by all enabled current drivers. This procedure can be repeated for multiple current samples to generate an arbitrary waveform.

The code (m_0, m_1) stored in the digital SRAM memory acts as the input to the control logic block and along with the $Clock$ and $Phase$ inputs configures the switch network to put each site into its desired state. The different states and the corresponding switch configurations are described in Table I. The state of switches in the two phases of operation is illustrated in Fig. 7(b) for two stimulation sites, A and B.

To prevent DC currents from going through the tissue, all stimulating sites that are not in use are configured as a high impedance node. Also, after a stimulation period all electrodes can be connected to a common analog line (CAL) in order to remove any charge that has accumulated at the electrode-tissue interface. This is activated by the switch S_5 and the user determines the timing of connection to CAL by controlling the m_0 and m_1 bits. During the CAL phase each stimulation site is

(a)

(b)
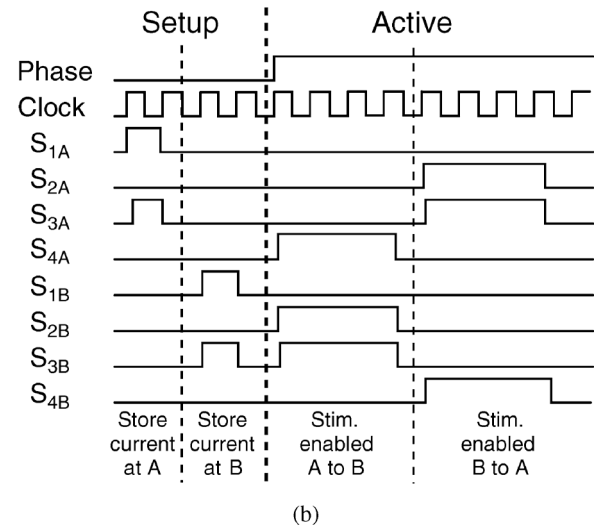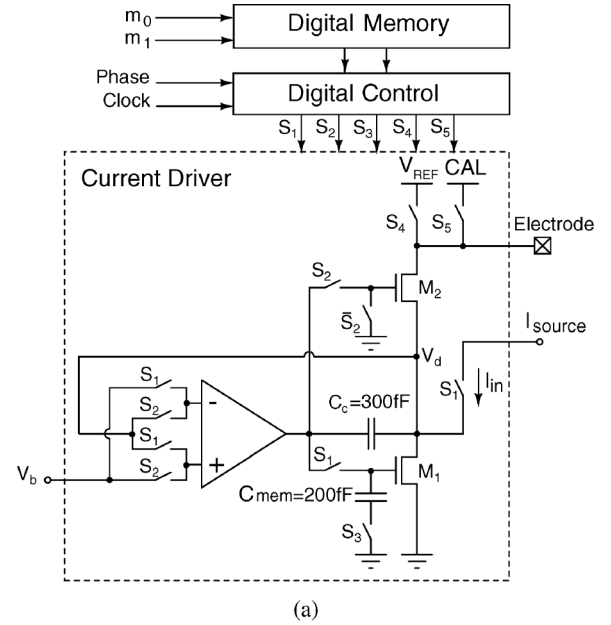
Fig. 7. (a) Current driver circuit diagram. (b) Timing diagram for implementing a biphasic stimulus.

TABLE I
STIMULATOR SWITCH NETWORK CONFIGURATION

State	ON Switches	Phase
High Impedance	-	-
CAL	S_5	Active
V_{REF}	S_4	Active
Current Storage	S_1, S_3	Setup
Current Delivery	S_2, S_3	Active

disconnected from the respective channel output. This ensures that no unsafe current flows through the tissue. Additionally, the voltage CAL provided from an off-chip voltage regulator can be connected through a resistor, in order to avoid excessive discharge current spikes.

The main components of the current driver are an operational transconductance amplifier (OTA), and two transistors M_1 (4×5.5 μm/0.5 μm) and M_2 (4×8 μm/0.5 μm). These

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Fig. 8. Current sink configured in (a) sampling (setup) phase and (b) hold (active) phase. The same OTA is reused.

Fig. 9. Folded-cascode OTA in the stimulator current sink (OTA1).

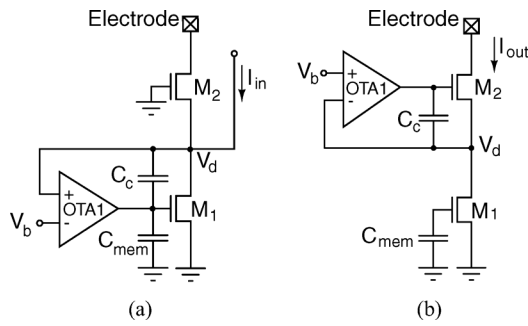components are reconfigured into two different circuits for current storage (during setup phase) and current driving (during active phase) using switches. The two circuit configuration are shown in Fig. 8. Fig. 8(a) shows the current driver configured for current sampling (setup) phase. In this phase, the circuit is a constant-V_{DS} current sampler [27]. The desired current flows through transistor M_1. The drain voltage of transistor M_1 is held constant at the potential of V_b (bias voltage provided off-chip) through the OTA feedback, which compensates for the channel length modulation effect. The gate voltage of M_1 is driven by the OTA to the proper level that corresponds to the current and is stored in the 200 fF capacitor C_{mem}. The sampling phase is as short as 33 μs.

Fig. 8(b) shows the current driver during the hold (active) phase, configured as a typical current sink. The negative feedback around M_2 serves two purposes. First, it boosts the output impedance of the current sink. This is a well established gain boosting technique that increases the output impedance of the current driver, making it less sensitive to the load impedance [16], [18]. Second, it forces the drain voltage of M_1 to the potential V_b. This, along with the sampled gate voltage that is kept by C_{mem}, ensures that the current flowing through M1 during the second phase accurately matches the stored current. Capacitor C_c is a 300 fF compensation capacitor and is used to stabilize the node V_d during the switching from one configuration to the other. Current sampling comes at the cost of a small overhead in power as the sampling phase is much shorter than the hold phase (as long as 33 μs for less than 5% capacitor C_{mem} charge leakage).

High output impedance of the current sink requires the OTA to have a large gain

$$R_{\text{out}} \approx A g_{m2} r_{o2} r_{o1}, \qquad (1)$$

where A is the gain of the OTA, g_{m2} is the transconductance of transistor M_2, r_{o2} is the output impedance of transistor M_2 and r_{o1} is the output resistance of transistor M_1. The OTA has a PMOS-input folded-cascode configuration, as shown in Fig. 9. It provides a gain of 93 dB at a common mode input voltage
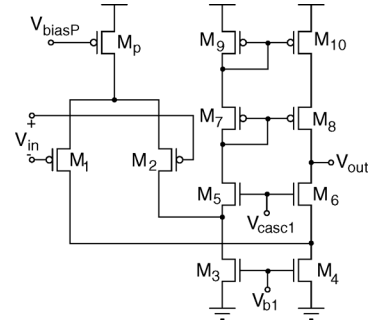
TABLE II
TRANSISTOR SIZES

Transistor (OTA1)	W/L (μm)	Transistor (OTA2)	W/L (μm)
$M_{1,2}$	2/4	$M_{1,2}$	$4 \times 5.35/7$
$M_{3,4}$	1/5	$M_{3,4}$	$2 \times 3/12$
$M_{5,6}$	1/6	$M_{5,6}$	1.5/10
$M_{7,8}$	1/4	$M_{7,8}$	1/20
$M_{9,10}$	1/4	M_p	2/6
M_p	1/5	$M_{9,10}$	1/3.25
$--$	$--$	$M_{11,12,13,14}$	1/20
$--$	$--$	$M_{15,16}$	1/20
$--$	$--$	$--$	$--$

Transistor (OTA3)	W/L (μm)	Transistor (Comp.)	W/L (μm)
$M_{1,2}$	$2 \times 1/4$	$M_{1,2,3,4}$	$2 \times 2/1$
$M_{3,4}$	1/6	$M_{5,6}$	1/2
$M_{5,6}$	1/15	$M_{7,8}$	0.8/0.35
$M_{7,8}$	1/12	$M_{9,10}$	$2 \times 1/1$
$M_{9,10}$	1/15	$M_{11,12}$	1/0.35
M_p	1/6	$M_{13,14}$	1/4
$M_{11,12}$	1/6.3	$M_{15,16}$	1/8
$M_{13,14,15,16}$	1/20	$M_{17,18}$	1/0.35
$M_{17,18}$	1/6	M_{19}	$4 \times 1/0.35$

$V_b = 300$ mV. The OTA consumes a bias current of 0.88 μA. The transistor sizes are listed in Table II.

D. Neurostimulator Experimental Characterization

The stimulator was experimentally characterized by feeding the stimulation current through an external resistor. Fig. 10 compares the measured and simulated input-output characteristics of the current driver. The output current is lower than the input current due to the effects of charge injection at the gate of transistor M_1. Due to the systematic nature of this error the mismatch can be calibrated for in software. Another method to avoid this issue is to use bottom plate sampling technique by slightly advancing the edge of the signal that turns off the switch S_3 with respect to that of switch S_1.

Fig. 11 shows the simulated and measured performance of the current driver under variable load conditions. The plot shows the operating region of the current driver for three neurostimulation current values.

The voltage at the electrode site can be as low as 700 mV for the driver to remain properly biased, resulting in a voltage compliance of 2.6 V for the supply voltage of 3.3 V. The 2.6 V compliance is sufficient for a nominal load (tissue impedance) of 10 kΩ when using the maximum stimulation current of 250 μA.

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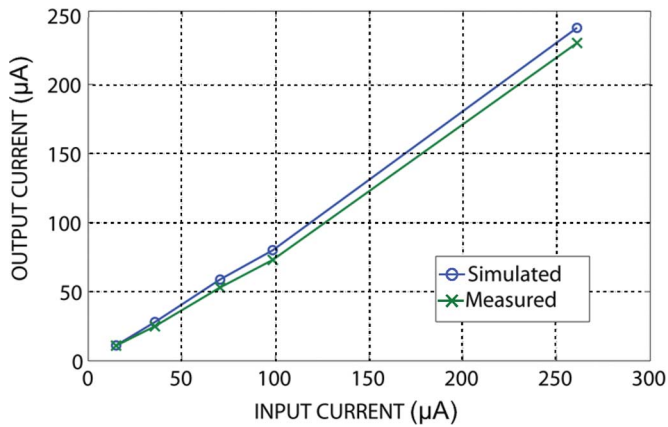

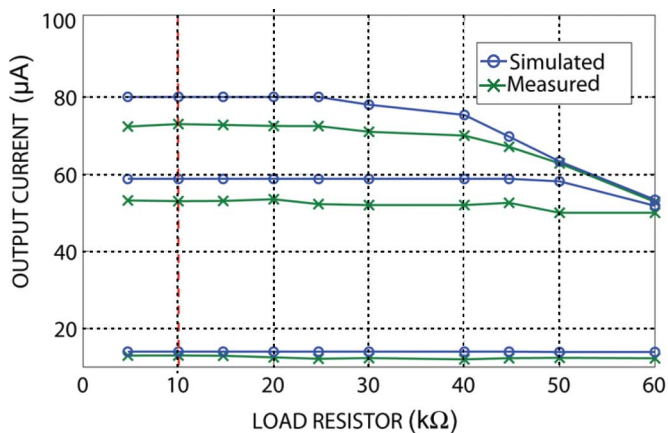Fig. 10. Transfer characteristic of the current driver for 10 kΩ load.

Fig. 11. Output of the current driver under variable load conditions.

Currents above 250 μA will drive the circuit out of the linear region even for the nominal load of 10 kΩ.

V. Neural Recording Channel

The system includes an array of fully differential digital neural recording channels in order to enable adaptive neurostimulation. The non-inverting input of the recording channel is connected to a local electrode. The inverting input of the recording channel has an option to either be connected to an adjacent electrode or a common reference electrode. Similar to the neurostimulator, these two configurations allow for two types of neural recordings: a localized differential (bipolar) recording, and a global (monopolar) recording with respect to a distant common reference.

Bipolar recording yields the difference between two signals recorded by two adjacent electrodes [28]. As a result, any noise on the reference electrode is eliminated and the recorded signals contain less contribution from remote signal sources [29]. Physiologically, a bipolar recording corresponds to the fluctuations of local electrical activity taking place between two adjacent electrodes.

Bipolar recording also subtracts common fluctuations at the two sites. When such signals need to be recorded, a common reference is used for the recording, known as monopolar recording. Each recording represents a global recording obtaining signals from a wider spatial area with respect to the common reference.
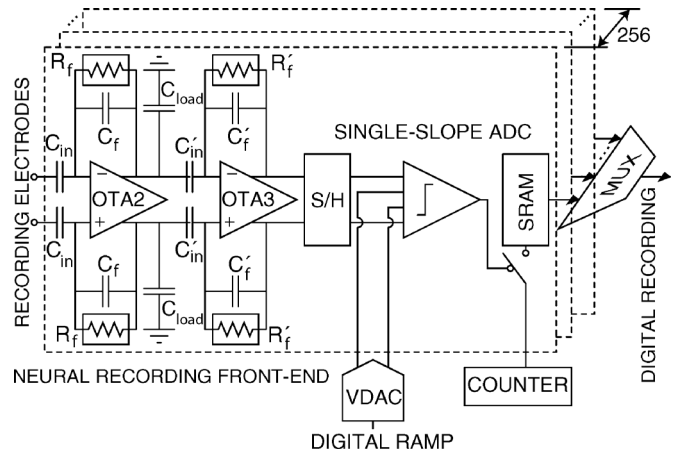

Fig. 12. Neural recording channel VLSI architecture.

A. Neural Recording Channel Architecture

The architecture of the recording channel is depicted in Fig. 12. Each recording channel consists of two stages of filtering and amplification, a sample-and-hold circuit and a single-slope ADC. The input capacitors reject electrode-tissue DC offset at the input terminals. The in-channel sample-and-hold cell allows for truly simultaneous multi-site neural recording without time-multiplexing. Truly simultaneous sampling is important in our implementation of the epileptic seizure detector described in Section VI-B, as it requires accurate computation of phase synchrony (without a time lag) among two or more neural signals.

The channel is fully differential to reduce sensitivity to the common-mode noise. Distributing the overall gain over two stages helps achieve a large gain while maintaining smaller capacitor sizes and higher linearity.

The differential signal transfer function of the first (and similarly the second) stage is

$$T(s) = \frac{s \frac{C_{\text{in}}}{C_f}}{s + \frac{1}{R_f C_f}}, \tag{2}$$

where R_f refers to the resistance of the feedback. The sizes of the capacitors are limited by the available area, whereas the capacitor size ratios are chosen to meet the channel design specifications.

The closed-loop gain is determined by the product $C_{\text{in}}/C_f \times C'_{\text{in}}/C'_f$. In the first stage $C_{\text{in}} = 4$ pF and $C_f = 100$ fF which results in a gain of 32 dB. In the second stage a variable gain amplifier is implemented by using a programmable bank of capacitors in the feedback. The input capacitor is $C'_{\text{in}} = 2.5$ pF. The capacitance in the feedback, C'_f, can be programmed to eight values from 25 fF to 200 fF. This results in eight gain modes from 22 dB to 40 dB. The overall gain of the two stages is therefore adjustable from 53 dB to 72 dB.

The high-pass filter corner frequency is determined by $1/(2\pi R_f C_f)$, where R_f is the feedback resistance. Since C_f should be small to ensure large gain, R_f should be high to set the high-pass corner frequency as low as possible. A good way to implement large resistance in CMOS technology without

sacrificing area is to use a MOS device in subthreshold region [30]. The HP cut-off frequency is tunable from 0.1 Hz to 10 Hz. Resetting the feedback resistive elements can be used to achieve faster recovery from saturation due to the stimulation artifact. The first stage low-pass filter cut-off frequency is set to 5 kHz by the combined effect of the load capacitor C_{load} and the bias current of the amplifier. By changing the bias current of the amplifier it can be tuned from 500 Hz to 10 kHz.

B. Neural Amplifier

The main considerations in the design of the neural amplifier are noise and power consumption, one coming at the expense of the other. Various OTA topologies have been used for the implementation of neural amplifiers, e.g., folded-cascode, current mirror and two-stage [31]–[34]. The common factor with these topologies is the large output swing. Large output swing is important at the output stage of the amplifier, but comes at a cost of higher power consumption due to the large number of current branches.

In the presented design the gain is distributed over two stages with the goal of saving power. Signal spectrum considerations matter in the choice of the first stage output dynamic range and thus of its OTA topology power requirements. In order to capture low-frequency potentials (LFPs) important for detecting epileptic seizures, the required lowest signal frequency is small (as small as 0.1 Hz). This cut-off frequency should be ideally set by the high-pass filter (HPF) of the second stage. For low noise, the 1st stage should ideally have a much lower HPF cut-off frequency than that of the second stage. This enables the second stage to filter the low-frequency noise due to the first-stage feedback pseudo-resistors. Such a design choice requires the first stage OTA to have a wide output dynamic range at the cost of more power. This is needed to avoid first-stage OTA output saturation due to low-frequency artifacts (i.e., falling below the cut-off frequency of the second stage HPF). However, in this implementation the junction leakage in the first stage pseudo-resistors when biased for such a low cut-off frequency results in prohibitively large input voltage drift. In this design the HPF frequency is set by the first stage at the expense of a moderate increase in noise. This in turn allows for the use of a telescopic cascode OTA in the first stage, which is a narrow-swing but low-power topology. This design choice also eliminates high non-linear distortion due to a non-linear pseudo-resistor in the feedback of the second stage that experiences large voltage swings. The fully differential telescopic OTA of the first stage and the common-mode feedback (CMFB) circuit are shown in Fig. 13. Transistor sizes in this amplifier are listed in Table II.

Two types of noise have to be accounted for in the design of the telescopic OTA. Both can be modeled as voltage sources in series with the input. The input-referred thermal noise per unit bandwidth is

$$\overline{V_n^2} = 2\left[\frac{4kT}{g_{m1}}\left(\frac{2}{3}\right)\left(1 + \frac{g_{m7}}{g_{m1}}\right)\right]. \tag{3}$$

To minimize the thermal noise contribution, transistors $M_{1,2,7,8}$ have to be biased such that $g_{m7,8} \ll g_{m1,2}$. For a fixed bias
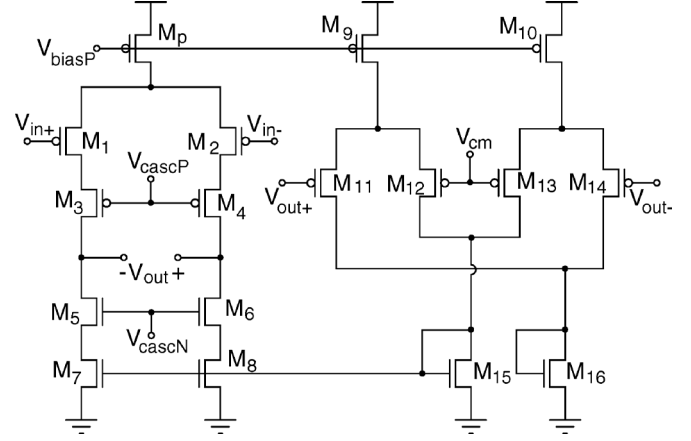

Fig. 13. Telescopic amplifier in the first stage of the recording channel (OTA2).

current it means that the sizes should be such that $W/L|_{7,8} \ll W/L|_{1,2}$, which puts $M_{1,2}$ in weak inversion and $M_{7,8}$ in strong inversion. Increasing the bias current will further increase $g_{m1,2}$ resulting in additional reduction of the thermal noise component at the expense of higher power dissipation.

The input-referred flicker $1/f$ noise per unit bandwidth is

$$\overline{V_n^2} = 2\left[\frac{K_P}{C_{\text{ox}}W_1L_1} + \frac{K_N}{C_{\text{ox}}W_7L_7}\left(\frac{g_{m7}}{g_{m1}}\right)^2\right]\frac{1}{f}. \tag{4}$$

The major contribution of $1/f$ noise comes from transistors $M_{1,2}$. Reduction in $1/f$ noise is achieved by choosing the input transistors to be of the PMOS type, which have a lower $1/f$ noise coefficient than NMOS transistors $(K_P < K_N)$, and maximizing the gate area of these transistors.

The CMFB circuit [35] is designed with the same bias current as the amplifier. The output swing of the CMFB circuit is maximized by increasing the overdrive voltage of the input transistors M_{11-14}. For a given bias current this is achieved by sizing M_{11-14} to have the minimal W/L ratio.

In the design of the second stage OTA, OTA3, a higher noise level can be tolerated due to signal amplification in the first gain stage. Therefore, the focus is on minimizing power dissipation and having adequate output swing. A folded-cascode OTA is chosen for the second stage with a total bias current of 1.5 μA, which is almost half of the first stage bias current. The CMFB circuit in the folded-cascode OTA is the same as the one in the telescopic OTA. The schematic of the folded-cascode OTA and the CMFB circuit is shown in Fig. 14. The sizes of the transistors in this implementation are listed in Table II.

The experimentally measured amplitude frequency response of the two filtering and amplification stages is shown in Fig. 15. The gain was set to the minimum and the high-pass filter corner frequency was adjusted by changing the bias voltage of the feedback pseudo-resistors. As described earlier in this section, the high-pass cut-off frequency of the channel is set by the capacitive and resistive feedback elements of the first stage. The resistive element is implemented as a PMOS transistor with the gate controlled by voltage V_{res}. As the signal frequency reduces and reaches the high-pass roll-off region, the first stage output voltage swing decreases and leads to an increase in the effective
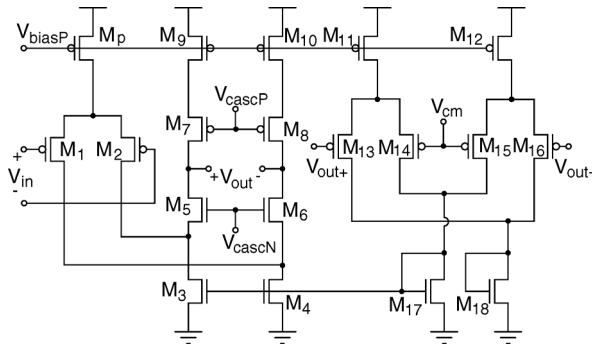
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Fig. 14. Folded-cascode amplifier in the second stage of the recording channel (OTA3).

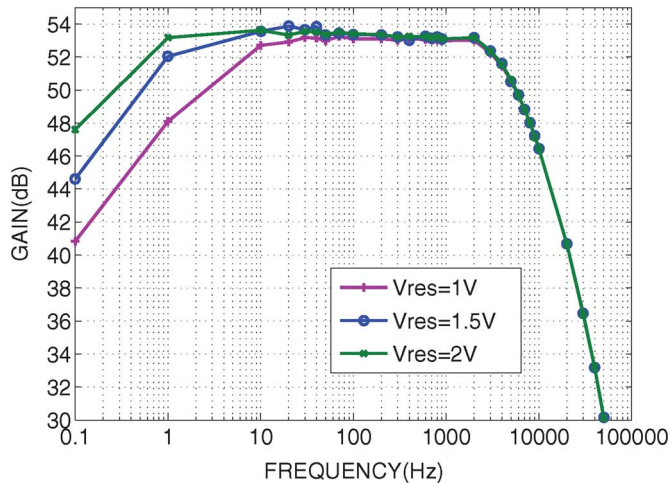

Fig. 16. Comparator in the ADC.

Fig. 15. Experimentally measured amplitude frequency response of the full channel with the gain set to minimum setting of 53 dB.

resistance of the feedback PMOS transistor [36]. This in turn pushes the pole to a lower frequency and exhibits itself as a reduction in the HPF roll-off slope, below the nominal 20 dB/dec value, near the nominal pole frequency. We have proposed solutions to this issue in [36].

The input-referred noise has been experimentally measured. Integrating the noise over the bandwidth of 10 Hz–5 kHz results in the overall input-referred noise of 7.99 μV_{rms}.

C. Sample-and-Hold Circuit and ADC

The architecture of the in-cell fully differential single-slope ADC is shown in Fig. 12. Considering the amplitude of the neural signals and the background noise at the recording site, an ADC with 8-bit resolution is sufficient for this application [20].

The in-channel ADC consists of a fully differential comparator and an 8-bit SRAM block. The differential ramp for the comparator and the 8-bit channel address are generated off-chip by a ramp generator and a counter. Both the ramp generator and the counter are common to all ADCs as quantization takes place simultaneously on all channels. The frequency of the clock that generates the digital ramp and the time-domain multiplexed address can be adjusted according to the signal that is being recorded. The address clock frequency for recording from 8 channels is 200 kHz and for recording from 256 channels is
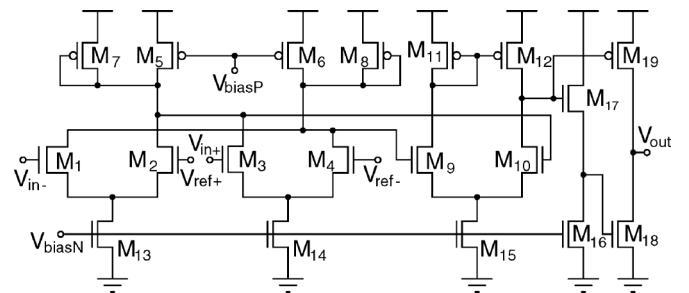
6.4 MHz. The ramp generator period is set to be equal to the address clock period to acquire one sample in each period. In future implementations the ramp generator and the counter can be implemented on chip as one of the peripheral circuits without significant area and power overhead.

To properly quantize the neural data one needs to sample at a Nyquist rate of twice the low-pass cut-off frequency with an additional margin to allow for the roll-off of the filter. This results in a sampling rate of 15 kHz per channel, or 65 μs sample time. All channels are sampled simultaneously with the sample stored in the analog memory as described in [37]. This takes 32 μs. Then the quantization begins on all channels simultaneously and takes 20 μs, which is the time it takes the counter to count to 256 with a clock of 12.5 MHz. The data is then read out by addressing each channel sequentially with 4-bit row/column-select signals passed through decoders. The readout rate is 20 MHz, limited by the instrumentation data rate. It takes 13 μs to read out all 256 channels.

The comparator [38] is designed to consume 13 μA from a 3.0 V supply. The ADC (comparator and SRAM) occupies an area of 0.00725 mm^2. The schematic of the comparator in the ADC is shown in Fig. 16. The transistor sizes of the comparator are listed in Table II.

D. Recording Channel Characterization

The full channel (amplifier and ADC) was characterized experimentally. A 50 Hz sine wave was applied differentially to the input of the first stage and passed through the two stages of amplification and the ADC. The spectrum of the output signal is shown in Fig. 17. The maximum channel low-pass filter (LPF) cut-off frequency is 10 kHz. In practice the LPF cut-off frequency is set to several hundred hertz as the energy of epileptic neural signals of interest is mainly concentrated well below this frequency. For this reason the tone frequency and the sampling rate to measure SNDR are chosen to be 50 Hz and 5.1 ksps, respectively, as depicted in Fig. 17. Due to a maximum pin count constraint, the ADC input is not connected to I/O pads, and the stand-alone ADC ENOB is not reported here. Instead, the ENOB is reported for the entire channel signal path. The dominant non-linearity limiting the ENOB of the channel to 5.1 bits is that of the pseudo-resistive feedback elements. We have recently reported on detailed analysis of such elements and their non-linearity in [36].

The channel ENOB of 5 bits or more has been found sufficient for the application of epileptic seizure detection [39]. The epileptic seizure detection algorithm [40], [41] performs 16-tap
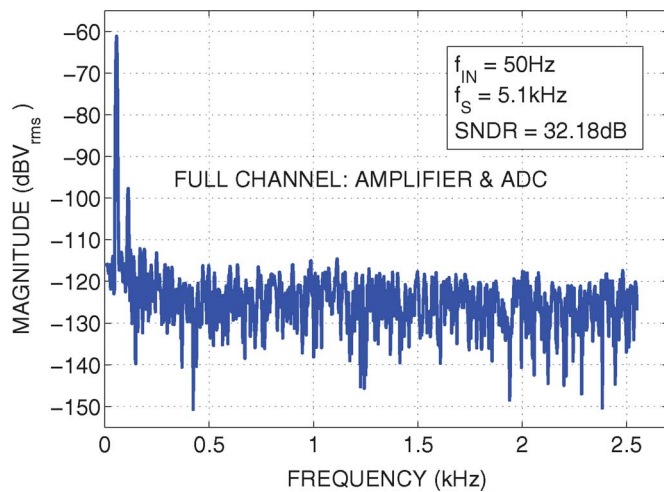
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Fig. 17.   Measured output spectrum for the full channel including the ADC.

TABLE III
IC EXPERIMENTAL CHARACTERISTICS

System	
Technology	$0.35\mu m$ CMOS
Supply Voltage	3.0V
Die Dimensions	3.5mm×3.65mm
No. of Recording Channels	256
No. of Stimulation Channels	64
Power Dissipation	13.5mW
Neural Amplifier	
Programmable Gain	53-72dB
Low Frequency Cut-off	0.1-10Hz
High Frequency Cut-off	500Hz-10kHz
Input-Referred Noise	$7.99\mu V$
Power Dissipation	$12.9\mu W$
NEF	8.9
CMRR (200Hz)	60dB
THD ($1mV_{pp}$)	0.8%
Stimulation Channel	
Quiescent Power	$2.76\mu W$
Output Current	$20\text{-}250\mu A$

FIR filtering on the digitized raw neural data. This filtering includes multiplication of the input by digital tap coefficients and subsequent addition over all 16 taps. It is shown in [39] that the filter output can be truncated to 10 bits without a significant loss in seizure detection accuracy. This implies that the channel ENOB of 5 bits is sufficient. The seizure detection algorithm is described in more detail in the next section.

VI.   EXPERIMENTAL VALIDATION

Measurement results from the 0.35 μm CMOS integrated circuit are summarized in Table III. 256 recording channels consume 13.5 mW from a 3 V supply. Power dissipation in the 64 stimulation channels is dominated by the output current. The integrated system was validated experimentally *in vitro* and *in vivo* as described next.

A.   In Vitro Validation

The integrated circuit bonded to a 64-shank Utah electrode array with low impedance iridium oxide tips, was validated experimentally in recording epileptic neural activity in a mouse hippocampus slice *in vitro*. An intact hippocampus slice was
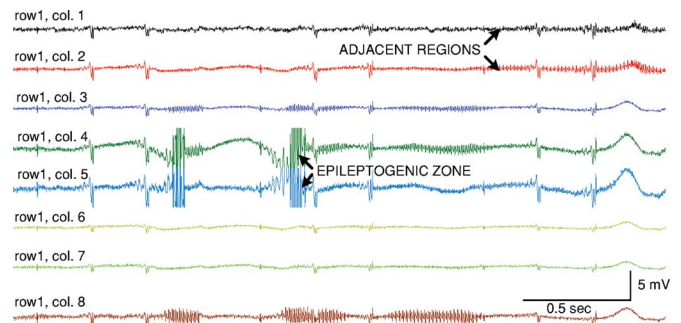

Fig. 18.   Epileptic neural activity recorded by the active probe through eight on-chip UEA electrodes in one row from a mouse hippocampus slice.

placed on the electrode array bonded onto the CMOS die and perfused. A low-glucose perfusing solution was used to invoke epileptic activity. Recorded neural spikes on 8 selected channels out of 64 are shown in Fig. 18. In this figure, electrographic seizure activity has originated from two sites, (1, 4) and (1, 5), and propagated to other adjacent channels. Proper analog circuit layout design techniques were employed to keep the channel-to-channel cross-talk below the noise floor. This is evident from observing traces 5 and 6 in Fig. 18 during the epileptic electrographic activity bursts. Experimental procedures were approved by the ethics committee of Toronto Western Hospital (Toronto) and experiments were conducted at the Neuroscience and Mental Health Research Institute, Toronto Western Hospital.

B.   In Vivo Validation

The integrated circuit was also validated in neural signal recording, epileptic seizure detection, and subsequent electrical stimulation for electrographic seizure abortion in acute *in vivo* rat experiments. Experimental procedures were approved by ethics committee of Hospital for Sick Children (Toronto) and experiments were conducted at the Neuroscience and Mental Health Research Institute, Hospital for Sick Children.

The epileptic seizure detection method was previously introduced by us in [40], [41]. We demonstrated that the phase locking value (PLV) between two or more EEG signals is a good precursor of ictal events and thus can be used to detect a seizure onset. PLV is proportional to the fluctuations in the phase difference of two channels and is calculated as the absolute value of the derivative of time series, $|d(\Delta\Theta)/dt|$, where $\Delta\Theta$ is the phase difference between two selected channels. Generally, phase differences and PLV are calculated using the mean phase coherence statistic (1 second running window), which is defined as PLV $= |\langle e^{d(\Delta\Theta)}\rangle|$.

Four Wistar rats (250 g–300 g) underwent craniotomy with general anaesthesia, as shown in Fig. 19(a). A microelectrode with a microcannula was implanted in the somatosensory area in the right hippocampus. Another microelectrode was implanted in the right frontal lobe. The reference electrode was placed in the left frontal lobe. The location of electrode implantation was chosen based on preceding seizure propagation studies, such as those described in Section VI-A. Placing the recording electrode in the epileptogenic zone (seizure origination area) generally yields the earliest seizure detection time. It is widely accepted

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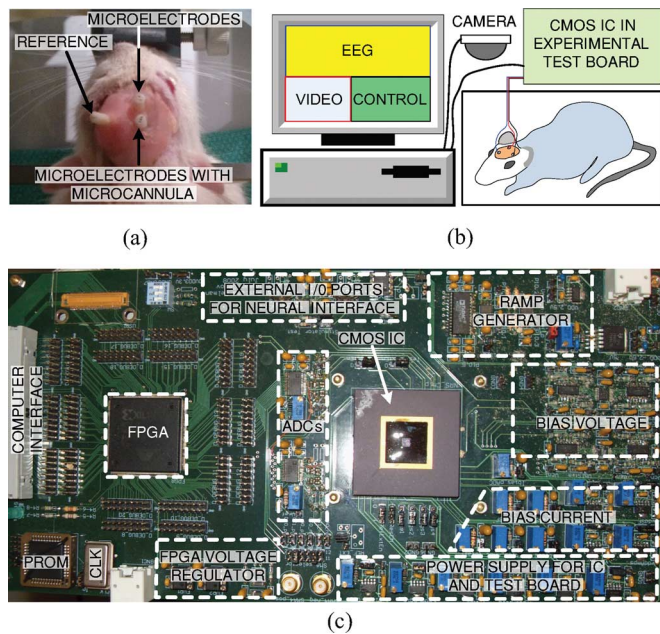
Fig. 19. *In vivo* experiment. (a) Microelectrodes implantation. (b) Video-EEG recordings setup. (c) PCB prototype used in the experiment.

that efficacy of seizure control improves with earlier seizure detection.

After the implantation, the rats were placed in a cage for video-EEG recording while freely moving, as illustrated in Fig. 19(b). Monopolar basal EEG recording was performed at 10 kHz sampling rate and animal behaviour was monitored simultaneously using video cameras for 7 days, 4 hours per day. The printed circuit board for *in vivo* recording is shown in Fig. 19(c).

Fig. 20(a) shows basal EEG recording from frontal lobe (V_F), and hippocampus (V_H) of a rat. The corresponding PLV computed off-chip for seizure onset detection is also shown. The PLV for the basal EEG recordings remained in the range of 0.4 to 0.8 under normal conditions.

Focal seizures were induced by intracerebral injection of 4-aminopyridine (4-AP, a selective blocker of the Kv1 family of voltage-activated K+ channels) of 300 nmol dose, diluted in $2\,\mu L$ of sterile 0.9% saline solution and sonicated for two minutes to have uniform suspension and adequate concentration of the drug. At first, the rats were anesthetized with isoflurane and $8\,\mu L$ of 4-AP solution was injected through the microcannula into the hippocampus. After injection, the rats were connected to the chip through the implanted electrodes for recording spontaneous recurrent electrographic seizures.

The rats were monitored for clinically associated behaviors for four hours by video cameras. Seizures were monitored and marked according to the Racine scale [42]. All seizure-induced animals were divided into two groups: (a) non-treatment and (b) treatment groups. In the non-treatment group (2 rats) seizures were monitored, marked and the seizure frequency per hour was determined for each rat. This group had 7 seizures per hour on average and their seizure behavior was noted in Racine scale of 0 to 3 (0—behavioral arrest (motionless), hair raising, excitement and rapid breathing; 1—mouth movement of lips and

tongue, vibrissae movements and salivation; 2 = head clonus and eye clonus; 3 = forelimb clonus, wet dog shakes) [42]. An induced electrographic seizure recording is shown in Fig. 20(b) where the PLV between V_F and V_H computed off-chip dropped abruptly down to 0.2 at seizure onset, indicating seizure onset detection.

The treatment group (two rats) received electrical stimulation upon seizure onset detection. Implanted microelectrodes of this group were connected externally to the presented chip. The recorded intracranial EEG was analyzed in a desktop computer-based seizure onset detector using Matlab, on-line in real time every two seconds. In response to a seizure onset, the seizure detector triggered the neurostimulators to send a burst of electrical stimulation current. This responsive system uses the lower PLV (seizure onset PLV threshold = 0.2) to trigger a 5 Hz 220 μA monophasic monopolar stimulation current for 5 seconds in the hippocampus. Stimulation pulse width is varied between 150 μs and 230 μs. Every cycle the injected charge is refracted from the tissue through the reference electrode.

Fig. 20(c) demonstrates the responsive electrical stimulation and seizure abortion in a treatment group rat hippocampus. In this experiment, recording was temporarily disabled during stimulation in order to avoid stimulation artifact.

The zoomed-in inset in Fig. 20(d) shows seizure onset detection in more detail. The system triggered the stimulation 7.5 times per hour on average. Late seizure detection was observed 0.75 times per hour and false detections happened 0.5 times per hour. Using the closed-loop stimulation, seizure frequency in the treatment group dropped down to the average of 0.75 seizures per hour (~89% seizure reduction). The efficacy of the system in seizure onset detection and seizure rate reduction in the non-treatment group and treatment group rats are summarized in Table IV. Next, we plan to monitor phase synchrony on multiple pairs of recorded signals to further improve seizure onset detection performance and to stimulate on multiple channels to further improve seizure control.

C. Comparative Analysis

Next, the proposed system is compared with recently published neuromonitoring and neurostimulation systems. In Table V, this design is compared with other current-mode stimulators. Previously published neurostimulators with more than 16 channels require time-multiplexing and cannot stimulate on multiple channels simultaneously. Larger currents, up to 1 mA, are achieved by having a higher power supply voltage [26]. The designs in [16] and [45] utilize an area-consuming active feedback in order to maximize the output impedance. The presented design performs simultaneous multi-site stimulation and has the lowest reported area.

Table VI compares the recording channel presented in this work with other published designs The low input-referred noise reported in [33] comes at the expense of increased power consumption. The design in [51] is the only one that reports a smaller area, but utilizes a denser 65 nm CMOS technology.

Table VII compares the neurostimulation and neuromonitoring system presented here to other bidirectional integrated neural interfaces. The design in [55] does not have an on-chip ADC. In [26] the low overall power consumption is in part due
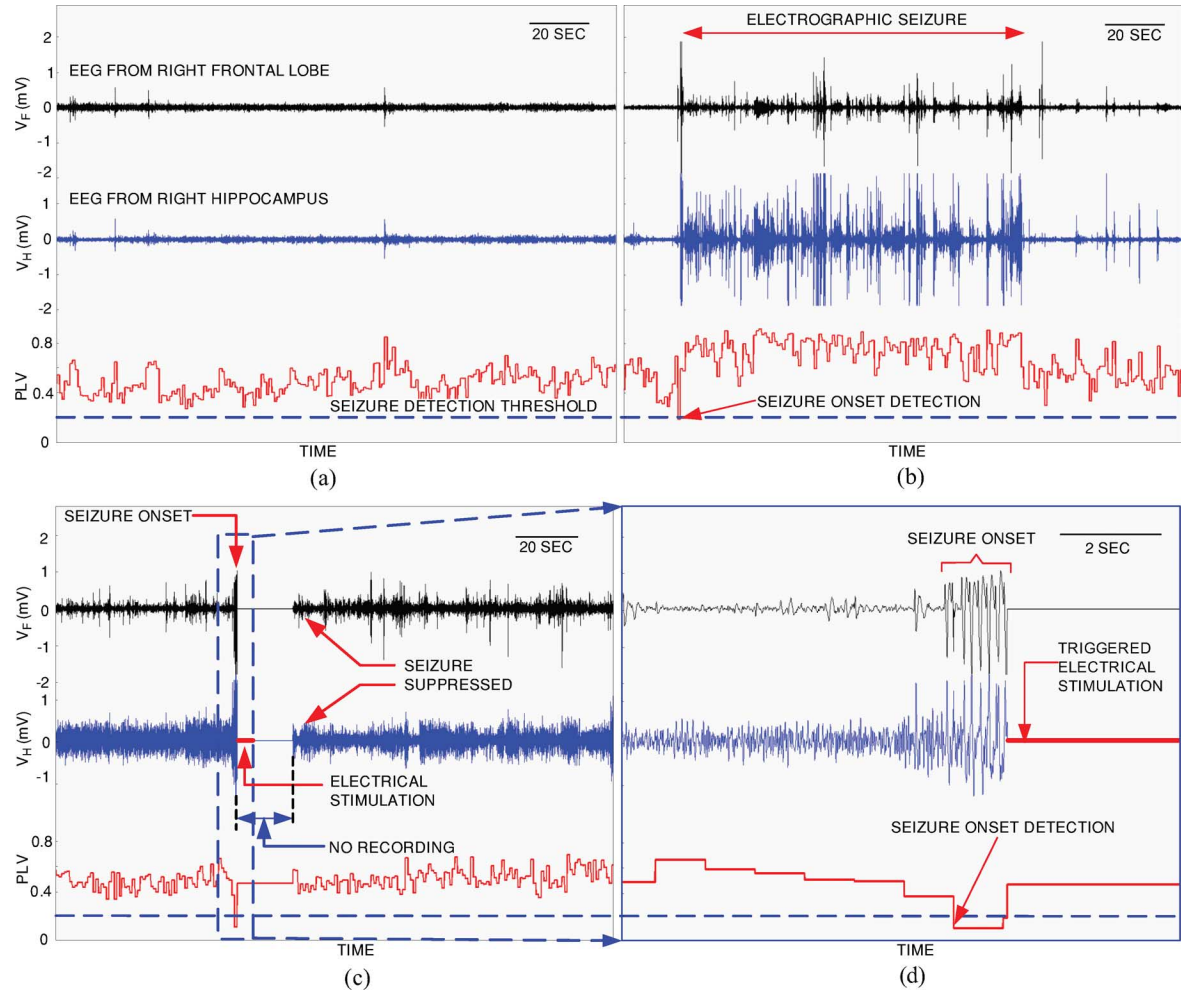
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Fig. 20.   Closed-loop electrical stimulation triggered by seizure onset detection, where V_F is the EEG signal from the right frontal lobe, V_H is the EEG signal from the right hippocampus, PLV is the synchrony index between V_F and V_H recordings: (a) Basal EEG recordings and their PLV, (b) induced electrographic seizure recordings from the non-treatment group and off-line seizure onset detection using PLV, (c) automatic seizure onset detection, self-triggered electrical stimulation, and subsequent seizure suppression in the treatment group, (d) zoomed-in inset of the automatic seizure onset detection and the responsive stimulation.

TABLE IV
EFFICACY OF THE SYSTEM IN SEIZURE SUPPRESSION

Parameter	Non-treatment (N=2)		Treatment (N=2)	
Rat#	1	2	3	4
4-AP dose	8μL	8μL	8μL	8μL
Seizure rate (per hour)	7	7	0.25	1.25
False positive (false alarm)(per hour)	0.5	0.75	0.25	0.75
False negative (missed)(per hour)	0	1	0.25	1.25
True positive (correctly detected)(per hour)	6.5	6	-	-
True negative (correctly reject)(per hour)	9	9	9	9
Detection sensitivity	100%	85.71%	-	-
Specificity	94.7%	92.3%	97.3%	92.3%
Seizure reduction	0%	0%	96.4%	82.1%

to the smaller number of recording channels which require a single ADC only. The design in [43] implements a closed-loop

SoC. However, the neural recording and stimulation channels have a large area, which makes the design unsuitable for scaling to a higher number of channels. The presented design incorporates the largest number of channels while consuming relatively low power and area.

VII. CONCLUSION

We presented an active probe for high-resolution neuromonitoring and responsive neurostimulation. It includes an integrated circuit with 64 neurostimulation channels and 256 fully-differential neural recording channels. A 8×8 400 μm-pitch Utah electrode array (UEA) is bonded directly onto the IC. The total power dissipation of the neural interface is 13.5 mW.

The programmable stimulators have a current sample-and-hold circuit which allows for truly simultaneous stimulation without a time lag inherent to time multiplexing. Re-use of the OTA in the stimulator for the sample and hold phases, and elimination of the DAC from every stimulator channel result in a compact design.

The recording channels perform simultaneous sampling and quantization with an ADC in every channel. This is important

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TABLE V
COMPARATIVE ANALYSIS OF CURRENT-MODE NEURAL STIMULATION ARRAYS

	CMOS Technology [μm]	Channel Count	In-channel Current Memory	DAC Architecture	Supply Voltage [V]	Output Current [μA]	Channel Area [mm^2]
[16]	1	4	No	per-channel	6	200-1000	0.38
[43]	0.35	4	No	per-channel	5	0-94.6	-
[44]	1.5	8	No	shared	±6	0-600	0.6
[26]	0.18	64	No	per-channel	1.8	0-10	-
[45]	1.5	32	No	per-channel	5	0-270	0.1
[46]	0.6	100	No	per-channel	5	0.85 - 216	-
[47]	0.35	1	No (adaptive)	per-channel	3.3	0-450	0.58
This work	0.35	64	Yes	shared	3.3	20-250	0.02

TABLE VI
COMPARATIVE ANALYSIS OF NEURAL RECORDING CHANNELS

	Channel Topology	Fully Differential	Technology [μm]	Noise [μV]	Bandwidth [Hz]	Power [μW]	Voltage [V]	NEF	Gain [dB]	Area [mm^2]
[32]	Two-stage	Yes	0.5	7.8	0.1 - 10k	114.8	3	18.7	40	0.107
[33]	Folded-cascode	Yes	0.6	5.9	10 - 100k	160	5	8.1	20	0.062
[48]	Telescopic	Yes	0.35	6.08	10 - 5k	8.4	3	5.55	33	0.02
[49]	Two-stage switch-capacitor	Yes	0.13	2.2	1 - 10k	68	1.2	4.5 (for spikes)	40-56	0.26
[50]	Chopper-stabilized instrumentation amplifier	No	0.18	0.91	0.1 - 100	66	1.8	-	40	-
[51]	Open loop with digital calibration	Yes	0.065	4.9	10k	5.04	0.5	5.99	-	0.013
[52]	Digitally-assisted closed-loop	No	0.18	0.8	0.5-100	-	1.8	12.3	3-100	-
[53]	Two-stage closed-loop	No	0.5	4.95	0.1 - 8k	-	3	-	67.8-78	-
[54]	Two-stage closed-loop	No	0.35	1.15	0.5 - 150	0.69	1	2.24	59 - 70	0.08
This work	Telescopic and folded-cascode	Yes	0.35	7.99	10 - 5k	12.9	3	8.9	53	0.035

TABLE VII
COMPARATIVE ANALYSIS OF BIDIRECTIONAL NEURAL INTERFACE (STIMULATION AND RECORDING) MICROSYSTEMS

	[33]	[48]	[55]	[26]	[43]	[56]	This work
Year	2006	2009	2008	2008	2011	2008	2009
Technology [μm]	0.6	0.35	0.35	0.18	0.35	0.8	0.35
Area [mm^2]	42.25	8.5	0.72	2.7	10.9	44.89	12.77
Stimulation							
No. of channels	128	128	16	64	4	4	64
Mode	Voltage	Voltage	Current/ Voltage	Current	Current	Current	Current
Output current	up to 10mA	-	0-100μA	0-10μA	0-94.5μA	-	20-250μA
Power/Ch. [μW]	150	51	-	7.4	-	5	2.76
Recording							
No. of channels	128	128	16	8	2	4	256
Fully differential	Yes	Yes	No	No	No	No	Yes
ADC Architecture	Column-parallel	Column-parallel	-	Single	In-Channel	-	In-channel
Power/Ch. [μW]	780	12.75	-	21.25	45	5	52
NEF	8.1	5.6	17.6-46.1	-	2.4	-	8.9
Parallel operation	No	Yes	No	No	No	Yes	Yes
On-chip 3D electrodes	No	No	No	No	No	No	Yes

for accurate subsequent phase synchrony computation. The fully differential design of the neural amplifiers allows for their integration with noisy digital circuits on the same die.

The integrated circuit has been experimentally validated in recording epileptic neural activity in a mouse hippocampal slice *in vitro* and in responsive self-triggered neurostimulation for seizure suppression in an acute epilepsy rat model *in vivo*. We demonstrate that closed-loop stimulation triggered by low phase synchrony reduced seizure rate by 89%.
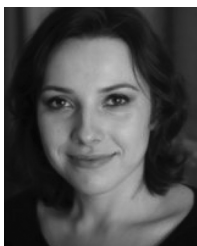
REFERENCES

[1] F. Sun, M. Morrell, and R. Wharen, "Responsive cortical stimulation for the treatment of epilepsy," *Neurotherapeutics*, vol. 5, no. 1, pp. 68–74, Jan. 2008.

[2] T. L. Skarpaas and M. J. Morrell, "Intracranial stimulation therapy for epilepsy," *Neurotherapeutics*, vol. 6, no. 2, pp. 238–243, Apr. 2009.

[3] M. Stead, M. Bower, B. H. Brinkmann, K. Lee, W. R. Marsh, F. B. Meyer, B. Litt, J. Van Gompel, and G. A. Worrell, "Microseizures and the spatiotemporal scales of human partial epilepsy," *Brain*, vol. 133, no. 9, pp. 2789–2797, Sep. 2010.

[4] B. Lysyansky, O. Popovych, and P. Tass, "Optimal number of stimulation contacts for coordinated reset neuromodulation," *Front. Neuroeng.*, vol. 6, no. 5, 2013.

[5] R. Shulyzki, K. Abdelhalim, A. Bagheri, C. Florez, P. Carlen, and R. Genov, "256-site active neural probe and 64-channel responsive cortical stimulator," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2011.

[6] Q. Bai and K. D. Wise, "Single-unit neural recording with active microelectrode arrays," *IEEE Trans. Biomed. Eng.*, vol. 48, no. 8, pp. 911–920, Aug. 2001.

[7] S. Kim, R. Normann, R. Harrison, and F. Solzbacher, "Preliminary study of the thermal impact of a microelectrode array implanted in the brain," in *Proc. 28th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, 2006, pp. 2986–2989.

[8] T. Seese, H. Harasaki, G. Saidel, and C. R. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating," *Lab. Investigat.*, vol. 78, p. 15531562, Dec. 1998.

[9] K. C. Cheung, "Implantable microscale neural interfaces," *Biomed. Microdevices*, vol. 9, no. 6, pp. 923–938, Dec. 2007.

[10] L. Theogarajan, J. Wyatt, J. Rizzo, B. Dorhan, M. Markova, S. Kelly, G. Swider, M. Raj, D. Shire, M. Gingerich, J. Lowenstein, and B. Yomtov, "Minimaly invasive retinal prosthesis," in *Prog. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2006, p. 54.

[11] J. Coulombe, M. Sawan, and J.-F. Gervais, "A highly flexible system for microstimulation of the visual cortex: Design and implementation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 4, pp. 258–269, Dec. 2007.

[12] Y. Y. Yao, M. N. Gulari, J. F. Hetke, and K. D. Wise, "A low-profile three-dimensional neural stimulating array with on-chip current generation," in *Proc. 26th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, Sep. 2004, pp. 1994–1997.

[13] J. Simpson and M. Ghovanloo, "An experimental study of voltage, current, and charge controlled stimulation front-end circuitry," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2007, pp. 325–328.

[14] J. C. Williams, J. A. Hippensteel, J. Dilgen, W. Shain, and D. R. Kipke, "Complex impedance spectroscopy for monitoring tissue responses to inserted neural implants," *J. Neural Eng.*, vol. 4, pp. 410–423, Nov. 2007.

[15] E. J. Tehovnik, "Electrical stimulation of neural tissue to evoke behavioral responses," *J. Neurosci. Methods*, vol. 65, pp. 1–17, 1996.

[16] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking capacitors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 231–244, Sep. 2008.

[17] T. G. Constandinou, J. Georgiou, and C. Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 2, pp. 106–113, Jun. 2008.

[18] M. Ghovanloo and K. Najafi, "A compact large voltage-compliance high output-impedance programmable current source for implantable microstimulators," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 1, pp. 97–105, Jan. 2005.

[19] M. Ortmanns, "Charge balancing in functional electrical stimulators: A comparative study," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2007, pp. 573–576.

[20] M. S. Chae, W. Liu, and M. Sivaprakasam, "Design optimization for integrated neural recording systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1931–1939, Sep. 2008.

[21] M. A. C. van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events," *Med. Biol. Eng. Comput.*, vol. 29, pp. 1035–1044, 1986.

[22] J. G. M. A. M. Levesque and A. Bortel, "High frequency (80–500 Hz) oscillations and epileptogenesis in temporal lobe epilepsy," *Neurobiol. Disease*, vol. 42, no. 3, pp. 231–241, 2011.

[23] D. Xing, C. Yeh, and R. M. Shapley, "Spatial spread of the local field potential and its laminar variation in visual cortex," *J. Neurosci.*, vol. 29, no. 37, pp. 11540–11549, Sep. 2009.

[24] J. N. Y. Aziz, K. Abdelhalim, R. Shulyzki, R. Genov, B. L. Bardakjian, M. Derchansky, D. Serletis, and P. L. Carlen, "256-channel neural recording and delta compression microsystem with 3D electrodes," *IEEE J. Solid-State Circuits*, vol. 44, pp. 995–1005, Mar. 2009.

[25] J. Viventi, D.-H. Kim, L. Vigeland, E. S. Frechette, J. A. Blanco, Y.-S. Kim, A. E. Avrin, V. R. Tiruvadi, S.-W. Hwang, A. C. Vanleer, D. F. Wulsin, K. Davis, C. E. Gelber, L. Palmer, J. V. der Spiegel, J. Wu, J. Xiao, Y. Huang, D. Contreras, J. A. Rogers, and B. Litt, "Flexible, foldable, actively multiplexed, high-density electrode array for mapping brain activity in vivo," *Nature Neurosci.*, vol. 14, pp. 1599–1605, Dec. 2011.

[26] J. Lee, H. Rhew, D. R. Kipke, and M. P. Flynn, "A 64 channel programmable closed-loop neurostimulator with 8 channel neural amplifier and logarithmic ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1935–1945, Sep. 2010.

[27] S. J. Daubert and D. Vallancourt, "Operation and analysis of current copier circuits," *Proc. IEEE*, vol. 137, pp. 109–115, Apr. 1990.

[28] J. Lachaux, D. Rudrauf, and P. Kahane, "Intracranial eeg and human brain mapping," *J. Physiol.*, vol. 97, no. 4–6, pp. 613–628, Jul. 2003.

[29] C. Tallon-Baudry, O. Bertrand, and C. Fischer, "Oscillatory synchrony between human extrastriate areas during visual short-term memory maintenance," *J. Neurosci.*, vol. 21, no. 20, Oct. 2001.

[30] K. Abdelhalim and R. Genov, "915-MHz wireless 64-channel neural recording SoC with programmable mixed-signal FIR filters," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 2011, pp. 223–226.

[31] M. Yin and M. Ghovanloo, "A low-noise preamplifier with adjustable gain and bandwidth for biopotential recording applications," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2007, pp. 321–324.

[32] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower CMOS integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 1, pp. 1–10, Feb. 2009.

[33] F. Heer, S. Hafizovic, W. Franks, A. Blau, C. Ziegler, and A. Hierlemann, "CMOS microelectrode array for bidirectional interaction with neuronal networks," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1620–1629, Jul. 2006.

[34] R. R. Harrison, "A versatile integrated circuit for the acquisition of biopotentials," in *Proc. IEEE Custom Intergrated Circuits Conf.*, Sep.. 2007, pp. 115–122.

[35] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. Hoboken, NJ, USA: Wiley, 1997.

[36] H. Kassiri, K. Abdelhalim, and R. Genov, "Low-distortion super-GOhm subthreshold-MOS resistors for CMOS neural amplifiers," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, Oct.–Nov. 2013.

[37] J. N. Y. Aziz, R. Karakiewicz, R. Genov, B. L. Bardakjian, M. Derchansky, and P. L. Carlen, "Real-time seizure monitoring and spectral analysis microsystem," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2006, pp. 2133–2136.

[38] R. Gregorian, *Introduction to CMOS OP-AMPs and Comparators*. Hoboken, NJ, USA: Wiley-Interscience, 1999.

[39] K. Abdelhalim, "Wireless neural recording and stimulation SOCS for monitoring and treatment of intractable epilepsy," Ph.D. dissertation, University of Toronto, Toronto, ON, Canada, 2013.

[40] J. L. P. Velazquez, L. G. Dominguez, V. Nenadovic, and R. A. Wennberg, "Experimental observation of increased fluctuations in an order parameter before epochs of extended brain synchronization," *J. Biological Phys.*, vol. 37, no. 2, pp. 141–152, 2011.

[41] K. Abdelhalim, V. Smolyakov, and R. Genov, "A phasesynchronization epileptic seizure detector VLSI architecture," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 5, pp. 430–438, 2011.

[42] R. J. Racine, "Modification of seizure activity by electrical stimulation: II. Motor seizure," *Electroencephalogr. Clin. Neurophysiol.*, vol. 32, pp. 281–294, 1972.

[43] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, "A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 731–745, Apr. 2011.

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[44] M. Sivaparakasam, W. Liu, M. S. Humayun, and J. D. Weiland, "A variable range bi-phasic current stimulus driver circuitry for an implantable retinal prosthetic device," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 763–771, Mar. 2005.

[45] M. Ghovanloo and K. Najafi, "A modular 32-site wireless neural stimulation microsystem," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2457–2466, Dec. 2004.

[46] B. Thurgood, D. Warren, N. Ledbetter, G. Clark, and R. Harrison, "A wireless integrated circuit for 100-channel charge-balanced neural stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 6, pp. 405–414, Dec. 2009.

[47] S. Arfin and R. Sarpeshkar, "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 1, pp. 1–14, Feb. 2012.

[48] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. Carlen, and R. Genov, "The 128-channel fully differential digital integrated neural recording and stimulation interface," *IEEE Trans. Biomed. Circuits. Syst.*, Jun. 2010.

[49] H. Gao, R. Walker, P. Nuyujukian, K. A. A. Makinwa, K. V. Shenoy, B. Murmann, and T. H. Meng, "HermesE: A 96-channel full data rate direct neural interface in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1043–1055, Apr. 2012.

[50] J. Yoo, L. Yan, D. El-Damak, M. B. Altaf, A. Shoeb, H.-J. Yoo, and A. Chandrakasan, "An 8-channel scalable EEG acquisition SoC with fully integrated patient-specific seizure classification and recording processor," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2012.

[51] R. Muller, S. Gambini, and J. Rabaey, "A 0.013 mm^2, 5 μW, dc-coupled neural signal acquisition IC with 0.5 V supply," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.

[52] J. Xu, R. Yazicioglu, B. Grundlehner, P. Harpe, K. A. A. Makinwa, and C. V. Hoof, "A 160 μW 8-channel active electrode system for EEG monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 555–567, Dec. 2011.

[53] S. B. Lee, H.-M. Lee, M. Kiani, U.-M. Jow, and M. Ghovanloo, "An inductively powered scalable 32-channel wireless neural recording system-on-a-chip for neuroscience applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 360–371, Dec. 2010.

[54] X. Zou, W.-S. Liew, L. Yao, and Y. Lian, "A 1 V 22 μW 32-channel implantable EEG recording IC," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2010.

[55] E. A. Brown, J. D. Ross, R. A. Blum, Y. Nam, B. C. Wheeler, and S. P. DeWeerth, "Stimulus-artifact elimination in a multi-electrode system," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 1, pp. 10–21, Mar. 2008.

[56] A. T. Avestruz, W. Santa, D. Carlson, R. Jensen, S. Stanslaski, A. Helfenstine, and T. Denison, "A 5 μW/channel spectral analysis IC for chronic bidirectional brain-machine interfaces," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3006–3024, Dec. 2008.

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