Low-Frequency Noise and Offset Rejection in DC-Coupled Neural Amplifiers: A Review and Digitally-Assisted Design Tutorial

Arezu Bagheri, *Student Member, IEEE*, Muhammad Tariqus Salam, *Member, IEEE*, Jose Luis Perez Velazquez, and Roman Genov, *Senior Member, IEEE*

***Abstract*—We review integrated circuits for low-frequency noise and offset rejection as a motivation for the presented digitally-assisted neural amplifier design methodology. Conventional AC-coupled neural amplifiers inherently reject input DC offset but have key limitations in area, linearity, DC drift, and spectral accuracy. Their chopper stabilization reduces low-frequency intrinsic noise at the cost of degraded area, input impedance and design complexity. DC-coupled implementations with digital high-pass filtering yield improved area, linearity, drift, and spectral accuracy and are inherently suitable for simple chopper stabilization. As a design example, a 56-channel 0.13 μm CMOS intracranial EEG interface is presented. DC offset of up to $\pm$50 mV is rejected by a digital low-pass filter and a 16-bit delta-sigma DAC feeding back into the folding node of a folded-cascode LNA with CMRR of 65 dB. A bank of seven column-parallel fully differential SAR ADCs with ENOB of 6.6 are shared among 56 channels resulting in 0.018 mm^2 effective channel area. Compensation-free direct input chopping yields integrated input-referred noise of 4.2 $\mu V_{\rm rms}$ over the bandwidth of 1 Hz to 1 kHz. The 8.7 mm^2 chip dissipating 1.07 mW has been validated *in vivo* in online intracranial EEG monitoring in freely moving rats.**

***Index Terms*—Biomedical electronics, brain, closed-loop DC offset rejection, dc-coupled neural signal monitoring, epilepsy, implantable biomedical devices, in vivo, microelectronic implant, mixed analog digital integrated circuits, neural recording.**

I. Introduction

RECORDING electrographic neural activity from many locations in the brain provides information from a large population of neurons and helps improve our understanding of functions of the brain and of various neurological disorders such as intractable epilepsy [1].

Acquiring electrographic neural data with high spatial resolution can also be used in developing brain-machine interfaces [2], and creating state-of-the-art neural prostheses [3]. Increasing the number of neural recording sites requires integrating many neural amplifiers on a single chip, which imposes various challenges including packing density, noise and power consumption.

Local field potentials typically have an amplitude of 20 μV to 1 mV and frequency content in the 1 Hz to 500 Hz range. The action potentials amplitude is typically approximately 70 μV but can be up to 5 mV in abnormal cases of multiple unit activity. Their frequency content is up to 5 kHz [4] (and higher in some cases). Of our particular interest is monitoring mammalian neuronal oscillations such as due to epilepsy in cortical networks, that are at the lower end of this frequency band [5].

Due to the small amplitude of the neural signals, noise and interference have an adverse effect on the recorded signal. The total noise of the recorded signal consists of the circuit thermal and flicker noise and the thermal noise of the recording electrode. Intrinsic circuit noise can be traded for low power and high density of integration. Different circuit techniques, such as PMOS-input amplifiers, increasing the gate area of the input transistors and chopping, are used to reduce the circuit noise [6]–[8]. In chopper stabilization technique, the OTA offset and low-frequency noise are up-modulated by the chopper switches to a higher (chopping) frequency where there is no $1/f$ noise and are filtered out by a low-pass filter.

Due to electrochemical reactions at the electrode-tissue interface, the neural tissue has different DC voltage levels at different electrodes. This voltage difference, known as input DC offset, causes a differential DC input signal that is typically 1–10 mV and can be up to a maximum of 50 mV. This DC component can saturate a high-gain DC-coupled differential amplifier.

Conventionally the input DC voltage is blocked by large AC-coupling capacitors that occupy a significant area in the recording channel. Recording low-frequency signals while rejecting the tissue DC voltage requires a very small-frequency well-defined high-pass pole. This high-pass pole is generally implemented with pseudo-resistors that suffer from nonlinearity for large output voltage swing [9], as well as excessive random variations over process and temperature. Additionally, input DC-blocking capacitors make signal chopping at the input more challenging. This leads to additional circuit overhead such as a further increased capacitor size to counter the noise multiplication effect [10], [11], as well as input impedance boosting and ripple compensation loops [11].

This paper is comprised of two parts. In the first part (Section II) a brief review of key integrated circuit design techniques that address issues raised in Section I is presented. Both

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A. Bagheri, M. T. Salam, and R. Genov are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: roman@eecg.utoronto.ca).

J. L. Perez Velazquez is with the Department of Neuroscience and Mental Health Research Institute, The Hospital for Sick Children, Toronto, ON M5P 4A2, Canada.

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AC-coupled and DC-coupled circuits for input offset rejection are surveyed. The latter can be significantly more compact due to the lack of large input capacitors. Chopper stabilization circuits for low-frequency noise reduction in AC-coupled neural amplifiers are also described with their limitations (mostly due to area, complexity and input impedance) highlighted. This motivates for a compact DC-coupled neural amplifier with a simple chopper stabilization implementation.

In the second part of the paper (Sections III–V) a step-by-step tutorial for such a neural amplifier design is given and experimental results are presented. Specifically, a compact 0.13 μm CMOS neural interface with 56 DC-coupled channels for recording intracranial EEG signals is presented. The tissue DC offset at the input of the amplifier is canceled by a digitally-assisted feedback configuration, which yields channel area reduction by eliminating the large AC-coupling capacitors. The integration area savings become even more apparent when the design is implemented in modern digital CMOS technology nodes, as in such nodes analog passives such capacitors do not scale down significantly. As importantly, in modern digital CMOS processes active analog components such as MOS transistors biased in the subthreshold region exhibit much degraded performance (e.g., leakage and non-linearity) which leads to drift and distortive high-pass filter cut-off frequency variations that can span as much as an order of magnitude in frequency. The presented digital feedback filtering technique enables maintaining a drift-free, well-controlled, digitally programmable and thus accurate high-pass filter cut-off frequency, a key challenging requirement for using integrated neural amplifiers in humans [7], [12], [13]. This technique is digital and is thus scalable to modern processes. An inherently simple chopper stabilization technique is introduced to reduce the low-frequency noise of the amplifier without the need for the aforementioned circuit overhead [10], [11]. This design extends on an earlier preliminary report of the principle in [14], and offers a more detailed analysis of the design and additional experimental results characterizing the circuit implementation and *in vivo* performance.

II. Review of Input Low-Frequency Noise and Offset Rejection Circuits

A. AC-Coupled Input Offset Rejection Circuits

Several integrated circuits for low-noise and low-power multiple channel neural recording have been introduced over the past decade. The conventional method to implement a neural recording front-end is the widely-used closed-loop capacitive-feedback amplifier [15]–[17]. The general circuit architecture in this method is shown in Fig. 1(a). The tissue DC offset is blocked by large capacitors $C1$ at the input. The gain is equal to $C1/C2$ and the high-pass pole is implemented by capacitor $C2$ in parallel with a highly resistive element in the feedback. The first drawback of this conventional method is the large area of the DC-blocking capacitors, preventing integration of many channels. Achieving small high-pass pole frequency (0.1–10 Hz) and large gain (50 dB) requires input capacitors in the order of 20 pF. These large capacitors also decrease the input impedance of the neural amplifier, which is equal to $1/jwC_1$. Reduced input impedance degrades the common-mode rejection ratio (CMRR) due to the voltage division effect. However, it should be noted that larger capacitors are better matched and thus improve CMRR. Therefore, a trade-off exists. Deciding which effect is stronger requires knowledge of the electrode capacitance and design technology specifications. This configuration also causes multiplication of the OTA noise, when referred to the input. The total input-referred noise of the amplifier is equal to [18]

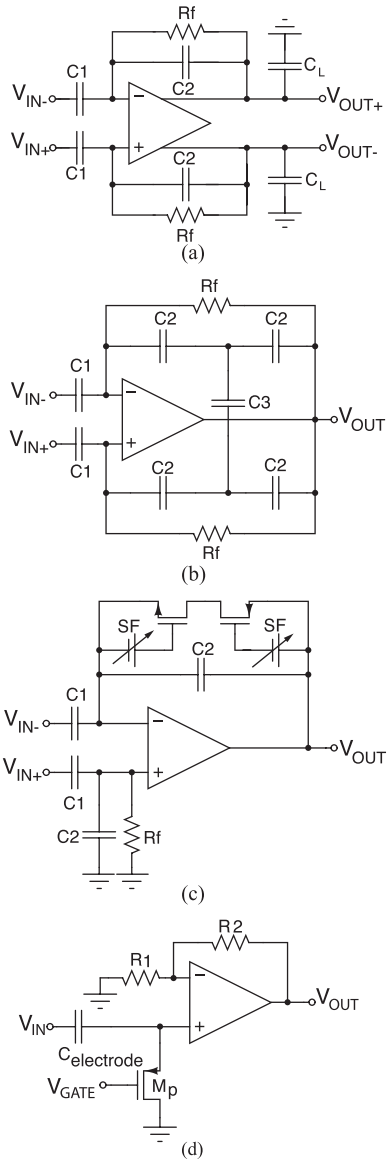

Fig. 1. Conventional neural signal recording circuit architectures. (a) Closed-loop capacitive-feedback neural amplifier. (b) Capacitive-feedback neural amplifier using capacitive T-network topology to reduce the effective feedback capacitance. (c) Capacitive feedback neural amplifier with enhanced linearity by using source-followers (SF). (d) DC rejection using the electrode capacitance and a resistive element.

$$\overline{V_{n,\mathrm{in}}^2} = \overline{V_{n,\mathrm{inOTA}}^2}\left(\frac{C_2 + C_1}{C_1}\right)^2 \tag{1}$$

where C_1 is the input capacitor, C_2 is the feedback capacitor, $V_{n,\mathrm{inOTA}}^2$ is the OTA input-referred noise power and $V_{n,\mathrm{in}}^2$ is the amplifier total input-referred noise power. Equation (1) shows

that reducing the gain increases the noise multiplication factor. Therefore the gain should be increased by using larger C_1 to reduce the overall input-referred noise.

The design technique illustrated in Fig. 1(b) [19] utilizing a capacitive-T topology in the feedback, reduces the effective feedback capacitor value. Therefore smaller input capacitors can be used for a given gain value. Reducing the feedback capacitors, while maintaining the same high-pass pole frequency, requires higher feedback resistance, which increases the circuit noise and imposes area overhead. The low-frequency noise reported in [19] is high (14.4 μV for 1.4 Hz–8.5 kHz bandwidth) and the area reduction achieved is not considerable, as extra capacitors are added in the feedback.

Another disadvantage of the circuit in Fig. 1(a) is that the resistive element in the feedback, when implemented as a highly-resistive triode-biased MOS transistor, exhibits nonlinear behaviour in the presence of a large output voltage swing as well as DC operating point drift due to transistor leakage. This nonlinearity causes distortion and makes the high-pass pole frequency time-variant [8]. The resistance of the active elements used instead of a passive resistor in most of the modern designs may have up to an order of magnitude variation over PVT or more as shown in [20]. This issue is addressed in the circuit shown in Fig. 1(c) [9], [20] by implementing the feedback resistor in the second stage by means of setting the gate voltages of two MOS transistors using two source-followers. In [9] the low-frequency distortion and drift are mitigated, but the large DC-blocking capacitors are still present.

In another method of input DC offset rejection illustrated in Fig. 1(d), a high-resistance device is used at the input, which along with the electrode capacitor forms a high-pass filter [21]. The design in [21] does not provide an accurate high-pass cut-off frequency due to the highly variable electrode capacitance. A conventional DC-blocking capacitor can also be used in this architecture, but has to be implemented offchip due to its large required value [22]. Alternatively an on-chip input capacitor can be used but requires either a large off-chip resistor or an on-chip MOS transistor biased in the subthreshold region. The latter approach adds extra noise to the front-end while providing no gain in the first stage, where the signal is most susceptible to noise.

B. Chopper Stabilization in AC-Coupled Neural Amplifiers

As mentioned in Section I, the band of interest for neural recording includes frequencies less than 100 Hz. Low-frequency flicker noise from the amplifier is dominant in this frequency band and chopper-stabilization technique is typically used to reduce the flicker noise. Using the chopper-stabilization technique in the circuit in Fig. 1(a) [15]–[17] for the same capacitor size would increase the noise at low frequencies by a considerable amount. The equivalent circuit including the OTA input-referred noise source is shown in Fig. 2(a). The chopper switches together with the OTA input transistors parasitic capacitors create a parasitic resistor at the input whose value is inversely proportional to the chopping frequency

$$R_{\rm eq} = \frac{1}{f_{\rm chop} C_{\rm in}} \tag{2}$$

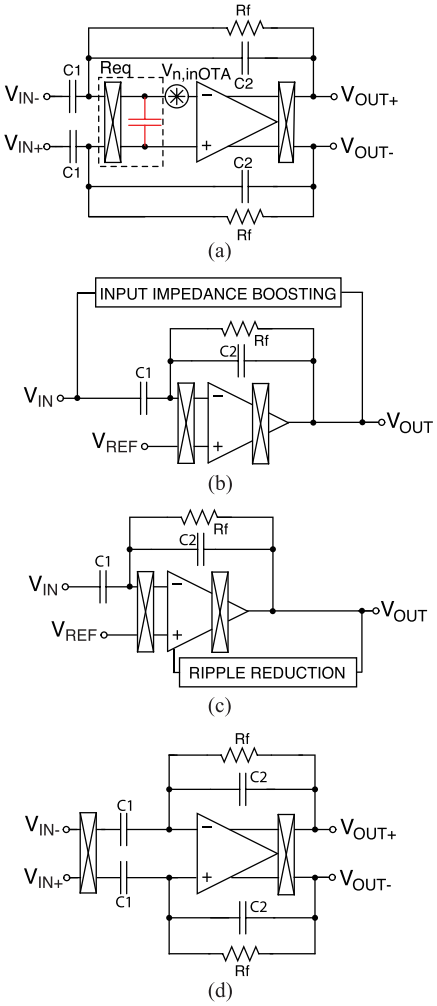

Fig. 2. Chopping in neural amplifiers. (a) Chopper-stabilized neural amplifier noise model. (b) Increasing the amplifier input impedance using an impedance boosting feedback circuit. (c) Reduction of the output voltage ripple due to the chopping switches. (d) Chopper switches are placed in front of the ac-coupling capacitors. Sub-figures (b) and (c) depict single-ended-output implementations for simplicity. In these cases internal current-mode chopping is implemented on the wide-band internal node of the differential cascode circuit. Differential versions of these circuits allow for output chopping to be implemented on the output voltage.

where $f_{\rm chop}$ is the chopping frequency and $C_{\rm in}$ is the input transistors parasitic capacitance. This resistance and the DC-blocking capacitors will shape the OTA thermal noise with $1/f$ characteristic when referred to the input [11]

$$\overline{V_{n,\rm in}^2} = \overline{V_{n,\rm inOTA}^2} \left(\frac{C_2 + C_1}{C_1} + \frac{2\pi f_{\rm chop} C_{\rm in}}{s C_1} \right)^2 \tag{3}$$

where $C_{\rm in}$ is the input transistors parasitic capacitance. Therefore, very large input capacitors in the order of 300–500 pF are required for C_1, to reduce the low-frequency noise [11]. These capacitors occupy a very large area and reduce the input impedance. In the work presented in [23] large resistors and capacitors are used off-chip to implement the high-pass filter and achieve infinite input impedance. Large capacitors are also used in [10] for DC blocking and enabling the incorporation of chopper switches. In these works only one channel is provided for biopotential recording.

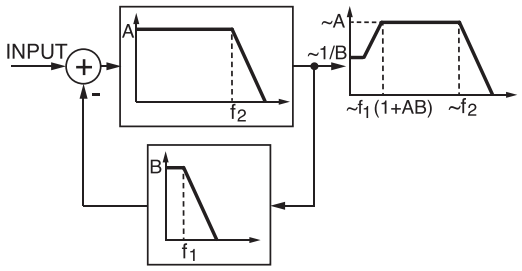

Fig. 3. The concept of implementing a high-pass filter using a low-pass filter in the feedback.

In order to increase the degraded input impedance in chopper-stabilized capacitive feedback amplifier, an input impedance boosting circuit can be used [11]. As shown in Fig. 2(b), the single-ended circuit feeds back a certain amount of current which forms a portion of the amplifier input current, and this effectively boosts the input impedance.

Another challenge is reducing the amplifier output ripple that is due to the up-modulated amplifier offset and can be reduced by low-pass filtering the output signal. As shown in Fig. 2(c) [11] the output ripple can be reduced by a digitally-assisted feedback loop that senses the ripple and subtracts it from the input.

As illustrated in Fig. 2(d) [7], another approach in implementing a chopper-stabilized neural amplifier is to place the chopper switches in front of the AC-coupling capacitors. This design suffers from a reduced input impedance, which is equal to [7]

$$Z_{\rm in} = \frac{1}{jw_{\rm sig}C_1 + jw_{\rm chop}C_1}$$
$$Z_{\rm in} = \frac{1}{jw_{\rm sig}(1 + f_{\rm chop}/f_{\rm sig})C_1} \quad (4)$$

where $f_{\rm chop}$ is the chopping frequency and $f_{\rm sig}$ is signal frequency. Increasing the ratio of the chopping frequency to the signal frequency, to up-modulate the flicker noise to a higher frequency further away from the signal band, reduces the input impedance.

C. DC-Coupled Input Offset Rejection Circuits

An alternative approach in designing neural signal amplifiers that block the tissue DC offset is using a low-pass filter in a feedback configuration, as illustrated in Fig. 3. The low-pass filter senses the DC at the amplifier output and subtracts it from the input to provide a high-pass filter as the overall transfer function. This technique is implemented in several different designs as follows.

The design shown in Fig. 4(a) [24] uses an analog integrator in the feedback with a large integrating time-constant to remove the low-frequency portion of the signal from the input signal path. This design requires a large power for the amplifier in the feedback. It uses a single-ended configuration which is not suitable for low-noise operation and high CMRR and PSRR (power supply rejection ratio). Also the voltage swing at the output of the amplifier can change the resistance of the diode-connected transistors [denoted as a boxed resistor in Fig. 4(a)] and modify the high-pass pole. The high-pass pole can also change by the variations in the open-loop gain of the feedback opamp.

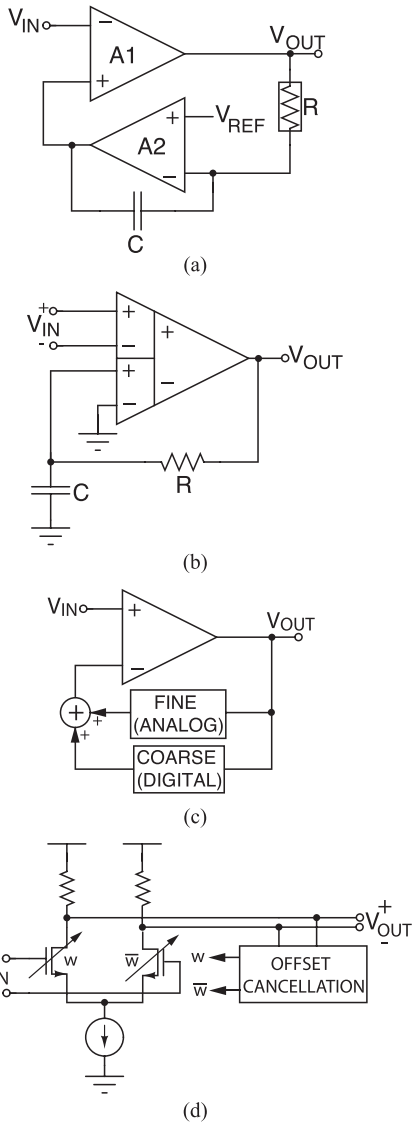

Fig. 4. DC-coupled neural recording front-end circuits using (a) an analog integrator, (b) a differential difference amplifier, (c) digital and analog DC servo loops, and (d) input transistor width modulation by an offset cancellation feedback.

The design shown in Fig. 4(b) [6] uses a differential-difference amplifier that cancels the low-frequency and DC portion of the signal by feeding them back through the second differential pair. It utilizes an R-C filter in the feedback as an analog low-pass filter. These passive components should be very large to achieve a small high-pass pole frequency. In [6] the passive components are implemented off-chip, which is not suitable for integrating a large number of channels on-chip.

The design shown in Fig. 4(c) [25] takes advantage of a digital low-pass filter in the feedback to reduce the power consumption, and an additional analog low-pass filter to reduce the dynamic range of the DC signal that goes through the digital path, relaxing the requirement for the DAC resolution. However, this design has area and power which are excessive for integrating many recording channels.

A fully-digital circuit can be used in the feedback to avoid these issues. A digital feedback loop does not require any large capacitors or pseudo resistors, which enables control of the

TABLE I
COMPARATIVE SUMMARY OF DIFFERENT TYPES OF NEURAL AMPLIFIERS FRONT-ENDS

Fig.	Amplifier Architecture	Reference	Year	Pros	Cons
AC-coupled					
1(a)	Closed-loop capacitive-feedback	[15], [16], [17]	2007-2010	Rail-to-rail DC rejection, accurate gain	Large cap area, OTA noise multiplication
1(b)	Capacitive feedback with T-network	[19]	2012	Input cap size reduction	Noise & area overhead due to larger feedback resistors required
1(c)	Capacitive feedback with source-followers	[8]	2012	Smaller low-frequency distortion	Large DC blocking caps
1(d)	Electrode capacitance and resistive element	[21]	2004	No extra input cap	Inaccurate high-pass pole
2(a)-(c)	Conventional chopper-stabilized	[11], [23], [10]	2010-2011	Noise and offset reduction	Extra large and off-chip input caps, requires input impedance boosting
2(d)	Chopper switches in front of input caps	[7]	2007	Input cap size reduction	Input impedance variation with chopping frequency
DC-Coupled					
4(a)	Analog integrator	[24]	2007	Elimination of input cap	Large feedback amplifier power
4(b)	Differential difference amplifier	[6]	2005	Elimination of input cap	Large off-chip passive components
4(c)	Digital and analog DC servo loops	[25]	2008	Digital feedback to relax analog feedback requirements	Excessive area and power
4(d)	Input transistor width modulation	[26]	2012	Fully-digital DC rejection	Flicker noise variation, area and complexity overhead

behaviour of the circuit with more flexibility and accuracy. Also implementing the integrator in the digital domain would require smaller area than that in the design in [24]. The neural amplifier shown in Fig. 4(d) [26] has such a digital feedback for DC and low-frequency suppression implemented off-chip. The off-chip digital filter may introduce an unknown delay to the low-frequency signal path, making it difficult to stabilize the feedback loop. The on-chip implementation of the digital filter is presented in [27] with a small number of channels (4). The input transistors are in the form of an array in order to adjust the transistor width according to the input offset, while maintaining constant input-referred noise and CMRR. However, according to the experimental results the input-referred noise and CMRR vary with the input offset. This is partly due to the optimization of the layout of the input transistor array for matching consideration. This along with the second digital loop for binary search add extra complexity to the system and impose area overhead. The design in [27] does not provide chopping for flicker noise reduction and its high-pass pole is programmable to the minimum frequency of 40 Hz.

This section served as a review of selected integrated circuit design techniques for low-frequency noise and offset rejection. The comparison of the presented techniques is summarized in Table I. Conventional AC-coupled circuits for input offset rejection have been presented first. Their key limitations are the large area of the input capacitors, the nonlinearity, DC point drift and the inaccurate high-pass filter cut-off frequency in large part due to the use of MOS resistors. Chopper stabilization circuits for low-frequency noise reduction in such AC-coupled neural amplifiers have also been summarized. Their key limitations are large area, reduced input impedance and added implementation complexity. Next it has been shown that DC-coupled implementations can be significantly more compact due to the lack of large input capacitors. Furthermore, a digitally-assisted DC-coupled implementation can be linear, drift-free and frequency-accurate as MOS resistors are eliminated. Also, as will be shown next, a simple chopper stabilization scheme with small area and high input impedance is inherently suitable to such a neural amplifier implementation.

The review in this section has served as a motivation for a compact digitally-assisted DC-coupled neural amplifier with an efficient chopper stabilization implementation described next. In the remainder of this paper, a step-by-step tutorial for such a neural amplifier design is given. Section III describes the arrayed VLSI architecture and circuit implementation of the presented neural recording interface with the design considerations for the main blocks introduced. Section IV presents the experimental results from the IC prototype. Section V compares the results with the state of the art in integrated neural interfaces. Section VI concludes the paper.

III. DESIGN TUTORIAL: DC-COUPLED NEURAL AMPLIFIER

The block diagram of the DC-coupled digitally-assisted integrated circuit presented here as a design example is shown in Fig. 5. It consists of 56 neural amplifiers each with a fully-differential low-noise folded-cascode OTA, seven column-parallel SAR ADCs, and a DC offset-canceling mixed signal DC servo feedback, one per channel. Groups of 8 channels in a column share one ADC. The digitally assisted feedback includes a digital low-pass filter (LPF) and a 4-bit offset-canceling current-output DAC. Each of these blocks is described in the following sections.

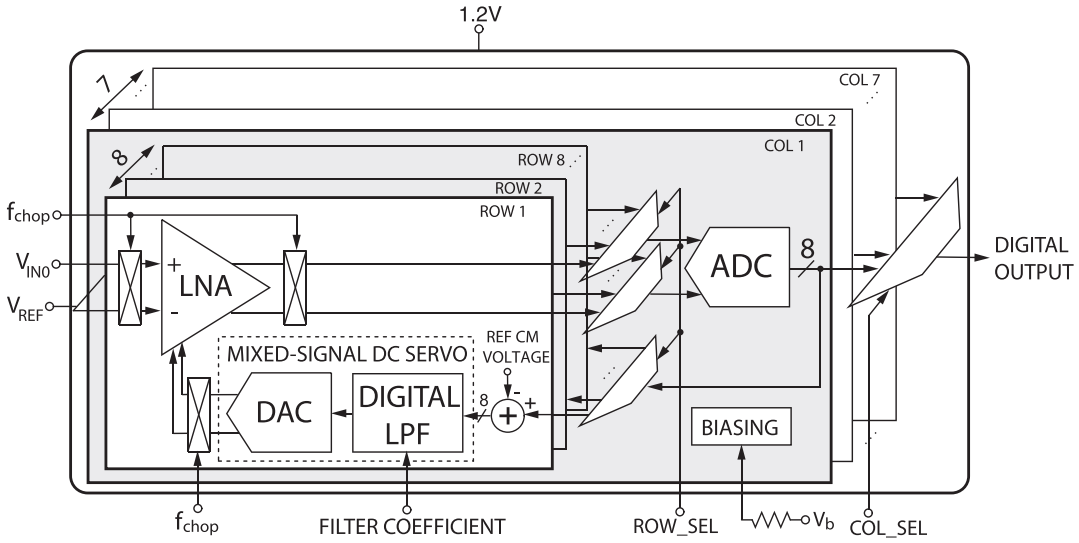

Fig. 5. Block diagram of the 56-channel neural interface with digitally-assisted input offset rejection and chopper stabilization.

A. Analog Front End

The front-end OTA and the feedback current-steering DAC block are shown in Fig. 6(a). Neural signal amplification and filtering are performed by the folded-cascode OTA, used as the front-end LNA. The fully differential architecture is chosen to reduce the common-mode noise and interference and to achieve a high CMRR, which is essential in a mixed-signal environment. Certain considerations have been taken into account for sizing the transistors in order to minimize the OTA input-referred noise. Flicker noise is minimized by using large PMOS transistor in the input pair (M1, M2) and also large W and L were used for output current sources (M4, M5, M10, M11). Thick-oxide PMOS transistors are used for the input pair, as marked in Fig. 6(a), in order to tolerate larger variations of the tissue voltage level. Input differential DC voltages in the range of $\pm$50 mV are within the design specifications and will be rejected. Typical DC offsets observed during neural signal recordings are well within these specifications. In the unlikely event that, during a neural signal recording, the differential DC voltage goes out of $\pm$50 mV range, an auxiliary reset signal can be used to reset the common mode input to the OTA (e.g., to short the inputs to remove a static charge accumulated in the tissue). Single-ended DC voltages that are too high can saturate the amplifier. The thick-oxide devices in this technology withstand input voltages of up to 3.3 V with the OTA input common-mode voltage range being 0.5–0.8 V. Thermal noise was minimized by biasing the input pair transistors in the subthreshold region, which provides maximum g_m/I_D. There is a trade-off between the noise and the output swing for biasing output current source transistors (M4, M5, M10, M11). Larger V_{eff} provides smaller g_m/I_D and reduces the thermal noise. However, it limits the OTA output swing. A large transistor was used for the tail current source (M3). In a conventional folded-cascode OTA with no DC offset cancelation circuit, the flicker and thermal noise of the tail current source are common-mode and therefore canceled by the differential architecture. However, in the presented architecture, an input DC voltage mismatch creates an imbalance in the OTA, which introduces these noise sources to the OTA output node. Therefore the gate area of the tail current source transistor is increased to reduce its flicker noise contribution. Transistor sizes in the OTA and the current steering DAC are listed in Table II.

A continuous-time common-mode feedback circuit, shown in Fig. 6(b), is used to set the DC level of the output nodes. It provides a control voltage to the gate of the transistors M10 and M11. The mixed-signal feedback ensures that the negative and positive output nodes are at the same DC level, and the CMFB circuit determines the output voltage level according to V_{CM}, which is provided off-chip through bias voltage DACs. The CMFB loop stability is ensured by setting the CMFB circuit pole far from the OTA dominant pole while maintaining large gain around the feedback loop. The transistor sizes for the CMFB circuit are given in Table II.

Chopper modulation is implemented by cross-coupled switches using transmission gates. Minimum-size switches are required in order to minimize residual offset due to charge injection and clock feedthrough. Different clock phases required for the chopper switches are generated off-chip through an FPGA. This prototype was developed to show the functionality of the mixed-signal feedback in the presence of large differential DC offsets at the input. Having the clocks required for the digital circuitry on-chip or off-chip does not affect the functionality of the system, since the frequency of operation is low and the delay of having the signals routed from off-chip is acceptable. In our latest higher-integrated versions of this design the digital clocks are implemented on-chip with an equivalent system performance. In order to remove flicker noise, the chopping clock frequency should be set higher than the $1/f$ corner frequency, which can be in the range of 1 Hz to 1 kHz depending on transistor sizes and biasing conditions. In the presented design the chopping clock frequency is set to 2 kHz.

The channel can be used with various frequency band settings, such as the following two key configurations. One, for recording high-frequency signals (e.g., in the range of 10 Hz to 5 kHz) without chopping, as flicker noise is not dominant in this frequency range. Two, for recording low-frequency signals (e.g., in the range 1 Hz to 1 kHz), where flicker noise is more prominent, with chopping. The entire neural signal band

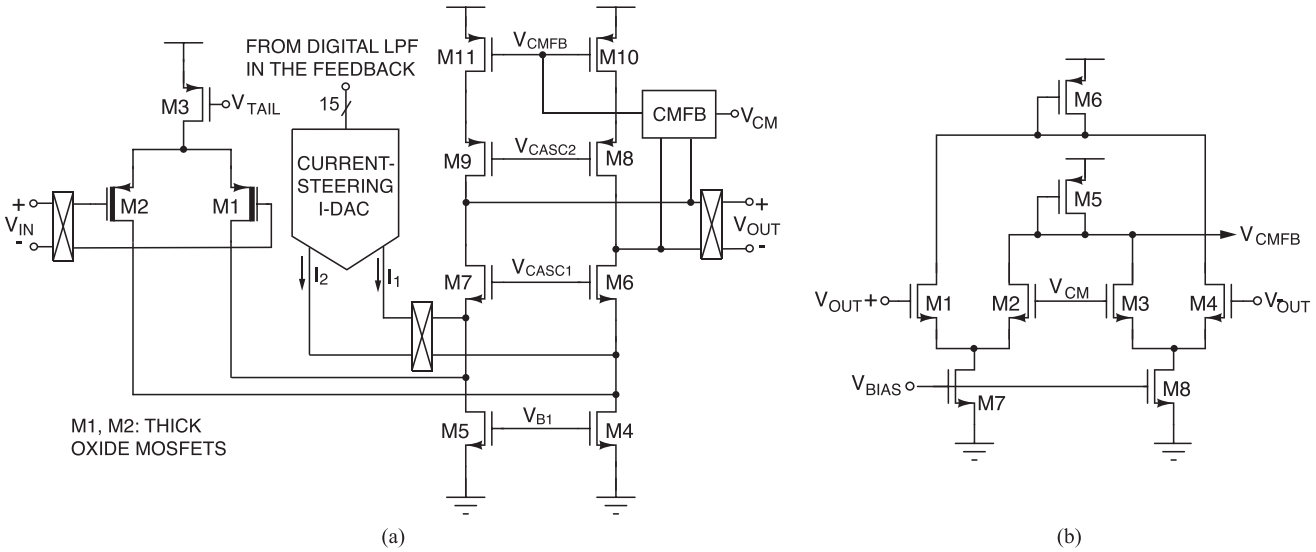

Fig. 6. (a) Circuit diagrams of the front-end folded-cascode OTA (b) and its CMFB circuit. The current-steering I-DAC provides current to the folding node of the folded-cascode OTA.

TABLE II
FRONT-END AMPLIFIER AND CMFB TRANSISTOR SIZES

Transistor (Amplifier)	W/L (μm)	Transistor (CMFB)	W/L (μm)
$M_{1,2}$	$40 \times 4/0.5$	$M_{1,2,3,4}$	$1/1$
M_3	$164 \times 0.5/5$	$M_{5,6}$	$3 \times 1/2$
$M_{4,5}$	$54 \times 0.25/15$	$M_{7,8}$	$3 \times 0.5/1$
$M_{6,7}$	$4 \times 1/1$	$--$	$--$
$M_{8,9}$	$4 \times 1/1$	$--$	$--$
$M_{10,11}$	$10 \times 1/3$	$--$	$--$

(up to 5 KHz) can also be captured, without chopping, at the cost of degraded flicker noise. The configuration control is implemented as follows (Fig. 5). The chopping clock f_{chop} is set to 1 (DC) for configuration 1 (no chopping is performed and the two input signals are passed through without swapping) or to the nominal chopping frequency for configuration 2. The word FILTER COEFFICIENT sets the feedback LPF corner frequency (f_1 in Fig. 3) and is digitally programmed such that the desired overall channel HPF corner frequency is set (equal to $f_1(1 + \text{AB})$ in Fig. 3, where A and B are the forward and feedback gains, respectively). The input signal is generally band-limited. The highest frequency of the input signal is limited by the type of electrode used, the front-end electrode multiplexer circuit design (if any), and the location of the recording. For example, scalp EEG electrodes and many ECoG (electrocorticography) electrodes commonly produce signals limited to 1 kHz maximum frequency whereas microelectrodes can record up to several kHz. When electrodes are multiplexed, passive anti-aliasing filters act as band limiters. For non-band-limited signals, a dedicated second-order switched-capacitor LPF (not shown in Fig. 5) that follows the amplifier has also been included in a version of this design in order to improve the frequency band selectivity and has been successfully experimentally tested.

Using this amplifier architecture has two advantages for input impedance when employing chopping. First, the mixed-signal feedback removes the DC blocking capacitor [C_1 in (3)] and thus eliminates the input-referred noise integration term. Therefore hundreds-of-pF capacitors for noise reduction, which also cause significant input impedance reduction, are not required. Second, C_1 in (4) is only the amplifier input transistors parasitic capacitance (Cgs) which is in the order of fF (compared to the DC blocking capacitors which are at least 20 pF). So the impedance reduction is much smaller compared to AC-coupled chopper-stabilized neural amplifiers.

The mismatches in the OTA circuit cause a systematic offset. This offset as well as the DC offset from the tissue are canceled by the mixed-signal feedback. However, when the chopper modulation is activated the OTA offset is up-modulated to the chopper clock frequency (2 kHz) and can not be sensed and removed by the low-cutoff-frequency (f1 in Fig. 3) digital low-pass filter. This up-modulated offset can be removed by an additional low-pass filter off-chip or in software. The ripple due to the OTA offset will be a high frequency signal with respect to the feedback path pole. Therefore it will be filtered and does not affect the functionality of the digital loop.

The chopper amplifier gain is calculated as [28], [29]

$$A_{\text{chopper}} = A_0(1 - 4\tau/T) \tag{5}$$

where A_0 is the OTA gain, T is the chopper clock period, and $\tau = 1/(2\pi\text{BW})$, where BW is the bandwidth of the OTA (5 kHz). As demonstrated by (5), chopping imposes a reduction in the unitless amplifier gain. For example, in order to achieve a 25 percent gain reduction, the amplifier bandwidth should be approximately 3 times larger than the chopping frequency. Such a gain reduction is in fact desirable as in the chopping configuration the inputs to the system are mainly local field potentials which can have significantly higher amplitudes (especially during pathological brain states when signals can reach several millivolts amplitudes, such as epileptic seizures we are interested in monitoring). This supports the choice of the chopping frequency and the amplifier bandwidth as 2 kHz and 5 kHz, respectively. The nominal amplifier gain (without chopping) is 52 dB. It should be noted that the OTA bandwidth

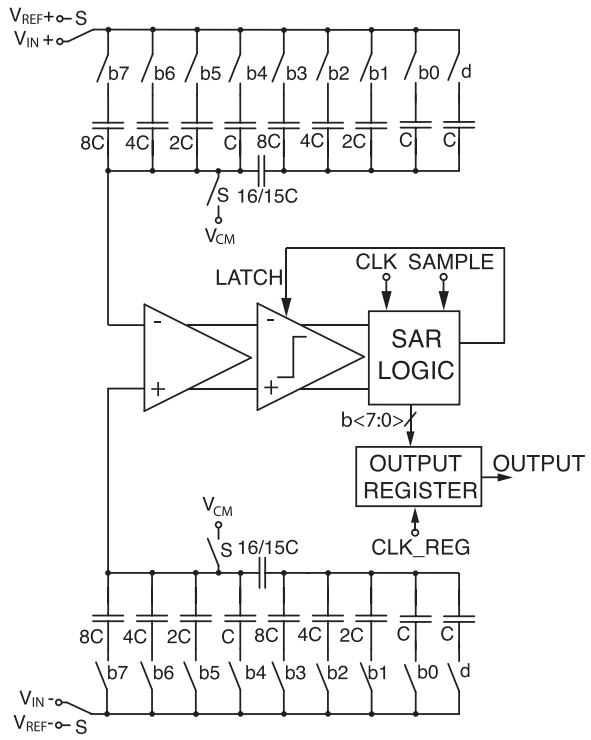

Fig. 7. Differential SAR ADC.

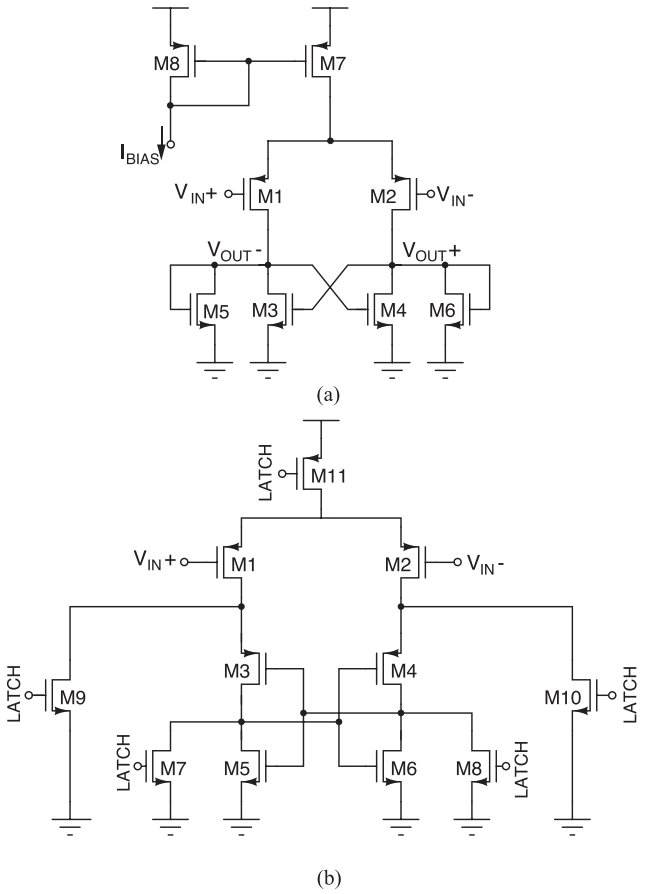

Fig. 8. The SAR ADC comparator circuit diagram. (a) Comparator preamplifier. (b) Comparator latch.

is set considering a trade-off between the amplifier input-referred noise and the gain error after chopping, since the OTA acts as an anti-aliasing filter for the ADC in this configuration. The OTA also provides the analog filtering to low-pass filter the shaped noise of the delta-sigma modulator employed in the current-output DAC, as is further explained in Section III-C3.

The input impedance of this architecture can be calculated using (2). The input capacitor consists of the parasitic gate capacitance (Cgs) of the thick-oxide transistors M1 and M2 which is equal to approximately 0.5 pF. With the chopping frequency of 2 kHz, the equivalent input resistance is approximately 1 GOhm. Due to the absence of hundreds-of-pF DC blocking capacitors the input impedance reduction is less compared to that in Fig. 2(a) and (b) and the impedance boosting circuitry is not required.

The total input-referred noise of the closed-loop system using superposition is equal to

$$\overline{V_{n,\mathrm{in}}^2} = \overline{V_{n,\mathrm{inOTA}}^2} + \overline{V_{n,\mathrm{IDAC}}^2} + \left(\frac{\overline{V_{Q,\mathrm{ADC}}}}{A_{\mathrm{OTA}}}\right)^2 \qquad (6)$$

where $V_{n,\mathrm{inOTA}}$ is the total input-referred noise of of the OTA, $V_{n,\mathrm{IDAC}}$ is the total noise contribution of the IDAC, $V_{Q,\mathrm{ADC}}$ is the quantization noise of the ADC and A_{OTA} is the amplifier gain. The OTA input-referred noise includes the thermal and flicker noise terms dominated by the input differential pair and the output current source transistors. In order to minimize the thermal noise contribution large g_{m1} and relatively small g_{m4} and g_{m10} are required. The output noise of the IDAC is dominated by the thermal noise from the tail reference current of the DAC slices. The tail current of the DAC slices can be considered as extra current sources on the folding node. Therefore, similarly to the folded-cascode OTA main current sources, the IDAC tail current sources should have small g_m and the IDAC noise contribution is referred to the input by dividing it by g_{m1}. The ADC quantization noise is referred to the input by dividing it by amplifier gain. When the chopper is activated the OTA flicker noise is up-modulated to a high frequency. However the IDAC and ADC noises pass through two sets of chopping switches and appear at a low frequency at the output of the OTA along with the signal.

The OTA requires 8.3 μA of current, which includes 4.9 μA to the input pair transistors and 3.4 μA into the cascode transistors. Also 1.2 μA of current is consumed in the biasing current mirror network of the OTA. All the currents are provided from a 900 nA external current source.

B. Fully Differential SAR ADC

The analog output from each channel is digitized by a column-parallel ADC. The ADC is shown in Fig. 7. It is implemented as an 8-bit capacitive charge-redistribution SAR ADC. This architecture was chosen for its low power consumption, and its medium speed and medium resolution which make it suitable for neural signal acquisition. Split-capacitor array is utilized to minimize the overall ADC area and power dissipation. Each unit capacitor is implemented using a MIM (metal-insulator-metal) capacitor with a unit size of 100 fF. The non-binary nature of the split-capacitor structure aggravates the effects of parasitic capacitors on the ADC resolution. In order to mitigate this issue, the middle capacitor value is reduced

TABLE III
ADC COMPARATOR AND IDAC TRANSISTOR SIZES

Transistor (Preamplifier)	W/L (μm)	Transistor (Latch and IDAC)	W/L (μm)
$M_{1,2}$	$4 \times 2.5/1$	$M_{1,2}$	$2 \times 1/1$
$M_{3,4}$	$2 \times 0.5/8$	$M_{3,4}$	$0.5/0.12$
$M_{5,6}$	$2 \times 0.5/8$	$M_{5,6}$	$1/0.12$
M_7	$8 \times 0.5/2$	$M_{7,8}$	$0.32/0.12$
M_8	$0.5/2$	$M_{9,10}$	$0.32/0.12$
–	–	M_{11}	$1/0.5$
–	–	$M_{12,13}$	$4/0.5$
–	–	M_{14}	$6 \times 0.5/5$

after post-layout simulations. The sampling rate of the ADC should be set on higher than the Nyquist rate. As the digital output of the ADC is fed back to the OTA through the mixed-signal feedback, the noise folded back to low frequency due to aliasing will appear at the output of the OTA and increase the input-referred noise of the analog front-end. The OTA provides first-order filtering. Simulation results show that the sampling rate of the ADC should be set at least 10 times higher than the OTA bandwidth to achieve lower than 10 μV input-referred noise (due to the first-order OTA amplitude response roll-off). The preamplifier and the latch inside the SAR ADC comparator are shown in Fig. 8(a) and (b), respectively. The transistor sizes for the comparator preamplifier and latch are given in Table III.

C. Low Frequency Suppressing Feedback

As mentioned in the previous sections, the differential DC voltage at the neural recording electrodes should be filtered (i.e., blocked) prior to amplification in order to avoid the DC drift that saturates the amplifier. The tissue DC offset and low-frequency signals are suppressed by a mixed-signal feedback, which functions as a DC servo loop. The feedback element has a low-pass transfer function and creates a high-pass characteristic in the closed-loop system as was described in Fig. 3. The stability considerations and the details about each block in the feedback are discussed in the following sections.

1) Loop Stability Considerations: Stability considerations must be taken into account for designing the feedback blocks. The transfer function of the feedback loop, illustrated in Fig. 5, in discrete-time domain is equal to

$$H(z) = \frac{H_{\mathrm{LNA}}(z)H_{\mathrm{ADC}}(z)}{1 + H_{\mathrm{LNA}}(z)H_{\mathrm{ADC}}(z)H_{\mathrm{LPF}}(z)H_{\mathrm{DAC}}(z)}$$

where H_{LNA}, H_{ADC}, H_{LPF}, and H_{DAC} are the z-domain transfer functions of the OTA, the SAR ADC, the digital low-pass filter, and the DAC, respectively and $H(z)$ is the closed-loop transfer function. The dominant pole in the feed-forward path is created by the OTA low-pass corner frequency. The digital filter should be designed such that sufficient phase margin is provided at the unity-gain frequency of the loop to ensure stability. Otherwise, unwanted oscillations or saturation will be observed in the output common-mode. Also, the delay in the ADC and the DAC cause a phase shift that may lead to instability.

For the ADC and DAC this delay is equivalent to Z^{-1} in the transfer function. If a causal and stable continuous-time IIR filter can be designed for the feedback low-pass filter, the corresponding casual and stable discrete-time filter can be implemented using a bilinear transform [30]. Assuming the on-chip ADC and DAC have a high sampling rate and do not contribute considerably to the reduction of the phase margin, the continuous-time transfer function is dominated by the OTA and LPF

$$H(s) = \frac{\frac{A}{1+s/p_2}}{1 + \frac{A}{1+s/p_2}\frac{B}{1+s/p_1}} \tag{7}$$

where A is the OTA DC gain, B is the feedback low-pass filter DC gain, and $-p_1$ and $-p_2$ are the LPF and OTA dominant poles, respectively. In order to achieve a 45-degree phase margin the two poles must be at least one order of magnitude apart from each other. A large gain in the OTA and the low-pass filter enables cancelation of a larger DC offset. However, the larger gain mandates a smaller pole in the low-pass filter (less than 5 Hz) to avoid instability. The sampling rate for the corresponding digital LPF in the feedback must be set equal to the ADC sampling rate (at least 25 kHz) to avoid aliasing. This leads to a digital filter with a very small 3 dB frequency to sampling rate ratio which is not trivial to design. Also, according to the feedback bandwidth extension property, the high-pass pole in the closed-loop transfer function is equal to the feedback LPF dominant pole times the loop DC gain. In the (7), if we assume $p_2 \gg p_1$ the transfer function can be rewritten as

$$H(s) = \frac{A(1 + s/p_1)}{1 + s/p_1 + AB}$$

which shows the closed-loop system has a zero at $-p_1$ and a pole at $-p_1(1 + AB)$. Thus the LPF pole must be decreased to less than 0.1 Hz to achieve a high-pass pole of less than 5 Hz in the overall transfer function.

Another way to implement the low-pass filter, that relaxes the stability requirements and provides a very small constant-value high-pass pole, is using an ideal integrator ($H(s) = 1/\mathrm{s}$). The closed-loop transfer function of a system using an ideal integrator is equal to

$$H(s) = \frac{\frac{A}{1+s/p_2}}{1 + \frac{A}{1+s/p_2}\frac{B}{s}} \tag{8}$$

where A is the OTA DC gain, B is the ideal integrator gain factor, and p_2 is the OTA dominant pole. For frequencies much smaller that p_2, $A_{\mathrm{midband,CL}} \sim A$. This transfer function has a zero at DC and two poles at

$$p_1', p_2' = \frac{\left(-1 \pm \sqrt{1 - \frac{4AB}{p_2}}\right) p_2}{2} \tag{9}$$

where p_1' and p_2' are the poles of the closed-loop system. p_2' is very close to p_2 and corresponds to the minus sign. Taking the partial derivative of p_1' and p_2' with respect to A (OTA gain) and p_2 (OTA bandwidth) yields

$$\frac{\partial p_1', p_2'}{\partial A} = \frac{\mp B}{\sqrt{1 - \frac{4AB}{p_2}}} \tag{10}$$

$$\frac{\partial p_1', p_2'}{\partial p_2} = \frac{-1}{2} \pm \left(\frac{1}{2}\sqrt{1 - \frac{4AB}{p_2}} + \frac{AB/p_2}{\sqrt{1 - \frac{4AB}{p_2}}}\right). \tag{11}$$

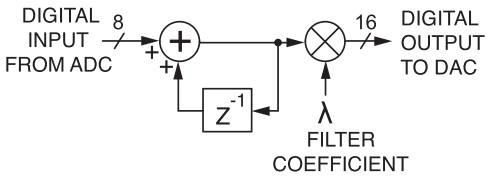

Fig. 9. Low-pass filter implemented as a digital integrator circuit.

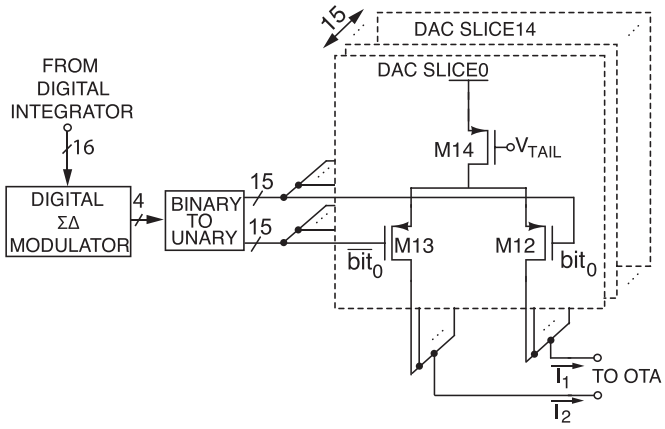

Fig. 10. The current-steering I-DAC in the feedback.

If the integrator gain factor is set such that $B \ll 1$ and $AB \ll p_2$ (10) will be equal to $-B$ for p_1' and $+B$ for p_2'. Also (11) will be equal to 0 for p_1' and 1 for p_2'. Therefore a constant high-pass pole (p_1') with very small variations over PVT corners can be achieved. An ideal integrator is impossible to achieve in the analog domain, however it can be designed fairly easily in the digital domain.

2) Digital Low-Pass Filter: Attenuation of the unwanted low-frequency drift requires the ability to program the bandwidth, enabling the removal of a specific portion of the low-frequency band that is not of interest in the recording. Programmability also enables adjusting the high-pass pole for compensation of process variations. Therefore it is essential to be able to define the high-pass pole with high precision. A digital low-pass filter provides easier programming to adjust the pole and enables creating a well-defined high-pass pole frequency. The digital integrator utilized as a LPF is shown in Fig. 9. In order to guarantee stability in the DC cancelation loop a first-order integrator is used as a low-pass filter, since for such low-pass filter the pole will be at zero. The integrator output is multiplied by a 5-bit filter coefficient (λ in Fig. 9). Multiplication is implemented as a shift register in which λ determines the number of shifts. The digitally-programmable high-pass pole does not vary with the large swing at the OTA output, or process and temperature variations and linearity is preserved at low frequencies. Theoretically, the sampling rate of the integrator should be set equal to that of the ADC (50 kHz). Since the signal of interest in the feedback path is low frequency, it is possible to use a lower clock rate for the integrator. The integrator sampling clock is set to 25 kHz, which is equivalent to dropping every other sample.

3) Current-Output DAC: The current-steering DAC is shown in Fig. 10. Transistor sizes are listed in Table III. The tail current source transistor considerations are the same as those in the OTA.

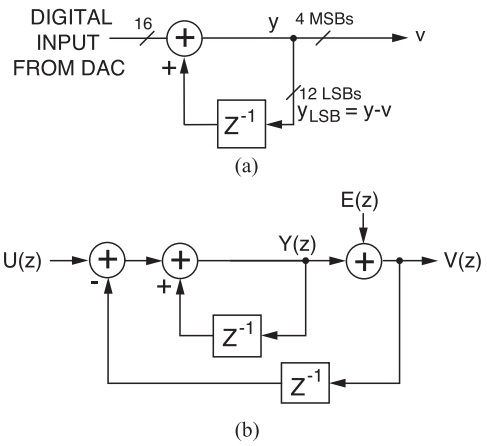

Fig. 11. Digital delta-sigma modulator in the DAC. (a) Block diagram. (b) z-domain model.

The integrator has a 16-bit output to integrate the DC offset while preserving the MSB for fast offset cancellation (corresponding to a larger high-pass pole). When λ is increased from 0 to higher values, more bits are shifted to the right for slower offset integration (corresponding to smaller high-pass pole). A first-order delta-sigma modulator is used after DC offset integration to reduce the number of bits from 16 (at the output of the integrator) to 4 [31], [32]. This lowers the area and resolution requirements for the subsequent digital-to-analog conversion. These binary 4 bits are subsequently converted to 15-bit thermometer-coded to control the IDAC.

Delta-sigma modulation shifts the quantization noise to high frequencies, and the shaped noise roll-off is determined by the order of the modulator. Typically, the shaped noise is filtered in the analog domain, and the order of the analog filter should ideally be one order higher than the modulator to provide sufficient removal of the quantization noise [32]. An explicit analog filter has not been used in the presented design in order to preserve the power and channel area reduction. The shaped noise is filtered by the feed-forward OTA low-pass characteristic. The first-order roll-off of the OTA introduces a portion of this noise to the ADC, which consequently leads to noise folding due to aliasing. This issue imposes a limitation on the order of the modulator. Therefore, a first-order modulator is used and the number of bits is reduced to 4, instead of 1, to reduce the amount of modulator shaped-noise fed to the ADC. Using multiple bits imposes additional DAC area requirement, as more transistor pairs are required in the current-steering DAC. However, it relaxes the requirement on the ADC sampling frequency and dynamic range, due to the smaller amount of modulation noise fed back to the feed-forward path. In order to further reduce the in-band noise and push it to higher frequencies, the modulator oversamples the integrator output at 5 MHz, which is 1000 times larger than the OTA 3-dB bandwidth.

The block diagram of the delta-sigma modulator is shown in Fig. 11(a). In this configuration the output of the summer in time domain equals

$$y(n) = u(n) + y(n-1) - v(n-1)$$

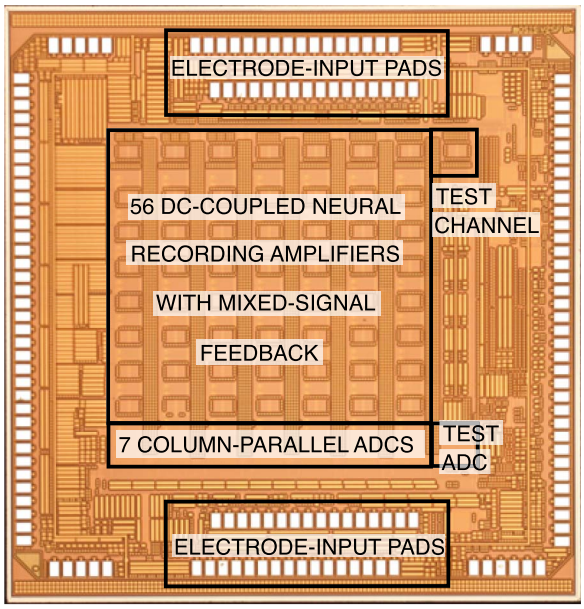

Fig. 12. The die micrograph of the 3 mm × 2.9 mm 0.13 μm CMOS neural recording interface.

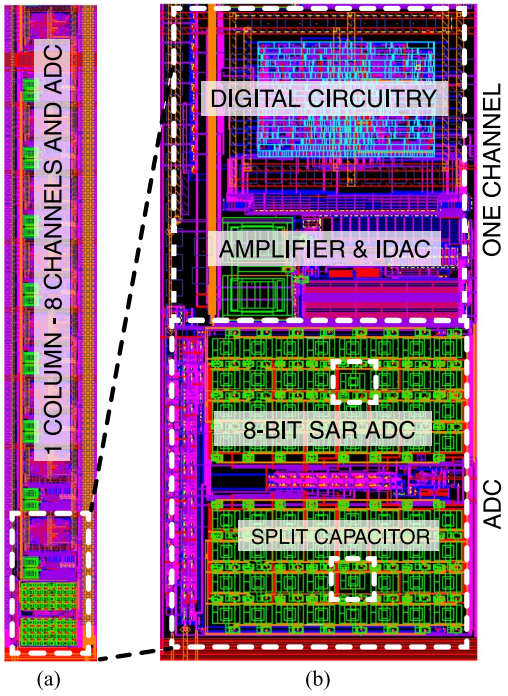

Fig. 13. (a) The layout of one column of the neural recording array. (b) The bottom-most channel in a column and the column parallel ADC zoomed in. The channel includes an amplifier, digital circuitry and an IDAC.

where $y(n-1) - v(n-1)$ denotes the 12-bit error fed back to the input. The linear z-domain model of the modulator is shown in Fig. 11(b). The output equals

$$V(z) = U(z) - V(z)Z^{-1} + Y(z)Z^{-1} + E(z)$$
$$V(z) = U(z) + (1 - Z^{-1})E(z)$$

in which the NTF(z) (noise transfer function) is a first-order function. The 4-bit code from the modulator is binary-to-thermometer encoded, to improve linearity and avoid glitches, and is used to control the current-steering DAC.

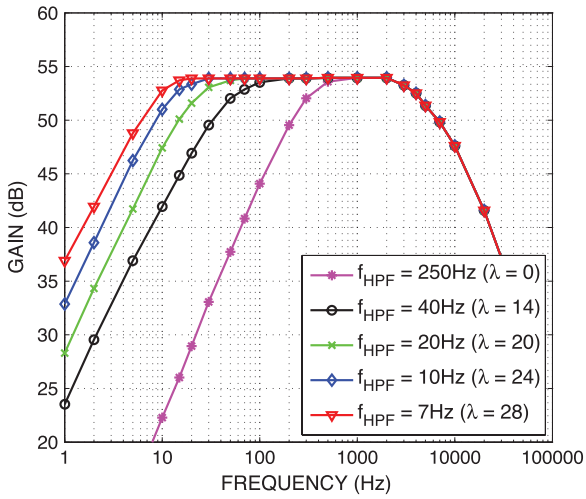

Fig. 14. Experimentally measured amplitude response of one channel for five different digital LPF gain coefficients.

IV. Experimental Results

A. IC Prototype and Testing Setup

Fig. 12 shows the micrograph of the prototype implemented in a standard 1P8M 0.13 μm CMOS technology. It occupies an area of 2.9 × 3 mm^2 and includes an array of 8 × 7 neural recording channels and a bank of seven column parallel SAR ADCs (plus one test channel and one test ADC). Fig. 13(a) shows the floorplan of one column in the array and Fig. 13(b) shows that of one channel including the amplifier, IDAC and digital circuitry, as well as the ADC. The first channel in a column has extra routing for the debugging option to use off-chip digital feedback. The total system power dissipation is approximately 1.07 mW from a 1.2 V supply.

The integrated circuit has been experimentally characterized using a test PCB. Two test channels are provided on the chip to monitor the analog output of the amplifier. These test channels include a source follower at the output to drive the capacitive load of the pads and an SMA cable from the amplifier output to a scope or a network analyzer (100 pF/meter). In order to generate signals in the order of a microvolt a 20 dB attenuator has been used.

B. IC Measurement Results

The experimentally measured amplitude frequency response of one neural recording channel is shown in Fig. 14. The figure shows the high-pass filter frequency adjusted from approximately 5 Hz to 250 Hz by modifying the digital integrator gain coefficient λ. The high-pass pole can also be modified by changing the integrator sampling frequency.

Fig. 15(a) shows the frequency response of 8 different channels from 5 different dice for minimum f_{HPF} setting ($\lambda = 28$). This figure shows a voltage gain spread between 50.7 dB and 54 dB and the low-pass filter corner frequency varies from 3 kHz to 6.5 kHz. Fig. 15(b) shows the histogram of midband gain variation for eight channels. This gain and bandwidth spread happens as a results of using the OTA in an open-loop configuration, in which the mismatch between transistors can cause random variations over PVT (process, supply voltage,

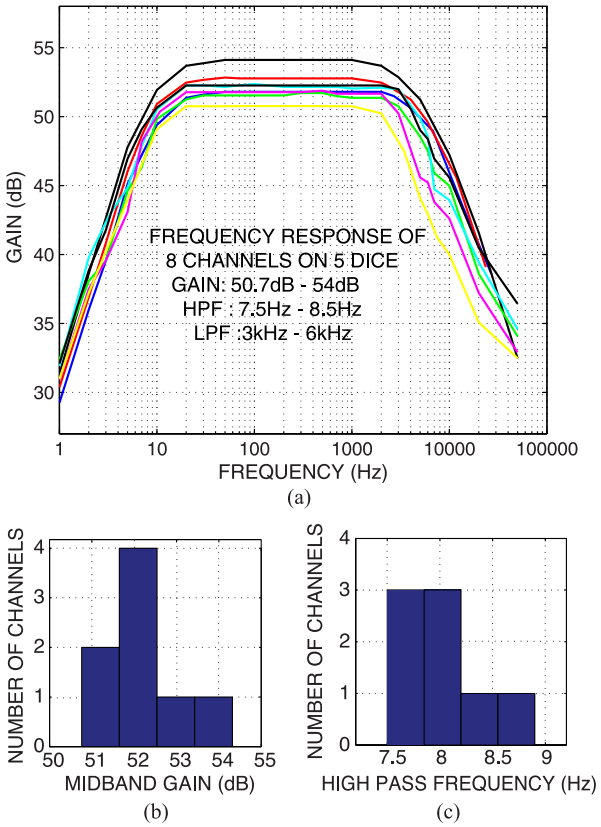

Fig. 15. (a) Experimentally measured amplitude response of eight different channels on five CMOS dice for $f_{\rm HPF} = 7.5$ Hz ($\lambda = 28$). Histogram of (b) $f_{\rm HPF}$ and (c) gain variation of the eight channels.

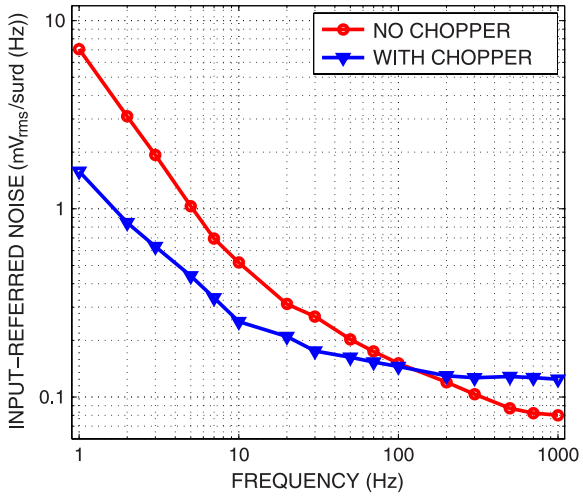

Fig. 16. Experimentally measured input-referred noise.

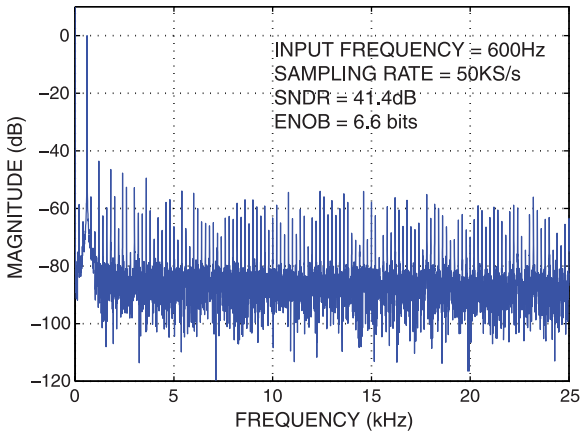

Fig. 17. Experimentally measured FFT of an ADC output for 600 Hz sinusoid input sampled at 50 kS/s.

temperature). As mentioned in Section III-C1, the digital feedback does not control the gain as a conventional analog feedback would ($1/\beta$ in the conventional β-gain feedback). The feedback element adds a certain amount of current to the input branches of the OTA to compensate for the input DC voltage imbalance making the output DC voltage levels at the negative and positive nodes equal. Therefore, the overall gain is equal to the OTA gain and follows the OTA gain variations over PVT. For higher-frequency (i.e., non-DC) signals the feedback element will appear non-existent. Fig. 15(c) shows the histogram of high-pass cut-off frequency, nominally set to 7.5 Hz (lambda $= 28$), for eight channels. This is the highest value we ever use for the HPF cut-off frequency. This is because our application is to monitor neuronal oscillations as described in Section I, not purely spikes. The spread of the HPF cut-off frequency at frequencies below 7.5 Hz is less than what is shown in Fig. 15(c). As shown in the analysis in Section III-C1, for a smaller integrator gain factor, there is less variation in the HPF cut-off frequency. The gain factor is set by lambda and it decreases with higher lambda setting. For lambda settings of higher than 14, AB is much smaller than p_2 and the variation in the HPF cut-off frequency is very small. Using this method, variation of less than 10 percent in the high-pass corner frequency can be achieved. As motivated in Section I, this is a key result of this work.

The output noise has been measured by a network analyzer. The integrated input-referred noise without chopping measured over the bandwidth of 10 Hz to 5 kHz is 5 $\mu V_{\rm rms}$ (at room temperature), which yields a noise efficiency factor of about 7 [33]. For a maximum offset of 50 mV at the input, the input-referred noise goes up to the worst case of 5.4 $\mu V_{\rm rms}$. It should be noted that the noise measured by the network analyzer includes the extra noise contribution from the sampling ADC due to noise folding, as explained Section III-B. The noise efficiency factor is calculated using the power consumption of the entire channel and the share of the ADC power for each channel. The noise figure can be easily improved by using a higher-order analog LPF in the feedforward path. The experimentally measured common-mode rejection ratio (CMRR) for a typical channel at 500 Hz is 65 dB.

The input-referred noise plot versus frequency without and with chopping at 2 kHz is shown in Fig. 16. Chopping reduces the integrated input-referred noise over the 1 Hz to 1 kHz bandwidth from 7.5 $\mu V_{\rm rms}$ to 4.2 $\mu V_{\rm rms}$. This is the noise of the entire system including OTA, ADC and IDAC. The remaining $1/f$ noise when chopping is likely due to the $1/f$ noise in the DAC as its output is not chopped. The higher thermal noise floor when chopping is likely due to folding of aliased noise back into the signal band.

The ADC performance has been characterized by a 600 Hz sine test input sampled at 50 kS/s. Such sampling rate is chosen according to the aliasing requirements. The experimentally

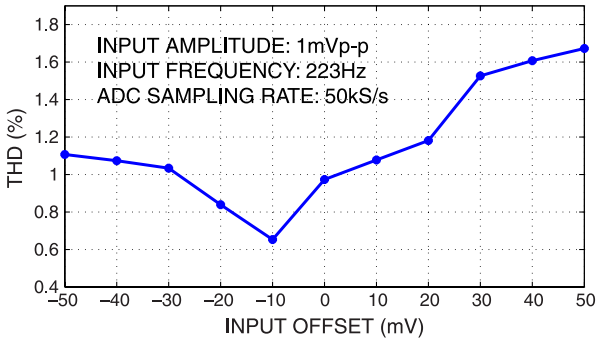

Fig. 18. Amplifier THD for 1 mVp-p, 223 Hz input signal for input offset voltages from −50 mV to 50 mV.

TABLE IV
IC EXPERIMENTALLY MEASURED CHARACTERISTICS

System	
Technology	0.13μm CMOS
Supply Voltage	1.2V
Die Dimensions	2.9mm×3mm
No. of Recording Channels	56
Area per Channel	150μm×120μm
Power Dissipation	1.07mW
SNDR	41.4dB
ENOB (front-end, ADC, digital and IDAC)	6.6 bits
Front-end	
Typical Gain	52dB
Gain Mismatch	50.7-54dB
Low-Frequency Cut-off (programable)	1-400Hz
Typical High-Frequency Cut-off	5kHz
High-Frequency Cut-off Mismatch	3-6.5kHz
Input-Referred Noise	5μV
Power Dissipation (per 1 ADC)	9.9μW
NEF	7
CMRR	65dB
THD (at 0mV offset)	0.95%
ADC	
Resolution	8-bit
Power Dissipation @ 50kSps	2.6μW
Input Range	600mVp-p
Max Sampling Rate	200kSps

measured ADC performance is shown in Fig. 17. The ENOB of two of the ADC outputs in two columns on the same die is measured to be approximately 6.6 when sampled at 50 kS/s. The ENOB reported includes the noise sources of the entire system (the LNA thermal and flicker noise, the IDAC thermal and flicker noise, and the quantization noise and nonidealities of the ADC). The ADC nominal sampling rate is 50 kS/s. This translates to the maximum signal bandwidth of 3.125 kHz for recording neural signal from 8 channels in a column. The nominal signal bandwidth specification for observing neuronal signal oscillations in the mammalian brain (e.g., due to epilepsy) is 1 kHz. This is sufficiently below the maximum allowed signal bandwidth of 3.125 kHz. This is the reason why the ADC power dissipation of 2.6 μW is measured when operating at 50 kS/s. For a constant supply voltage the power dissipation of the ADC scales linearly with frequency to the maximum sampling rate of 200 kHz.

The experimentally-measured total harmonic distortion (THD) of the front-end versus input offset voltage is shown in Fig. 18. The THD was measured with an amplifier input amplitude of 1 mVp-p for different input offset voltages from −50 mV to 50 mV. The ADC sampling frequency was set to 100 kS/s.

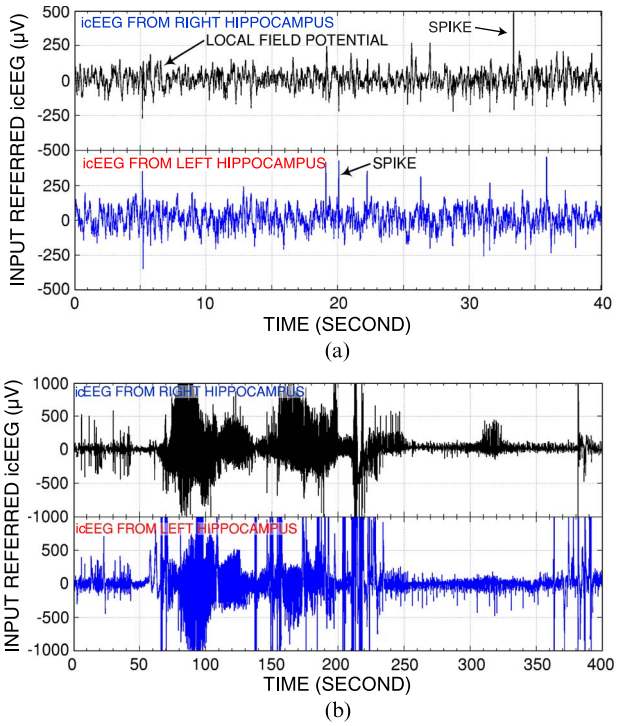

Fig. 19. Intracranial EEG (icEEG) experimentally recorded from a Wistar rat brain. (a) Spikes and local field potential recording. (b) Abnormal (epileptic seizure) intracranial EEG recordings.

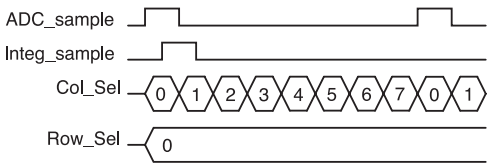

Fig. 20. Timing diagram showing the sequence of sampling clocks and channel select controls.

For input offsets higher than ±50 mV the amplifier output is saturated.

Each channel consumes 12.5 μA in the front-end (OTA and DAC), from which 8.3 μA is used in the OTA, 3 μA is used in the biasing network, and 1.2 μA is consumed in the current-steering DAC, all from a 1.2 V supply voltage (15 μW in total). The digital block in each channel consumes 2.9 μA and the ADC in each column consumes 2.2 μA from a 1.2 V supply (2.64 μW).

Each channels in the neural recording array occupies 0.018 mm^2, which includes the analog front-end and the digital feedback. The area of the digital section can be easily reduced by using a smaller technology node. A 40 times area reduction has been observed by synthesizing the same RTL verilog code in a 28 nm technology. Each differential SAR ADC area is 0.03 mm^2. A large portion of this area is occupied by the capacitors in the split-capacitor array.

System-level experimental results are summarized in Table IV.

C. In Vivo EEG Recording Results

The integrated circuit was validated in on-line *in vivo* experiments in freely moving Wistar rats. Three depth electrodes were implanted into the hippocampus and the frontal lobe of a rats, with two electrodes connected to the inputs of two channels of

TABLE V
COMPARISON OF FULLY INTEGRATED NEURAL RECORDING ICS

Reference	[15]**	[35]	[16]**	[11]	[19]	[24]	[6]	[36]	[27]**	THIS WORK	
Conf./Journ.	JSSC Harrison	ESSCIRC Lacaita	JSSC Ghovanloo	TBioCAS Van Hoof	BioCAS Xu	TBioCAS Sawan	TCAS-I Chan	ISSCC Yuce	JSSC Rabaey		
Year	2007	2010	2010	2011	2012	2007	2005	2008	2013		
System											
CMOS Tech.	0.5μm	0.35μm	0.5μm	0.18μm	0.35μm	0.18μm	0.5μm	0.35μm	65nm	0.13μm	
Area(mm)^2	27.3	8.4	16.3	6.48	N/A	N/A	4.8	63.4	N/A	8.7	
Supply(V)	3.3	3.0	3.0	1.8	3	1.8	$\pm$1.5	3.3	0.5	1.2	
Power(mW)	13.5	17.2	7.05	0.16	0.06	0.08	1.4	6.0	N/A	1.07	
# Rec. Chan.	100	16	32	8	1	1	1	128	4	56	
LNAs											
Fully Diff.	No	No	Yes	No	No	No	Yes	Yes	Yes	Yes	
Power/ch.(μW)	38	9	75	20	6	8.5	1000	11	2.6	18	
Area/ch.(mm^2)	0.04	0.04	0.1*	0.2*	0.056	0.05	0.56	0.3*	0.03	0.018	
Gain(dB)	60	60	68-78	10-40	38	50	0-80	57-60	46	50-54	
BW(Hz)	300-5k	10k	0.1-8k	0.5-1k	1.5-8.5k	98-9.1	0.3-150	0.1-20k	1-10k	1-5k	
Noise(μV_{rms})	5.1	3.1	9.3	0.8	6.72	5.6	0.86	4.9	6.5	4.2 w/ chopping, 7.5 w/o chopping	5 at 0mV offset, 5.4 at 50mV offset
Noise BW(Hz)	300-5k	300-10k	1-10k	0.5-100	100-8.5k	100-9k	0.3-150	N/A	10-10k	1-1k	10-5k
NEF	N/A	2.5	N/A	12.3	8.5	4.9	N/A	N/A	4.3	7	
# chop. Amp	0	0	0	8	0	0	1	0	0	56	
ADC											
Type	1xSAR	1xSAR	PWM	N/A	N/A	N/A	N/A	1xSAR	1xVCO-based	8xSAR	
Resolution	9b	8b	N/A	N/A	N/A	N/A	N/A	6-9b	10b	8b	

* Estimated

** Includes wireless communication and power management

the neural recording integrated circuit and the third one acting as a reference electrode, connected to 0.6 V reference voltage. The amplifier was programmed for a bandwidth of 5 Hz to 5 kHz. Fig. 19(a) shows the normal (i.e., non-epileptic) intracranial EEG recorded from the right (top) and left (bottom) hippocampus. Local field potentials and single-neuron activity can be easily observed.

Kainic acid was injected into a rat brain to induce a non-convulsive epileptic seizure in the rat. The recorded abnormal activity is shown in Fig. 19(b). These are typical recordings of seizures in a rat model of epilepsy.

V. DISCUSSION AND COMPARATIVE ANALYSIS

The presented design example uses an amplifier in an open-loop configuration, which causes a spread in the amplifier gain and LPF cutoff frequency values due to the transistors mismatch. This effect consequently causes different values for input-referred noise from channel to channel. This issue can be mitigated by calibration in software. Another solution we have implemented is modifying the SAR ADC to become a multiplying ADC (MADC) as presented in [34]. Using multiplying ADC mismatch effects can be captured by programming the gain-calibrating multiplication factor in the feed-forward path. The LPF cutoff frequency mismatch is easily eliminated by an extra LPF [9].

The multiplexing control signals and ADC clocks are provided through an FPGA off-chip. The channels are scanned using two control signals Row_Sel and Col_Sel, as shown in Fig. 5. ADCs are time multiplexed due to the limited silicon space available for the presented prototype. Due to ADC column-wise time multiplexing, the feedback loop requires a period of time for baseline stabilization. This time ranges from 4 ms for lambda set to 0 to 600 ms for lambda set to 24. Changing Row_Sel causes the DC stabilization feedback loop to open and close and would require such a delay time for the loop to stabilize. Due to this delay required for loop stabilization, for tests where real-time recording is desired, Row_Sel is kept constant. The Col_Sel scans the outputs of the ADCs at the rate of 8 times the ADC sampling rate as there are 8 columns in the array each with one ADC, with the last column providing only one row for a single test channel. Since the output multiplexer is connected to all the ADCs, Col_Sel must scan through all the

8 columns in the array. The sequence of sampling clocks and channel select controls is demonstrated in Fig. 20.

All the digital inputs are provided off chip and include clocks to the ADC and integrator and the array scanning control signals. The inputs which should be synchronized are the scanning control signals and the ADC sampling clock, which is done fairly easily in software off-chip, due to the low speed of the control signals compared to the gate delays. We have also implemented another prototype of the presented front-end (within a large-scale implantable neurostimulator system) where an ADC is implemented within each channel under the same area constraint [34]. In that case all channels operate in real time and no such latency constraint exists.

A comparison with other reported integrated neural recording interfaces is given in Table V. As explained in Section II, using chopper switches in AC-coupled amplifiers requires capacitors larger than 500 pF, which make the amplifier unsuitable for integrating a large number of channels. The presented design has the smallest area per channel among the fully-integrated neural recording interfaces. The area can be reduced further using smaller technology nodes as explained in Section IV. In all the designs, excluding [27], the high-pass pole is implemented using passive components which makes the system prone to nonlinearity and distortion, as explained in Section II. In this design, the high-pass pole is implemented in the digital domain which makes it well-defined and more accurate. Power dissipation is comparable as the digital active feedback block imposes a power overhead. This design provides the highest channel integration density, with moderate input-referred noise and power consumption.

VI. Conclusion

One of the challenges in neural amplifier design is removing the tissue DC offset, which can saturate the amplifier. Conventionally, a large capacitor is placed at the input to block the tissue DC voltage. Using a digital low-pass filter in the feedback is an alternative approach to reduce the neural recording channel area. In this paper we presented such a DC-coupled digitally-assisted chopper-stabilized neural recording IC. The 0.13 μm CMOS die integrates 56 compact fully differential recording amplifiers with seven column-parallel differential SAR ADCs. The DC-blocking capacitors at the input of the amplifier are replaced by a mixed-signal feedback, that senses the DC offset at the output of the amplifier and feeds a certain amount of current back to the amplifier to cancel the DC offset. This approach provides a significant area reduction and ability to use chopper switches for flicker noise reduction. Area reduction enables integrating many neural recording channels on a single chip to achieve finer spatial resolution in the recorded neural data. The total power dissipation of the integrated circuit is 1.07 mW from a 1.2 V supply. The integrated circuit has been validated *in vivo* in online intracranial EEG recording in freely moving rats.

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Arezu Bagheri (S'11) received the B.Sc. degree from the University of Tehran, Tehran, Iran, and the M.A.Sc. degree, both in electrical and computer engineering, from the University of Toronto, Toronto, ON, Canada.

She worked as a Research Assistant at the Intelligent Sensory Microsystem Laboratory at the University of Toronto and her research focused on DC-coupled digitally-assisted neural recording amplifiers. Currently, she is an Analog Design Engineer at Semtech Snowbush IP, working on design and development of high-speed SerDes devices. She was the recipient of the Ontario Graduate Scholarship in 2011.

Muhammad Tariqus Salam (M'09) received the B.Sc. degree in electrical and electronics engineering from the Islamic University of Technology, Gazipur, Dhaka, Bangladesh, the M.A.Sc. degree in electrical and computer engineering from Concordia University, Montréal, Montréal, QC, Canada, and the Ph.D. degree in electrical engineering from École Polytechnique de Montréal, University of Montréal, in 2003, 2007, and 2012, respectively.

He finished his first postdoctoral training in the Intelligent Sensory Microsystems Laboratory and Hospital for Sick Children Hospital. Currently, he is in his second postdoctoral fellowship in Toronto Western Hospital with an industrial partner. His specific research interests are in the areas of low-power circuit design, brain-machine interface, mental disease diagnosis, and closed-loop therapy.

Jose Luis Perez Velazquez was born in Zaragoza, Spain. He received the degree of "Licenciado" in Chemistry (biochemistry, University of Zaragoza, Zaragoza, Spain, and the Complutense University of Madrid, Spain), and the Ph.D. degree from the Department of Molecular Physiology and Biophysics, Baylor College of Medicine, Houston, TX, USA.

He homologated to Doctorate in Chemistry by the Spanish Ministry of Culture in 1997. He is an Associate Scientist in the Neuroscience and Mental Programme and the Brain and Behaviour Center at the Hospital For Sick Children, Toronto, ON, Canada, and Associate Professor at the University of Toronto.

Roman Genov (S'96–M'02–SM'11) received the B.S. degree in electrical engineering from the Rochester Institute of Technology, NY, USA, in 1996, and the M.S.E. and Ph.D. degrees in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, USA, in 1998 and 2003, respectively.

He held engineering positions at Atmel Corporation, Columbia, MD, USA, in 1995, and Xerox Corporation, Rochester, NY, USA, in 1996. He was a Visiting Researcher in the Laboratory of Intelligent Systems at Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1998, and in the Center for Biological and Computational Learning at Massachusetts Institute of Technology, Cambridge, MA, USA, in 1999. Currently, he is an Associate Professor in the Department of Electrical and Computer Engineering at the University of Toronto, Toronto, ON, Canada. His research interests are primarily in the area of implantable, wearable, and disposable biomedical electronics. This includes analog and digital VLSI circuits, systems and algorithms for electrical, chemical and photonic sensory information acquisition, and energy-efficient signal processing with various medical applications such as brain-silicon interfaces and DNA microarrays.

Dr. Genov was a corecipient of Best Paper Award of the IEEE Biomedical Circuits and Systems Conference, Best Student Paper Award of IEEE International Symposium on Circuits and Systems, Best Paper Award of IEEE Circuits and Systems Society Sensory Systems Technical Committee, Brian L. Barge Award for Excellence in Microsystems Integration, MEMSCAP Microsystems Design Award, DALSA Corporation Award for Excellence in Microsystems Innovation, and Canadian Institutes of Health Research Next Generation Award. He was a Technical Program Co-chair at the IEEE Biomedical Circuits and Systems Conference. He was an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II: EXPRESS BRIEFS and IEEE SIGNAL PROCESSING LETTERS. Currently, he is an Associate Editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and serves on the Imagers, MEMS, Medical, and Displays Subcommittee of the International Solid-State Circuits Conference.