Circuits and Technologies for Highly Integrated Optical Networking IC's at 10 Gb/s to 40 Gb/s

S.Voinigescu, P.Popescu, P.Banens, M.Copeland, G.Fortier, K.Howlett, M.Herod, D.Marchesan, J.Showell, S.Szilagyi, H.Tran, and J.Weng

Quake Technologies Inc.
Ottawa, Ontario, Canada

Abstract

This paper presents a comparative overview of the performance of Si CMOS, SiGe BiCMOS and III-V HBT and FET technologies for 10-40Gb/s fiber-optic applications. Active and passive device performance requirements, as well as on-chip isolation issues are first addressed. Fundamental building blocks are overviewed and the pros and cons of each technology implementation are discussed. Finally, a sub 2.5W, highly integrated 10Gb/s SiGe BiCMOS implementation of a 10Gb/s to 622Mb/s transceiver is described in detail. The transceiver achieves the highest level of integration, providing EOI (electro-optical-interface) and SerDes (Serializer-Deserializer) functions.

Introduction

Bandwidth demand in local area networks (LAN) and over the Internet is growing quickly due to applications such as full-motion video, multimedia, e-commerce, and advanced digital services. This exponential need for bandwidth is creating huge demand on the short to medium reach applications. At the forefront of addressing this, the IEEE 802.3ae standards committee is developing Ethernet specifications for 10Gb/s premises networking applications. Current generation Ethernet LANs are being deployed with 10/100 Mb/s connections at the desk and 1 Gb/s on the LAN backbones. 10Gb/s physical layer (PHY) IC offerings used in long haul (transport or wide area networks: WAN) applications exist [1] but power, cost, and footprint issues limit the sustainability of the end product for Very-Short-Reach (VSR), Storage Area Networks (SAN), LAN, and MAN (Metropolitan Area Networks) applications.

This paper will start by discussing the markets for 10Gb/s and 40Gb/s applications, then overview the competing semiconductor technologies vying for implementing these functions. Next, basic building blocks such as VCO's, MUX/ DEMUX, 50 Ohm output drivers and their technology requirements will be addressed. Finally, a highly integrated solution for a complete physical layer will be discussed.

10Gb/s and 40Gb/s Markets and System Applications

A. Market Segments

The 10Gb/s applications, as segments, given below are represented with an approximation of their associated reach:

- Ultra Long Haul: >500km
- Long Haul/WAN: >100km
- Metro/MAN: 2km-100km
- Short Reach/LAN: <2km
- VSR/Intershelf/Infiniband/Fibre Channel: <100m

Regardless of the reach and data rate of a typical application, fiber-optics modules have very similar architectures, containing both digital (MUX, DEMUX), as well as analog building blocks (TransImpedance Amplifier TIA, Post Amplifier, Driver, Clock and Data Recovery and transmit Phase-Lock-Loop), as illustrated in Fig.1.

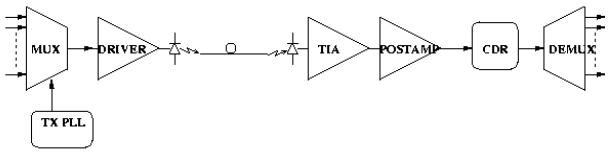

Fig.1: Typical PHY block diagram for 10 Gb/s and 40Gb/s fiber systems.

In 2000, 1 Gb/s ports are shipping at a rate of 4.4 million per year (source: DellOro Group). The next generation networks will have 1 Gb/s to the desktop and 10 Gb/s backbones. While the IEEE addresses the specific needs of Ethernet markets, an industry consortium, the Optical Internetworking Forum (OIF), is agreeing on a common interface at the physical layer addressing interoperability between data and optical networks. MANs can reach up to 100 km and have overlapping component needs with the Ethernet market. Following the emergence of the 10Gb/s Ethernet market, the Infiniband and Fibre Channel markets are expected to develop with a lag of 12-18 months. Infiniband is a replacement for the PCI bus and initial specifications with channel speeds of 1 Gb/s and 2.5 Gb/s are now being defined; the next generation will run at 10 Gb/s. Similarly, Fibre Channel links at 1 and 2 Gb/s are now being deployed in SANs and a 10 Gb/s specification is currently being developed.

10Gb/s and 40Gb/s SONET/SDH is a segment within the traditional telecom market with predominantly WAN applications. WANs require high performance EOI functions. SerDes functions do not differ from a MAN application.

10Gb/s Parallel Fiber applications are typically custom approaches used to route optical signals efficiently between in-building equipment. Parallelism occurs in bundles of 4, scaling to 12, and requires VSR EOI and SerDes functions.

B. Market Trends

Mirroring what is in the process of happening at 2.5Gb/s, the 10Gb/s requirements will follow the 2.5Gb/s trend of ever higher levels of integration (assuming the associated power, price, and footprint reductions). In the last months product announcements in the 2.5Gb/s space, namely fully integrated SerDes transceivers and arrayed 2.5Gb/s EOI and SerDes have been made. All products are highly integrated components that reduce the number of chips required in a 2.5Gb/s system from 4 or 5 to 2 or 3. In the GBIC market, a similar trend occurred over the last years. With these precedents, it is clear that high levels of IC integration in the 10Gb/s and eventually 40Gb/s markets are logical steps in optimizing such systems in terms of speed, power and cost performance. Indeed highly integrated SiGe transceivers in the 10Gb/s range have been reported in research publications during the last two years [2-5].

Semiconductor Technologies

A. Technology Requirements

The first generation OC192 (10Gb/s) systems of the mid 90's [1] have relied exclusively on GaAs HBT, GaAs MESFET and GaAs p-HEMT technologies to deliver the performance required in modules with low level of integration dominated by a mix-and-match of discrete components and IC's. It is also noteworthy that the raw transistor speed of these technologies, with typical f_T and f_{MAX} values of 60-70GHz, far exceeded the capabilities of Si-based state-of-the art devices at the time. This situation is now being tipped in favor of SiGe npn and CMOS transistors as their cutoff and oscillation frequencies exceed 40GHz.

Below is a list of critical active and passive device requirements for successful implementation of highly integrated PHY IC's.

- Transistor speed: f_T>4x bit rate, f_{MAX}>5x bit rate i.e. 40GHz/50GHz for 10Gb/s systems, and 160GHz/200 GHz for 40Gb/s, respectively. These f_T and f_{MAX} values must be reached at $V_{CE}=V_{CC}/3$ or $V_{DS}=V_{DD}/2$ over all process corners and entire temperature range.
- large Q, high resonant frequency (f_{RES}) inductor, MIM capacitor and varactor diode with $C_{MAX}/C_{MIN} > 2$.
- back-end with large number of metal layers which helps integration levels.
- low-k, moderate thickness dielectrics for good isolation and low-parasitic capacitance.

B. Transistor Performance

The most relevant transistor performance for fiber-optic IC's is adequately captured by the following figures of merit:

- peak f_T and f_{MAX} values (determine circuit speed);
- peak f_T current density J_{cpfT} (determines power dissipation);
- $I_{cpfT}/C_{BC}(C_{GD})$ i.e. the ratio of the peak f_T current and output capacitance (intrinsic slew-rate);
- BV_{CEO}/BV_{DG} (dictates output swing and is at least two times larger for GaAs and InP devices than for Si-based devices operating at the same speed);
- turn-on/threshold voltage: V_{BE}/V_T (limits the minimum value of the power supply voltage and favors CMOS over bipolar devices, and InP and SiGe HBT's over GaAs HBT's);
- minimum feature size (affects power dissipation, and integration levels and favors Si CMOS and SiGe BiCMOS due to the more mature processing techniques)
- thermal resistance (is related to the semiconductor material and to the minimum feature size and affects indirectly the integration levels and the transistor speed that can be achieved under reliable operating conditions).

Transistor f_T and f_{MAX} characteristics are shown in Fig.2 as a function of collector/drain current for a state-of-the-art, second generation 0.25µm SiGe BiCMOS process. SiGe HBT f_T and f_{MAX} values in the 70GHz to 90GHz range or even higher have been announced by several foundries [6-8] over the last two years. These figures match some of the best GaAs HBT transistor performance, albeit with lower breakdown voltages (2.5-2.8V vs. 10V) and higher peak f_T current densities (2mA/µm^2 vs. 0.8mA/µm^2).

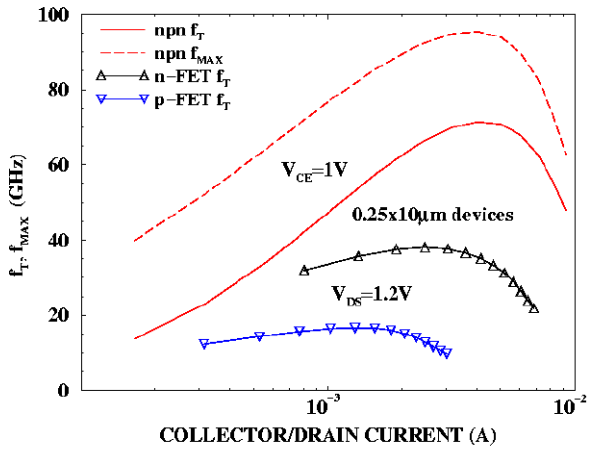

Fig.2: 0.25x10µm^2 npn, f_T and f_{MAX} characteristics as a function of the collector current. 0.25x10µm^2 n- and p-channel MOSFET f_T vs. I_{DS} characteristics are also shown.

For the same generation of lithography, n-channel MOSFET's display half the speed of the SiGe HBT with p-channel device performance yet another factor of 2 behind. An interesting feature of Si/SiGe n-MOS and npn transistors is that their

peak f_T currents are comparable and scale up with every new technology generation [9-10].

For 40Gb/s applications, devices with over 160GHz f_T and f_{MAX} values are required and such performance has so far been reached only by InP HBT's [11] and HEMT's [12]. Fig. 3 compares the f_T and f_{MAX} collector current dependence for state-of-the-art SiGe and InP (D)HBT's. The InP devices enjoy a factor of 2 speed advantage in f_T (160GHz vs. 70GHz), f_{MAX} (200GHz vs. 100GHz), peak f_T current densities (1.2mA/μm^2 vs. 2mA/μm^2) and BVCEO (6V vs. 2.8V).

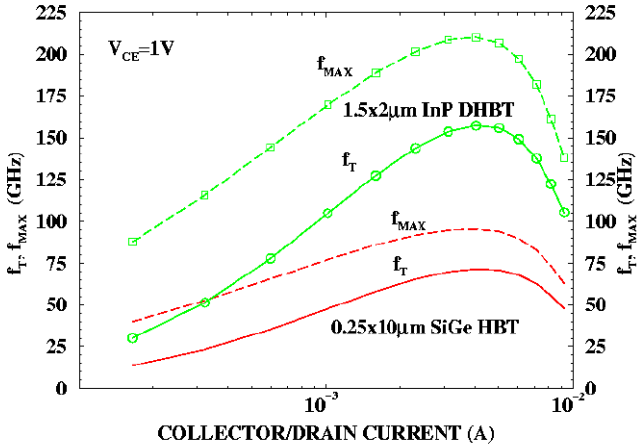

Fig.3: 0.25x10μm^2 SiGe HBT vs. 1.5x2μm InP DHBT [11], f_T and f_{MAX} characteristics as a function of the collector current.

The V_{CE} and V_{DS} dependence of f_T and f_{MAX} is shown in Fig. 4 for SiGe HBT's and Si MOSFET's. While f_T is a fairly weak function of the collector/drain voltage, f_{MAX} has a strong dependence on V_{CE}/V_{DS}, [9] thus making it difficult to achieve high circuit speed in conjunction with a reduced supply voltage. The f_{MAX} of MOSFET devices is very layout and process dependent (due to gate resistance) [9-10] and it only scales as $l_G^{-1/2}$ (where l_G is the gate length), unlike f_T, which scales as $1/l_G$. InP/GaAs HBT's and FET's have similar dependence of f_{MAX} on V_{CE}/V_{DS} as Si/SiGe devices but more severe self-heating typically reduces both f_T and f_{MAX} at large V_{CE}/V_{DS}, thus canceling out the speed advantage that larger supply voltages may bring.

Fig. 5 summarizes the f_T scaling of Si CMOS and Si and SiGe bipolar devices with process feature size. SiGe HBT's have been aggressively scaled in the last two generations in order to retain their x2 and x4 speed advantage over n-channel MOSFET's. In general, for the same f_T, the n-MOS feature size is two generation ahead of the bipolar one. However, as a rule of thumb, for CMOS to truly exhibit its low power advantage over bipolar devices, the f_T of the p-channel device must be sufficiently high to meet the application requirements, i.e. 40GHz for 10Gb/s. Otherwise, power-hungry CML-like implementations using n-MOSFET's and resistive loads must be employed in order to achieve 10Gb/s rates. Such 10Gb/s results have been obtained in production 0.18μm CMOS technologies [13] but they typically consume more current than corresponding SiGe BiCMOS implementations.

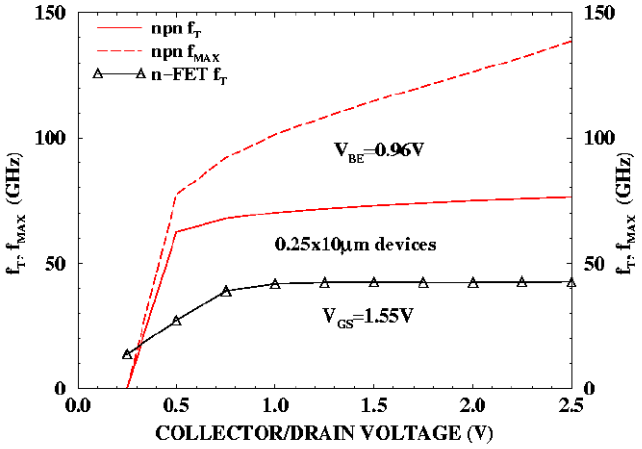

Fig.4: 0.25x10μm^2 npn f_T and f_{MAX} characteristics as a function of the collector-emitter voltage, V_{CE}. For comparison, the V_{DS} dependence of an 10x 0.25μmx10μm n-channel MOSFET is also shown.

f_T values of up to 160GHz have been recently reported for SiGe HBT's. Such performance has only been reached at very high current densities, exceeding 6mA/μm^2, and with breakdown voltages of 1.5-1.8V [8]. These high cutoff frequency figures have so far failed to be concomitantly accompanied by similar f_{MAX} values.

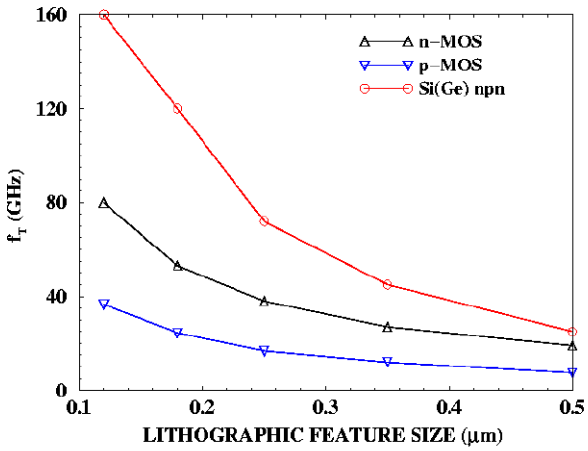

Fig.5: Scaling of Si CMOS and Si(Ge) npn devices as a function of feature size. The 0.12μm npn results are based on experimental data presented at the 2000 GaAs IC symposium with 0.15μm emitter widths [8].

The intrinsic slew rate is an important figure of merit for bipolar digital circuits and output drivers. Typical values are 1V/ps in state-of-the-art InP DHBT processes [11], 0.5V/ps for the SiGe HBT's, and 0.7V/ps for the 0.25μmx10μm n-

MOSFETs of Figs. 2 and 3. In the case of MOSFET's, the slew rate is very high but the device performance is offset by the low output resistance.

Table 1 summarizes the transistor performance for the main semiconductor technologies. Because of the large turn on voltage (1.4V), GaAs HBT's [14] can only be used with supply voltages of 5V or higher.

Table 1: Performance of State-of-the-Art Semiconductor Technologies

Device Param	InP DHBT	GaAs HBT	SiGe HBT	n-MOS	p-MOS
size	1μm	2μm	0.25μm	0.12μm	0.12μm
f_T	160 GHz	70 GHz	70 GHz	80 GHz	38 GHz
f_{MAX}	200 GHz	70 GHz	90 GHz	80 GHz	40 GHz
J_{cpfT}	1.2 mA/μm^2	0.8 mA/μm^2	2 mA/μm^2	2.6 mA/μm^2	1.3 mA/μm^2
I_{cpfT}	1 ps/V	0.5 ps/V	0.5 ps/V	1.4 ps/V	0.7 ps/V
BV_{CEO}	6 V	>10 V	2.8V	>1.2V	>1.2V
V_{BE}/V_T	0.8 V	1.4 V	0.9 V	0.35 V	-0.35 V

C. Passive Devices: MIM capacitors, inductors, varactors

Recent results indicate that inductors with Q's larger than 10 and resonant frequencies beyond 50GHz can be realized on Silicon substrates [15]. Measured characteristics of a 425pH octagonal inductor are shown in Fig.6 as a function of frequency. The peak Q is above 12 in the 20GHz to 50GHz range, about 40% lower than that of III-V inductors of comparable size and operating in the same frequency range.

Si varactor diode Q(f) characteristics, obtained from S parameter measurements, are shown in Fig.7 for voltages between 0 and 5V. The Q remains higher than 4 up to 50GHz even at a varactor voltage of 0V while the capacitance ratio is higher than 2.5. In general, such a high varactor capacitance ratio is difficult to achieve in III-V technologies where varactor diodes are rarely integrated in a fast HBT process due to conflicting epitaxial layer requirements.

D. Layout and isolation issues.

Silicon-based technologies have been traditionally assumed to lack the low-loss and good isolation properties of III-V technologies. Despite the fact that circuit techniques such as top-metal over first-metal ground planes and top-metal over salicided polysilicon ground planes have been recently developed to overcome the disadvantages of the lossy silicon substrate [14], the loss and parasitic capacitance of interconnect over Si substrates continue to be (somewhat) higher than those over semi-insulating III-V substrates. However, it not readily appreciated that coupling between interconnect lines is significantly higher in III-V than in advanced Si technologies. Fig. 8 illustrates the cross-coupling between two adjacent metal interconnect lines on Si and InP substrates. The Si transmission line is between top metal layer and the first metal layer, the latter used as ground plane. In the InP case, the line is placed on top of the semi-insulating substrate while the ground is on the back of the 100 μm thick wafer.

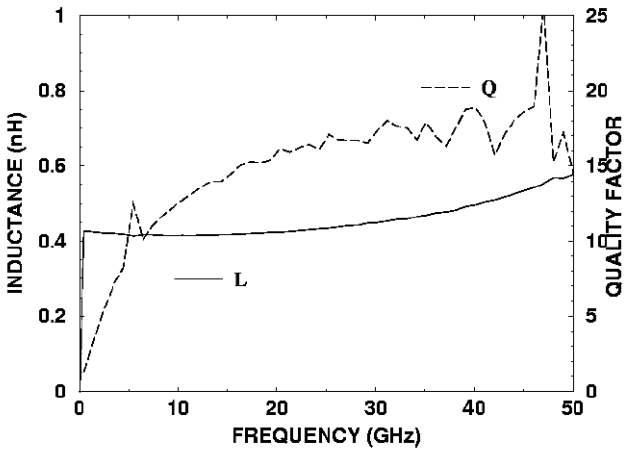

Fig.6: Measured inductance and quality factor of a 0.425nH octagonal inductor in a SiGe HBT process [15]

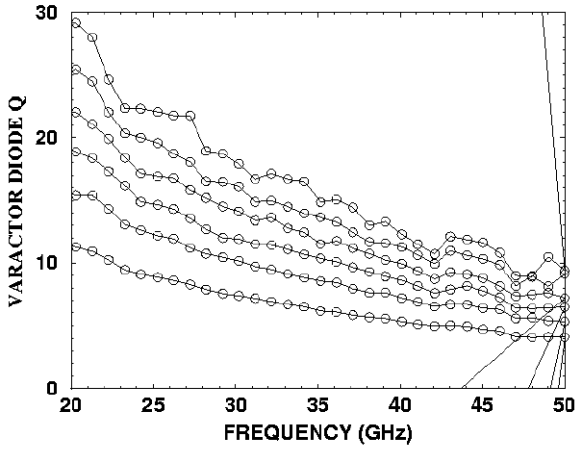

Fig.7: Measured quality factor of a 2x1.6μmx20μm multi-stripe varactor diode in a SiGe HBT process as a function of frequency and varactor voltage between 0V and 5V.

The thicker InP substrate and its higher dielectric constant in comparison with the silicon-dioxide thickness and permitivity seriously impede high interconnect densities and integration levels. Ironically, this problem can only be fixed in III-V technologies by resorting to silicon-like interconnect with many metal layers and low-k dielectrics where the transmission lines have ground planes above the III-V substrate [11-12].

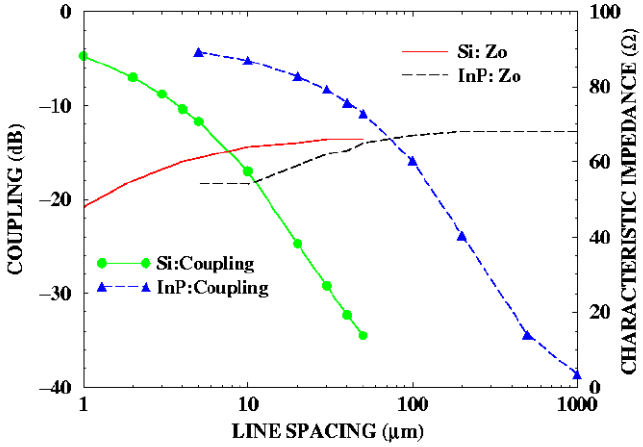

Fig.8: Coupling and characteristic impedance of two adjacent, infinitely long, microstrip lines on Si and InP substrates as a function of the spacing between lines.

On silicon substrates, tie-downs can be used in conjunction with trenched n-wells and ample first metal ground planes to reduce cross coupling through the substrate. Each circuit block is surrounded by a sufficiently wide guard-ring made of the above combination to achieve 50-60dB isolation even above 10GHz [2-4, 14]. In order to reduce the noise generated by the substrate resistance under the signal pads, and in order to isolate them from the substrate, a salicided n-well is placed under the signal pad. The n-well is grounded outside the pad, thus forming a reverse-biased junction with the substrate. The pad behaves like an ideal high Q (>20 at 26GHz) capacitor. This solution provides as high a Q as a pad with first metal ground plane under it, but with much lower capacitance. A typical 60x60μm^2 pad has 28fF capacitance, comparable to that of a similar size pad on 75μm thick GaAs or InP substrates, and is usable beyond 40GHz [3, 14-15].

Building Blocks

The building blocks making up a fiberoptic system, Fig. 1, have different requirements in terms of transistor and passive device performance. The requirements for various digital and analog blocks are summarized below:

- Digital blocks: a) high f_T/f_{MAX} (speed); b) low peak f_T current density to reduce power dissipation; c) low Vbe to reduce power supply and power consumption; d) small device size (power dissipation); e) fine metal pitch (integration).
- VCO requirements: a) high Q inductor for low noise, b) high Q varactor with large capacitance ratio to cover process spread; c) high Q, low parasitic capacitance MIM capacitor for low noise and large oscillation frequency and tuning range; d) high f_{MAX} transistor for large power and low-noise; e) low 1/f noise transistor.
- 50 Ohm driver requirements: a) large intrinsic slew-rate for bandwidth and S_{22} matching; b) large breakdown voltage for voltage swing; c) high f_{MAX} to achieve the bandwidth.
- Transimpedance and Post Amplifier: a) high f_{MAX} for bandwidth and b) low noise figure for good sensitivity.

For analog applications f_{MAX} is more important than f_T. For Si technologies f_{MAX} values have so far been stuck at around 100GHz even in the most advanced experiments [6-8]. It is generally accepted that the analog functions place more demanding requirements on the speed of transistor technologies than do digital functions [16]. One exception is the master-slave D-type flip-flop in the decision circuit which is typically clocked at a frequency equal to the data rate i.e. 10GHz for 10Gb/s systems and 40GHz for 40Gb/s systems [11]. At such high speeds, both bipolar and FET digital circuits use CML topologies buffered by emitter/source follower stages. It is also very common to use E^2CL logic in bipolar digital circuits in order to make up for the drop in beta at high frequencies [16]. Such a topology does not favor low supply voltage and power dissipation. The sensitivity of HEMT or CMOS digital circuits is systematically lower than that of the corresponding bipolar implementations due to the poor V_T (as opposed to V_{BE}) match.

It has been possible to implement most of these analog and digital functions, including 5V drivers, in a production GaAs HBT process [1]. In general, PLL and CDR circuits are either implemented using discrete components or integrated in Si or SiGe bipolar processes, even for 40Gb/s systems [2,4-5,17-18]. III-V HEMT's and MESFET's have been the technology of choice for modulator drivers at 10Gb/s and 40Gb/s [17]. 10Gb/s receivers have been demonstrated in SiGe HBT processes [2,4-5]. Separate TIA's and 3V laser/modulator drivers have been fabricated in Si bipolar or SiGe HBT technologies [16]. Digital functions, clocked at 5GHz, have also been realized in 0.18μm CMOS [13] but it is highly probable that 10Gb/s 3V or 5V drivers will not be realizable in present or future generation Si CMOS.

If the circuit specifications and architecture of the present OC-192 systems is to be scaled to OC-768 ones, circuits with rise/fall times below 10ps and jitter values below 0.25ps will be required. Such circuit performance has not yet been achieved even in research reports [6,11,19-20]. It is most probable that the first commercial 40Gb/s systems will have relaxed clocking schemes i.e. at 20GHz rather than at 40GHz [16,18-19].

A family of 20GHz to 40GHz SiGe HBT VCO's with 12-15% tuning bandwidth will be described in the remainder of this section. Such circuits have proven hardest to integrate with acceptable performance at 10Gb/s because of the difficulty of integrating on the same substrate high quality

inductors, varactors and fast transistors. Fig.9 shows the schematics of a 20GHz VCO [15]. It has a differential varactor-tuned LC Colpitts topology in common-base configuration, with two inductors or a single, center-tapped 3-terminal inductor. This topology is scalable over a wide range of frequencies from 1.5GHz to 120 GHz [3, 15, 21-22] and employs resistive emitter degeneration R_E to suppress harmonics and to reduce up(down) converted noise. The VCO can also operate on the second harmonic of the VCO tank, i.e. 40GHz, when the signal is collected at node X. Fig. 10 illustrates the measured impedance as a function of control voltage and frequency for the half-circuit of the VCO tank, consisting of inductor L_B, MIM capacitor C_E and multi-stripe varactor diode D1. In order to characterize the resonator performance, the S parameters were measured between 10GHz and 40GHz with 50MHz steps for each varactor bias. The resonant frequency was obtained from the peak, and the Q (larger than 4) was calculated from the 3dB half-window, respectively, of the magnitude of the measured tank impedance. The resonant frequency of on-chip LC tanks is tunable over a 15% bandwidth and has low sensitivity to temperature variations [3, 15]. The measured phase noise of the 20GHz VCO is 100dBc at 1MHz from the carrier. When operated on the second harmonic of the tank, the VCO frequency was tunable over the 40GHz to 45GHz range.

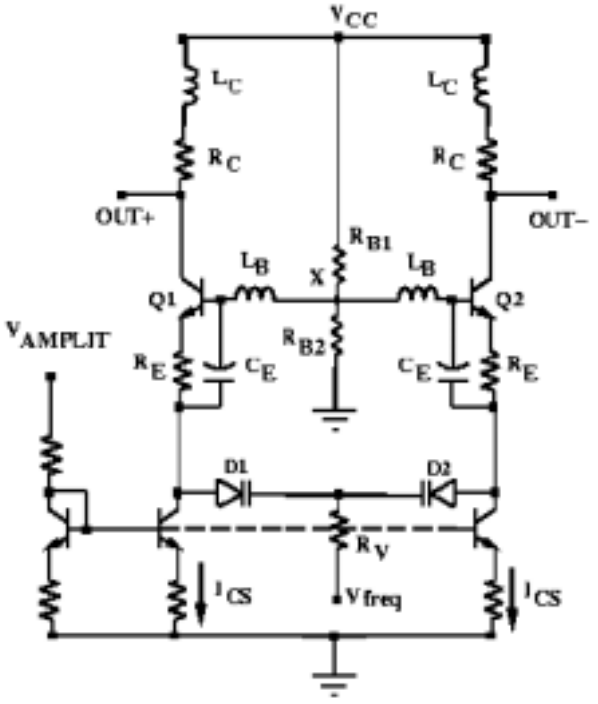

Fig.9: Schematic of a L-C-varactor VCO operating in the 20-30GHz range.

Technology Choices

For 10 Gb/s SERDES functions operating at or below 3.3V supply, 0.12µm CMOS and first/second generation SiGe BiCMOS (f_T=40GHz, f_{MAX}=50GHz) will most likely become the technologies of choice. 10Gb/s short to medium reach applications require the most cost effective yet performant technology available. SiGe BiCMOS is a technology that has been in high volume production, driven by consumer wireless applications, for the last 2 years. It is perfectly suited for the EOI family at 10Gb/s because of the high speed (SiGe) bipolar transistors and CMOS for some control implementation. Technology needs for SerDes are similar to EOI in terms of speed performance. From the point of view of implementing large amounts of digital logic, the CMOS is crucial. SiGe BiCMOS is ideally suited for its speed (bipolar) and digital capability (CMOS). For arrayed SERDES functions, 0.12µm sub-micron CMOS is needed to keep die size and power consumption as low as possible. However, such a CMOS process is higher cost than conventional "digital" CMOS processes as it will have to integrate high quality varactor, MIM capacitor and thick top-metal inductors.

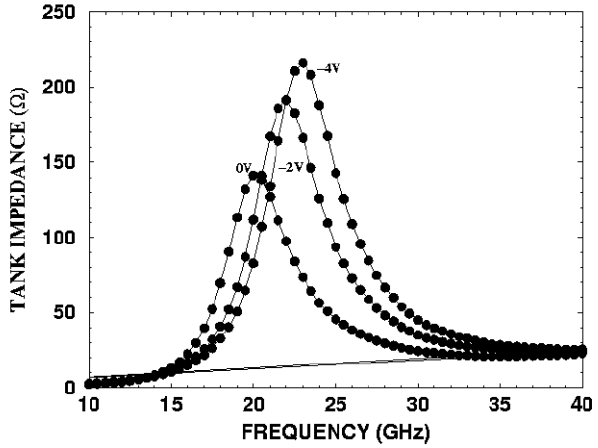

Fig.10: Measured impedance of a 20GHz VCO L-C-varactor tank fabricated in a SiGe HBT process as a function of frequency and varactor voltage [15].

GaAs HBT's and p-HEMT's will retain the 5V modulator driver markets in long-haul 10Gb/s SONET/SDH applications. For requirements at 40Gb/s serial and above, no technology is currently mainstream enough to be cost-effective and manufacturable in high volume. First products will have lower levels of integration and reduced functionality (i.e. 4:1 MUX or 1:4 DEMUX, 40Gb/s to 10Gb/s) and most likely use InP (D)HBT's. Third generation SiGe BiCMOS (f_T, f_{MAX} > 150GHz) will take over the SerDes function as the technology matures. Modulator driver functions will most likely be implemented in GaAs p-HEMT and InP DHBT technologies.

Examples of highly integrated circuits

A. 10Gb/s Transimpedance-Limiting Amplifier

Fig. 11 shows the block diagram of a single-chip transimpedance limiting amplifier (TIALA) for OC-192 SONET/SDH STM-64 and 10 Gigabit Ethernet (IEEE802.3ae, 10GE) applications with data rates up to 10.7Gb/s. The circuit has differential output and features an auto-zero dc feedback to compensate for any offset

throughout the amplifier for the entire range of input currents: 10µA to 1.8mA. The equivalent input noise current is 15pA/rtHz and the total differential transimpedance gain is 30KOhm. LOSS-OF-SIGNAL and PIN photodiode monitoring functions are also included. The total power consumption is 200mW from a single 3.3V supply.

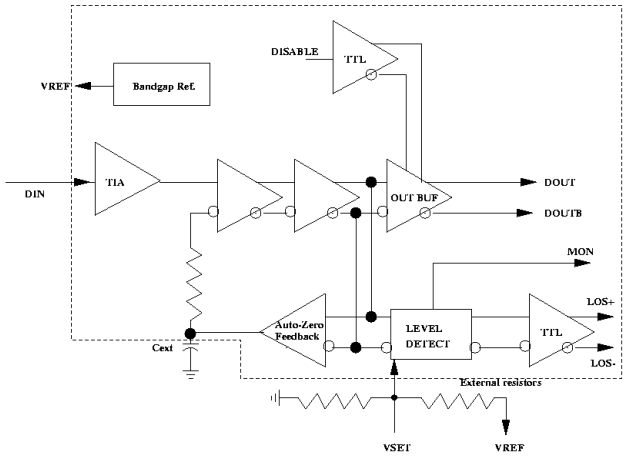

Fig.11: Block diagram of a 10.7Gb/s TIALA featuring linear monitor and LOS functions, as well as a dc-autozero feedback.

B. 10Gb/s to 622 Mb/s SerDes with CDR and Clock Generation Unit (CGU).

Fig. 12 shows the block diagram of a fully integrated, OIF99.102.6 compliant, transmit and receive SerDes for OC-192 SONET/SDH STM-64 and 10 Gigabit Ethernet (IEEE802.3ae, 10GE) applications. It contains a 16:1 multiplexer (MUX), 1:16 demultiplexer (DEMUX) with differential 622Mb/s LVDS I/Os, clock and data recovery (CDR), transmit phase-lock-loop (TX PLL) with programmable bandwidth, and a 100 Ohm differential output driver with programmable wave shape. Other features include a programmable transmit clock and data phase aligner, a synchronization/lock indicator, selectable 155MHz, 311MHz or 622MHz reference clock, low-noise 10GHz VCO's and an internal serial loopback for diagnostic test. The chip operates from a single positive 3.3V supply with a total power consumption of 2.1W. The chip whose layout is shown in Fig.13 has over 10000 HBT's and over 3000 MOSFET's, is fabricated in a 0.35µm SiGe BiCMOS process and is packaged in a 27mmx27mm PBGA package. Fig. 14 presents the measureded 10.3Gb/s eye-diagrams with a 2^{31}-1 bit pattern at a single-ended output demonstrating separate positive and negative peaking control. The bit error rate is better than 10^{-13}.

Conclusions

The main semiconductor technologies which vie for the implementation of highly integrated 10Gb/s and 40Gb/s PHY IC's have been compared based on system and circuit block requirements. SiGe BiCMOS and 0.12µm CMOS with f_T and f_{MAX} values for npn, p- and n-channel MOSFET's in excess of 40GHz will most likely become the prevailing technologies for 10Gb/s PHY IC's. At 40Gb/s I/O speeds InP DHBT's (for digital functions) and GaAs(InP) p-HEMT's (for analog functions) will play a significant role in the near term, with third generation SiGe BiCMOS picking up as higher volumes and technology advances will force higher levels of integration. Two highly integrated SiGe BiCMOS 10Gb/s SerDes and EOI chips, with a combined power dissipation of less than 2.5W from a single 3.3V supply, were presented.

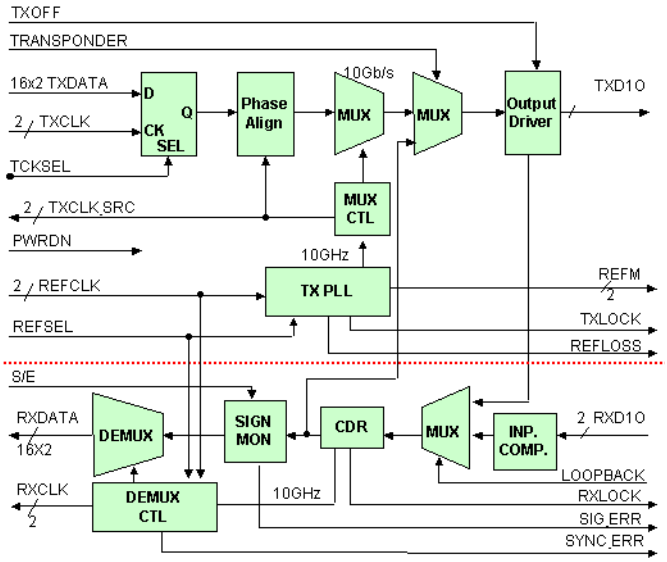

Fig.12: Block diagram of a 10Gb/s SERDES featuring 16:1 MUX/DEMUX, Clock Generation Unit, CDR, output driver with wave shape control.

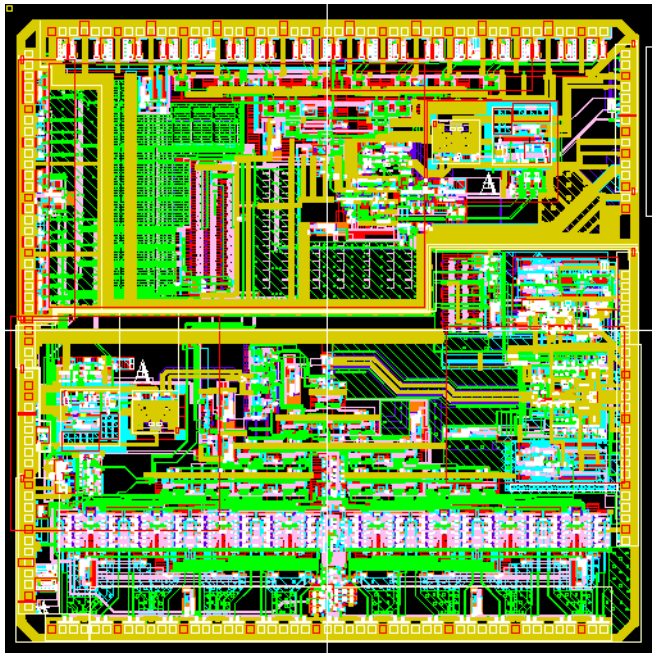

Fig.13: Layout of the 10Gb/s SERDES.

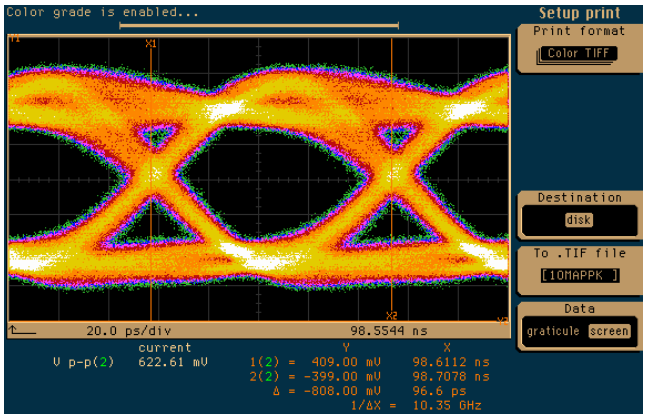

Fig.14: a) Measured 10.3Gb/s eye-diagram at the transmitter output with positive peaking only.

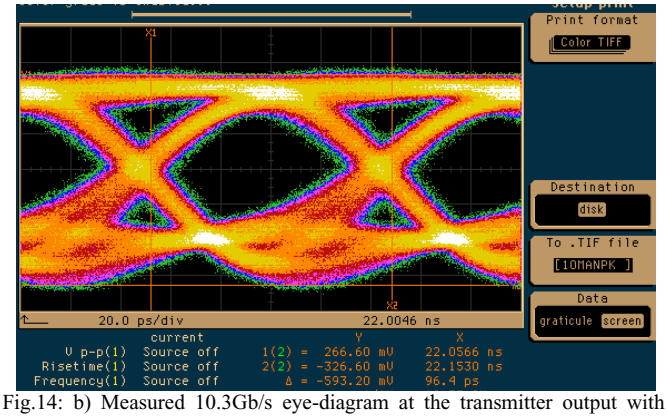

Fig.14: b) Measured 10.3Gb/s eye-diagram at the transmitter output with negative peaking only.

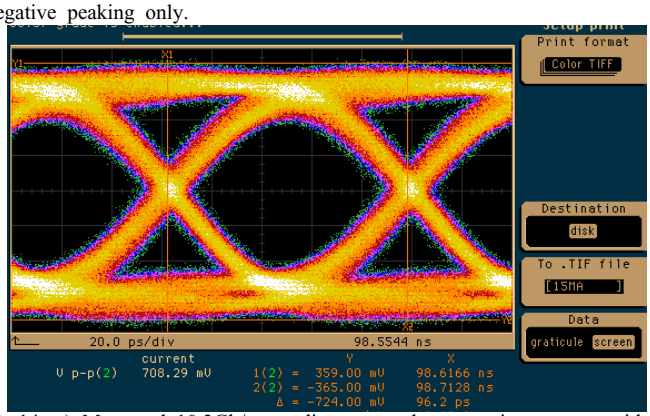

Fig.14: c) Measured 10.3Gb/s eye-diagram at the transmitter output with no peaking.

References

1. B. Beggs, "GaAs HBT 10Gb/s Product," IEEE MTT-S International Microwave Symposium Workshop, June 13-19, 1999, Anaheim, Ca.
2. R.Hadaway, P.Schvan, S.Voinigescu, Y.Greshishchev, D.Marchesan, J.Ojha, P.Dawe, "Application of SiGe HBTs to Datacom and Wireless", MRS, San Francisco, April, 1998.
3. S.P. Voinigescu, M.A. Copeland, D. Marchesan, P. Popescu, and M.C. Maliepaard, "5GHz SiGe HBT Monolithic Radio Transceiver With Tunable Filtering", Digest of Papers, RFIC Symp., pp.131-134 1999.
4. Y. Greshchev, P.Schvan, J. Showell, M-L Xu, J.Ojha, and J.Rogers, "A Fully Integrated SiGe Receiver IC for 10Gb/s Data Rate", ISSCC Digest, pp.52-53, 2000.
5. M.Menghelli, B. Parker, H.Ainspan, and M.Soyuer, "SiGe BiCMOS 3.3V Clock and Data Recovery Circuits for 10Gb/s Serial Transmission Systems", ISSCC Digest, pp.56-57, 2000.
6. T.Masuda, K-I Ohhata, F. Arakawa, N. Shiramizu, E. Ohue, K.Oda, R. Hayami, M. Tanabe, H. Shimamoto, M. Kondo, T. Harada, and K. Washio, "45 Ghz Transimpedance 32 dB Limiting Amplifier and 40Gb/s 1:4 High-Sensitivity Demultiplexer with Decision Circuit using SiGe HBTs for 40Gb/s Optical Receiver", ISSCC Digest, pp.60-61, 2000.
7. R. Tang et al., "A low-Cost Modulator SiGe BiCMOS Technology and Analog Passives for High-Performance RF and Wide-Band Applications", IEEE BCTM, pp.102-105, 2000.
8. S.Subana, G.Freeman, D.Ahlgren, B.Jagannathan, D.Greenberg, J.Johnson, P.Bacon, R.Najarian, D.Herman, and B.Meyerson, "Review of Silicon-Germanium BiCMOS Technology after 4 Years of Production and Future Directions", IEEE GaAs IC Symposium Technical Digest, pp.7-10, 2000.
9. S.P.Voinigescu, S.W.Tarasewicz, T.MacElwee, and J.Ilowski, "An Assessment of the State-of-the-Art 0.5mm CMOS Technology for RF Applications,", IEDM Techn. Digest, pp.721-724, 1995.
10. S.P.Voinigescu, P.B. Rabkin, C.A.T. Salama, and P.A. Blakey, "2D Numerical Investigation of the Impact of Compositional Grading on the Performance of Submicrometer Si-SiGe MOSFET's", IEEE Trans. ED, vol.42, pp.1039-1046, 1995.
11. J.Godin, M.Riet, S.Blayac, Ph.Berdaguer, J.-L.Benchimol, A.Konczykowska, A.Kasbari, Ph.Andre, N.Kauffman, "Improved InGaAs/InP DHBT Technology for 40Gbit/s Optical Communication Circuits", IEEE GaAs IC Symposium Technical Digest, pp.77-80, 2000.
12. T.Otsuji, K.Murata, T.Enoki, and Y.Umeda, "An 80-Gbit/s Multiplexer IC Using InAlAs/InGaAs/InP HEMT's", IEEE JSSC, vol.33, pp.1321-1326, 1999.
13. A.Tanabe, M.Umetani, I.Fujiwara, T.Ogura, K. Kataoka, M.Okihara, H. Sakaruba, T.Endoh, and F. Masuoka, "A 10Gb/s Demultiplexer IC in 0.18mm CMOS using Curent Model Logic with Tolerance to the Threshold Voltage Fluctuations, " ISSCC Digest, pp.62-63, 2000.
14. S.P.Voinigescu, D.Marchesan, J.L.Showell, M.C.Maliepaard, M.Cudnoch, M.G.M.Schumacher, M.Herod, G.E.Babcock, P.Schvan,and R.A.Hadaway, "Process- and Geometry Scalable Bipolar Transistor and Transmission Line Models for Si and SiGe MMICs in the 5- 22GHz Range," Proc.of IEDM, pp.307-310, 1998.
15. S.Voinigescu, D.Marchesan, M.A.Copeland, "A Family of Monolithic Inductor-Varactor SiGe-HBT VCOs for 20GHz to 30GHz LMDS and Fiber-Optic Receiver Applications,", Proc. 2000 RF IC Symp, Boston.
16. H.-M. Rein, "Si and SiGe Bipolar IC's for 10 to 40 Gb/s Optical-Fiber TDM Links", Int.J.of High-Speed Electron. Syst., vol.9, pp.1-37. 1998.
17. M. Wurzer, J. Bock, H. Knapp, W. Zirwas, F. Schumann, and A. Felder, "A 40Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz fT Silicon Bipolar Technology", IEEE JSSC, vol.34, pp.1320-1324, 1999.
18. M. Wurzer, T.F. Meister, H. Schafer, H. Knapp, J. Bock, R. Stengl, R. Aufinger, M. Franosch, M. Rest, H.-M. Rein, and A. Felder, "42 GHz Static Frequency Divider in a Si/SiGe Bipolar Technology", ISSCC Digest, pp.122-123, 1997.
19. Y.Miyamoto, M.Yoneyama, T. Otsuji, K.Yonenaga, and N.Shimizu, "40-Gbit/s TDM Transmission Technologies Based on Ultra-High-Speed IC's", IEEE JSSC, vol.34, pp.1246-1253, 1999.
20. J.P. Mattia, R. Pullela, Y. Baeyens, Y-K Chen, H-S Tsai, G. Georgiou, T.W. Von Mohrenfels, M. Reinhold, C. Groepper, C. Dorschky, and C. Schulien, "A 1:4 Demultiplexer for 40Gb/s Fiber-Optic Applications", ISSCC Digest, pp.64-65, 2000.
21. L.Dauphinee, M.A.Copeland, and P.Schvan, "A Balanced 1.5GHz VoltageControlled Oscillator with an Integrated LC Resonator," IEEE ISSCC Digest, pp.390-391, 1997.
22. Y. Baeyens, R.Pullella, C. Dorschky, J.-P. Mattia, R.Knopf, H.-S. Tsai, G. Georgiou, R. Hamm, Y.C. Wang, Q. Lee, Y.-K. Chen, "Compact Differential InP-Based HBT VCO's with Wide Tuning Range at W-Band", IEEE MTT-Symposium Technical Digest, 2000.