A 60 mW per Lane, 4×23-Gb/s
$2^7 - 1$ PRBS Generator

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Outline

- Motivation
- System overview
- PRBS generator topology
- Latch design
- Measurement results
- Summary
Motivation

• On-chip BIST for 80-Gb/s transceiver

• Minimize power and area without compromising speed
  – At system level by topology choice
  – At transistor level

• Investigate techniques for further power reduction of high-speed digital blocks
System Overview

- SWITCH
- 2^7-1 PRBS Gen.
- SEL
- PRBS Checker + Counter
- 8 to 4 MUX
- 23 Gb/s
- 4 to 1 MUX
- Output Buffer
- 92 Gb/s
- CLK IN
- Clock Buffers
- 11.5 GHz
- PRBS OUT
- 50 Ω Buffer
PRBS Generator Topology

Series $2^7-1$ PRBS Generator

$x^7 + x^6 + 1 = 0$

Only 1 PRBS output but need 8
PRBS Generator Topology

Series Generator
PRBS Generator Topology

Series Generator
PRBS Generator Topology

Series Generator

Inefficient due to phase-shifting and retiming overhead
PRBS Generator Topology

Series Generator

Parallel Generator [1]
PRBS Generator Topology

Series Generator

Parallel Generator [1]

8 DFFs
8 XORs
140 mW
42% power savings

15 DFFs
11 XORs
242 mW
12-GHz Latch Design

- Start from the BiCMOS cascode D-Latch [2]
12-GHz Latch Design

- Remove the output source-followers
12-GHz Latch Design

- Remove the inductors to save area
12-GHz Latch Design

- Share the clock emitter followers for 2 blocks

12-GHz DFF

24-Gb/s 2:1 MUX
12-GHz Latch Design

- Reduce tail current to 1 mA

![Diagram of 12-GHz Latch Design](image)

- \[ I_{\text{tail}} = 1\, \text{mA} \]
- \[ 300 \, \text{mV Swing} \]
- \[ \text{min. size HBT} \]
  \[ 1.5 \times J_{\text{peak-f}_T} = I_{\text{tail}} \]
- \[ L = L_{\text{min}} \]
- \[ W = \frac{I_{\text{tail}}}{0.3 \, \text{mA/\mu m}} \]
Final Generator Schematic

Power Consumption: 235 mW
Die Photo

- 0.13 SiGe BiCMOS
- $f_T = 160$ GHz
- Chip:
  - 1 mm × 0.8 mm
  - 940 mW
- PRBS Generator:
  - 393 μm × 178 μm
  - 235 mW
Measurement Setup

- Spectrum analyzer to verify tone spacing
- Oscilloscope capable of locking to PRBS
Experimental Results - 12 Gb/s

94.5 MHz = \frac{12 \text{ Gb/s}}{127 \text{ bits}}
Experimental Results - 23 Gb/s

180.9 MHz = \frac{23}{127} \text{ bits}
Experimental Results - 24 Gb/s

- Cannot guarantee error-free time-domain PRBS at 24 Gb/s

189.2 MHz = \frac{24 \text{ Gb/s}}{127 \text{ bits}}
Further Power Reduction

- **Same technology**
- **Removed current source**
- **$V_{DD} = 1.8 \text{ V}$, $I_{\text{total}} = 1 \text{ mA}$**
- **Power reduced:**
  \[ 2.5 \text{ mW} \rightarrow 1.8 \text{ mW} \]
- **Same speed: 12 \text{ GHz}**
- **Simulated with extracted layout parasitics**

\[
L = L_{\text{min}} \\
W = \frac{I_{\text{bias}}}{0.15 \text{ mA/\mu m}}
\]
\[
I_{\text{bias}} = 0.5 \text{ mA}
\]

min. size HBT
\[0.75 \times J_{\text{peak-f}_T} = I_{\text{bias}}\]
Scaling to Next Tech. Node

- 90 nm SiGe BiCMOS [3]
- HBT $f_T$: 160 → 230 GHz
- MOS $f_T$: 80 → 120 GHz
- Same power: 1.8 mW
- $f_T$ improvement: $\times \sqrt{2}$
- Inductive peaking: $\times 1.5$
- $\Delta V$ reduced: $\times 1.3$
- Speed increased: 12 GHz → 30 GHz
- Simulated with extracted layout parasitics
Summary

• Presented a parallel architecture, 4-channel $2^7$-1 PRBS generator

• Demonstrated a 2.5-mW 12-GHz latch in 0.13 μm SiGe BiCMOS process

• Investigated ways for power reduction
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Questions?
Back-up Slides
DFF Schematic