Design Methodology and Applications of SiGe BiCMOS Cascode Opamps with up to 37-GHz Unity Gain Bandwidth

S.P. Voinigescu, R. Beerkens, T.O. Dickson, and T. Chalvatzis*

University of Toronto
**STMicroelectronics, Ottawa*

Outline

- Introduction
- Opamp design
- Application to 1.2-GHz bandpass filter
- Conclusions

Motivation

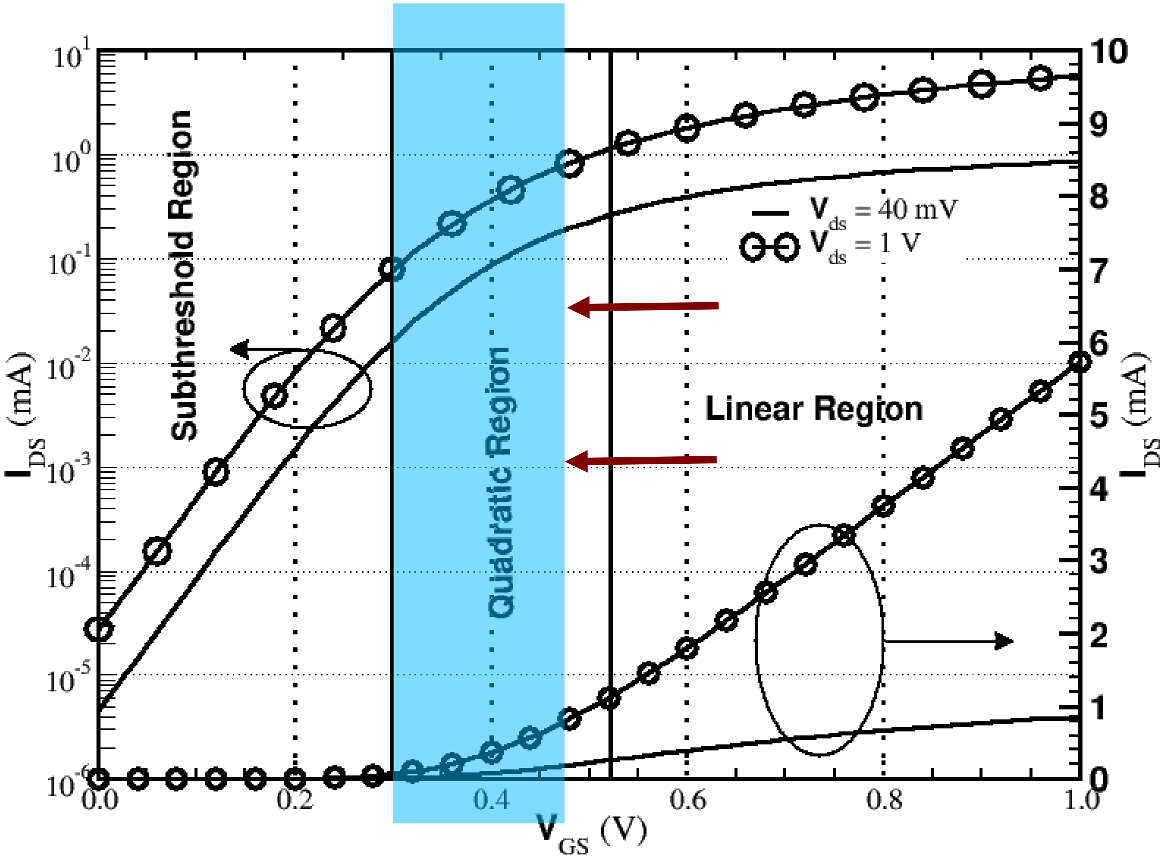
- Opamps are useful in a variety of low-cost RF applications
- Opamp UGB has not kept pace with MOS/HBT f_T/f_{MAX}

Goal

Design methodology for large UGB opamps with good phase margin

Challenges for opamp design in nanoscale (Bi)CMOS

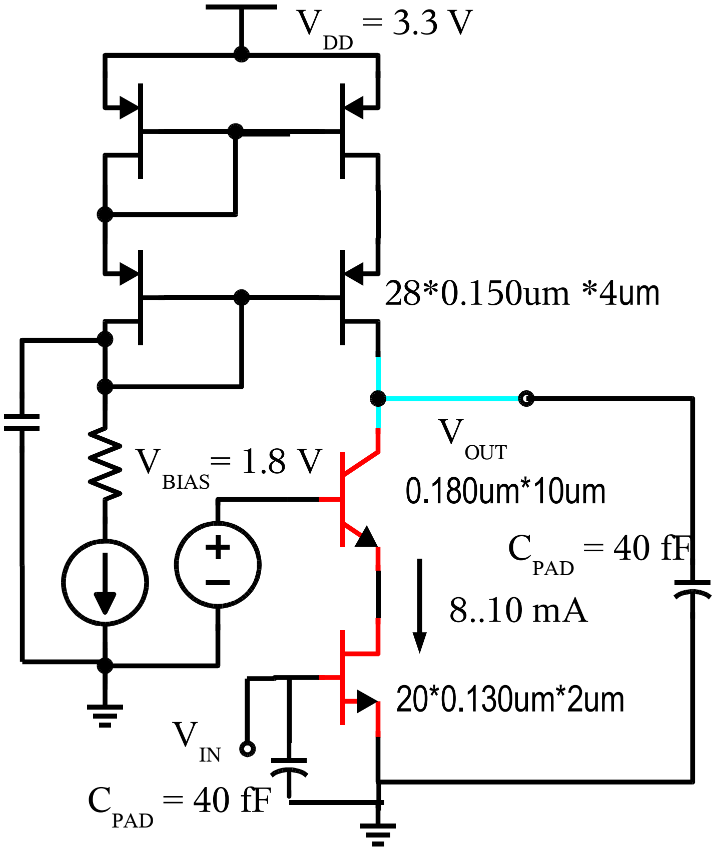
- Square-law in sub 130-nm MOSFETs invalid for most bias range
- Traditional biasing at low V_{eff} makes nanoscale CMOS opamps suffer from
  - sensitive to PVT variation
  - modest bandwidth
  - poor linearity
  - model inaccuracy



How do we maximize opamp bandwidth?

- By selecting a high-bandwidth topology with good stability
- By (unconventionally) biasing and sizing transistors for high UGB

Topology: MOS-HBT cascode with p-MOS cascode load



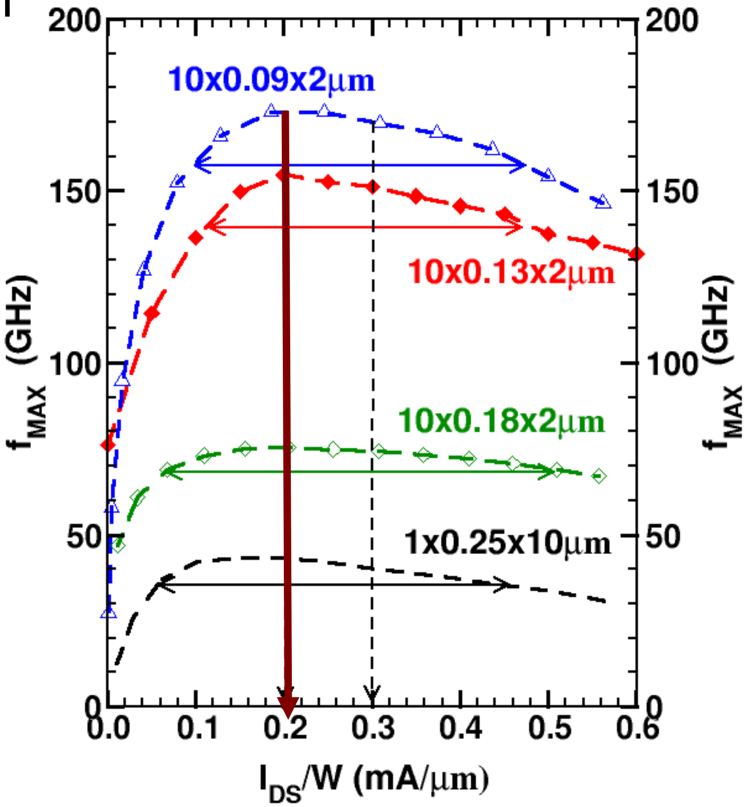
- Miller effect completely eliminated
- Good gain: $A_V = g_{mn} {}^{*} g_{mp} r^2_{op}$
- Unlike HBT-HBT cascode, input time constant $R_G(C_{gs} + C_{gd} + C_{pad})$ is minimized through layout (R_G)
- Dominant pole at output

$$C_{out} = C_{bc} + C_{cs} + C_{db,pMOS} + C_{gd,pMOS} + C_L$$

Single-pole frequency response beyond $UGB = \frac{g_{m,nMOS}}{2\pi C_{out}}$

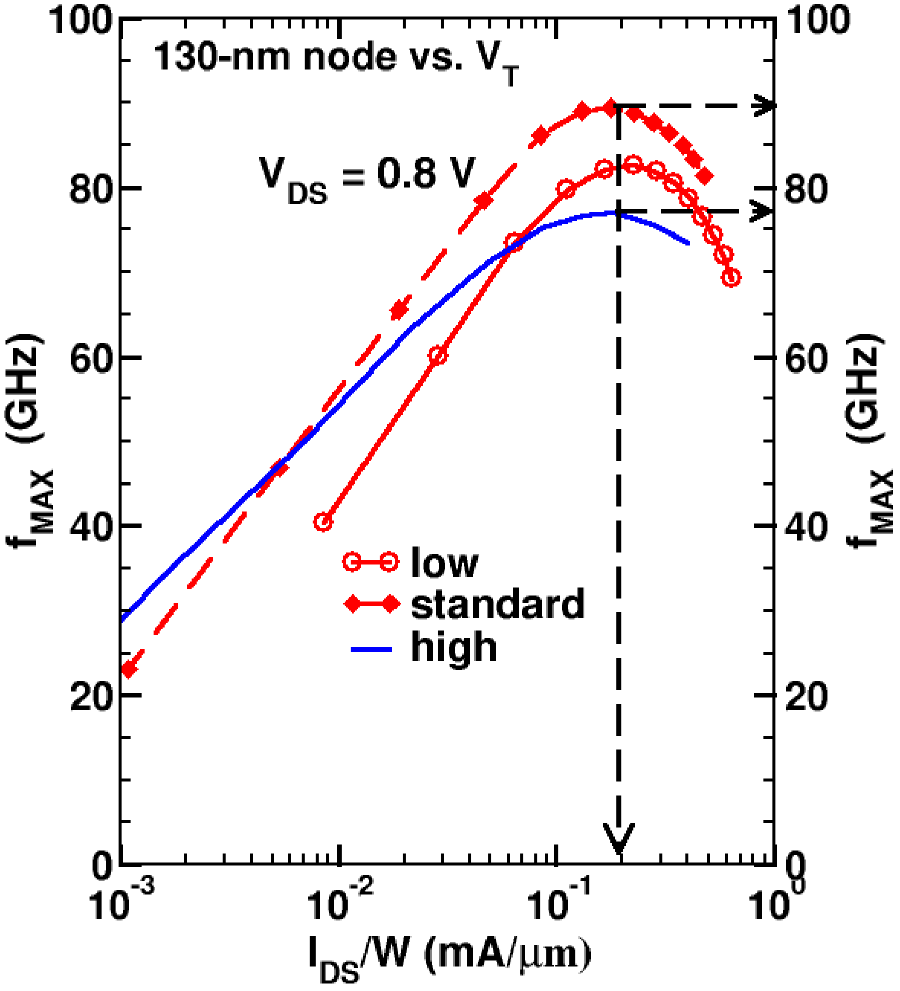
Opamp biasing

- HBT biased at peak f_{MAX} current density (1.2 mA/µm)
- MOSFETs biased at peak f_{MAX} current density (0.2 mA/µm)
  - $\mathrm{f}_{\mathrm{MAX}}$ and gain remain flat for I_{DS} = 0.15 to 0.4 mA/µm
  - 170 GHz @ 0.14 mW/µm of gate finger width



Opamp biasing (ii)

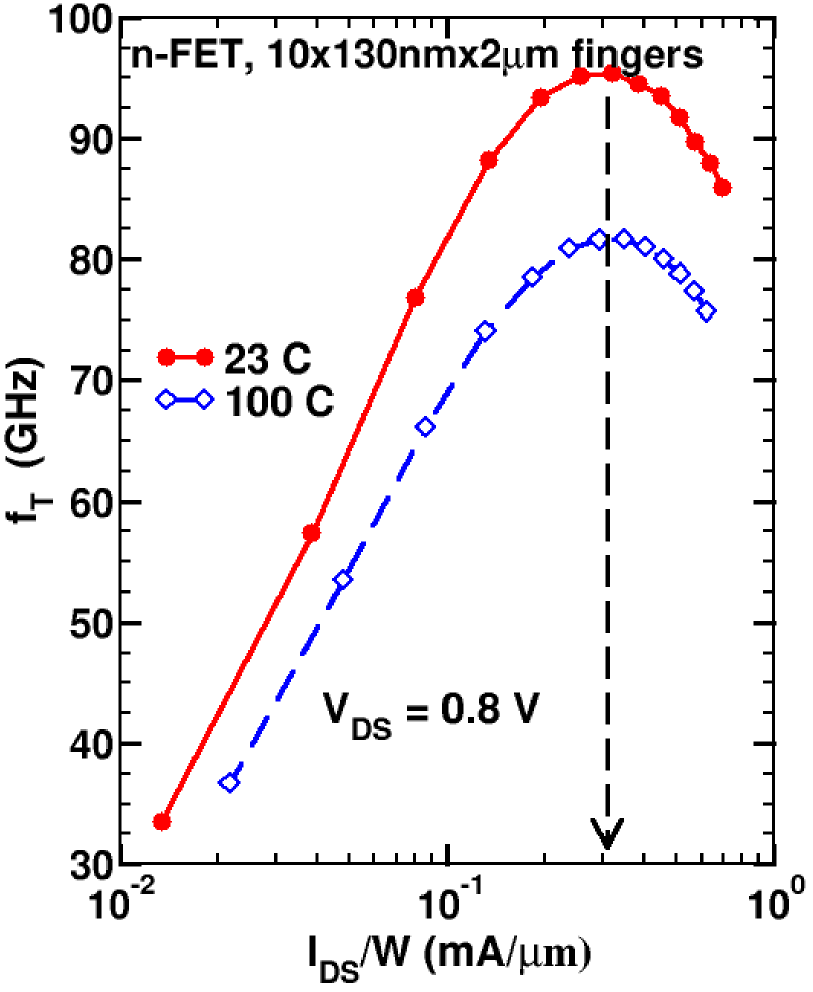
- MOSFETs f_{MAX} current density invariant over devices with
  - low,
  - standard, and
  - high V_T

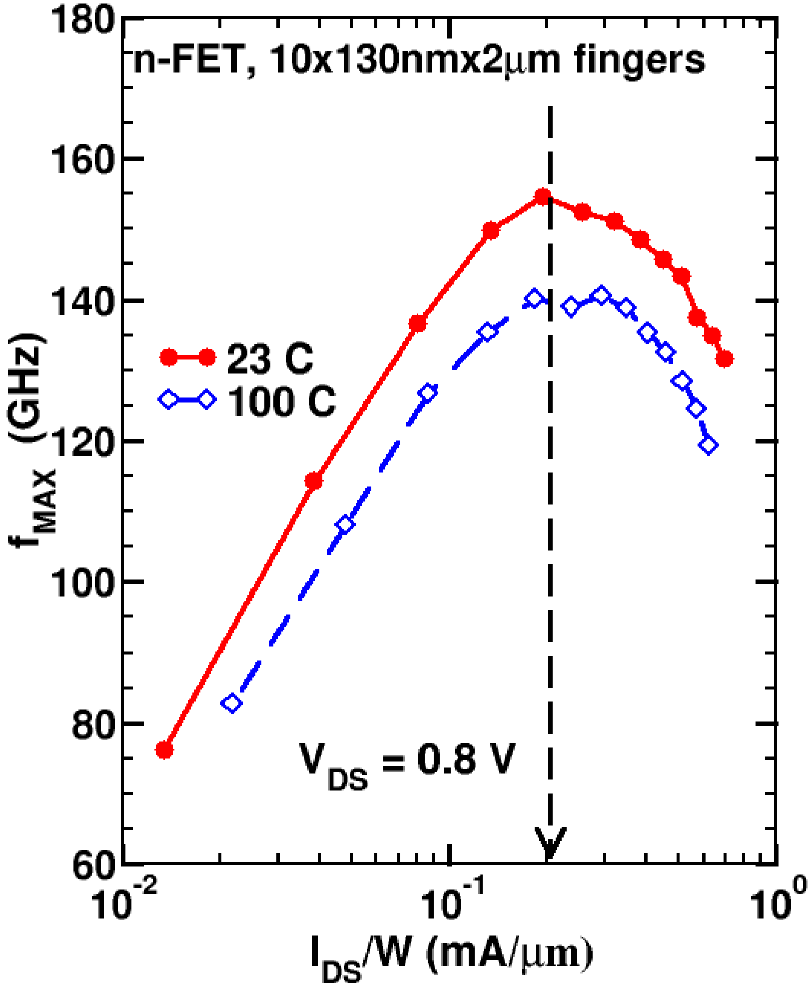


Sorin Voinigescu et al. CSICS-2005, Nov. 2nd, 2005

Opamp biasing (iii)

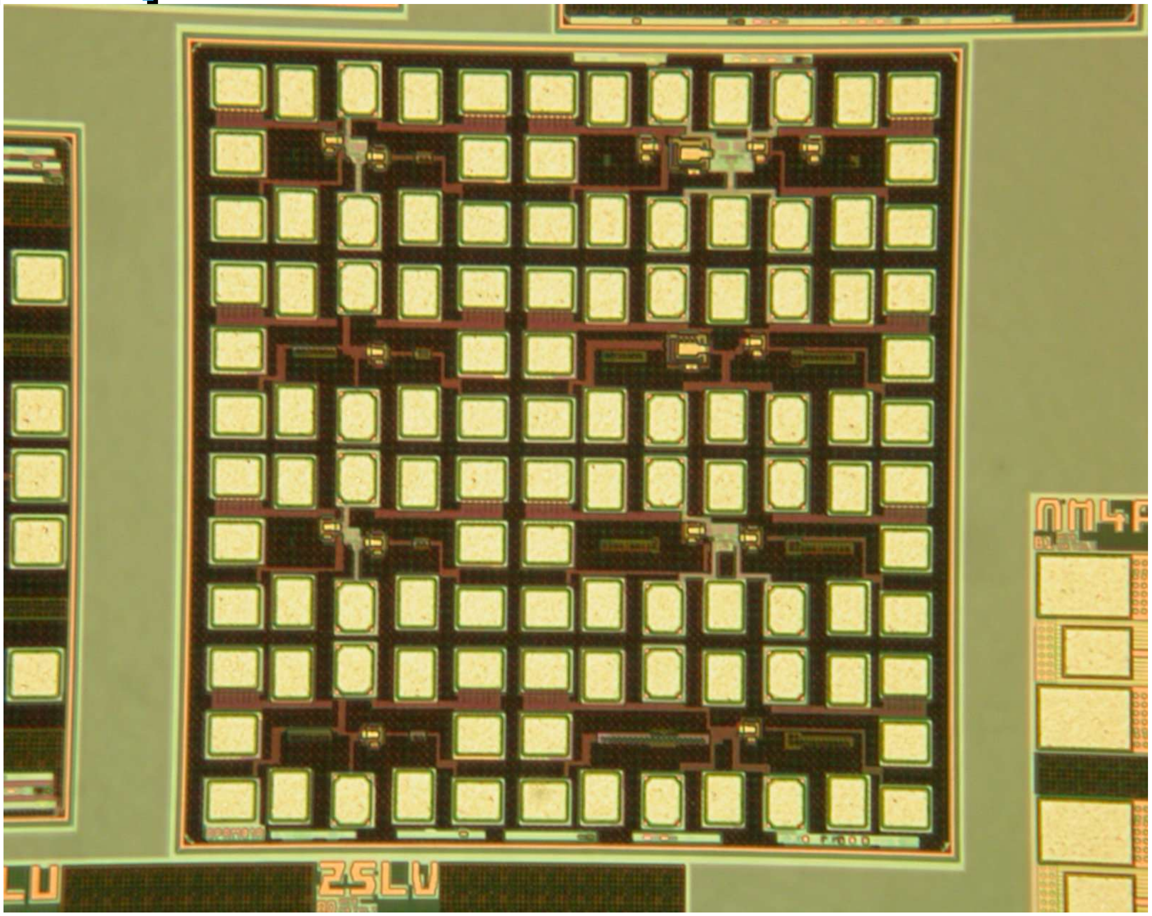
- The peak f_T/f_{MAX} current densities are constant with temperature





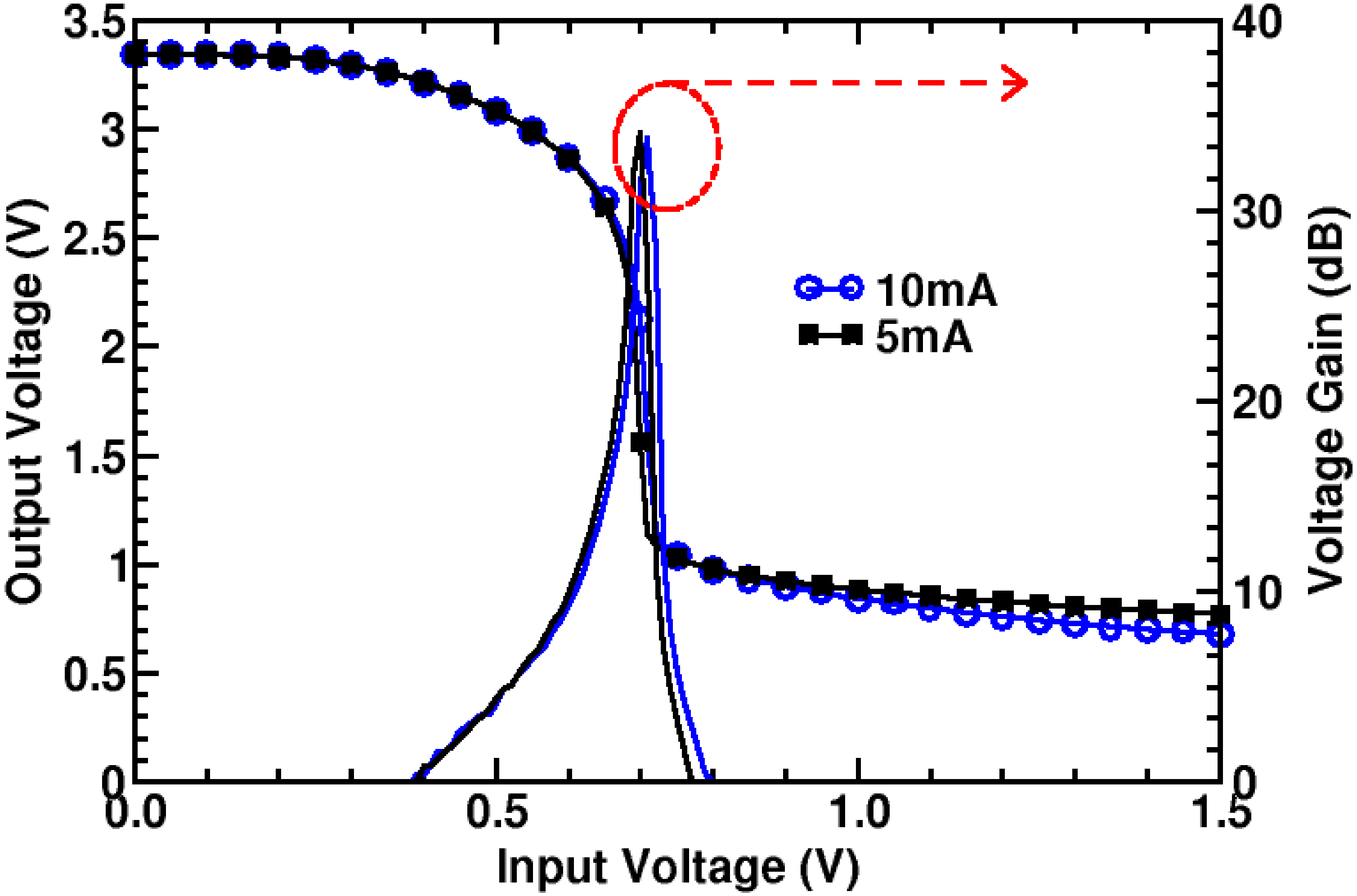
Sorin Voinigescu et al. CSICS-2005, Nov. 2nd, 2005

Opamp test structure measurements



- 130nm SiGe BICMOS with HBT f_T/f_{MAX}= 150/150 GHz
- 4 opamp half circuit test structures
- 4 differential opamp test structures

Opamp half ckt. DC transfer characteristics

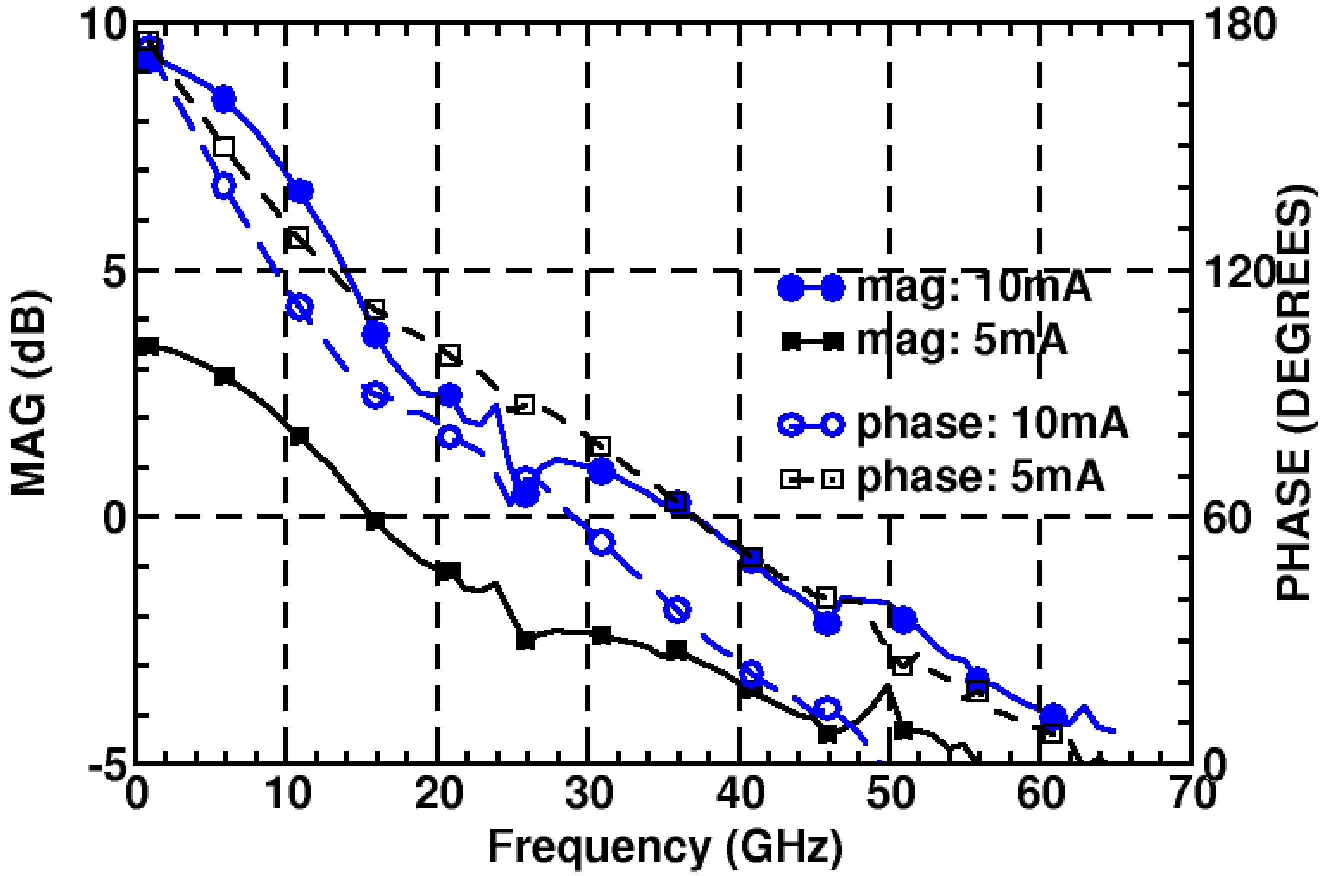


- 5 mA and 10 mA versions
- 36 dB gain at 0.25 mA/µm in both

- V_{OMAX}= 2.8 V
- V_{OMIN} = 1 V

Sorin Voinigescu et al. CSICS-2005, Nov. 2nd, 2005

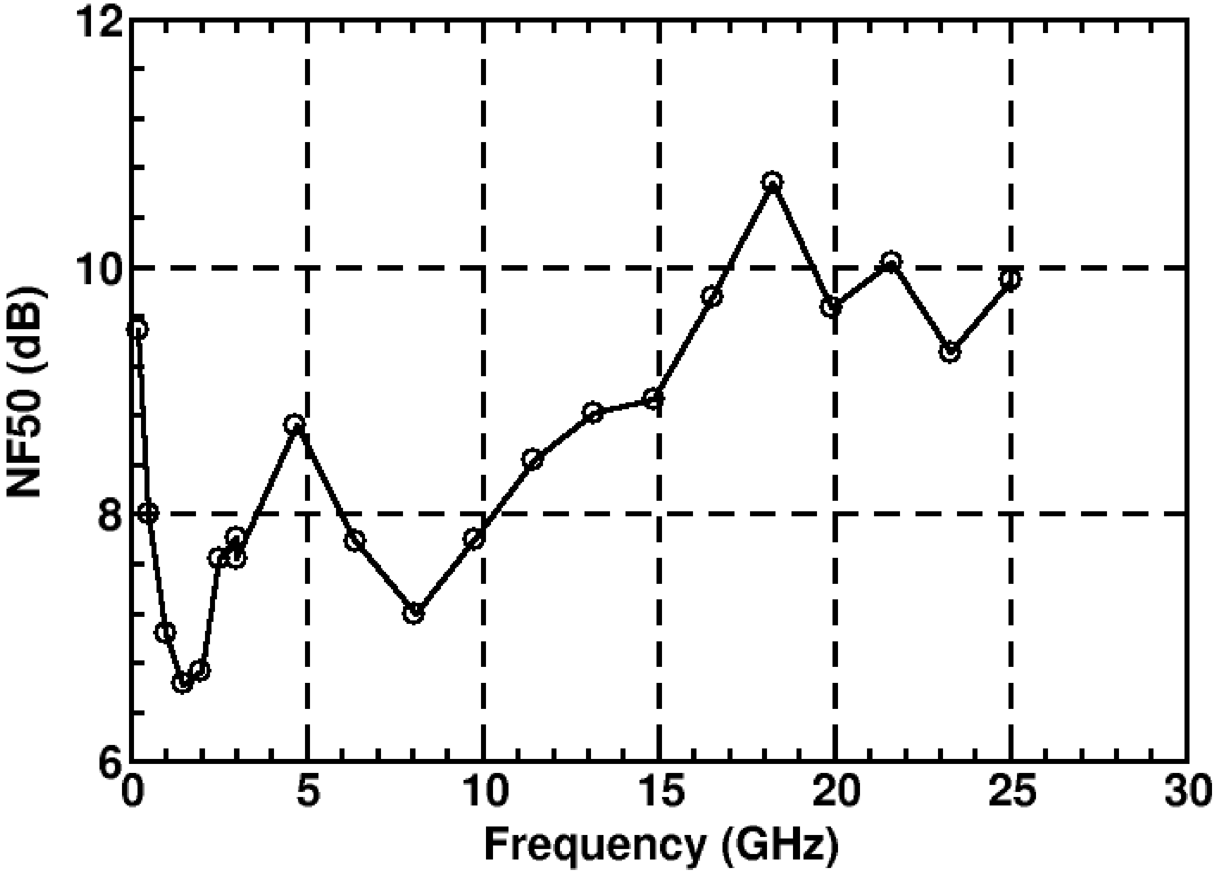
Opamp half-ckt. frequency response with 50 Ohm load



10mA version: UGB= 37(7)-GHz (1pF), PM= 37^{O} w/o comp

5mA version : UGB=15.5(3)-GHz (1pF), PM=110^{O} w/o comp

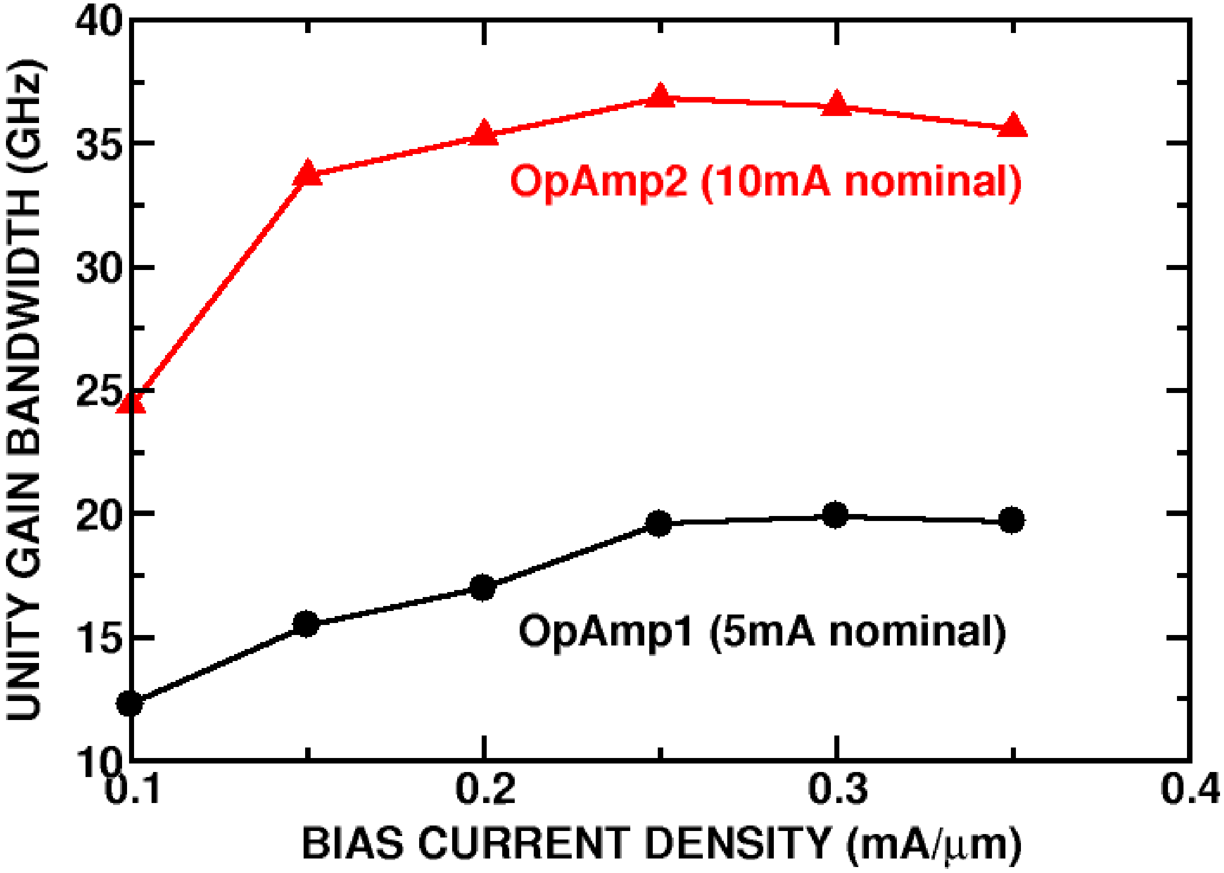
Opamp half-ckt. noise figure in 50 Ohm system



NF50 = 7-8 dB for 10mA version (no reactive matching employed)

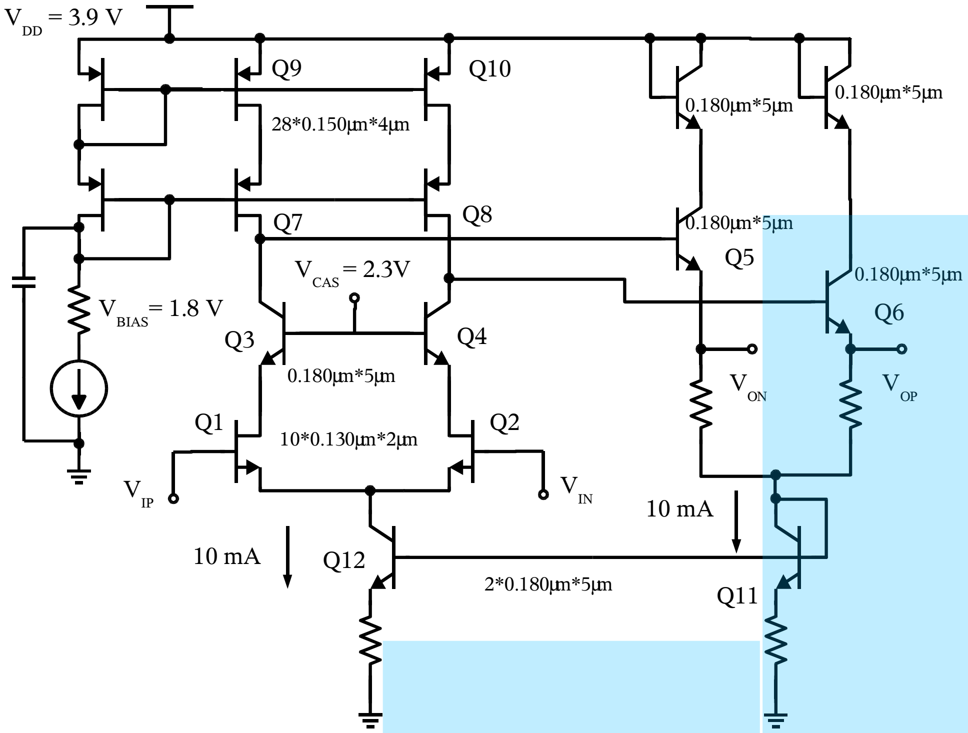
Half ckt. UGB vs. MOSFET current density

- Opamp reaches maximum UGB beyond the peak f_{MAX} current density
- UGB varies by less than 10% for I_{DS}= 0.2 to 0.4 mA/µm

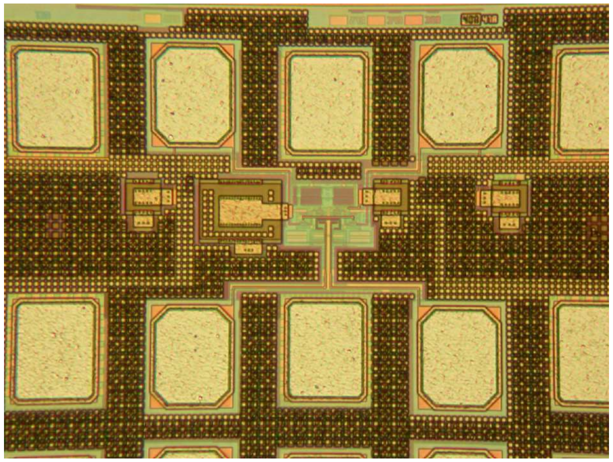


Sorin Voinigescu et al. CSICS-2005, Nov. 2nd, 2005

Fully differential amplifier CM feedback



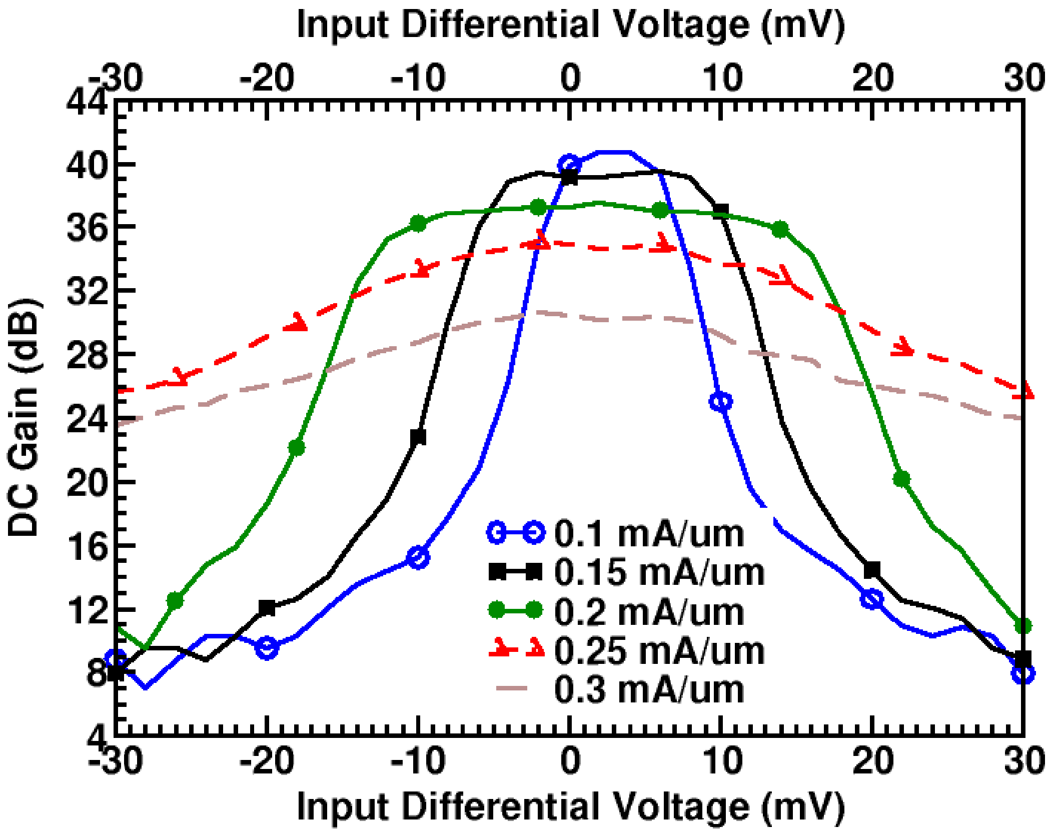
- Emitter followers provide:
  - broadband CM feedback
  - DC level-shifting at output
  - reduced impact of load capacitance on UGB

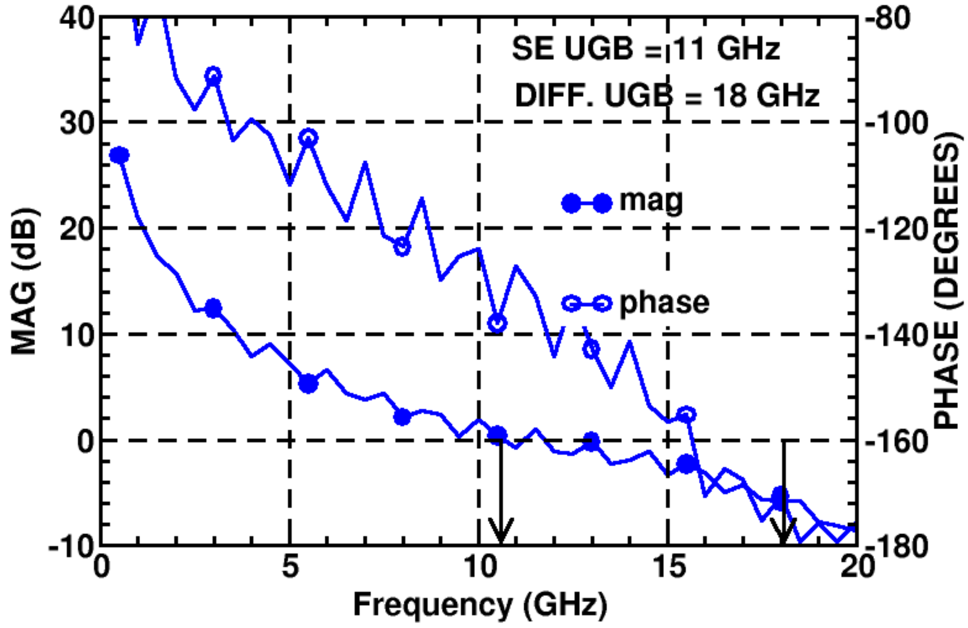


Sorin Voinigescu et al. CSICS-2005, Nov. 2nd, 2005

Measurements

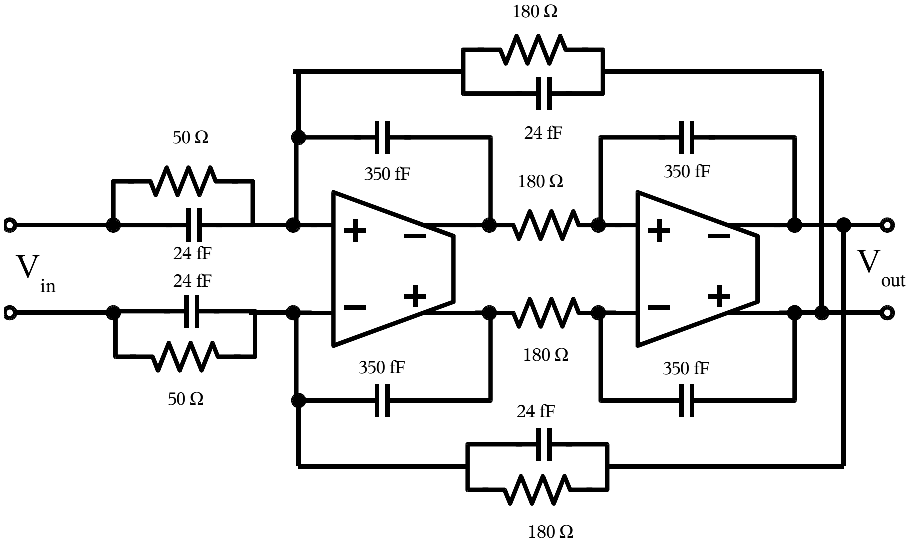
- Differential DC gain versus
  - MOSFET current density
  - Input differential voltage

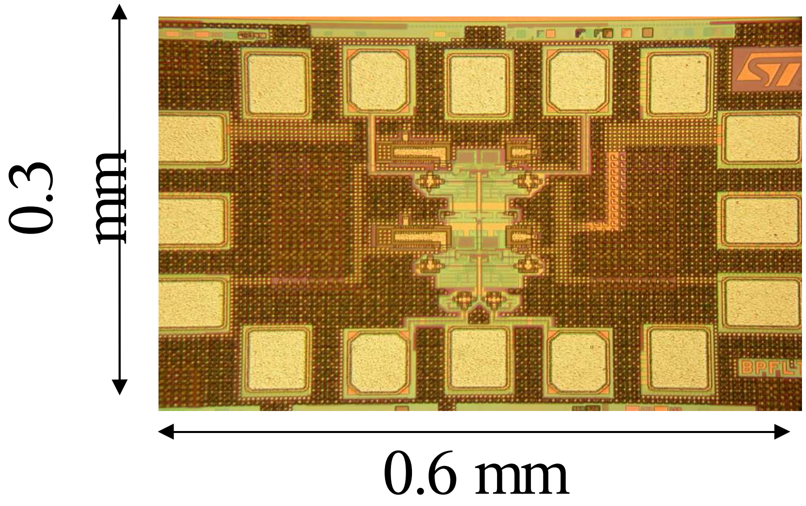


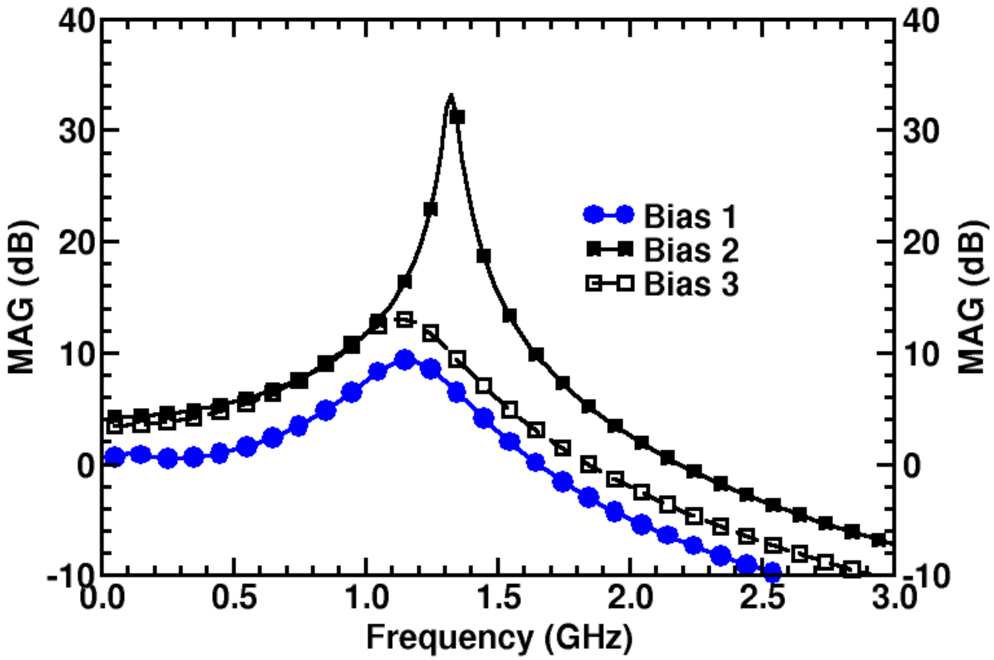


- UGB
  - 11 GHz single-ended
  - 18 GHz differential
- PM > 40^0

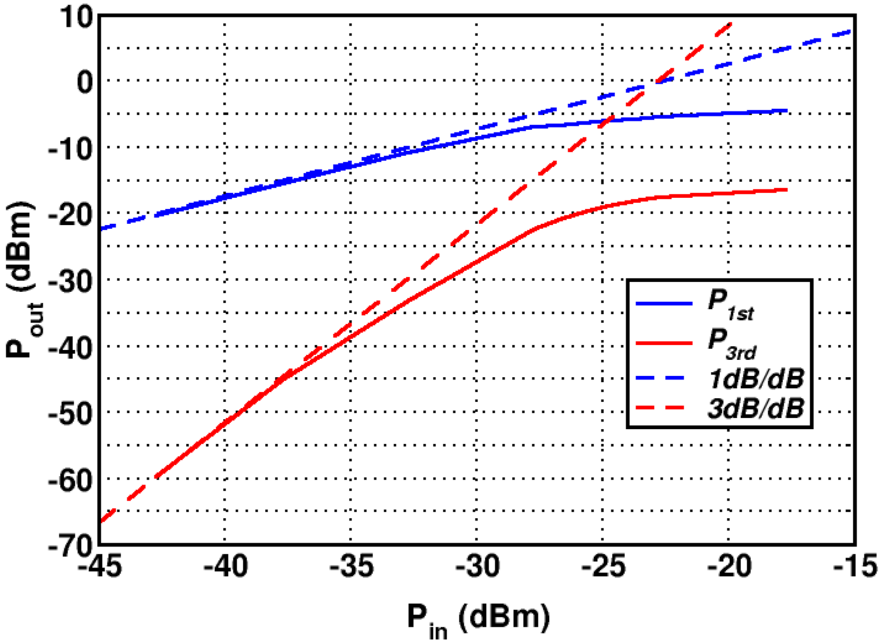
1.2-GHz biquad bandpass filter



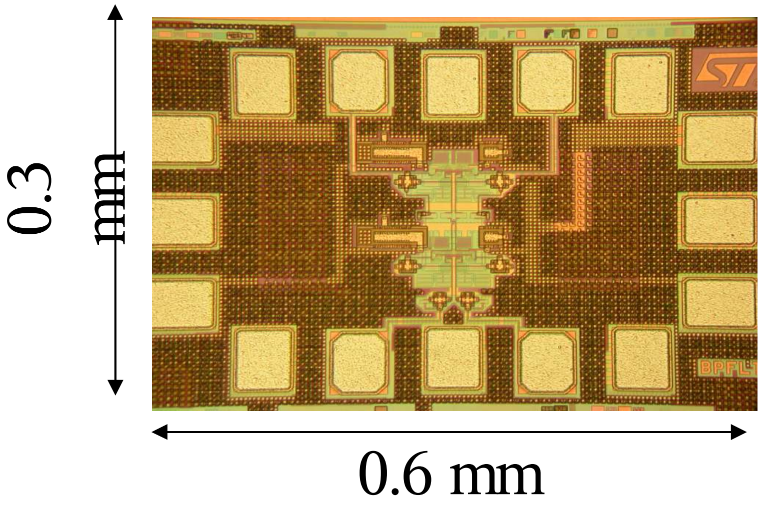


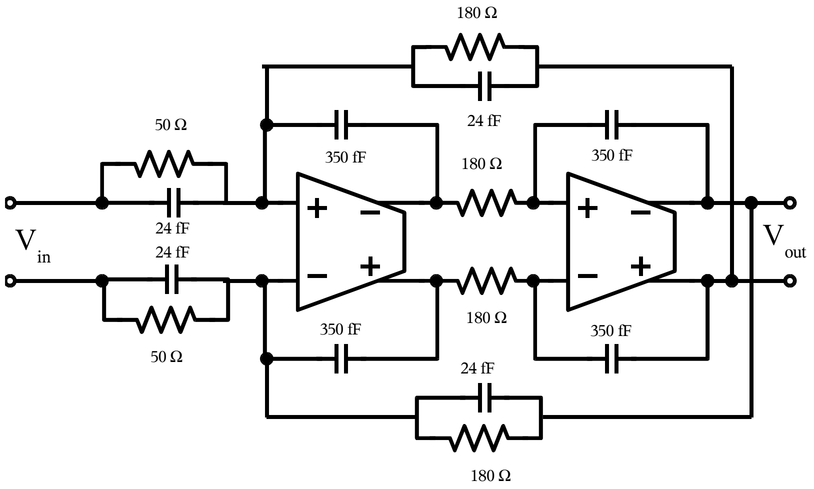


P_{out} vs P_{in}



Opamp filter vs. Gm-LC filter



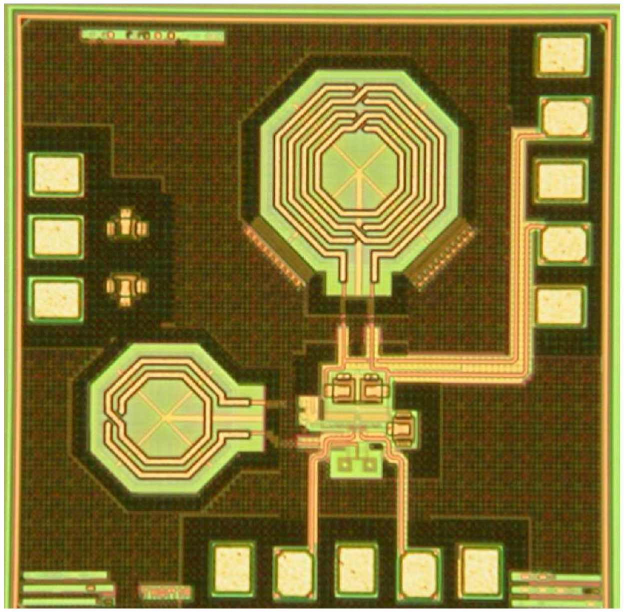


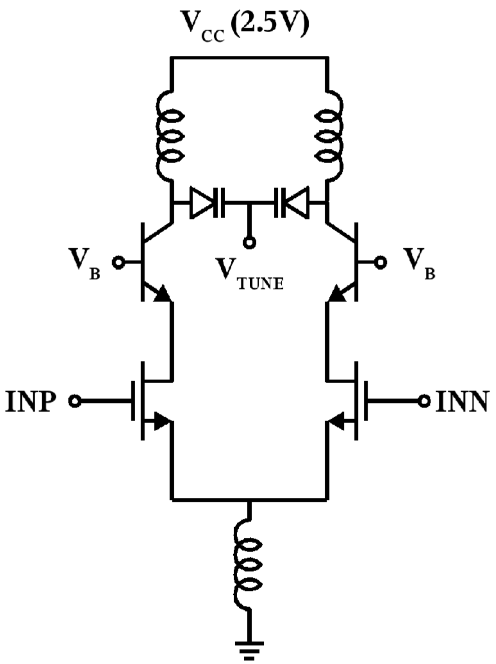
- 2-stage opamp filter:

  $0.3 \times 0.6 mm^2$

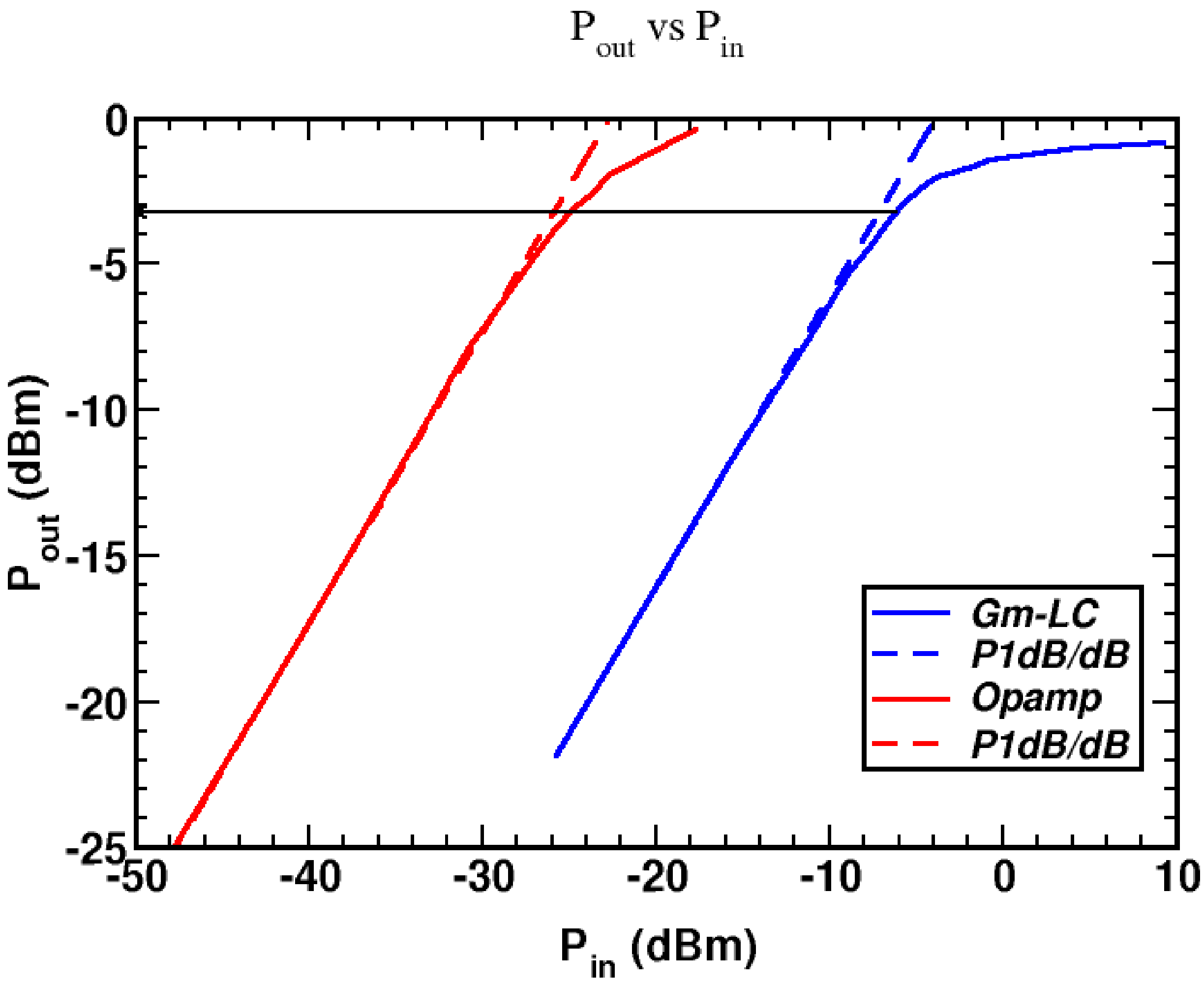
- 1-stage gm-LC filter:

  $0.96 \times 0.96 mm^2$





4th order (2-stage) gm-LC vs. 2-stage opamp filter



- P_{1dB} determined by filter gain and O_{1dB}
- Same O_{1dB}

Summary

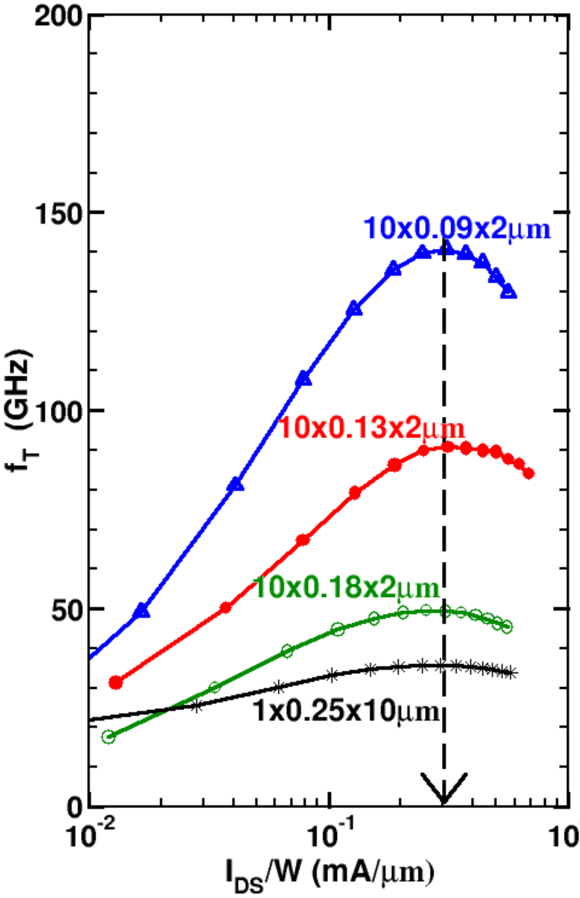
- MOS-HBT cascode topology maximizes UGB with good stability
- Radical approach to biasing CMOS-based opamps at peak f_{MAX} current density ensures:
  - maximum UGB
  - robustness to I_D, T, L, V_T variation
  - good linearity
- 1.2-GHz Biquad filter with 2 opamps and CMF demonstrated
- Linearity & power comparable to g_m-LC filter but 5x area reduction
- Portable between 130-nm and 180-nm nodes (G. Ng et al. SiRF 2006)

Acknowledgements

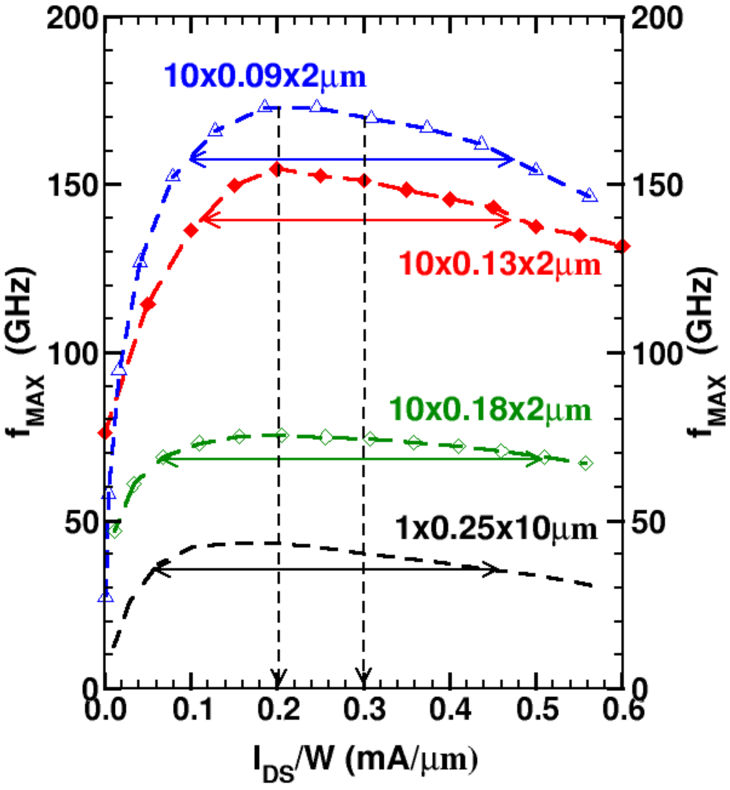
- Bernard Sautreuil & Steve McDowall of STMicroelectronics
- CFI, OIT and NIT for equipment

Backup

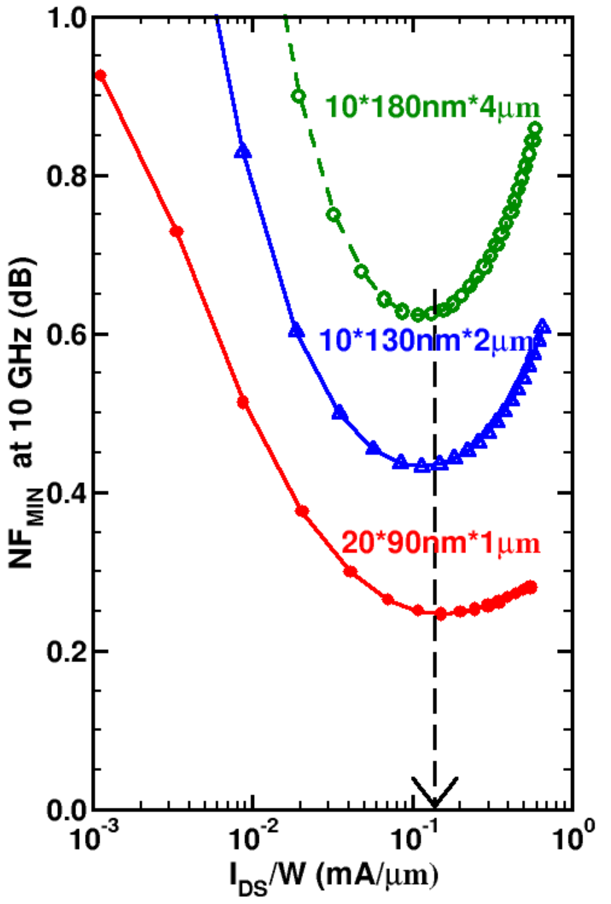
n-MOSFET characteristic current densities invariant across technology nodes and foundries (NF sims)



Peak f_T @ 0.3 mA/µm

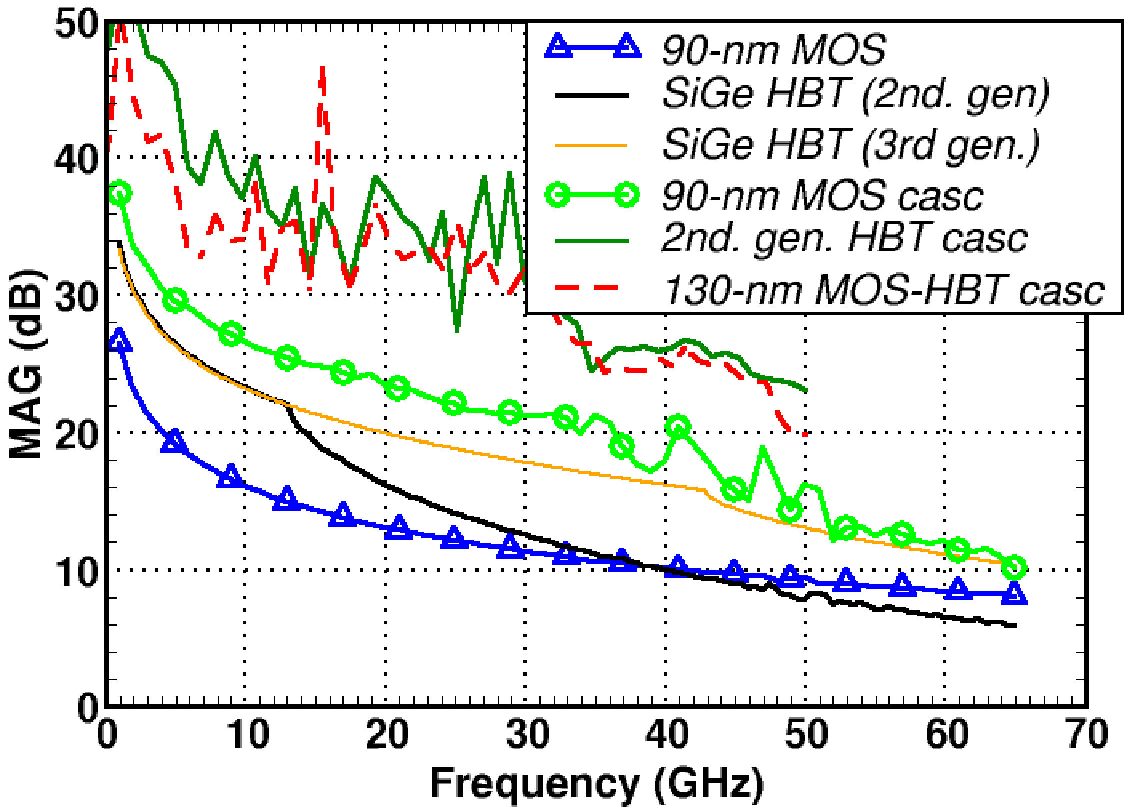


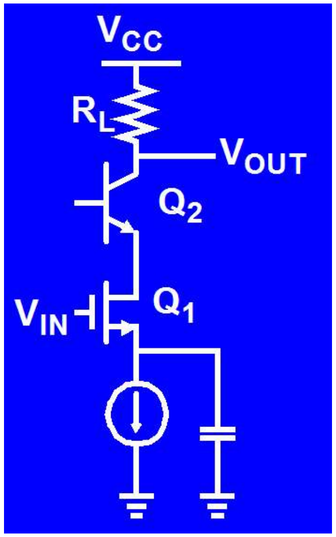
Peak f_{MAX} @ 0.2 mA/µm



NF_{MIN} @ 0.15 mA/µm

Comparison of power gain in 90nm MOSFETs and HBTs



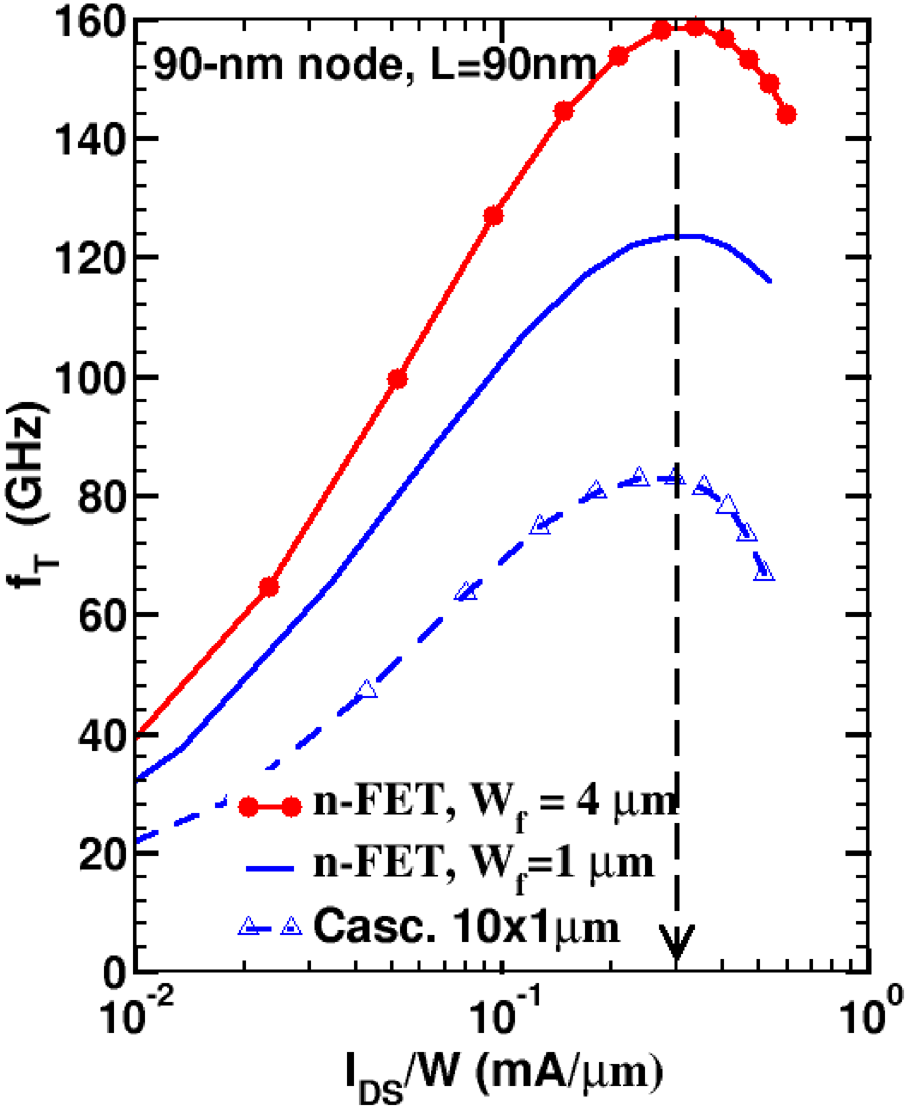


MOS-HBT
Cascode

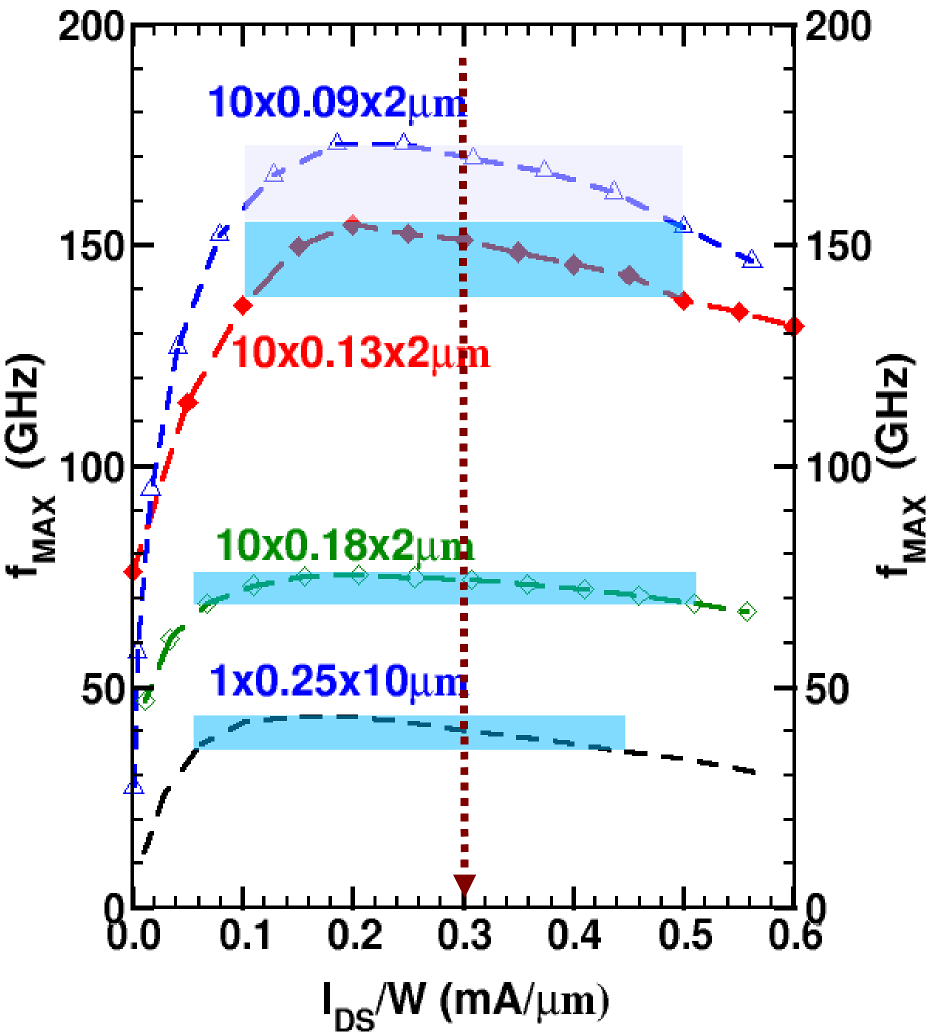
- *MAG > 6 dB at 65 GHz in* both HBTs and FETs
- MAG of MOSFET cascode (barely) larger than that of MOSFET @ 65 GHz
- Use CS/CE or HBT-based cascodes

Characteristic MOSFET current densities invariant over topologies

- *The peak f_T current density of a MOSFET cascode stage remains 0.3 mA/µm*
- *Cascode stage can be treated as a composite transistor in circuit design (f_T, f_{MAX}, NF_{MIN})*
- f_T of MOSFET cascode is < 60% of MOSFET f_T



Opamp biasing (iiV): best linearity bias



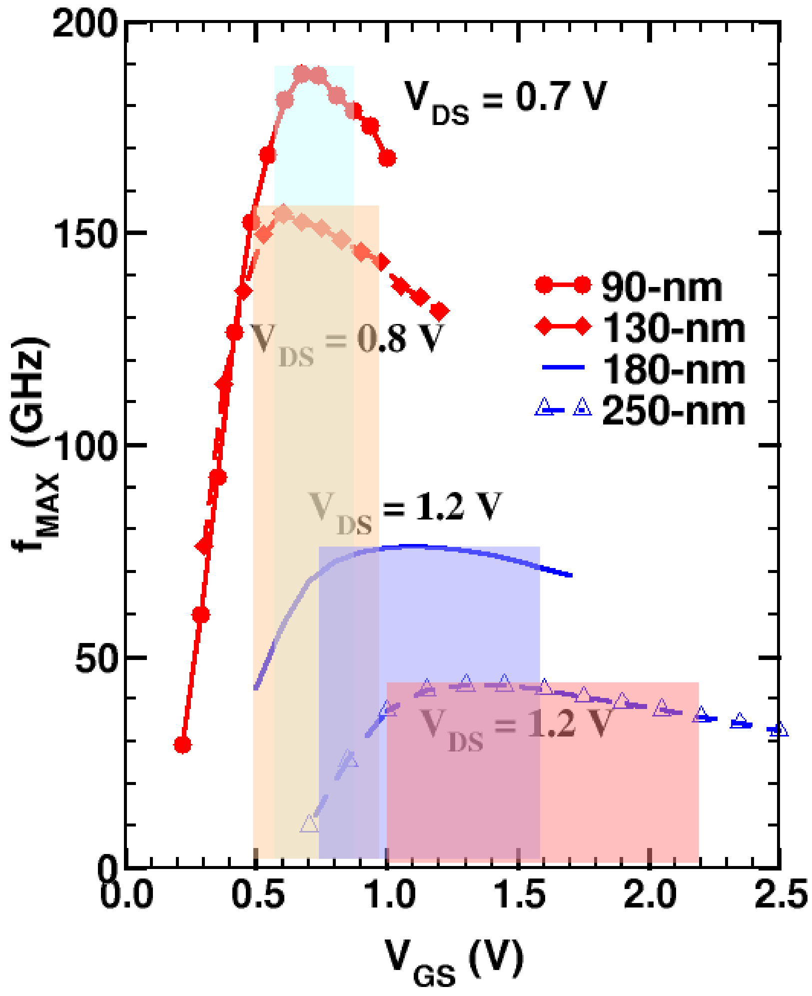
- Linearity depends on $f_{MAX}(I_{DS})$ flatness at peak

$$OIP1, OIP3 \sim \frac{f_{MAX}}{\frac{\partial^2 f_{MAX}}{\partial I^2_{C(DS)}}}$$

...but optimal linearity bias corresponds to peak f_T: 0.3 mA/μm

- Allows for 400 μA_{pp}/μm or 460 mV_{pp} of linear swing: i.e. >40% of V_{DD}.

Impact of scaling on OP_{1dB}



- Linearity depends on $f_{MAX}(V_{GS})$ flatness at peak
- Linear voltage swing at input/output decreases with every new node
- Current swing is constant over nodes
- Current and transistor size must be increased to generate the same power as in older nodes

$$OP_{1dB} \propto \frac{\Delta I_{DS} \times V_{MAX}}{16} = 25 \frac{\mu W}{\mu m}$$ in 90-nm MOSFETs

$$OP_{1dB} \propto \frac{\Delta I_{DS} \times V_{MAX}}{16} = 188 \frac{\mu W}{\mu m}$$ in SiGe HBTs

*) V_{MAX} is the maximum safe voltage

Sorin Voinigescu et al. CSICS-2005, Nov. 2nd, 2005

Conclusions

- CMOS characteristic densities largely invariant across nodes and foundries
- Constant-current density biasing in analog/RF CMOS minimizes impact of L, I_{DS}, T, and V_T variation
- Characteristic current densities in MOSFETs are invariant over topologies (CS, MOS-MOS and MOS-HBT)

Implications for circuit design

- CMOS CML gates, LNAs, TIAs, Opamps, VCOs, Mixers, PAs can be designed algorithmically and ported across nodes and technologies