Design Methodology for a 40-GSamples/s Track and Hold Amplifier in 0.18-μm SiGe BiCMOS Technology

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***Abstract*—A 40-GSamples/s track and hold amplifier (THA) is designed and fabricated in 0.18-μm SiGe BiCMOS and operates from a 3.6-V supply. The total power consumption is 540 mW with a chip area of 1.1 mm^2. Time domain measurements demonstrate 40-GHz sampling and S-parameter measurements show a 3-dB bandwidth of 43 GHz in track mode. For 19-GHz input signals, a total harmonic distortion of −27 dB at the 1dB compression point has been measured and a spurious-free dynamic range of 35 dB has been achieved.**

***Index Terms*—Analog-to-digital converter, DSP-based equalizer, equalization, SiGe BiCMOS, track and hold amplifier.**

I. Introduction

IN THE PAST, optical fiber was considered to be an infinite bandwidth medium. However, the rapid scaling of data rates over optical networks has exposed two important fiber impairments: polarization mode dispersion (PMD) in single-mode fibers and differential mode dispersion in multi-mode fibers. Thus, to ensure error-free communication at bit rates above 10 Gb/s, some method of data equalization is required.

Electronic equalization integrated in the receiver offers lower cost and faster adaptation than all-optical dispersion compensation. Decision feedback and analog equalizers have been demonstrated up to 40 Gb/s [1], [2]. It can be argued that analog equalization is more practical at high data rates than digital equalization. However, assuming high-speed analog-to-digital converters (ADCs) can be realized, digital equalization is more robust, scalable, and offers more flexibility. Fig. 1 illustrates a system block diagram of a DSP-based fiber optic equalizer. At the heart of this system is an ADC clocked at the full bit rate. The design of a 40-GSamples/s track and hold amplifier (THA) is a prerequisite to implementing 40-Gb/s ADCs. Applications for mm-wave THAs and ADCs are not limited to DSP-based equalizers. THAs can also be used for satellite and wireless communication [3], [4], high-speed soft-decision-based forward error correction systems [5], military radar systems [6] and instrumentation (i.e., wide bandwidth sampling oscilloscopes) [7].

The fastest THA reported to date is a switched emitter-follower, 5-bit, 18-GSamples/s THA implemented in SiGe HBT technology [7]. A 3-bit, 40-GSamples/s ADC–DAC, employing a switched diode bridge sampler as its input stage, is presented in [6]. The sample and hold (S/H) block is followed by a rather high-noise emitter-follower/differential pair (EF/DIFF) stage with resistive degeneration, which acts as a preamplifier before the quantizer. Since the switched diode bridge provides no gain, its input-referred noise is further degraded by the high noise of the second stage (EF/DIFF). The reported spurious-free dynamic range (SFDR) at frequencies beyond 15 GHz is less than 13 dB (1.5 bits) and the overall bandwidth is limited by the S/H block to 13 GHz [6].

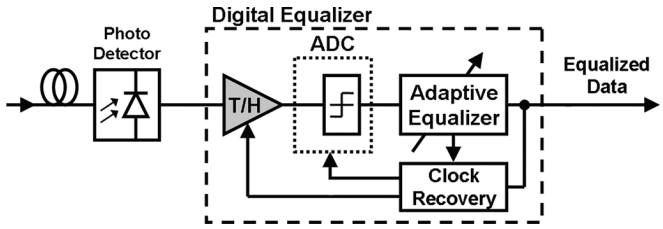

Fig. 1. System block diagram of a DSP-based fiber optic equalizer.

In this work, the design and characterization of the first 40-GSamples/s switched emitter-follower THA is described. It is based on a topology first proposed in [10] and also used in [7]–[9]. Unlike [6], the order of the sampling block and of the preamplifier is reversed, and unlike [6]–[10], a low-noise preamplifier is used as an input stage. This combination is one of the underlying reasons for achieving good performance. Sampling frequency and bandwidth of 40 GHz are achieved by applying a systematic design methodology which combines a low-noise broadband front-end, signal feedthrough cancellation, and a droop-rate-minimizing architecture. The bandwidth of every circuit block is optimized with attention to proper biasing, layout, and component sizing. The design methodology of the THA is covered in Section II and the measurement results are presented in Section III.

II. Track and Hold Amplifier Design

Fig. 2 shows a simplified block diagram of the track and hold amplifier. At the front end is a differential broadband low-noise amplifier (LNA) which is noise and impedance matched to 50Ω per single-ended input. Its linearity, bandwidth, and noise figure determine the overall system performance. The output of the LNA goes to an emitter-follower/differential pair (EF/DIFF) stage which, in turn, drives the track and hold block at the core of this system. The output of the track and hold stage

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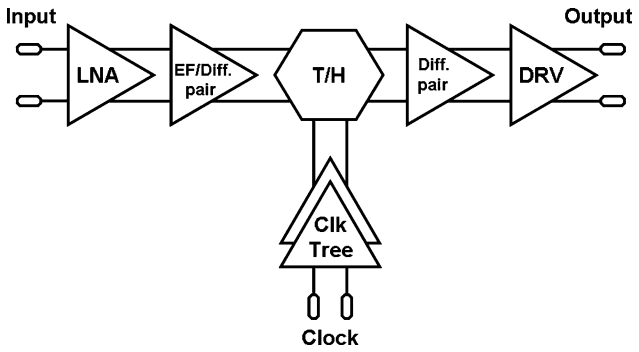


Fig. 2. Simplified block diagram of the 40-GSamples/s THA.

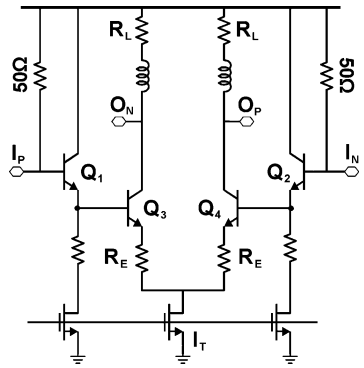


Fig. 3. Schematic of an emitter-follower/differential pair (EF/DIFF).

is buffered by a differential pair and fed to a linear output driver with 50-Ω output impedance. A high-bandwidth clock distribution network delivers a 40-GHz differential clock signal to the THA. The following sections cover the design methodology for each block.

A. Broadband Low-Noise Amplifier (LNA)

Traditionally, designers have used emitter-followers and heavily degenerated differential pairs as input stages [7]–[11] (shown in Fig. 3). While this approach can provide adequate bandwidth and linearity, using 50-Ω resistive loads for matching or heavy resistive degeneration (R_E) results in poor noise figure. In contrast, a transimpedance amplifier (TIA), Fig. 4, can be designed to provide simultaneous noise and impedance matching without the need for 50-Ω matching resistors [12]. It employs a shunt–shunt feedback scheme which can be used to adjust the input impedance by varying the feedback resistor R_F.

The linear output voltage swing of the TIA is set to 600 $\mathrm{mV_{P\text{-}P}}$. Input impedance matching is achieved as described in [12], which results in the use of 200-Ω feedback resistors, R_F. To improve the linearity at the input of the TIA, two 15-Ω degeneration resistors are also added. It is important to note that the linear output swing must be chosen with consideration to the desired bandwidth as well. A large value for R_L would result in a low pole frequency at that node, limiting the overall bandwidth. In this design, simulations show that the bandwidth of the TIA exceeds 40 GHz. Noise matching is achieved by sizing the input transistors (Q_3, Q_4) to have

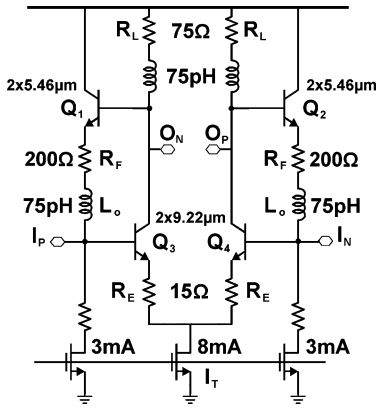


Fig. 4. Schematic of a transimpedance amplifier (TIA).

50-Ω optimum source impedance. Given noise parameters G, G_C, R, and B (technology constants which depend on the bias current density), and $\omega_o = \omega L_o/R_F$, the following equation can be used to determine the optimal emitter length of the input devices at angular frequency ω [12]:

$$l_{E\,\mathrm{OPT}} = \frac{1}{\omega}\left[\frac{1}{R_F\,(1+\omega_o^2)} + \frac{1}{Z_o}\right]\sqrt{\left(\frac{R}{(G/R)+G_C^2+B^2}\right)}. \tag{1}$$

The transistors are biased at minimum noise figure current density J_{OPT} and ω is set for (2π) 20 GHz. The bandwidth of this stage is further enhanced by using inductive peaking both in the feedback path and at the output. The feedback inductor L_o also filters high-frequency noise. The measured noise figure of SiGe HBT TIAs and emitter-follower/differential pairs for 40-Gb/s applications were compared in [13], demonstrating the superiority of the TIA stage.

B. Emitter Follower/Differential Pair and Track and Hold Stages (EF/DIFF and T/H)

The output of the TIA is fed to an emitter-follower/differential pair stage which in turn drives the track and hold (T/H) block, as shown in Fig. 5. The T/H block consists of a pair of switched emitter-followers and the hold capacitor, C_H [10]. The behaviour of the circuit in "Track" and in "Hold" modes must be optimized as each mode of operation contributes to the overall system performance.

1) Track Mode Operation: Fig. 6 illustrates the equivalent half-circuit schematic of the T/H block in track mode. During track mode, the signal $\mathrm{Clk_N}$ is at a "high" current mode logic (CML) level while the signal $\mathrm{Clk_P}$ is "low". Thus, currents I_{T1} and I_{T2} flow through the transistors Q_1 and Q_2, respectively, which act as emitter-followers. The signal $\mathrm{In_P}$ (for instance) is amplified by the EF/DIFF stage and buffered by the two consecutive emitter-followers before arriving at the output terminal $\mathrm{O_N}$. However, there are a few major sources of nonidealities in track mode; for instance, modulation of the base-emitter voltage of the emitter-follower Q_1 as a function of the input voltage and the nonlinearities of the emitter-follower/differential pair.

During track mode, the current of Q_1 is modulated by the current i_{CH} required to charge and discharge the hold capacitance. This modulation leads to variations in the base-emitter

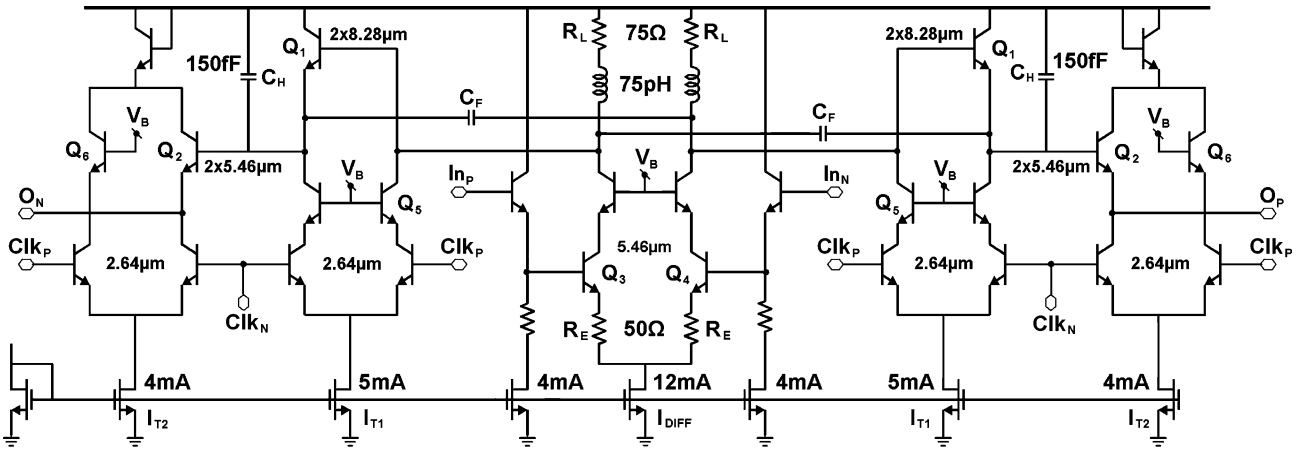


Fig. 5. Circuit diagram of the emitter-follower/differential pair followed by the track and hold block. Signals $\mathrm{In_N}$ and $\mathrm{In_P}$ are provided by the TIA output.

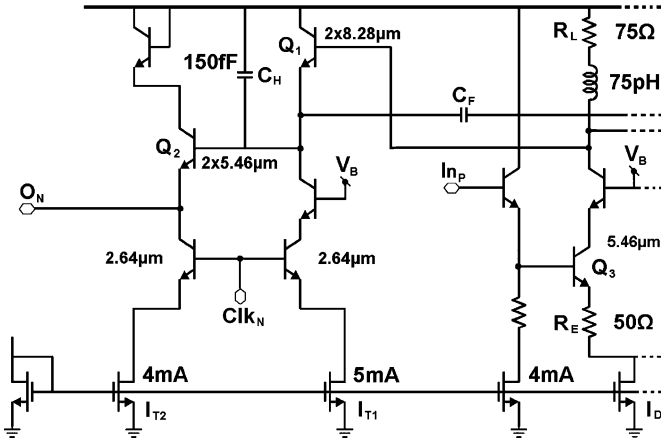


Fig. 6. Equivalent T/H half-circuit in track mode.

voltage of Q_1 as a function of the input voltage and is undesired. If $v_{\rm in}$ and $v_{\rm out}$ denote the small-signal input and output voltages and V_t is the thermal voltage kT/q, the output voltage of the switched emitter-follower is given by [10]

$$v_{\rm out} = v_{\rm in} - V_t \ln\left(\frac{I_{T1} + 2i_{CH}}{I_{T1}}\right). \tag{2}$$

For a sinusoidal input with frequency $f_{\rm in}$ and amplitude A, the maximum charge current is

$$i_{CH} = C_H \frac{dv_{\rm in}}{dt} = 2\pi f_{\rm in} A C_H. \tag{3}$$

Given that the circuit is implemented differentially, only the third-order harmonic is of interest. It can be shown that the third-order harmonic ($D_{\rm HD3}$) is [10],

$$\begin{aligned} D_{\rm HD3} &= \frac{V_T i_{CH}^3}{12 I_{T1}^2 \left(\dfrac{A I_{T1}}{2} + V_T i_{CH}\right)} \\ &= \frac{V_T \left(2\pi f_{\rm in} A C_H\right)^3}{12 I_{T1}^2 \left[\dfrac{A I_{T1}}{2} + V_T \left(2\pi f_{\rm in} A C_H\right)\right]}. \end{aligned} \tag{4}$$

It is immediately apparent that the total harmonic distortion can be improved by increasing the tail current I_{T1} or by reducing the hold capacitance C_H. Increasing the tail current beyond 5 mA makes transistor Q_1 too large, resulting in inadequate bandwidth. On the other hand, reducing the hold capacitance excessively would result in significant hold mode distortion.

Based on a maximum swing of 240 $\mathrm{mV_{P\text{-}P}}$ at the input of the TIA, the gain of the two blocks preceding the T/H, a sampling rate of 40-GSamples/s, and a tail current of 5 mA, a hold capacitance of 175 fF was chosen to attain 28 dB of linearity. Simulations indicate a total of 25 fF of parasitic capacitance at the hold node. The remaining required capacitance is provided via a 150-fF MIM capacitor. The size of the hold capacitance also impacts the hold mode performance of the THA. As a result, a compromise between the track mode and hold mode performance is made to achieve acceptable bandwidth and linearity.

The EF/DIFF stage preceding the T/H block is also optimized for linearity. Referring to Fig. 5, the maximum linear input swing of the EF/DIFF stage can be calculated based on the circuit component parameters and biasing. Given the small-signal gain $G_{v/v\text{-}Diff}$ of the differential pair, the collector-emitter voltage $V_{CE\text{-}Q3,4}$, and tail current $I_{\rm DIFF}$, the maximum linear input voltage swing is

$$\begin{aligned} &\mathrm{MaxSwing} = \\ &\min\left(\frac{I_{\rm DIFF} R_L}{G_{v/v\text{-}Diff}}, \frac{2(V_{CE\text{-}Q3,4} - V_{CE\text{-}SAT})}{G_{v/v\text{-}Diff}}, (1 + g_{m\text{-}Q3,4} R_E) 2V_T\right). \end{aligned} \tag{5}$$

Knowing the desired signal amplitude at the input of the T/H block, one can ensure sufficient linear voltage swing range, both at the input and output. Transistors $Q_{3,4}$ are biased at peak f_T current density $J_{\rm PfT} = 1.2$ mA/μm to maximize speed. Inductive peaking is used to extend the 3-dB bandwidth of this stage.

Due to large capacitive loads at their emitters, which can lead to negative resistance and oscillation, transistors Q_1 and Q_2 are biased at 1/4 and 1/3 peak f_T current density, respectively. Biasing these transistors at higher current densities would result in excessive peaking in the AC response of the circuit. The switching transistors in this block are biased for maximum

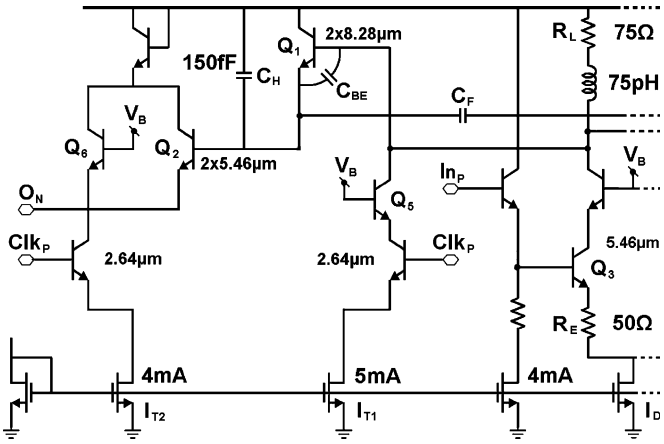


Fig. 7. Equivalent T/H half-circuit in hold mode.

switching speed at 1.5 times peak f_T current density, when fully switched.

2) Hold Mode Operation: During hold mode, the signal $\mathrm{Clk_N}$ is at a CML level "low" while the signal $\mathrm{Clk_P}$ is "high". Thus, I_{T1} and I_{T2} flow through Q_5 and Q_6, respectively (Fig. 7). The hold capacitance is now isolated from the input by Q_1 and separated from the next stage by Q_2. Three major hold mode distortions degrade the performance of the circuit: 1) inadequate isolation from the input to the hold node due to Q_1 remaining on; 2) input signal coupling to the hold capacitance C_H through $C_{BE\text{-}Q1}$; and 3) signal droop during hold mode.

During hold mode, C_H must be isolated from the input signal, which arrives from the EF/DIFF stage. I_{T1} is routed away from Q_1, through the resistive load R_L. The resulting voltage drop at the base of Q_1 reduces $V_{BE\text{-}Q1}$ by nearly a half of its DC value to ensure that Q_1 is fully turned off. The voltage drop at the base of Q_1 can be approximated by

$$\Delta V_{b\text{-}Q1} \approx I_{T1}R_L + V_T \tag{6}$$

and is set to approximately $V_{BE\text{-}Q1}/2$. It is important to note that the value of R_L is chosen to concurrently satisfy linearity and isolation criteria.

Hold mode signal feedthrough occurs as the input signal couples through the parasitic capacitance $C_{BE\text{-}Q1}$ to the hold capacitance C_H. The hold mode feedthrough is

$$V_{\mathrm{fth}} = \frac{C_{BE\text{-}Q1}}{C_{BE\text{-}Q1} + C_H} V_{\mathrm{in}}. \tag{7}$$

In a high-speed THA, the hold capacitance must be small to improve bandwidth and total harmonic distortion (THD). Furthermore, transistor Q_1 is large and therefore $C_{BE\text{-}Q1}$ is also large. Hence, signal feedthrough poses limitations on the effective number of bits the THA can achieve. With the addition of two feedthrough cancellation capacitors C_F, feedthrough can be reduced. Due to the differential nature of the circuit, the feedthrough caused by capacitors C_F is of opposite polarity compared to $C_{BE\text{-}Q1}$. Therefore, signal feedthrough can be expressed as

$$V_{fth} = \frac{C_{BE\text{-}Q1}}{C_{BE\text{-}Q1} + C_H} \left(\frac{C_{BE\text{-}Q1} - C_F}{C_{BE\text{-}Q1}} \right) V_{\mathrm{in}}. \tag{8}$$

If $C_{BE\text{-}Q1} = C_F$, hold mode signal feedthrough should be completely eliminated. However, the addition of capacitors C_F significantly degrades the bandwidth of the system. Note that the impact of C_F is doubled due to the Miller effect. As a result, in this design only partial feedthrough cancellation ($C_F = 0.66C_{BE\text{-}Q1}$) is applied in order to achieve more bandwidth.

Signal droop during hold mode is caused by the gradual discharge of the hold capacitance and must be minimized. In this design, Q_2 isolates the hold capacitor from the next stage. The current required by the input of the next stage (roughly I_{TAIL}/β) is provided by the emitter current of Q_2, and not by the discharge current of C_H. This approach improves the droop rate by a factor of β. The disadvantage is the need to provide a high-speed clock to these switching pairs. This droop rate improvement technique has been employed in [8] and [10], but some designs, such as [7] and [9], omit the second switching emitter-followers.

The input-referred noise power spectral density of the first two stages of the THA (TIA + EF/DIFF) obtained from simulation reaches a value of 4 nV/$\sqrt{\mathrm{Hz}}$ at 20 GHz and a maximum of 5 nV/$\sqrt{\mathrm{Hz}}$ at 40 GHz. The equivalent input-referred noise integrated from 10 MHz to 40 GHz is 757 $\mu\mathrm{V_{RMS}}$, (−50 dBm). For a receiver with signal-to-noise ratio (SNR) of 17 dB, corresponding to an eye Q of 7 and a bit-error rate (BER) of 10^{-12}, this results in an input sensitivity of 5.3 mV.

C. Clock Distribution Network (Clock Tree)

The clock path converts a single-ended 150 $\mathrm{mV_{P\text{-}P}}$ clock input to a differential signal with 300 $\mathrm{mV_{P\text{-}P}}$ per side swing and drives four switched emitter-follower pairs in-phase. Its bandwidth must exceed 40 GHz. The clock distribution consists of a tree of emitter-follower inverters (EF/INV), each with a fan-out of two. The four differential outputs of the clock tree drive the T/H circuit through double emitter-follower stages (EF/EF). Fig. 8 illustrates the schematic of the final two stages, EF/INV–EF/EF.

D. Output Driver

The output driver is a differential pair with 50-Ω loads and a tail current of 24 mA. Resistive degeneration (20 Ω) is used to accommodate an input swing of 500 $\mathrm{mV_{P\text{-}P}}$ per side (determined by the desired input swing of the TIA and the overall system gain). The output return loss is improved by inductive peaking. A differential pair stage precedes the output driver and acts as a level shifter and buffer. The transistors in both stages are biased at peak f_T current density for maximum speed.

Fig. 9 presents the simulation results for the entire chip. Fig. 9(a) shows the single-ended outputs with a 10-GHz sinusoid signal sampled at 40 GHz. The 40-GHz clock signal is superimposed to illustrate the location of the sampled values. Fig. 9(b) shows the differential output of a 10-GHz signal sampled at 40 GHz. It can be observed that the common mode clock feedthrough is significantly reduced.

E. Layout and Fabrication

The chip was fabricated in Jazz Semiconductor's SBC18HX 0.18-μm SiGe BiCMOS technology with a f_T of 160 GHz. The chip area is 1.1 $\mathrm{mm^2}$ and the die photo is shown in Fig. 10. The

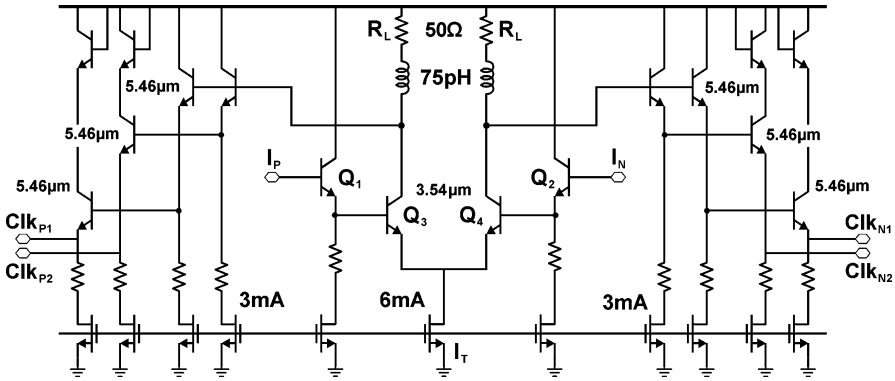


Fig. 8. Schematic of the emitter-follower inverter and double emitter-followers used in the clock network.

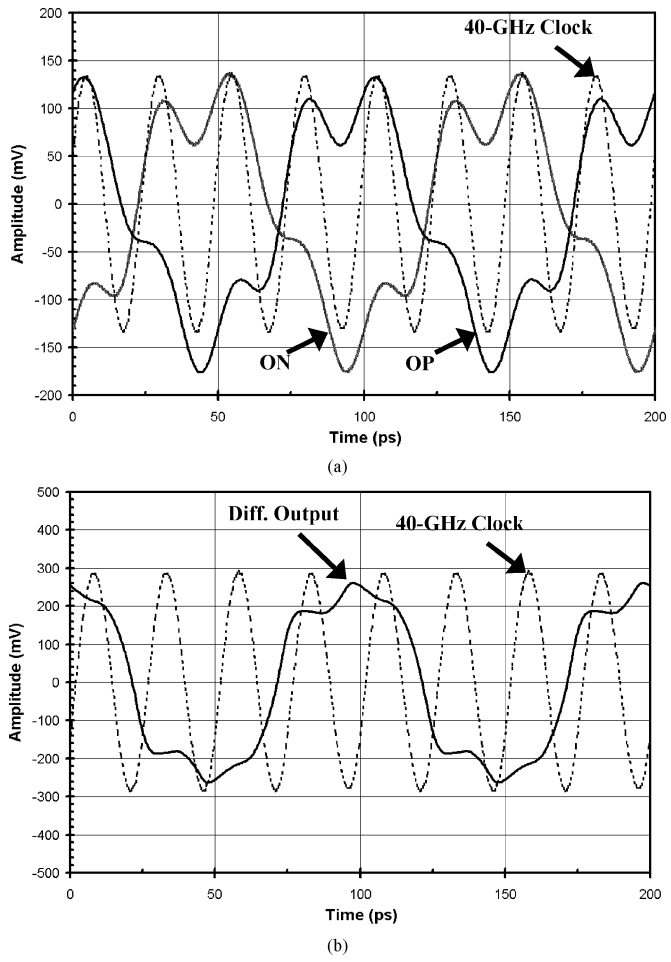


Fig. 9. Simulated (a) single-ended and (b) differential outputs of a 10-GHz sinusoid sampled at 40 GHz.

circuit blocks of the THA are indicated in the die photo. Careful attention was paid to layout symmetry. Each block consists of identical half-circuits to ensure matching and low skew propagation, both in the signal and in the clock paths. The inductors were designed using ASITIC [14] and are realized in the thick top metal layer.

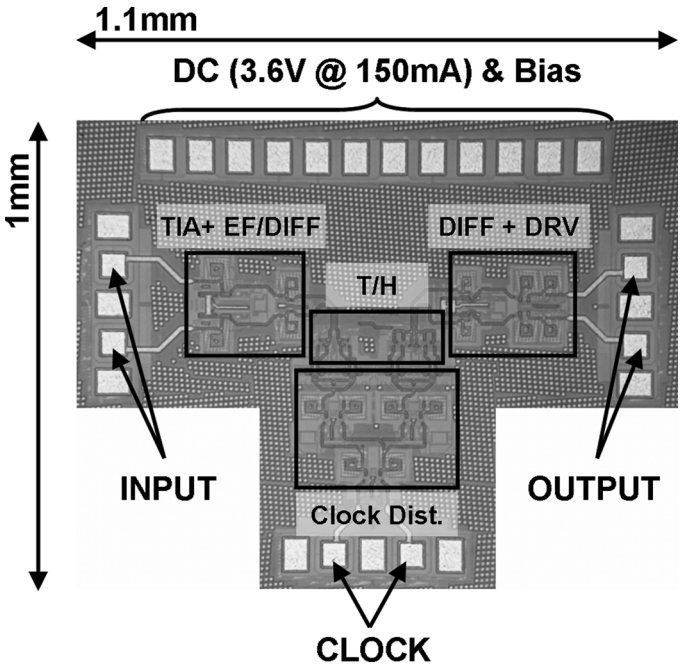


Fig. 10. Chip micrograph of the 40-GSamples/s THA.

III. Measurement Results

The circuit operates from a 3.6-V supply and draws 150 mA (540 mW). Due to the large number of stacked transistors in the track and hold block, a 3.3-V supply was not sufficient. The T/H block and the clock distribution network consume 24 mA and 75 mA, respectively, while the remaining current is drawn by the input and output stages. All measurements were conducted on-wafer.

The simulated and measured S-parameters are shown in Fig. 11. The measured single-ended input and output return loss are better than -15 dB up to 26 GHz and 42 GHz, respectively. S_{21} shows a bandwidth of 43 GHz when the circuit is configured in track mode. The ripple in the measured S_{21} of the circuit (which is not present in the simulated S_{21}) is due to larger than anticipated inductors in the differential pairs and the peaking due to the emitter-followers in the track and hold block.

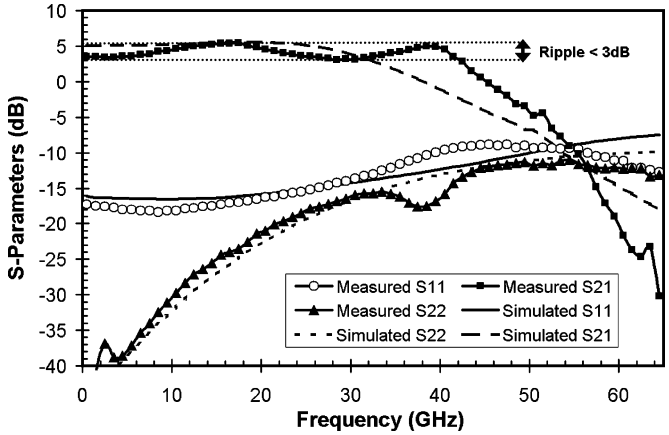


Fig. 11. Simulated and measured single-ended THA input return loss (S_{11}), output return loss (S_{22}), and transmission (S_{21}).

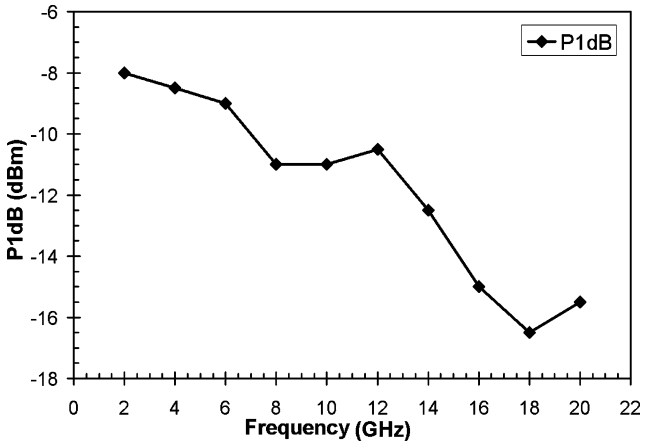
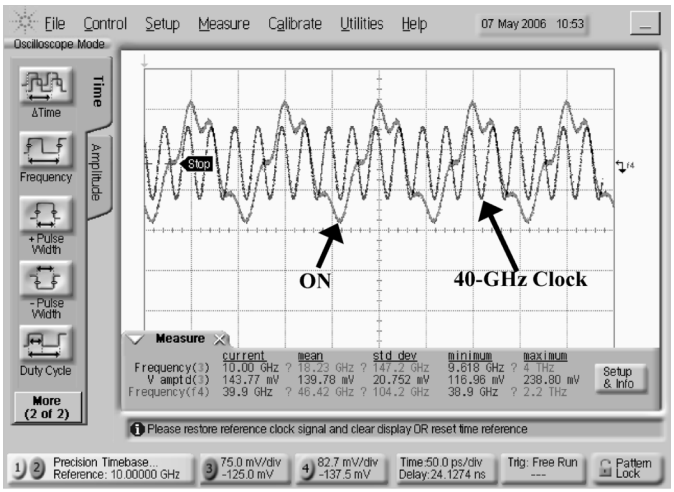
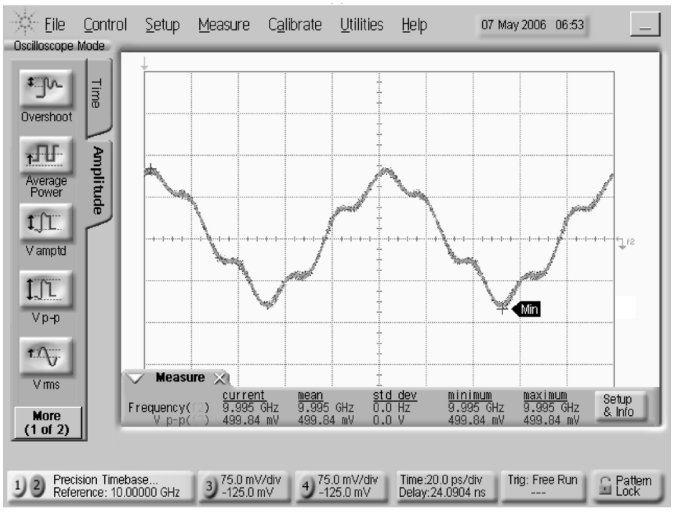


Fig. 13. Measured P1dB versus input frequency at 40 GSamples/s.



(a)



(b)

Fig. 12. Measured (a) single-ended and (b) differential outputs of a 10-GHz sinusoid sampled at 40 GHz.

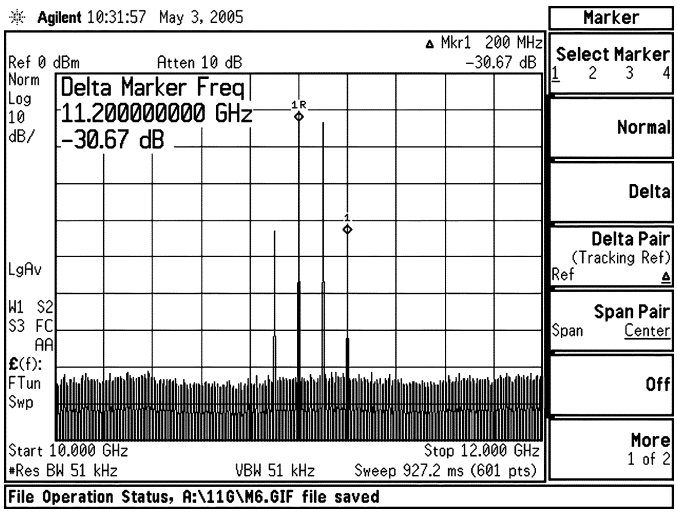


Fig. 14. Spectrum of IIP3 measurement at 11 GHz.

Time domain measurements were conducted using an Agilent 86100C DCA-J oscilloscope and an Agilent E8257D signal source. The two outputs of the THA were displayed on channels 3 and 4, respectively, and the differential output was calculated using the built-in functions of the oscilloscope. A constant delay was added to one of the channels to compensate for the difference in electrical delays between cables. The input power used is −12 dBm with −16 dBm of clock input power. Fig. 12 illustrates the measured single-ended and differential outputs of a 10-GHz signal sampled at 40 GSamples/s. In Fig. 12(a), the measured 40-GHz clock signal is superimposed on the single-ended output signal to more clearly indicate the location of each sample. As in the simulations, clock feedthrough (which appears in common mode) is present in the single-ended output and is significantly reduced in the differential measurement.

The spectral content of the output signal was captured using an Agilent E4448A PSA spectrum analyzer. The input compression point of the circuit was measured for frequencies ranging from 2 to 20 GHz and is plotted in Fig. 13. Figs. 14 and 15 show the spectra for two tone tests at 11 and 19 GHz, respectively, for input signal powers of −14 dBm and −24 dBm. The input tones were separated by 100 MHz. The measured IIP3 is illustrated as

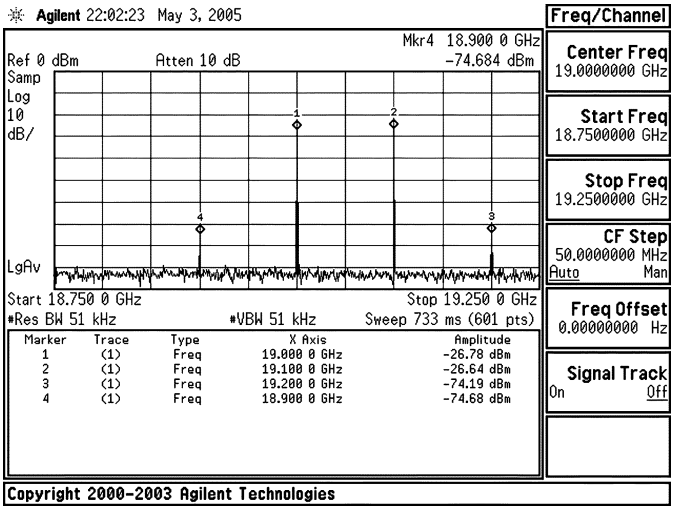


Fig. 15. Spectrum of IIP3 measurement at 19 GHz.

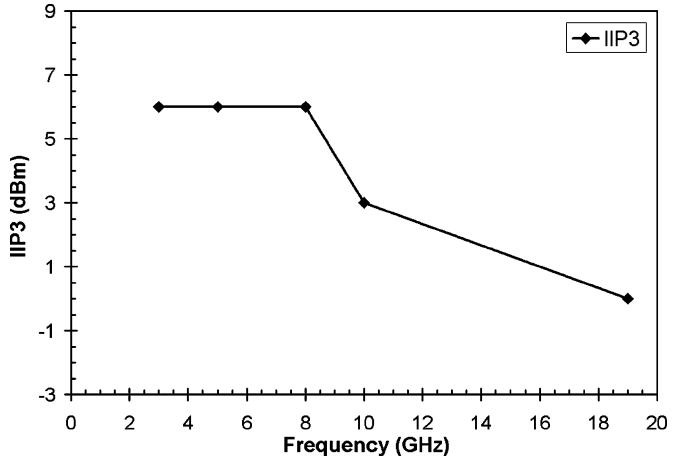


Fig. 16. Measured IIP3 versus input frequency.

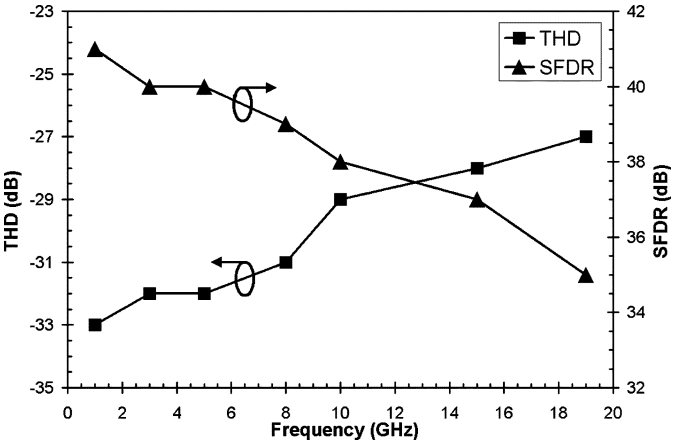


Fig. 17. Measured THD at the 1dB compression point and SFDR versus input frequency at 40 GSamples/s.

a function of frequency in Fig. 16 and has a 3-dB bandwidth of 10 GHz.

Fig. 17 shows the measured SFDR and THD. The SFDR was calculated as the difference between the measured fundamental signal power and that of the third-order harmonic at the input power where the harmonic power exceeds the noise floor. THD values were measured as the difference between the fundamental signal power and the third-order harmonic at the P1dB input power. For a 19-GHz input, the SFDR and THD were 35 dB and -27 dB, respectively. The single-ended spectral characteristics of a beat frequency test with $f_{\rm in} = f_s + \Delta f$, $f_{\rm s} = 40$ GHz, and $\Delta f = 2$ MHz are shown in Fig. 18. The difference between the power of the fundamental and of the second- and third-order harmonics is 24.7 dB and 42 dB, respectively, for a -16 dBm input signal power. It is expected that the second harmonic content should be much lower when the circuit is measured and operated in differential mode. Table I compares this work with other state-of-the-art track and hold amplifiers presented to date. It demonstrates the highest sampling frequency and track mode bandwidth.

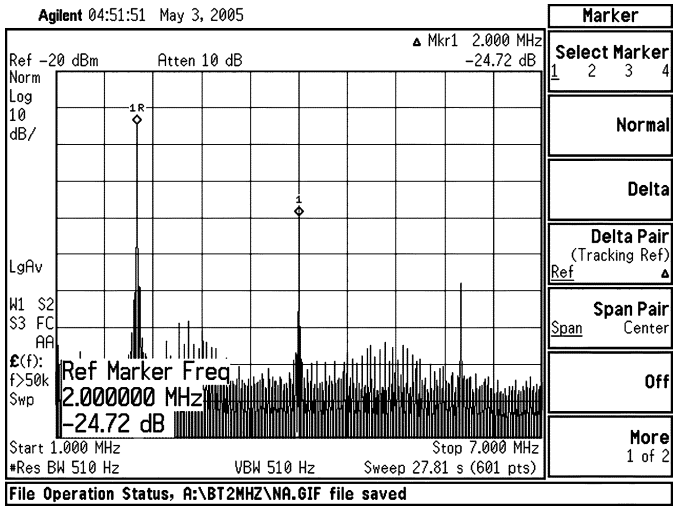


Fig. 18. Beat frequency test: input signal at 40.002 GHz sampled at 40 GHz.

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART TRACK AND HOLD AMPLIFIERS

	f_{sample} [GS/s]	Track ω_{3dB} [GHz]	THD [dB @ f_{in}]	Supply [V]	Power [mW]	Process [N / f_T]
This Work	**40**	**43**	**-27 @ 19 GHz -29 @ 10 GHz**	**3.6**	**540**	**SiGe 160 GHz**
[3]	10	>10	-30 @ <10 GHz	5.2	550	SiGe 45 GHz
[4]	12.1	5.5	-49.5 @ 3 GHz	3.5	700	SiGe 200 GHz
[7]	18	7	-32.3 @ 2 GHz	3.5	128	SiGe 120 GHz
[8]	12	14	-23.3 @ 12.001 GHz	-5.2	390	InP 120 GHz
[15]	10	2.5	-41 @ 1 GHz	3.3	70	SiGe 200 GHz

IV. CONCLUSION

A 40-GSamples/s THA was designed and fabricated. Following a systematic design procedure, and combining a low-noise front-end, signal feedthrough cancellation, and a second pair of switched emitter-followers for droop rate improvement has yielded the highest sampling frequency for a switched emitter-follower THA. For 19-GHz input signals,

a THD of −27 dB at the 1dB compression point has been measured and an SFDR of 35 dB has been achieved.

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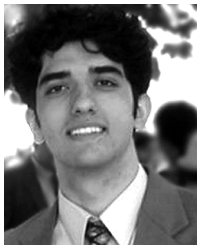

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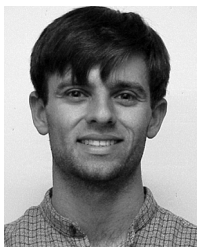

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