65-nm CMOS, W-Band Receivers for Imaging Applications

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***Abstract*-Two 76-92 GHz receivers, featuring 3-stage cascode LNAs coupled through a transformer to a double-balanced Gilbert-cell mixer and differential DC-5GHz IF buffer, are reported in 65-nm general purpose (GP) CMOS technology. One receiver features a traditional LNA with series-series inductive feedback, while the LNA of the second receiver employs a shunt-series, transformer-feedback cascode stage. Both receivers have a differential down-conversion gain of 12 dB, an input P_{1dB} of -13 dBm, and a double-sideband noise figure of 9-10 dB. They each occupy an area of 550μm×550μm and consume 94 mW. An LO-to-RF isolation of 60 to 59 dB was measured for LO signals in the 80-85 GHz range. The transformer-feedback provides a broader bandwidth input match, lower than -10 dB from 74 to 95 GHz.**

I. Introduction

CMOS technology has emerged during the last three years as a potential candidate for low-cost radio ICs in the 60-GHz band [1]-[7]. More recently, with the first reports of 80-100 GHz amplifiers in 90-nm and 65-nm technologies [8],[9], and with SiGe BiCMOS building blocks and transceivers showing robust performance margin over process and temperature at 80GHz [10] and even operation at 160 GHz [11], the prospect of large SOCs operating at 100 GHz and beyond no longer appears far-fetched [12].

In this paper, we demonstrate the first CMOS W-band receivers, as illustrated in the block diagram of Fig. 1. One receiver features a new cascode stage with shunt-series transformer feedback which is based on a recently-published UWB common-source LNA [13]. For comparison, the second receiver employs a standard cascode LNA with inductive degeneration. It is demonstrated theoretically and validated experimentally that the transformer feedback allows for the same flexibility to match the noise and input impedance as the series-series, inductor-feedback LNA, and that the two receivers and LNAs have almost identical gain, noise, and linearity performance. In addition, the transformer-feedback LNA offers a certain degree of ESD protection without increasing the capacitance of the input pad.

II. LNA Design

A. Inductive-Feedback LNA

The popularity of the cascode LNA topology with series-series inductive feedback (Fig.2) is due to the fact that it lends itself to an algorithmic design methodology [14], even at mm-waves [8],[15]. Moreover, a unique, optimal design exists that simultaneously matches the input and noise impedances of the first stage of the LNA to Z_0 (typically 50 Ω). Noise impedance matching is accomplished by sizing the transistor (i.e. changing g_m and C_{in}) at the minimum noise figure current density bias, while input resistance matching is realized by choosing the appropriate value for L_S [14].

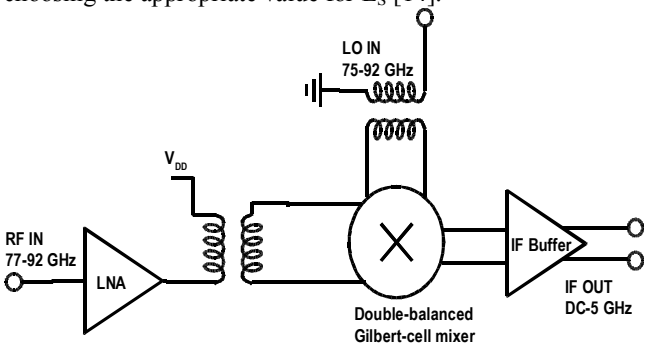

Fig. 1. Receiver block diagram

Mathematically, this can be captured using the noise impedance formalism and Z-matrices. The expressions of the optimal noise impedance and minimum noise figure of the amplifier with feedback can be cast as (1) and (2), respectively.

$$R_{sopt} = \sqrt{R_{sopta}^2 + \frac{R_{uf}}{G_{na}} + 2R_{cora}\Re(z_{11f}) + \Re^2(z_{11f}) + \frac{|Z_{corf} - z_{11f}|^2 G_{nf}}{G_{na}}} \quad (1)$$

$$F_{MIN} = 1 + 2G_{na}[R_{cora} + R_{sopt} + \Re(z_{11f})] \quad (2)$$

where subscript "a" denotes the parameters of the amplifier network (i.e. of the MOS cascode) and subscript "f" describes the parameters of the feedback network .

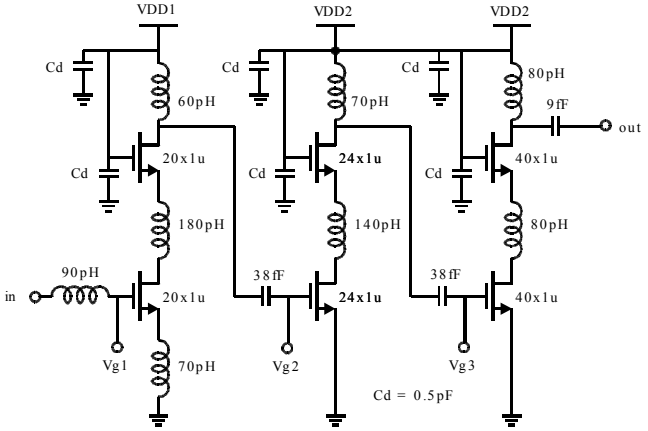

Fig. 2. Inductive-feedback LNA schematic.

From (1) and (2) one notices that, if the feedback (L_S) and gate (L_G) inductors are ideal (i.e. Q is infinite and G_{nf} =0, R_{uf}=0, Z_{corf}=0, $Z_{11f} = Z_{12f} = j\omega L_S$, Z_{12a} =0) the noise figure of

the noise-matched LNA is identical to the minimum noise figure of the cascode. At the same time, from (1), the real part of the optimal noise impedance is identical to that of the main amplifier. Only the imaginary part changes due to L_S.

B. Transformer-Feedback LNA

A wideband LNA with shunt-series feedback was recently proposed [13]. It uses transformer feedback in the first CS stage, while the second stage is formed by a transimpedance amplifier. An alternate, loss-less shunt-series feedback topology, that retains the broadband input impedance and noise impedance matching, employs a cascade and is illustrated by the first stage of the LNA shown in Fig. 3.

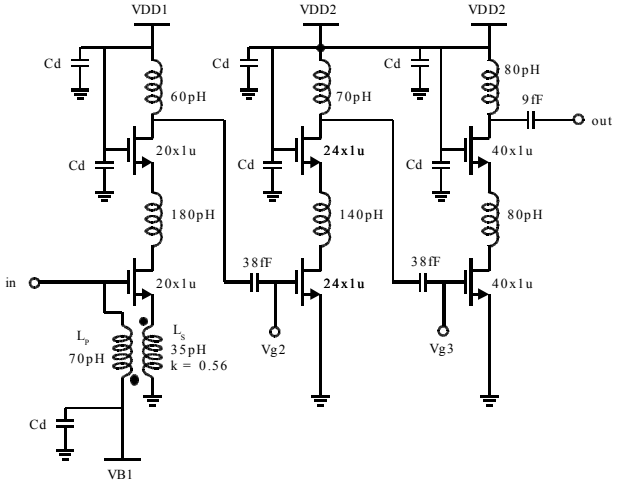

Fig. 3. Shunt-series, transformer-feedback LNA schematics.

This circuit can be analyzed using g-network parameters, the noise admittance formalism, and the theory of noise in networks with shunt-series feedback [16]. The g-matrix entries of the transformer-feedback network can be expressed as:

$$g_{11f} = -\frac{j}{\omega L_P},\ g_{12f} = -g_{21f} = \frac{M}{L_P},\ g_{22f} = j\omega L_S\left(1-k^2\right) \tag{3}$$

where L_P, L_S, and M are the inductance of the primary, the inductance of the secondary, and the mutual inductance of the transformer, respectively. If its imaginary part is tuned out by the parallel inductance of the transformer primary, the input admittance of the amplifier with feedback is cast as (4).

$$Y_{IN} \approx g_m \frac{M}{L_P} \tag{4}$$

Similar to the LNA with inductive degeneration, it becomes a function of the feedback (transformer) parameters M., L_P, and of the MOSFET transconductance, g_m.

The expressions of the optimal noise admittance of the amplifier with feedback and of its minimum noise figure are derived as:

$$G_{sopt} = \sqrt{G_{sopta}^2 + \frac{G_{uf}}{R_{na}} + 2G_{cora}\Re\left(g_{11f}\right) + \Re^2\left(g_{11f}\right) + \frac{\left|Y_{corf} - g_{11f}\right|^2 R_{nf}}{R_{na}}} \tag{5}$$

$$F_{MIN} = 1 + 2R_{na}[G_{cora} + G_{sopt} + \Re(g_{11f})] \tag{6}$$

If the transformer is lossless, $R_{nf} = 0$, $G_{uf} = 0$; $Y_{corf} = 0$ and Real (g_{11f}) = 0. As a result, the amplifier's G_{sopt} (5) and NF_{MIN} (6) become identical to those of the MOSFET cascode. Therefore, despite the different input stage topology, the LNAs of Figs.2 and 3 have similar flexibility in adjusting the optimal noise conductance, from g_m, and the input resistance (conductance), from Lp/M, to the desired values.

In both LNAs, the transistor in the first stage is biased at 0.25 mA/μm for low-noise, while those in the second and third stages are biased for maximum linearity at 0.3 mA/μm [3]. The current through the last stage of the LNA is the same as that of a recently reported 60-GHz CMOS PA [3]. After extraction of transistor layout parasitics, the simulated gain and NF of the LNAs are 17 dB and 7 dB, respectively.

III. Mixer and IF Amplifier Design

The mixer employs a double-balanced Gilbert-cell topology with inductive degeneration, common-mode inductor, and broad-banding [4], as illustrated in Fig. 4. The MOSFETs in the transconductor are biased for low-noise at 0.25 mA/μm. Dual-coil, vertically-stacked transformers are used at the LO and RF ports for single-ended to differential conversion and to provide bias to the mixer through the center taps.. The IF-buffer is terminated on-die with 50-Ω loads and is biased at 0.3mA/μm, for maximum linearity. The simulated down-conversion gain of the two receivers is 18 dB.

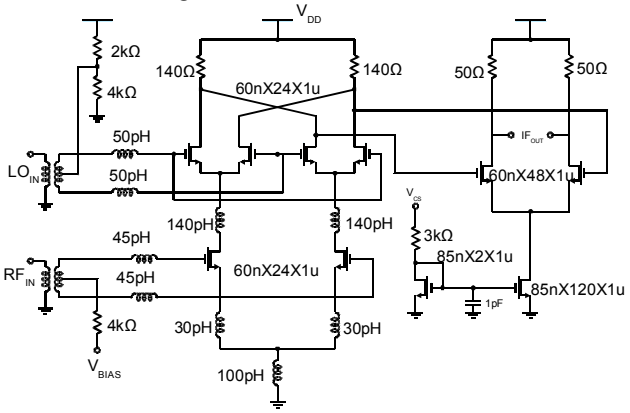

Fig. 4. Mixer and IF buffer schematics.

IV. Fabrication and Experimental Results

The circuits were fabricated in STM's digital 65-nm CMOS process with standard 7-layer Cu back-end. The f_T and f_{MAX} of both LP and GP n-MOSFETs with 80 gate fingers and 1μm finger width, contacted on one side of the gate, were measured on the same die as the receiver. Because GP transistors exhibit 30% higher g_m (1.05mS/μm) and f_T (165GHz at V_{DS}=0.7V), 15% higher f_{MAX} (240 GHz), and 0.3V lower V_{GS} at peak f_T bias, they were used exclusively in all circuits. The die photograph of the receiver with transformer feedback is shown in Fig. 5. The receiver occupies 550μm×550μm, including all pads. The three transformers (i) at the LNA input on the left, (ii) between the LNA and mixer in the center, and (iii) at the LO-port of the mixer on the right-side, are clearly visible. The differential IF output is located at the bottom of the die with 50-Ω lines leading off to the pads.

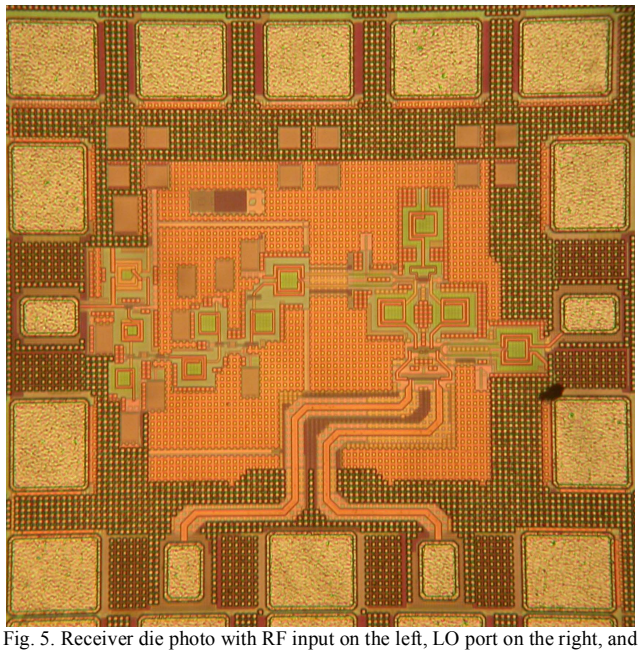

Fig. 5. Receiver die photo with RF input on the left, LO port on the right, and differential IF output at the bottom.

The circuits were tested on wafer using 50-75GHz and 75-100 GHz Millitech multipliers, an Agilent E4448A PSA series spectrum analyzer with W-band down-convert mixer, Agilent W8486A 75-110GHz power sensor, an ELVA-1 75-110GHz noise source with the HP 8970B noise figure meter, and a variable 0-30 dB, W-band waveguide attenuator.

Fig. 6 compares the differential down-conversion gain, the receiver noise figure, and the return loss at the RF port of the two receivers. For reference, the gain of the inductor-feedback LNA is also plotted. The two receivers have remarkably similar gain (12 dB) and noise figure (9-10 dB). As expected, the S_{11} of the receiver with transformer-feedback LNA is as low as -30 dB at 90 GHz and remains below -10 dB from 74GHz beyond the measurement range of 94 GHz. The 3-dB bandwidth of both LNAs extends from 76 GHz to 93 GHz, with a peak gain of 8 dB centered at 85 GHz. Although at the correct frequency, the peak gain is 8-9 dB lower than the simulated value. DC measurements conducted on the LNA breakouts and on transistors indicate a 20-30% decrease in the DC transconductance due to contact via resistance on the source stripes and in the slotted metal ground plane. The series resistance, rather than parasitic capacitance, was identified as the main reason for the severe degradation in gain, similar to the one observed in a 65-nm LP CMOS LNA implemented in a different process [12]. This problem appears to be more severe in the single-ended LNA, but does not affect the gain of fully differential circuits such as the mixer, IF buffer and a 90-GHz static frequency divider (to be reported elsewhere). For this reason, the receiver measurements were conducted with higher supply voltages, in the 1.8-2.2V range. In all cases, the V_{GS} of individual transistors remains in the 0.65-0.7V range, while V_{DS} does not exceed 1.1 V.

The double-sideband DSB noise figure of the two receivers is plotted in Fig. 7 vs. the current density of the input stage MOSFET. The minimum occurs at a current density of 0.25-0.3mA/μm, higher than in a 60-GHz receiver implemented in 90-nm GP CMOS technology [4]. The increased optimal noise figure current density at 85 GHz, a trend also observed in SiGe HBT circuits [12], needs further investigation since the peak f_T (0.3mA/μm) and peak f_{MAX} (0.2 mA/μm) current densities in both LP and GP n-MOSFETs are unchanged from those of earlier generations [17].

Fig. 8 reproduces the down-conversion gain and DSB NF of the transformer-feedback receiver as a function of the IF/RF frequency when the LO signal is fixed at 85 GHz - where the maximum LO power of +5 dBm is provided by the multiplier- and the RF signal is swept from 80 GHz to 85 GHz. The differential down-conversion gain reaches 12 dB while the double-sideband noise figure remains at 9-10 dB for IF frequencies in the 0.6-GHz to 1.8-GHz range.

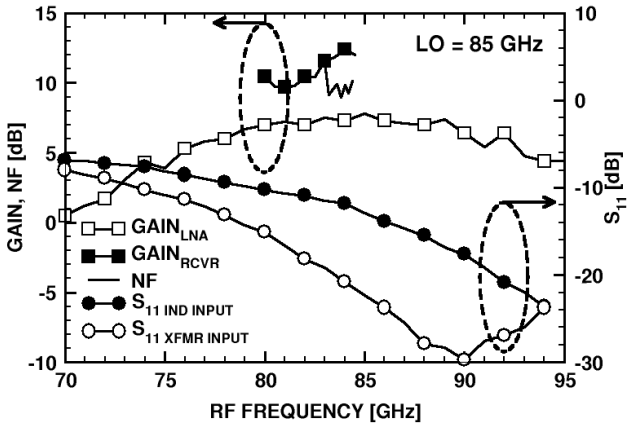

Fig. 6. Measured differential conversion gain, NF and S_{11} at RF port of the two receivers as functions of the RF frequency when the LO is 85 GHz. The gain of an inductor-feedback LNA breakout is also shown for reference.

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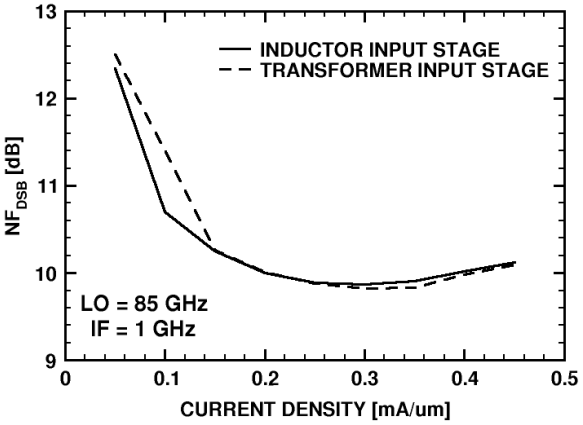

Fig. 7. Measured receiver DSB NF vs. MOSFET current density.

The excellent linearity of the receiver with transformer-feedback LNA is demonstrated in Fig. 9 for an RF input of 77 GHz and an LO signal at 75 GHz. P_{1dB} reaches -13 dBm while the differential down-conversion gain at 77 GHz drops to 10 dB, which corresponds to the lower end of the 3-dB bandwidth of the LNA, as seen in Fig. 6. The same values, within 0.5 dB, were measured for the receiver with inductor-feedback

LNA. Finally, the LO-to-RF leakage was measured for both receivers, with the spectrum analyzer connected to the RF port and applying a +5 dBm signal at the LO port. The isolation remains better than -60 dB for the measurement range of 80-85 GHz. Most of the isolation is provided by the LNA block whose isolation, lower than -42 dB, was obtained from S-parameter measurements between 55 and 94 GHz.

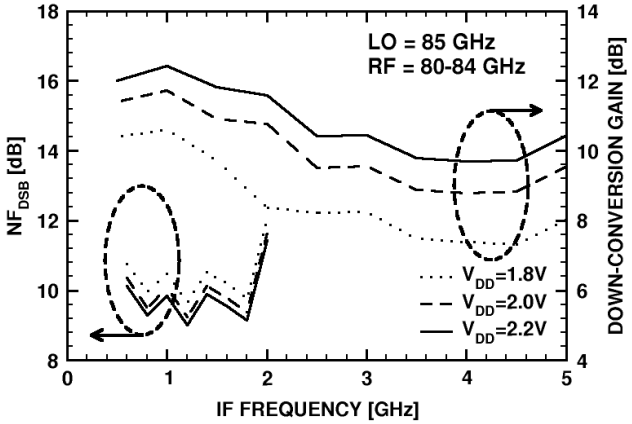

Fig. 8. Conversion gain and DSB NF of the receiver with transformer-feedback LNA as a function of RF/IF frequency and of supply voltage.

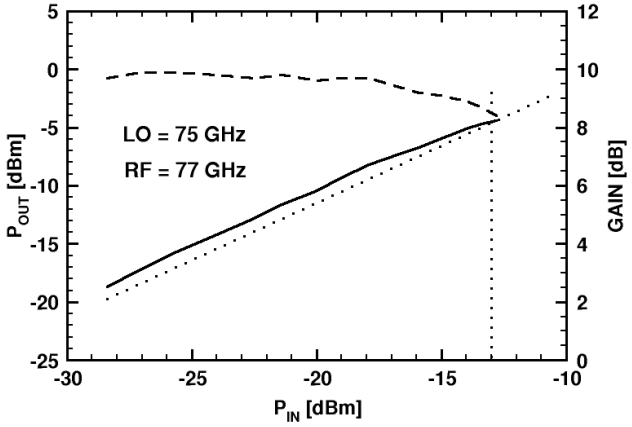

Fig. 9. Linearity of the receiver with transformer-feedback LNA at 77 GHz.

V. Conclusion

The first W-band receivers in CMOS have been reported. A shunt-series, transformer-feedback LNA topology was demonstrated that allows for ESD protection and broadband input matching in the 75-94 GHz band without compromising noise figure and gain when compared to a traditional cascode topology with inductive degeneration. Because only lumped inductors and transformers are used for impedance matching and for single-ended-to-differential conversion, the whole receiver die is only 0.3 mm^2. The large IF-bandwidth, exceeding 4.5 GHz, the small area, and the low power dissipation recommend these receivers for imaging and remote sensing arrays, as well as for high-data rate wireless personal area networks. Although setting a record for CMOS technology, this work has identified several issues of concern related to the design of mm-wave circuits in 65-nm CMOS. Unlike 130-nm and 90-nm amplifier designs at mm-waves [3],[4],[8], it was found that the DC series resistance of the contacts to source stripes and in the slotted metal ground plane significantly degrades DC transconductance and high frequency gain. One solution appears to be the deployment of fully differential topologies with merged transistor source and drain regions which place all contacts in common mode.

Acknowledgments

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