5-GHz SiGe HBT Monolithic Radio Transceiver with Tunable Filtering

Miles A. Copeland, *Fellow, IEEE*, Sorin P. Voinigescu, *Member, IEEE*, David Marchesan, *Member, IEEE*, Petre Popescu, *Associate Member, IEEE*, and Michael C. Maliepaard, *Member, IEEE*

***Abstract*—A wide-band CDMA-compliant fully integrated 5-GHz radio transceiver was realized in SiGe heterojunction-bipolar-transistor technology with on-chip tunable voltage controlled oscillator (VCO) tracking filters. It allows for wide-band modulation schemes with bandwidth up to 20 MHz. The receiver has a single-ended single-sideband noise figure of 5.9 dB, more than 40 dB on-chip image rejection, an input compression point of −22 dBm, and larger than 70 dB local-oscillator–RF isolation. The phase noise of the on-chip VCO is −100 and −128 dBc/Hz at 100 kHz and 5 MHz offset from the carrier, respectively. The transmitter output compression point is +10 dBm. An image rejection better than 40 dB throughout the VCO tracking range has been demonstrated in the transmitter with all spurious signals 40 dB below the carrier. The differential transceiver draws 125 mA in transmit mode and 45 mA in receive mode from a 3.5-V supply.**

***Index Terms*— Clock distribution network, image-reject-filter, inductors, low-noise amplifier, mixer, resonators, SiGe HBT, single-chip radio, transceiver, transmission lines, varactors, voltage-controlled oscillator, wireless ATM.**

I. Introduction

BASED ON THE proliferation of high-speed wireline Internet access at 2–10 Mb/s, one can envision future demand for wireless access at comparable rates. Unlike the crowded 2-GHz band, the 5-GHz bands, with over 300 MHz available, appear extremely attractive for high-speed applications such as wireless asynchronous transfer mode (ATM) and wide-band fixed-radio access. This would allow for several high-definition television (HDTV) channels and Internet services, as a potential low-cost alternative to 28-GHz local-to-multipoint distribution system (LMDS). The 5-GHz band is also an adequate entry point for SiGe heterojunction bipolar transistor (HBT) technology without performance overkill, as would be the case at 1–2 GHz where state-of-the-art Si bipolar and 0.35-μm CMOS and BiCMOS technologies are already squeezing out GaAs technologies from most applications, except some power amplifiers (PA's). A 5-GHz radio transceiver has recently been reported in Si BiCMOS technology [1]. The voltage-controlled oscillator (VCO) and the image reject filters (IRF's) were not included on-chip.

This paper describes details of an SiGe HBT 5-GHz radio transceiver with superior performance and a higher level of integration, including the VCO and tunable VCO-tracking IRF's [2]. The goal is to realize a single-chip radio front-end at 5 GHz with very demanding wide-band CDMA-like (W-CDMA) performance specifications [3]. Inductors were used extensively for a number of reasons. First, since they have negligible dc voltage drop, lower power supply voltages are possible. Second, they reduce noise and improve linearity and selectivity. Selectivity is critical in classic superheterodyne radio design to adequately isolate signals at different frequencies, such as the IF and RF. It is even more important when the system blocks are integrated on a single chip. Similarly, a fully differential architecture was employed in order to reduce common-mode (even harmonic) effects, minimize on-chip crosstalk, and reduce the impact of ground inductance. By integrating the IRF's on-chip, the need for additional RF p-i-n's and 50-Ω interfaces with the outside world is removed. This saves power and reduces package complexity and cost. Also, the potential for crosstalk between the RF pins of the package, a severe problem at 5 GHz, is diminished. If off-chip IRF's were used, only a single-ended realization would be feasible [1] because of RF pin count. Finally, a new broad-band low-power clock-distribution network, relying on low-loss 100-Ω differential transmission lines and a resistive power splitter, allowed for the integration of a low-phase noise *LC* VCO, without increasing the RF pin count.

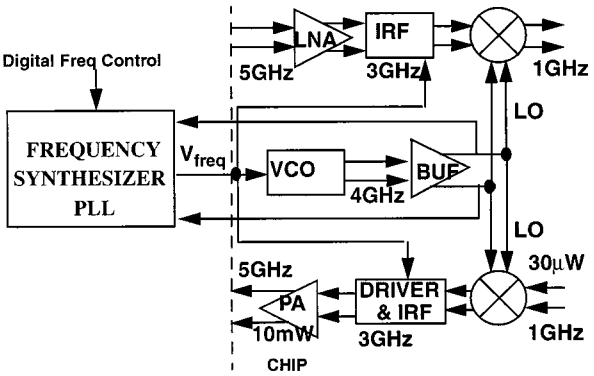

Fig. 1. Block diagram of the single-chip 5-GHz transceiver.

II. Chip Architecture and Schematics

Fig. 1 shows a block diagram of the new SiGe HBT radio transceiver chip together with an external synthesizer. The chip contains an *LC*-tuned 1–5-GHz transmitter, a 5–1-GHz receiver, and a shared 4-GHz varactor-tuned *LC* VCO. Varactor-tuned 3-GHz IRF's are integrated into both the transmitter and receiver. The IRF's remove the image signal by notch rejection [4]. The notch frequency tuning is designed to track the on-chip

Manuscript received October 28, 1999.

M. A. Copeland is with Nortel Networks, Ottawa, Ont., Canada K1Y 4H7, and is also with Carleton University, Ottawa, Ont., Canada K1Y 4H7.

S. P. Voinigescu, D. Marchesan, P. Popescu, and M. C. Maliepaard are with Nortel Networks, Ottawa, Ont., Canada K1Y4H7.

Publisher Item Identifier S 0018-9480(00)00858-9.

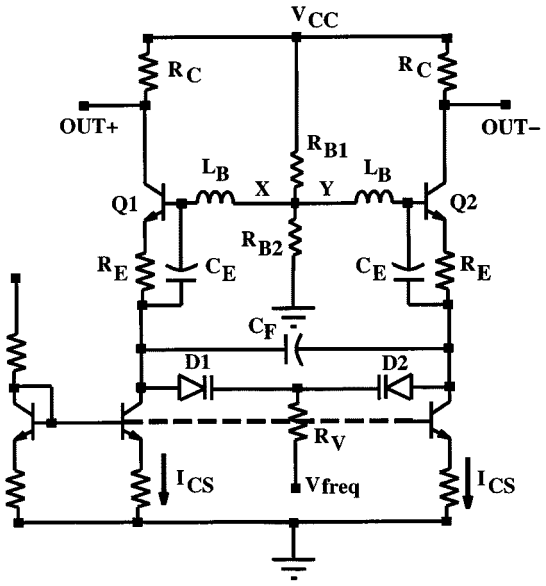

Fig. 2. VCO schematic.

VCO over 350 MHz with 1-GHz separation, allowing for a fixed IF of 1 GHz. The receiver IF output at 1 GHz would be followed in a conventional superheterodyne receiver by off-chip channel-select filtering and perhaps a second IF. However, we propose final integration of the receiver using IF sampling with a bandpass $\Delta\Sigma$ analog-to-digital converter (ADC) [5]. This would remove the need for precise analog filters and be the final step to a fully integrated one-chip radio.

Fig. 2 shows the schematics of the VCO core. It has a differential varactor-tuned *LC* Colpitts topology in common-base configuration, with two inductors [6] and, in addition, with resistive emitter degeneration R_E to suppress harmonics and to reduce up- (down-) converted noise. The VCO core is buffered by a differential amplifier (not shown), which provides the interface to the impedance-matched on-chip LO distribution network. The clock-distribution network consists of a 100-Ω differential resistive Wilkinson power splitter, which feeds two sets of differential transmission lines conveying the LO signal to the up- and down-convert mixers in the transmitter and receiver, respectively. Each transmission line has 100-Ω characteristic impedance with layout optimized using n^+ ground planes to reduce losses while maximizing characteristic impedance [7]. A large characteristic impedance is highly desirable in order to reduce the power dissipation in the line termination resistors, which must be provided both in the upconverter and downconverter. The LO distribution transmission lines are 1–1.2-mm long and can cause significant reflections of the third harmonic of the LO if they are not adequately matched beyond 12 GHz.

The fully differential receiver, shown schematically in Fig. 3, has 14 on-chip inductors and contains a 5-GHz tuned low-noise amplifier (LNA), which drives an RF- and IF-tuned double-balanced mixer [8]. Points X and Y, where the receiver IRF is connected, are indicated in the figure. For testing purposes only, the 1-GHz IF signal is extracted via a separately biased differential buffer with 50/100-Ω single-ended/differential impedance matching. The buffer, with a voltage gain of one, was designed to allow for more than 1-V swing per side so as not to degrade the linearity of the receiver. In order to avoid cluttering the schematics, the IF output buffer and IRF schematics are not shown. This receiver architecture with tunable IRF has the benefit of lower noise and lower power in comparison with recent receivers relying on image reject I-Q mixers [9], [10].

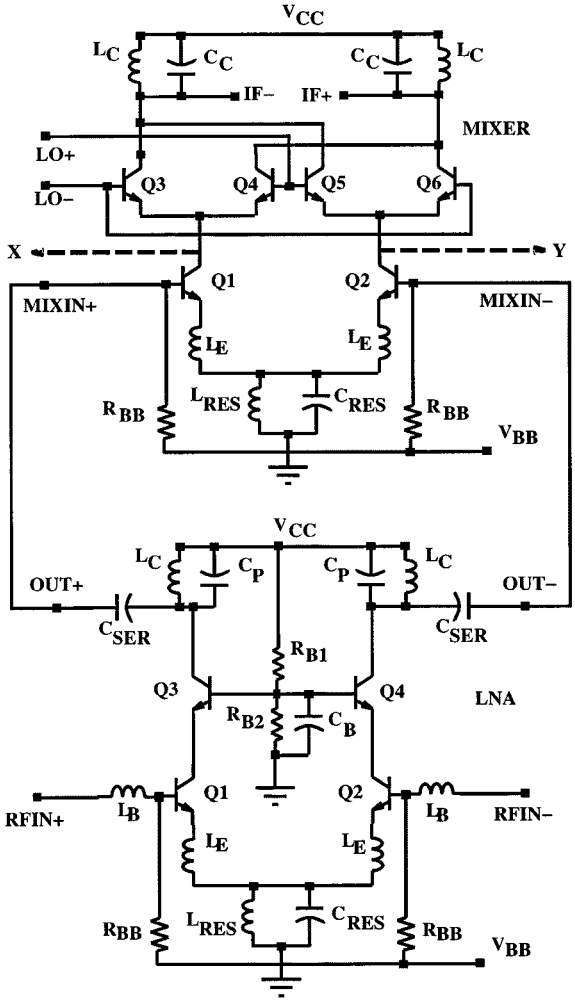

Fig. 3. Receiver schematics.

The fully differential transmitter of Fig. 4 features 17 on-chip inductors and a double-balanced 1–5-GHz upconvert mixer, followed by a 5-GHz driver amplifier and a linear PA stage. Points X and Y show where the transmitter 3-GHz IRF is connected. The outputs of the upconverter, driver, and PA are *LC* tuned at 5 GHz. The bias currents through the differential upconverter, driver, and PA are 4 , 10, and 85 mA, respectively.

III. Circuit Design Issues

This section describes the key design solutions that made possible the realization of the RF transceiver front end. First, the new method is presented of achieving monolithic tracking of the IRF's on the transceiver, so that more than 40 dB of image rejection, tunable over 350 MHz, is achieved on-chip over a 20-MHz wide channel. Circuit-level details of the VCO and tracking IRF implementation will be given. Second, a description of the input and interstage impedance- and noise-matching techniques employed for the differential building blocks will be addressed.

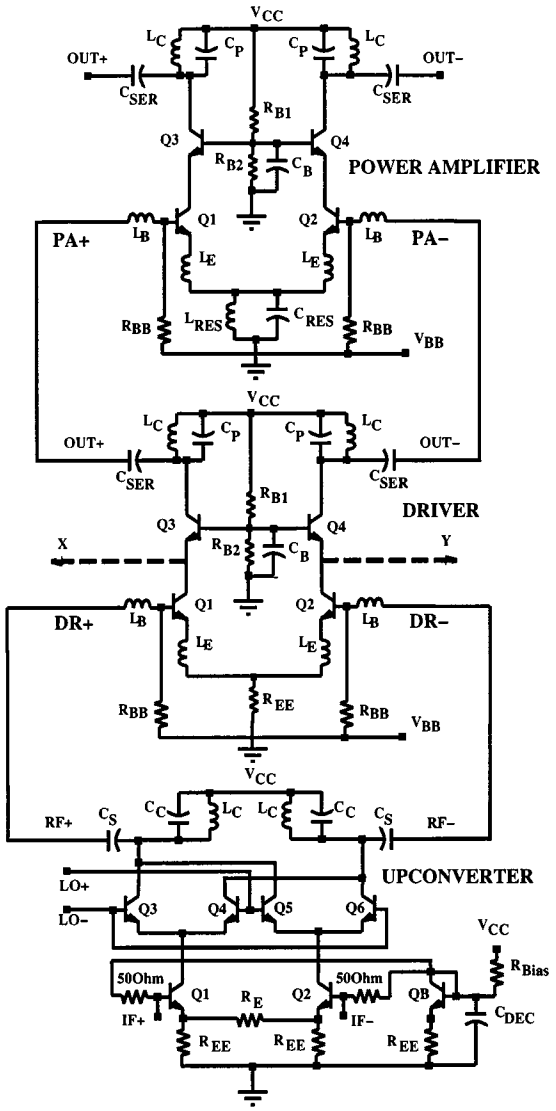

Fig. 4. Transmitter schematics.

Third, common mode and harmonic suppression are discussed, as well as the stability of differential circuits with inductor-matching networks, inductor degeneration, and common-mode resonant *LC* tanks. The modeling issues concerning passive devices and distributed interconnect parasitics, as well as the iterative simulation methodology used in the chip design, are explained. Finally, critical layout aspects that have led to the successful integration of the transceiver chip without compromising performance are overviewed.

A. VCO–IRF Tracking

The system-level diagram of the chip was shown in Fig. 1, along with a frequency synthesizer (to the left-hand side of the dashed line). The synthesizer was not integrated on this chip, although it would be practical to do so [11], [12]. In order to make monolithic tracking possible, the same basic circuit topology was employed for the resonators in both the IRF's and the VCO. The low-frequency VCO control voltage that is developed automatically by the feedback loop in the frequency synthesizer, V_{freq} in Fig. 1, can then be used to control the frequency of the resonators in the IRF's as well. Since the IRF and VCO resonators match, as the LO frequency is set digitally in the frequency synthesizer ("Digital Freq Control" in Fig. 1), the image reject frequency would, in principle, automatically track the RF frequency so as to maintain a fixed IF frequency. The same *LC*-varactor resonant circuit architecture as in the VCO of Fig. 2 was used for the IRF's, except that one end of the inductors, points X and Y in Fig. 2, were disconnected and were instead connected differentially inside stages of the transmitter and receiver, points X and Y in Figs. 3 and 4, to realize the notch filters. The basic IRF principle is to form a differential series resonator with negative resistance control (via the bias current I_{CS} in Fig. 2), such that points X and Y looking into the inductors of Fig. 2 exhibit zero resistance at series resonance. These points are then connected appropriately to other circuits so as to shunt current to ground at the desired notch frequency.

Discussing the receiver first, the series resonances of X and Y were connected to the emitters of a Gilbert cell mixer quad, as shown in Fig. 3. This gave a substantial improvement over an earlier receiver implementation [4], where an additional amplifier stage was needed between the LNA and mixer to provide an insertion point for the notch filter. That led to an unfavorable linearity/noise figure tradeoff because of the extra gain. In the implementation of this paper, on the other hand, the more usual connection of an LNA/mixer combination was achieved (from LNA collector tank to RF inputs of the mixer), while there was sufficient gain from the receiver input to the mixer quad so that input referred noise arising from the notch resonators was insignificant. Further, nonlinear (e.g., second harmonic) effects at the notch resonators caused by the LO drive to the mixer were found, through both simulation and measurement, to have no discernible impact on the linear behavior of the notch filter. Representative frequencies for the receiver are: RF: 5 GHz, VCO: 4 GHz, and image frequency: 3 GHz, for a 1-GHz IF.

Since the VCO and IRF frequencies are 1-GHz apart, the matching between their two similar topology resonators is lost, to a degree. For example, a tuning range of 350 MHz requires a smaller percentage variation of total capacitance in the VCO as compared to the IRF. Thus, the VCO requires a larger relative component of fixed capacitance (i.e., C_F in Fig. 2). Since the capacitance structures used in the two cases are different, good modeling of strays is vital to get good tracking. Other factors which also affect the design for tracking are as follows.

1) In the VCO, the bias current I_{CS} of the bipolar junction transistor (BJT) pair $Q1$ and $Q2$ must be set to higher values, e.g., 2–2.5 mA, to cause oscillation, while in the IRF's, a lower bias current, e.g., 0.7–0.8 mA, is desired for maximum notch depth. The base-to-emitter capacitances will, therefore, be different for the two cases. This problem is solved by adding a fixed capacitance C_E, as shown.
2) In the VCO, points X and Y are at a perfect virtual ground for difference mode, while in the IRF, these points are connected to the emitters of the mixer quad, which have some finite capacitance and resistance to ground. The common-mode behavior of the two resonators is also different since, in the VCO, X and Y

have high common-mode impedance through the bias resistors R_{B1} and R_{B2}.

3) The inductors in the VCO, being at higher frequency than in the IRF's, are closer to self resonance (for the same size inductor) and, hence, good modeling of inductors is important beyond just linear scaling.

Moving on to the transmitter schematic of Fig. 4, the IRF here is used to attenuate the image caused by the mixing of the 1-GHz transmit IF and the 4-GHz LO. The desired RF is 5 GHz and the image is 3 GHz, as in the receiver. The same resonators as in Fig. 2 are used, but points X and Y are connected to the emitters of the common-base BJT pair in a cascode driver stage between the transmit mixer and the PA, as shown in Fig. 4, again, so as to provide a short circuit to ground for image frequency currents. There are necessary differences in the IRF resonator design from the receiver case, as a result of the larger power requirements that make the emitter capacitance and resistance loading the series IRF resonator different.

B. Input and Interstage Noise and Impedance Matching

Cascode stages with inductive emitter degeneration L_E are used in differential configurations in the receiver and transmitter, as shown in Figs. 3 and 4. The cascode stage has the advantage of low current and very good input–output isolation, allowing for the independent optimization of the input and output matching networks. The inductive degeneration provides excellent linearity and low noise without the penalty of a dc voltage drop, and also gives very good circuit performance over temperature and process variation, unlike resistors and capacitors. On the down side, inductors are difficult to model prior to fabrication when there are no measured data for model fitting. Also, for stability reasons, it is critical that the inductor model be accurate up to frequencies above the third harmonic of the RF signal and certainly up to at least its self-resonance frequency.

On-chip conjugate matching, consisting of inductors L_C, L_B (when necessary), capacitors, C_P, C_{SER}, and interconnect transmission lines, is used between the LNA and mixer (Fig. 3), and between the upconverter, driver, and PA (Fig. 4). The interstage networks are individually optimized. While this complicates the design process, which becomes iterative, it does bring the benefit of maximizing the power gain with minimum power dissipation. In addition, in the receiver, conjugate matching between the LNA and mixer ensures that the noise-figure contribution of the mixer is minimized. To further reduce bias currents and power dissipation for a given voltage swing and linearity requirement, the interstage impedance levels are maximized. The maximum impedance level possible is limited to 200–400 Ω by the Q of the collector resonant *LC* tank loads. This is a fundamental limitation to on-chip power reduction.

Optimal transistor sizing and the inductive emitter degeneration are employed in concert for simultaneous noise and input-impedance matching in both the LNA and mixer [8]. Series, partly bondwire and partly on-chip inductors (L_B) are used at the inputs of the LNA to tune out the reactive part of the input and noise impedances. No external matching components are required at the chip boundaries since the matching is entirely provided by on-chip and bondwire inductances. The low-noise design of the mixer and LNA allows for the optimal partitioning of gain across receiver blocks in order to maximize receiver linearity without degrading the overall noise figure [8]. The higher noise figure is the major disadvantage of broad-band image-reject I-Q mixers relying on a pair of mixers loading the LNA output [9], [10].

There are several differences compared to the design presented in [8]. First of all, in order to simplify testing and for possible single-ended use, the single-ended (unused input terminated in 50-Ω input impedance of the differential LNA was designed to be 50 Ω. With an ideal (infinite impedance) common-mode current source, this would result in a differential mode impedance of 50 Ω, and a half-circuit impedance of 25 Ω. However, because a finite impedance $L_{\rm RES}$-$C_{\rm RES}$ tank, tuned on the second harmonic, was used for common mode and even harmonic rejection, it was found by simulation and confirmed through differential S-parameter measurements, that the half-circuit input impedance should be 30 Ω instead of 25 Ω. The resultant difference mode impedance is 60 Ω. Therefore, the size and bias current, i.e., 4 mA, of transistors $Q1$ and $Q2$ of the LNA (Fig. 3) were chosen appropriately (twice as large as in the design of [8]) in order to provide coincident noise and input impedance match for a single-ended source impedance of 50 Ω. Secondly, in order to minimize layout area and reduce the number of inductors, the mixer input impedance is complex, with the real part approaching 150 Ω per side. Again, the size and bias current, i.e., 1.5 mA, of transistors $Q1$ and $Q2$ in the mixer (Fig. 3) were designed so as to provide simultaneous noise and impedance match to the complex output impedance of the LNA. The total current drawn by the differential LNA and mixer core is 11 mA. An extra 14 mA is drawn by the bias circuit and by the 100 Ω per side matching network seen at the LO inputs of the mixer. A 50-Ω LO distribution network would have doubled the bias current through the matching resistors.

C. Common Mode and Harmonic Rejection and Stability Issues

Odd-order currents generated by nonlinearity, e.g., in the input transistors of a differential pair, cause difference mode voltages in the output, while even order harmonics cause common-mode-type voltages. Therefore, it is important that the differential circuits have good common-mode and even-mode rejection, as well as be unconditionally stable in common mode. In principle, the even-order components will be cancelled in a differential output if the common-mode impedance seen in the emitters of the differential pairs $Q1, Q2$, in Figs. 3 and 4 is large. The topology used in the present radio design, featuring *LC* collector tanks and a common-mode $L_{\rm RES}$-$C_{\rm RES}$ tank tuned on the second harmonic, ensures that dc common-mode signals and offsets, as well as signals at the second harmonic, are suppressed. The differential amplifiers employed have a gain of zero at dc and good common-mode rejection up to the second harmonic of the RF signal. However, at frequencies above this, the common-mode rejection is reduced and common-mode instabilities can occur. Indeed, time-domain simulation in the progress of this design, in particular, after extraction of layout parasitics, showed that the presence of even-order harmonics

could significantly reduce the signal swing range of the desired difference-mode signals.

The potential instability arising beyond the self-resonance of the emitter degeneration inductors is due to the resultant negative resistance at the base input of the differential pairs in Figs. 3 and 4. There is a similarity with the Colpitts oscillator used in this paper [6], which oscillates because capacitance from the emitter to ground appears as negative resistance to base currents [13]. Looking at the equivalent situation in differential amplifier stages, any capacitance from the emitters of the differential pair to ground can act similarly. For example, in the PA of Fig. 4, the inductors L_E can appear capacitive to base currents at high frequency, causing difference and common-mode stability problems. In addition, in common mode, the collector–substrate capacitance of transistor current sources and interconnect capacitance can create common-mode negative resistance and, hence, instability. The $L_{\rm RES}$-$C_{\rm RES}$ resonant tanks employed for common mode and second harmonic rejection also become capacitive above resonance, generating common-mode negative resistance at the base of $Q1$ and $Q2$ in the LNA, mixer, and PA. Therefore it is imperative to use small-signal linear-frequency simulation to check the common mode, as well as the difference mode stability at frequencies beyond the third harmonic of the RF signal. This was necessary in the present design since, after parasitic interconnect extraction, potential instabilities were noticed at 14 GHz in the transmitter and at 25 GHz in the receiver. In order to ensure unconditional common-mode stability, the Q of the $L_{\rm RES}$–$C_{\rm RES}$ tanks was reduced by adding a resistance in series with the capacitor so as to suppress its capacitive effect above its resonant frequency. In the transmitter driver (Fig. 4), the original transistor-based current source was replaced with the resistor $R_{\rm EE}$ for similar reasons.

D. Simulation Issues

In the face of all the above issues, it is demanding to guarantee stability and achieve accurate tracking, i.e., to keep the notch centered well enough to automatically reject the image frequency as the transmitter and receiver RF frequency is changed. The accuracy of computer-aided design (CAD) tools for a reliable design at these frequencies has not generally been achieved in the past. Precise modeling of parasitic capacitances within transistors, fixed capacitors, and varactors is required, as well as in transmission line and inductor models. We have been able to achieve this to a considerable degree. A new design infrastructure and methodology has been developed [7], [14], which gave first-pass success of the chip in IBM's SiGe technology [2].

During the design process, extensive resimulations were performed, first to get the general range of active and passive device parameters on initial design, and then to adjust the design, in particular, inductor and metal–insulator–metal (MIM) capacitor values, for better tracking and stability in the light of predicted parasitics arising from extraction of the actual first layout. For example, in the receiver, modeling the interconnect as transmission lines rather than as lumped capacitance to substrate has typically led to a 5% reduction in the resonant frequency of *LC* tanks and has shifted the optimal input and noise impedance matching frequency. This has been accounted for in the design.

The chip was statistically simulated over process variations after layout extraction, including parasitic distributed interconnect. In retrospect, the statistical simulations gave a fairly optimistic estimate of process spread. It turned out that appropriate best/worst corner simulations [7] were much closer in capturing the actual process spread with less simulation time. At the moment, the inductor models are not scalable, causing problems in the best/worst case, as well as in statistical simulations. Variations in inductor characteristics (mostly in parasitic capacitances and Q) are not captured for that reason. HSPICE was used to perform all simulations: small-signal S-parameters, LNA noise figure, large-signal transient, and fast Fourier transform (FFT) of the whole transceiver performance. The receiver noise figure, as well as the differential and common-mode stability, were simulated at schematic level using SpectreRF. Lack of suitable scalable transmission-line models at the time of this design made SpectreRF unusable for final extracted layout simulations. HSPICE was employed for that purpose.

E. Layout Issues

Substrate tie-downs were used in conjunction with trenched n-wells and ample first metal ground planes to reduce cross coupling through the substrate. Each circuit block was surrounded by a sufficiently wide guard ring made of the above combination. Wide low-inductance top metal lines over first metal planes were used to provide bias supply. Appropriate resonance-free MIM-capacitor based decoupling was provided on each supply line. Such isolation and bias decoupling techniques are critical for achieving spurious-free and stable operation of the single-chip radio. In addition, in order to reduce the noise generated by the substrate resistance under the signal pads, and in order to isolate them from the substrate, a salicided n-well is placed under the signal pad. The n-well is grounded outside the pad, thus forming a reverse-biased junction with the substrate. The pad behaves like an ideal high Q (> 20 at 26 GHz) capacitor. This solution provides as high a Q as a pad with first metal ground plane under it, but with much lower capacitance. A typical 60×60 μm^2 pad has 28-fF capacitance and is usable beyond 40 GHz [7].

IV. Fabrication and Technology Characterization

The radio transceiver was fabricated in IBM's SiGe HBT technology. All 33 inductors, multistrip varactors, MIM capacitors, and most multistrip transistors were custom designed for this particular chip. No prior device models or measured data were available. In order to interpret the experimental results and to close the loop on the accuracy of the device models and circuit synthesis methodology, a large number of circuit breakouts and device structures were also fabricated and measured. Transistor f_T and $f_{\rm max}$ characteristics are shown in Fig. 5 as a function of collector current, as measured in our laboratory on a fast wafer. The f_T and $f_{\rm max}$ were obtained from the intercept of the current gain $H_{21}(f)$ and unilateral power gain $U(f)$ characteristics, respectively, based on on-wafer S-parameter measurements in the 0.1–110-GHz range. A two step deembedding technique was employed, relying on on-wafer open and shorted pad structures. Pad (25×40 μm^2) capacitance was 10 fF, the input and output

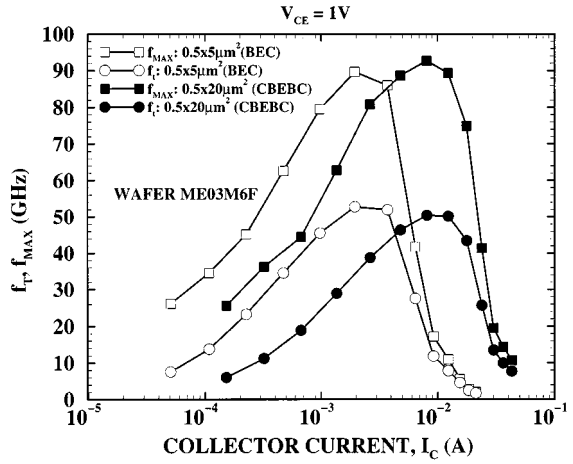

Fig. 5. Measured f_T and $f_{\max}$ as a function of collector current for $0.5 \times 5\ \mu m^2$ and $0.5 \times 20\ \mu m^2$ transistors at $V_{CE} = 1$ V. BEC signifies one base, one emitter, and one collector contact geometry. CBEBC signifies collector–base–emitter–base–collector contact geometry.

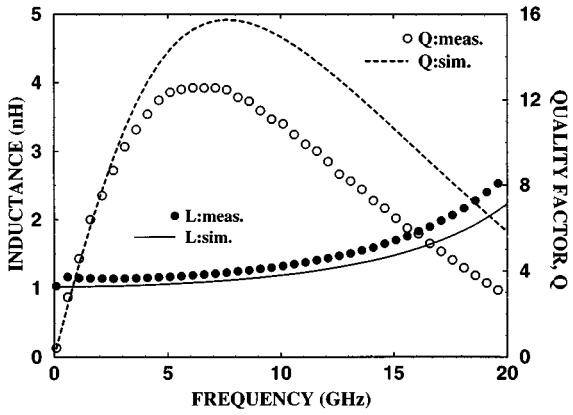

Fig. 6. Typical inductor characteristics as a function of frequency.

lead inductances were 30 pH, and the ground inductance was 5 pH. The reduced capacitive, inductive, and resistive parasitics of the transistor fixture and deembedding structures ensured that even the smallest devices ($0.5 \times 1\ \mu m^2$) could be accurately measured. The available power gain of the deembedded transistors was typically 6 dB at 40 GHz. The appropriate number of base and collector contacts for multistrip transistors ensured that, as the collector current scales with transistor size, both f_T and $f_{\max}$ remained constant, as illustrated in Fig. 5.

Measured characteristics of the VCO tank inductor are shown in Fig. 6 as a function of frequency. The peak Q is above 12 at 5–6 GHz and remains higher than 11 in the tuning range of the VCO oscillation frequency. The simulated characteristics are also plotted for comparison. The model underestimated the inductance by 10% in the 0–20-GHz range and overestimated the Q by more than 20% above 5 GHz, due to the inadequate modeling of substrate losses. The model was not fitted to the measured data, as this would have defeated the purpose of inductor synthesis. In general, for all inductors, the measured inductance was 5%–10% higher than the model prediction, the error being larger for devices with wider metal strips, typically used in the transmitter, due to the larger power levels and bias current requirements.

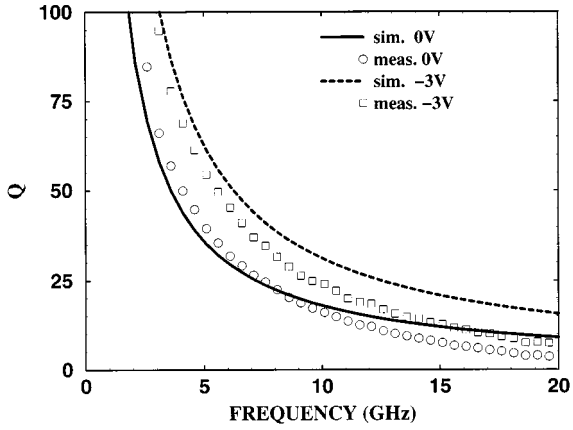

Fig. 7. Multistrip varactor quality factor.

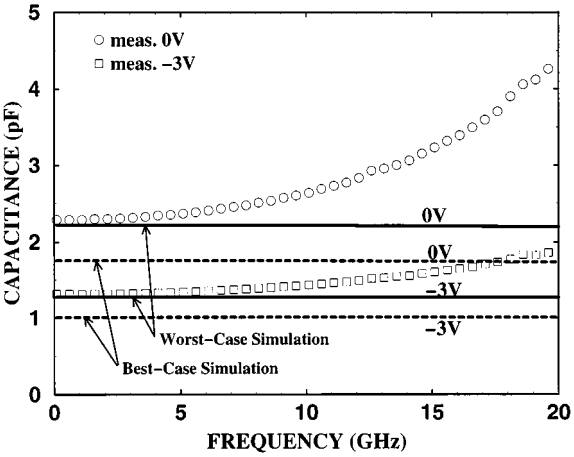

Fig. 8. Multistrip varactor apparent capacitance as a function of frequency.

Varactor diode $Q(f)$ and $C(f)$ characteristics, obtained from S parameter measurements, are shown in Figs. 7 and 8, respectively, for 0 and 3 V reverse bias. The interdigitated device, similar to the one used in the VCO tank, has 25 strips, each $2.8 \times 20\ \mu m^2$, sharing the same trenched well in order to reduce the parasitic capacitance to the substrate and the series resistance, thus maintaining a high Q. The measured Q remained above 20 up to 10 GHz, throughout the useful bias range. The simulated best- and worst-case $C(f)$ characteristics are also shown, suggesting that the measured data falls just outside the worst-case process corner, which represents maximum tolerated capacitance values. This result was also confirmed by measurements of the transistor base–collector junction capacitance, which was 15%–20% higher than nominal on this particular batch. Inductive effects, signaled by the increase of the measured apparent capacitance at frequencies beyond 5 GHz, were not captured by the present varactor model.

Fig. 9 illustrates the measured Q and resonant frequency as a function of control voltage and temperature for the half-circuit of the VCO tank containing an inductor, MIM capacitor, and multistrip varactor. In order to characterize the resonator performance, the S parameters were measured between 3 and 5 GHz with 20-MHz steps for each varactor bias. The resonant frequency was obtained from the peak, and the Q was calculated from the 3-dB half-window, respectively, of the magnitude of the

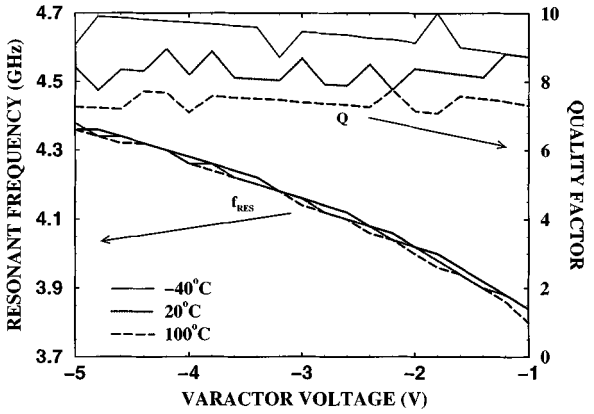

Fig. 9. Measured Q and resonant frequency as a function of control voltage and temperature for the half-circuit of the VCO tank containing an inductor, MIM capacitor, and multistrip varactor.

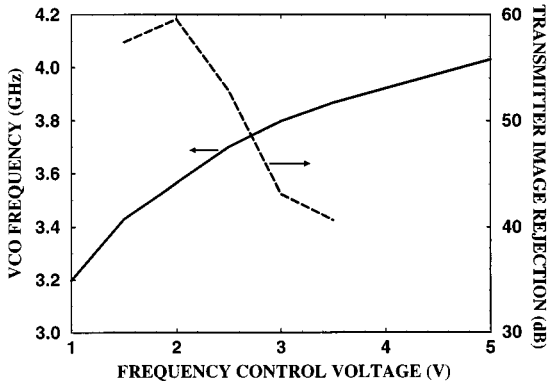

Fig. 11. VCO frequency and transmitter image rejection as a function of the frequency control voltage simultaneously applied on the control pads of the VCO and of the transmit IRF. Typical control range is 1.5–3.5 V. The VCO power changes less then 1.2 dB across the whole tuning range.

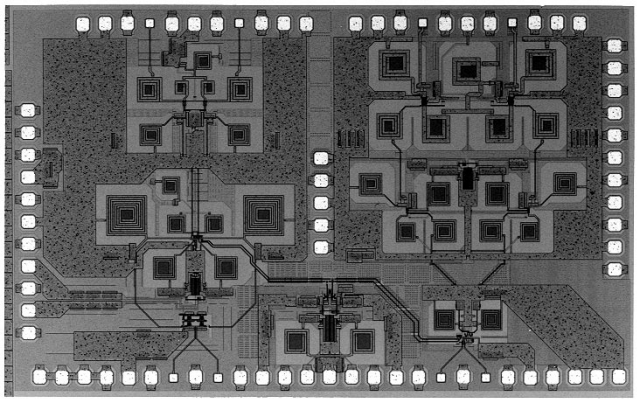

Fig. 10. Transceiver micrograph showing the receiver at the left, transmitter at the right, and VCO at the bottom. The 5-GHz differential RF ports are at the top while the 1-GHz IF ports are at the bottom.

measured tank impedance. The Q of the tank, around 7.5 at 20 °C, is practically independent of the varactor control voltage and changes by 20% over the whole temperature range −40 °C to +100 °C. The tank Q is dominated by the inductor and its ohmic losses, the latter being a function of temperature. This suggests that the phase noise of the VCO is a very weak function of the control voltage. The resonant frequency of the tank changes in the range −40 °C to +100 °C by only 20 MHz, and 40 MHz, for varactor voltages of −5 V and −1 V, respectively. Also, results based on a partial wafer mapping carried out on three wafers from two different batches showed 10–20-MHz variations in the VCO frequency, demonstrating that the resonant frequency of on-chip *LC* tanks has low sensitivity to both temperature and in-batch process variations. Even though there is practically no process spread on inductor values, the present process margin for varactor capacitance (allowing over 20% variation) needs to be significantly reduced if large-scale production of VCO's is to be achieved without having to select "nominal" wafers.

V. Experimental Performance of the Transceiver Chip

The transceiver chip photomicrograph, with an area of 4.2 mm × 2.6 mm, is shown in Fig. 10. Stand-alone versions of the transmitter, receiver, and buffered VCO were also fabricated and tested individually. In general, all large-signal receiver, transmitter, and VCO measurements were carried out on the transceiver chip. Small-signal S-parameter and noise measurements were performed on individual transmitter and receiver chips, without the VCO.

A. VCO

The measured tuning range of the buffered VCO, included on the transceiver chip, is larger than 350 MHz for the nominal control voltage range of 1.5–3.5 V, as illustrated in Fig. 11. Fig. 12 shows the measured single-sided phase noise of a stand-alone buffered version of the VCO as −100 dBc/Hz and −128 dBc/Hz, at 100-kHz and 5-MHz offsets, respectively, from a 3.91-GHz carrier. This performance is superior to that of recent similar or lower frequency monolithic VCO implementations [6], [15]. A double-conversion scheme was used in the measurement with an HP4352B phase meter and an HP70427A downconverter having an IF of 300 MHz, as displayed. Phase noise measurements were found to be very sensitive to the type of bias supply used. Best results were obtained with the internal low-noise bias supply source of the phase noise meter. The impact of emitter degeneration resistors R_E was also investigated. The lowest phase noise was obtained with an emitter degeneration resistor of 10 Ω. The buffered output power is adjustable up to −6 dBm. The VCO core itself requires 5 mA, while the buffered version draws a total of 20 mA from a 3.5-V supply.

B. Receiver

The receiver large —signal performance was measured on the transceiver chip with the on-chip VCO on, working under nominal bias current conditions. Fig. 13 shows the large signal IF output power as a function of the input power when the signal was applied and extracted single-ended. The input compression point is −22 dBm and the single-ended gain is 19 dB. The gain was increased by 2 dB, with a commensurate decrease in the input compression point, when the VCO output power was increased. This demonstrates that, as verified in simulation, the receiver linearity is limited by the IF output swing and, hence,

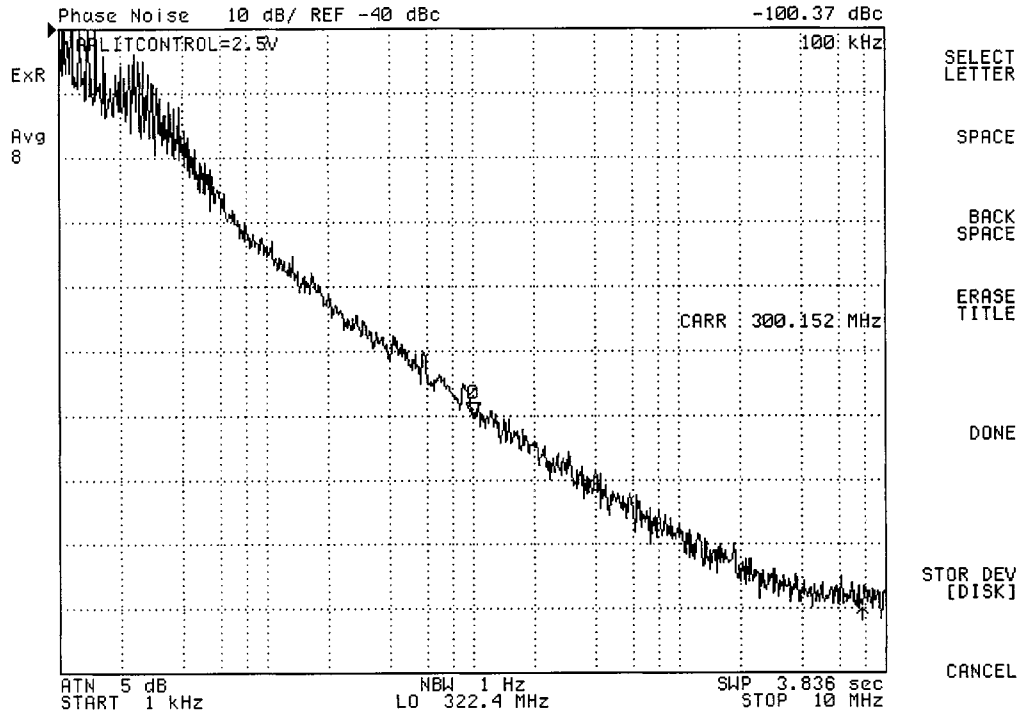

Fig. 12. Measured VCO phase noise at 100-kHz offset from the 3.91-GHz carrier. A double-conversion scheme was used in the measurement with an HP4352B phase meter and an HP70427A downconverter having an IF of 300 MHz, as displayed.

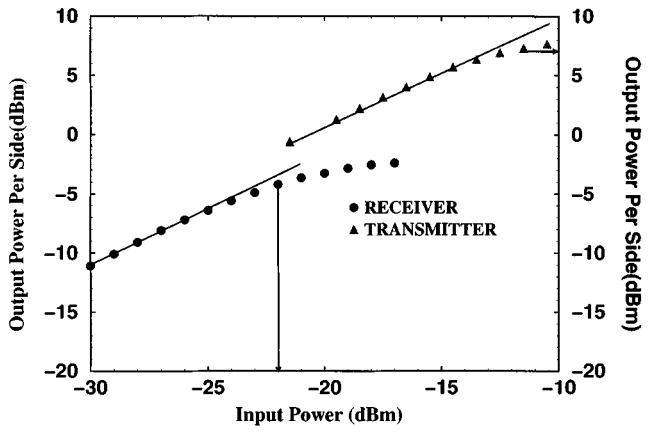

Fig. 13. Transceiver 1-dB compression point measurement with on-chip VCO. The signal is applied and extracted single-ended. The unused input and output are terminated in 50 Ω.

by the supply voltage. The inductive degeneration and bias currents of the mixer and LNA are high enough to not compromise linearity.

Fig. 14 (top) shows the measured receiver spectrum at a single-ended IF output. The 1-GHz IF signal power is −20 dBm, downconverted from the −40 dBm 5-GHz RF signal. The largest spur, less than −50 dBm, is the second harmonic of the VCO. The LO signal leaking into the IF output is −58 dBm. As a result of more than 65-dB isolation between the receiver input and output, the RF signal is attenuated below the −80-dBm noise level. Fig. 14 (middle) demonstrates the receiver single-ended image rejection. The IF signals from four separate measurements are superimposed. First, a 1-GHz IF signal of about −20 dBm is obtained with an RF signal at 5 GHz. Three image signals are then applied around 3 GHz within a 20-MHz band and each corresponding IF signal level is recorded. More than 40-dB image rejection, tunable over 350 MHz, is achieved on chip over a 20-MHz-wide channel. The image rejection is 50 dB for narrower channels, as shown in the figure. The measured LO-to-RF isolation is better than 70 dB, as illustrated in Fig. 14 (bottom).

Small-signal S-parameter measurements were carried out on a receiver-only chip in order to determine the input and output matching of the receiver (the presence of the VCO precludes S-parameter measurements on the transceiver chip). The downconvert mixer was biased as an amplifier with dc bias on the LO inputs such that only half of the mixing quad is active. The results, shown in Fig. 15, indicate that the single-ended input and output return loss are better than 20 dB at 5 and 1 GHz, respectively. The tunability of the image rejection is once more demonstrated by the S_{21} curve. Notice that S_{21} is different from the real downconversion gain because the mixer is biased as an amplifier.

A single-ended single-sideband receiver noise figure of 5.9 dB was measured on the receiver chip with an external VCO. The differential receiver noise figure, which cannot be measured due to lack of suitable equipment, is expected to be 4.5 dB. This prediction is based on the simulated difference of 1.4 dB between the single-ended and differential noise figure of the LNA. Simulation indicates that the differential noise figure should be equal to the noise figure of the half circuit. The measured noise figure of the LNA half-circuit (Fig. 16) is 2.6 dB, 0.4 dB larger than simulation. The single-ended noise figure of the differential LNA, measured in 50 Ω is 4.2 dB,

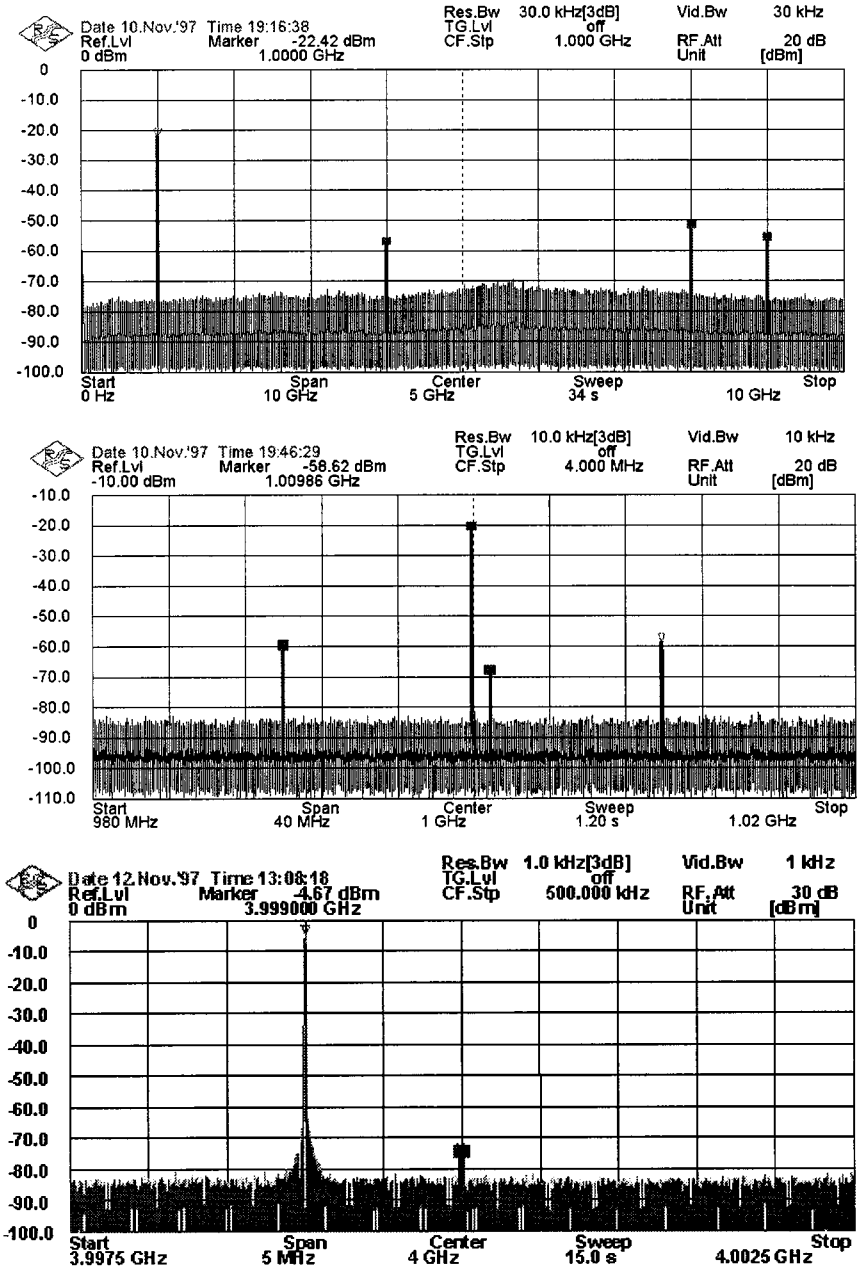

Fig. 14. Top: Receiver single-ended IF spectrum showing the 4-GHz LO, 1-GHz IF, 8- and 9-GHz spurs. Middle: Receiver IF output showing 40-dB image rejection over a 20-MHz channel bandwidth obtained by sweeping the frequency of an image signal applied around 3 GHz. Bottom: Receiver LO-to-RF leakage with two superimposed traces: i) output spectrum of the external LO set at 3.999 GHz and -4.67 dBm. ii) RF leaking signal of -76 dBm at a single-ended RF input with the LO tuned to 4 GHz.

0.7 dB higher than simulation, and only 0.1 dB larger than the measured minimum noise figure. These results indicate that the contribution of the mixer and output buffer to the overall receiver noise figure is only 1.7 dB, confirming the good noise and interstage matching between the mixer and LNA, as well as the low-noise design of the mixer. All the noise-figure data mentioned here refer to the receiver and LNA with full on-chip matching. The packageable versions of the receiver and LNA have lower noise due to the fact that part of the input inductor is provided by the higher Q bondwire. It was found through measurements that each inductor L_B at the input of the LNA contributes 0.6 dB to the noise figure.

To support the discussion in Section III on the differential and single-ended input impedance and noise matching, an SPTS-4 system from ATN Microwave Inc., Billerica, MA, was used to measure the single-ended and differential S-parameters of a stand-alone LNA and its half-circuit. The results are shown in Fig. 17.

C. Transmitter

The output compression point of the transmitter is $+7$ dBm per side (Fig. 13). From this figure, one can deduce that the single-ended gain is 20 dB. Fig. 18 shows typical transmitter small-signal power gain and isolation curves obtained from

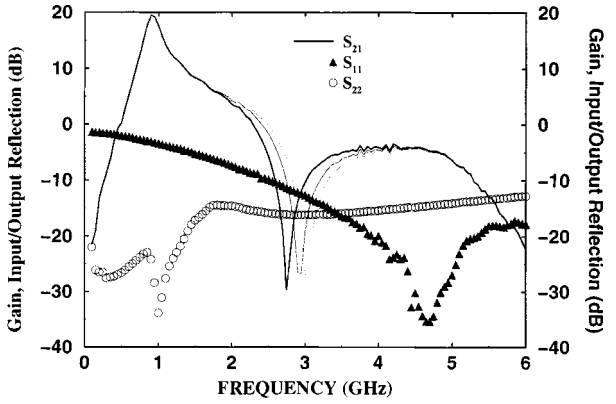

Fig. 15. Receiver single-ended S-parameters. The IRF control has been set at 1.5 2.5, and 3.5 V to demonstrate tunability. The LO inputs to the mixer have 0.4-V dc differential bias.

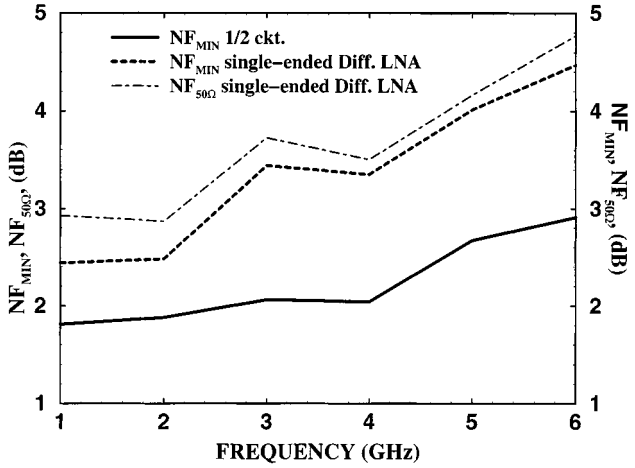

Fig. 16. Measured noise figure in 50 Ω and the minimum noise figure of single-ended differential and half-circuit LNA's.

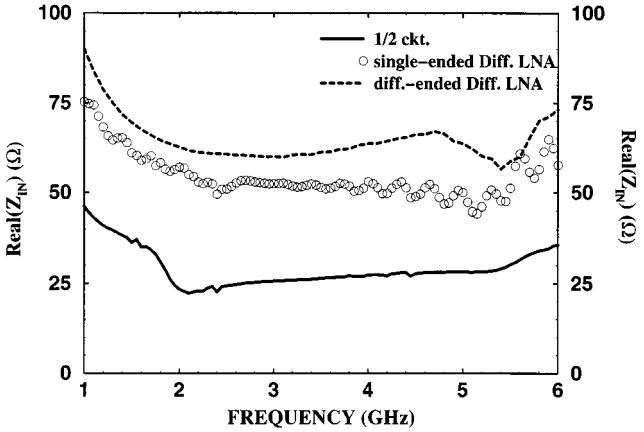

Fig. 17. Real part of the input impedance of the differential LNA, measured single-ended (one input terminated with 50-Ω resistor) and differentially, and the measured input impedance of the LNA half-circuit.

S-parameter measurements. Here, the mixer of the transmit side of Fig. 1 was biased as an amplifier, as in the receiver case, by applying dc bias on the LO inputs. The IF input was swept from 0 to 10 GHz. The RF–IF isolation in the transmitter is higher than 75 dB up to 10 GHz, the measurement being limited

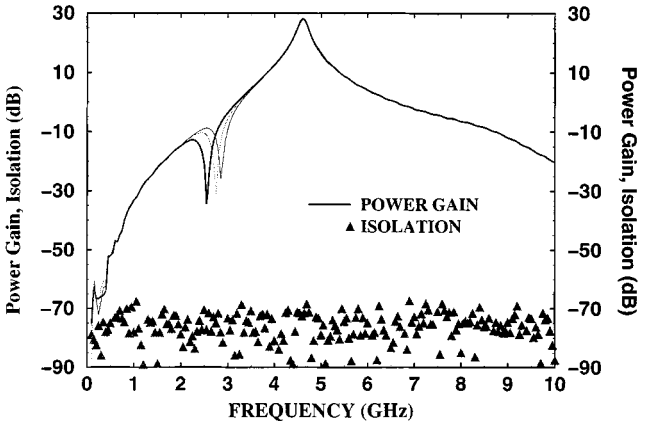

Fig. 18. Transmitter single-sided gain and isolation. The IRF control has been set at 1.5, 2.5, and 3.5 V. The LO inputs to the upconverter have 0.4-V differential bias.

by the dynamic range of the network analyzer. The isolation is at least 10 dB better in the transmitter than in receiver because of the insertion of wider n-well–p^+-junction isolation regions. The resonance peak in the gain, at 4.65 GHz, is 12.3% below the design goal of 5.225 GHz. The center of the tunable notch is also 12% below the notch frequency goal of 3.225 GHz. The discrepancy is attributed mostly to a systematic under prediction at this stage of the on-chip inductances and varactor capacitance, as discussed in Section IV. However, the tracking behavior is much better than the systematic behavior, as shown in Fig. 11. It is noteworthy that, although the actual resonant frequencies achieved were systematically low, the VCO and IRF tracked very well. With careful tuning of notch depth and IRF frequency control voltage, 70 dB of image rejection of the upconverter 3-GHz image was achieved. When the VCO and IRF frequency inputs were joined and the voltage tuned from 1.5 to 3.5 V, the image rejection stayed at 40 dB over the 20-MHz range, as shown in Fig. 11. A further 30–40 dB of rejection is provided by the off-chip duplexer filter. In addition to the image suppression, all other spurs are more than 45 dB below the carrier, even with single-ended output.

The transceiver operates from a 3.5-V supply and, with the buffered VCO on, draws 125 mA in transmit mode and 45 mA in receive mode. Table I summarizes the transceiver performance. All measurements reported here have been performed on-wafer using multiple wedge probes. Separate packageable versions of the transmitter and receiver have also been fabricated to be used in applications where the transmitter and receiver are simultaneously on.

VI. Conclusions

These results, including VCO noise, demonstrate that W-CDMA compliance is achievable at 5 GHz with a fully integrated transceiver in cost-competitive Si-based technology. Measured on-chip isolation is better than 75 dB up to 10 GHz and remains above 60 dB up to 26 GHz, suggesting that integrating the low-frequency part of a complete radio is feasible without crosstalk problems. The linearity, image rejection, and noise figure of the transceiver make it versatile enough to

TABLE I
TRANSCEIVER PERFORMANCE

Parameter	Value
RX Noise Figure (Single-Ended)	5.9 dB Single Side-Band
RX Input Compression Point	-22 dBm
RX Conversion Gain (Single-Ended)	19 dB
RX on-chip Image Rejection	> 40 dB
RX LO-RF Isolation	>70 dB
RX LO-IF Isolation	>50 dB
RX RF-IF Isolation	>65 dB
VCO Phase Noise (at 100KHz, 5MHz)	-100 dBc/Hz, -128dBc/Hz
VCO tuning range (1.5V to 3.5V)	350 MHz
TX Output Compression Point	+10 dBm
TX Conversion Gain (Single-Ended)	20 dB
TX Image Rejection	> 40 dB
TX IF-RF Isolation	> 75 dB
TX LO-RF Isolation	> 40 dB
RX+VCO Bias Current	45 mA
TX+VCO Bias Current	125 mA

permit various types of modulation and coding schemes such as Gaussian multiple shift key (GMSK), QPSK, and CDMA. For applications requiring higher output power, an external PA must be provided. In order to make the radio transceiver design possible, accurate CAD design tools and a reliable design methodology for high-gigahertz-range Si analog narrow-band circuits were developed, including on-chip tracking IRF filters, accurate prediction in the simulation of distributed passive parasitics, interstage noise and impedance matching, common mode and harmonic rejection, and common-mode stability. Considering that this was the first run of such a design, the first complete exercise of the design methodology, and the first system level chip we have fabricated in the IBM SiGe process, the design methodology has been successful. We believe that we have demonstrated that, with enough rigor, it is possible to do first-pass narrow-band high-speed circuit design.

ACKNOWLEDGMENT

The authors appreciate the discussions on simulation and integration issues with their colleagues Dr. Y. Greshishchev and Dr. P. Schvan, and would also like to thank R. Hadaway for his support and IBM for technology access.

REFERENCES

[1] M. Madihian, T. Drenski, L. Desclos, H. Yoshida, H. Hirabayashi, and T. Yamazaki, "A 5-GHz-band multifunctional BiCMOS transceiver chip for GMSK modulation wireless systems," *IEEE J. Solid-State Circuits*, vol. 34, pp. 25–32, Jan. 1999.

[2] S. P. Voinigescu, M. A. Copeland, D. Marchesan, P. Popescu, and M. C. Maliepaard, "5 GHz SiGe HBT monolithic radio transceiver with tunable filtering," in *RFIC Symp. Dig.*, 1999, pp. 131–134.

[3] M. Barberis, "Designing W-CDMA Mobile Communication Systems," *Commun. Syst. Design*, pp. 25–32, Feb. 1999.

[4] J. Macedo, M. A. Copeland, and P. Schvan, "A 2.5 GHz silicon image reject filter," in *Proc. CICC*, 1996, pp. 193–196.

[5] W. Gao and W. M. Snelgrove, "A 950 MHz second-order integrated *LC* bandpass DS modulator," in *Proc. VLSI Circuits Symp.*, 1997, pp. 111–112.

[6] L. Dauphinee, M. A. Copeland, and P. Schvan, "A balanced 1.5 GHz voltage controlled oscillator with an integrated LC resonator," in *IEEE ISSCC Dig.*, 1997, pp. 390–391.

[7] S. P. Voinigescu, D. Marchesan, J. L. Showell, M. C. Maliepaard, M. Cudnoch, M. G. M. Schumacher, M. Herod, G. E. Babcock, P. Schvan, and R. A. Hadaway, "Process- and geometry scalable bipolar transistor and transmission line models for Si and SiGe MMIC's in the 5–22 GHz range," in *Proc. IEDM*, 1998, pp. 307–310.

[8] S. P. Voinigescu and M. C. Maliepaard, "5.8 GHz and 12.6 GHz Si bipolar MMICs," in *IEEE ISSCC Dig.*, 1997, pp. 372–373.

[9] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, and K. Halonen, "A wide-band direct conversion receiver for WCDMA applications," in *IEEE ISSCC Dig.*, 1999, pp. 220–221.

[10] J. R. Long and M. Maliepaard, "A 1 V 900 MHz image-reject downconverter in 0.5 μm CMOS," in *IEEE CCICC Dig.*, 1999, pp. 665–668.

[11] W.-Z. Chen and J.-T. Wu, "A 2 V 1.6 GHz BJT phase-locked loop," in *IEEE CCICC Dig.*, 1998, pp. 563–566.

[12] N. M. Filiol, T. A. D. Riley, C. Plett, and M. A. Copeland, "An lower ISM band frequency synthesizer and GMSK modulator," in *Proc. SCIRC'97*, pp. 60–63.

[13] G. D. Vendelin, A. M. Pavio, and Ulrich L. Rhode, *Microwave Circuit Design*. New York: Wiley, 1990, ch. 6, p. 409.

[14] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1430–1439, Sept. 1997.

[15] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz CMOS voltage-controlled oscillator," in *IEEE ISSCC Dig.*, 1999, pp. 402–403.

Miles A. Copeland (M'65–SM'85–F'89) received the B.Sc. degree in electrical engineering from the University of Manitoba, Winnipeg, Man., Canada, in 1957, and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, Ont., Canada, in 1962 and 1965, respectively.

From 1965 to 1996, he was a Professor with the Department of Electronics, Carleton University, Ottawa, Ont., Canada. He is currently retired and an Emeritus Professor, continuing with graduate student supervision, and consulting with Nortel Networks, Ottawa, Ont., Canada.

Sorin P. Voinigescu (M'90) received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, Ont., Canada, in 1994. His Ph.D. dissertation discussed the design and fabrication of VLSI compatible Si/SiGe p-MOSFET's.

From 1984 to 1991, he worked in research and development and academia in Bucharest, Romania, where he designed and lectured on microwave semiconductor devices and microwave integrated circuits. In 1994, he joined Nortel Networks, Ottawa, Ont., Canada, where he has been responsible for projects in high-frequency characterization and statistical scalable compact-model development for Si, SiGe and III–V heterostructure devices. His current duties involve coordinating the modeling infrastructure development and prototyping of wireless and broad-band fiber-optic transceivers in emerging semiconductor technologies. He has authored or co-authored over 25 refereed technical papers spanning the simulation, modeling, design, and fabrication of GaAs- and Si-based heterostructure devices and circuits. He holds two U.S. patents in these areas.

David Marchesan (M'96) received the B.A.Sc. degreee from the University of Waterloo, Waterloo, Ont., Canada in 1993, and the M.Sc. degree from McMaster University, Hamilton, Ont., Canada in 1995, both in physics.

In 1995, he joined the Microelectronics Group, Nortel Networks, Ottawa, Ont., Canada , where he has been involved in silicon-based wireless radio-frequency integrated-circuit/monolithic-microwave integrated-circuit (RFIC/MMIC) circuit design and the high-frequency modeling and characterization of integrated passive components and bipolar transistors. His current area of interest is high-speed analog circuit design for next-generation fiber-optic transceivers.

Petre Popescu (A'95) graduated from the Polytechnic Institute of Bucharest, Bucharest, Romania.

In 1987, he joined Nortel Networks, where he is currently Senior Advisor of high-speed IC design. His current interests are in high frequency and high-speed IC architectures.

Mr. Popescu is a member of Quebec Order of Engineers (OiQ).

Michael C. Maliepaard (M '89) received the B.Sc. degree from the Queen's University Kingston, Kingston, Ont., Canada, in 1985, and the Ph.D. degree from Cambridge University, Cambridge, U.K. in 1989, both in physics.

In 1989, he joined Nortel Networks, Ottawa, Ont., Canada, as a Reliability Physicist in their Silicon Process Technology Department, where his work focused on providing electrostatic discharge (ESD) protection, latch-up immunity, and hot-carrier characterization for CMOS and BiCMOS processes. He also provided design, modeling, and characterization of EPROM and fuse PROM core cells. After a period involved with parametric yield issues for the Silicon Laboratory, he joined the Technology Alliances Department, where he has led projects to evaluate external technologies for both wireless and broad-band applications. His research interests include high-performance benchmark circuit design and measurement, and high-performance semiconductor technology definition.