

A 20-GHz InP–HBT Voltage-Controlled Oscillator With Wide Frequency Tuning Range

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Abstract—This paper presents the design and implementation of a 20-GHz-band differential voltage-controlled oscillator (VCO) using InP heterojunction-bipolar-transistor process technology. Aimed at 20- or 40-Gb/s fiber-optic applications, the design is based on a single-stage feedback amplifier with no intentional L or C . The salient features of the proposed VCO are wide frequency tuning range compared to LC oscillators, and low power consumption and transistor count compared to ring-oscillator counterparts. The implemented VCO has an adjustable frequency range from 13.75 to 21.5 GHz and provides two complementary outputs. Total power consumption at 18.6 GHz is 130 mW, while the phase noise is -90.0 dBc/Hz measured at 1-MHz offset frequency.

Index Terms—Differential stage, heterojunction bipolar transistor, high-speed circuit, indium phosphide, phase noise, SONET, voltage-controlled oscillator.

I. INTRODUCTION

THE ever-increasing demand for bandwidth in data communication systems, e.g., synchronous optical networks (SONETs), has motivated research on very high-speed devices and circuits. A new generation of optical carrier systems designed for data rates of 20 Gb/s, 40 Gb/s, and higher are beyond the reach of today's silicon CMOS or conventional bipolar processes. Indium–phosphide (InP) technology offers an attractive choice for high-speed optoelectronic integrated circuits (OEICs) due to its higher speed and the availability of optoelectronic transducers (E/O, O/E) compatible with fiber-optic systems. InP heterojunction bipolar transistors (HBTs) exhibit device f_T exceeding 150 GHz and benefit from low-loss and low-parasitic interconnects due to the semiinsulating substrate.

Due to their material properties, InP-based HBTs have several advantages over their GaAs-based counterparts. The merits include higher peak and saturated electron velocities, resulting in lower parasitic resistances and shorter transit times, low V_{BE}

turn-on voltage and useful current gain at very low-current densities. Moreover, with 50% larger thermal conductivity, InP HBTs generally exhibit lower sensitivity of device parameters to temperature, resulting in lower self-heating under bias. Other features of InP HBTs are low $1/f$ noise corner frequency down to 10 kHz, a key feature for many low phase-noise applications, and high-efficiency devices for creating oscillators [1]–[3]. Another feature in modern InP HBTs is the removal of collector material beneath the base layer, resulting in a cantilevered base layer resting upon a pedestal-like collector layer [4], [5]. This removal of excess collector material under the base layer (i.e., base undercut profile) greatly reduces the base–collector capacitance C_{BC} .

The InP process considered in this paper provides high-speed NPN HBTs with a single 1.5- and 2- μm -wide emitter strip, while emitter lengths are scalable from 2 to 20 μm . Unity current gain frequency (f_T) of the HBTs peaks at a collector current density, which is also the maximum allowable current density for these devices. Maximum collector–emitter breakdown voltage is about 3 V. At a typical collector current density of 0.7 mA/ μm^2 and collector–emitter voltage of 1.2 V, estimated f_T is about 100 GHz. Two metallization layers are available for interconnections with a minimum metal pitch of 7 μm . Lossy transmission lines consisting of top-metal 75- μm semiinsulating InP substrate and backside ground plane can also be used. Other available components in this technology are NiCr resistors, metal–insulator–metal (MIM) capacitors, and Schottky diodes. All active and passive components have process- and geometry-scalable models [6] with built-in parasitic elements (RLC) and self-heating and breakdown models for the HBTs.

This paper presents the design and implementation of a differential InP–HBT voltage-controlled oscillator (VCO) suitable for a 20- or 40-Gb/s (OC-768) SONET/synchronous digital hierarchy (SDH) system. The VCO must operate over process and temperature variations and exhibit a wide adjustable frequency range. VCOs with center frequencies of 20 and 40 GHz are two options for a 40-Gb/s system, depending on the architecture used for clock and data recovery. A 20-GHz design is employed here. The design must be fully differential to provide two outputs with 180° phase difference and low skew and jitter. The two complementary outputs can be used with two parallel latches to re-time the data stream on both positive and negative clock transitions, effectively creating a 40-Gb/s data interface. The proposed VCO can be used in clock-and-data recovery phase-locked loop (PLL) (receive side), as well as clock synthesizer (transmit side) of a fiber-optic system. At a specified

Manuscript received March 30, 2001. This work was supported by the Natural Sciences and Engineering Research Council of Canada, by Micronet, by Nortel Networks, by Gennum, by Mitel, and by PMC-Sierra Inc.

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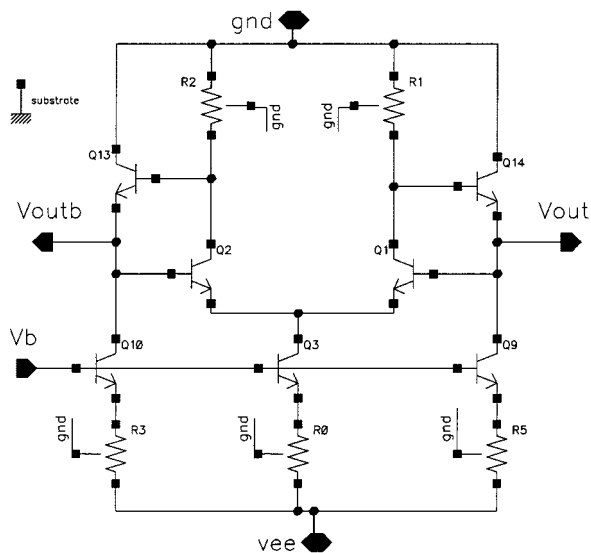


Fig. 1. Differential VCO with common-collector feedback.

supply voltage of -3.3 V, the VCO maximum power consumption must not exceed 200 mW.

In Section II of this paper, the design details of the proposed wide tuning-range differential VCO is described. Section III presents the experimental results, and is followed by a conclusion in Section IV.

II. WIDE TUNING-RANGE VCO DESIGN

The VCOs proposed here are fully differential and are based on the use of regenerative feedback applied to a differential amplifier. The idea is to obtain 180° frequency-dependent phase shift within a single-stage differential cell relying on poles and right-half-plane (RHP) zeros obtained in a cascode configuration followed by emitter-follower buffers. To create the positive feedback, another 180° phase shift is obtained by swapping the differential feedback lines from the output to the input of the amplifier. The proposed circuit can be treated as a feedback amplifier, or as a *single-stage* ring oscillator. Ultrafast InP HBTs push the main pole of the amplifier to a very high frequency, effectively close to secondary poles and RHP zeros, thus making it possible to achieve 180° phase from the differential cell at a frequency where small-signal gain is above 0 dB. In this manner, a *short* ring oscillator is realized with a single buffered stage; hence, saving on power consumption, device count, and die area.

Fig. 1 shows the schematic of the simplest n-p-n-only differential oscillator core. This core oscillator consists of a differential input pair (a common-emitter pair) cascaded through an emitter-follower buffer. HBTs with emitter width of $1.5\text{-}\mu\text{m}$ and emitter lengths of 6- to $15\text{-}\mu\text{m}$ have been used in this circuit. In order to comply with the maximum current limit, the HBTs are biased around $0.7\text{ mA}/\mu\text{m}^2$, i.e., at a level safely below their peak- f_T point. Also, in order to avoid breakdown, maximum V_{CE} is maintained at 2 V for dc quiescent point design and 3.3 V when signal swing is considered. The simple structure of this oscillator results in a very high oscillation frequency above

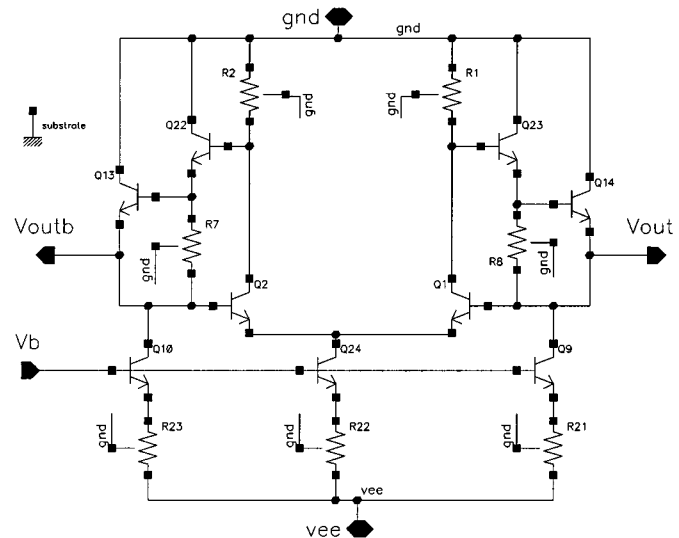


Fig. 2. Differential VCO with Darlington-pair feedback.

40 GHz. However, maintaining oscillation over a moderate frequency range is a difficult task due to insufficient phase shift around the loop. This factor causes oscillation to fail when this circuit configuration is implemented with conventional (lower speed) bipolar transistors [7]. Simulations for the InP oscillator of Fig. 1 show that a 5% tuning range can be obtained based on typical process models and a -3.3-V power supply.

In order to improve the loop phase condition necessary for oscillation, a Darlington pair can be used in the feedback network in cascade with the common-emitter amplifier, as shown in Fig. 2. The delay introduced by the extra transistor in the Darlington pair improves the phase condition to the point where a 30% tuning range is achieved around the midband oscillation frequency. Naturally, the addition of a delay element in this loop results in a reduction of the maximum oscillation frequency. Simulations indicate that the maximum oscillation frequency of the core oscillator in Fig. 2 is approximately 30 GHz.

Another way of introducing excess phase or delay in a single-stage differential cell is to add a transistor pair in the gain section of the loop. A suitable approach is to add an extra HBT in a common-base configuration to the collector of each common-emitter HBT to form a cascode configuration, as shown in Fig. 3(a). Both C_{BE} and C_{CE} of the common-base transistor play a major role in the loop phase, compared to the previous circuit (Fig. 2) where mainly the C_{BE} of the extra transistor in the Darlington pair was increasing the delay around the loop. Similar to the previous two core oscillators, this oscillator was simulated with its respective layout parasitics using the HSPICE scalable models developed for the InP HBTs. Simulations reveal that the core oscillator of Fig. 3(a) achieves a 50% tuning range, while maximum oscillation frequency is just a few gigahertz less than the maximum frequency achieved in the Darlington-based oscillator of Fig. 2. Robust oscillation is maintained under all simulated process models and temperature variations; as a result, this circuit was chosen for implementation and is studied in detail throughout the remainder of this paper.

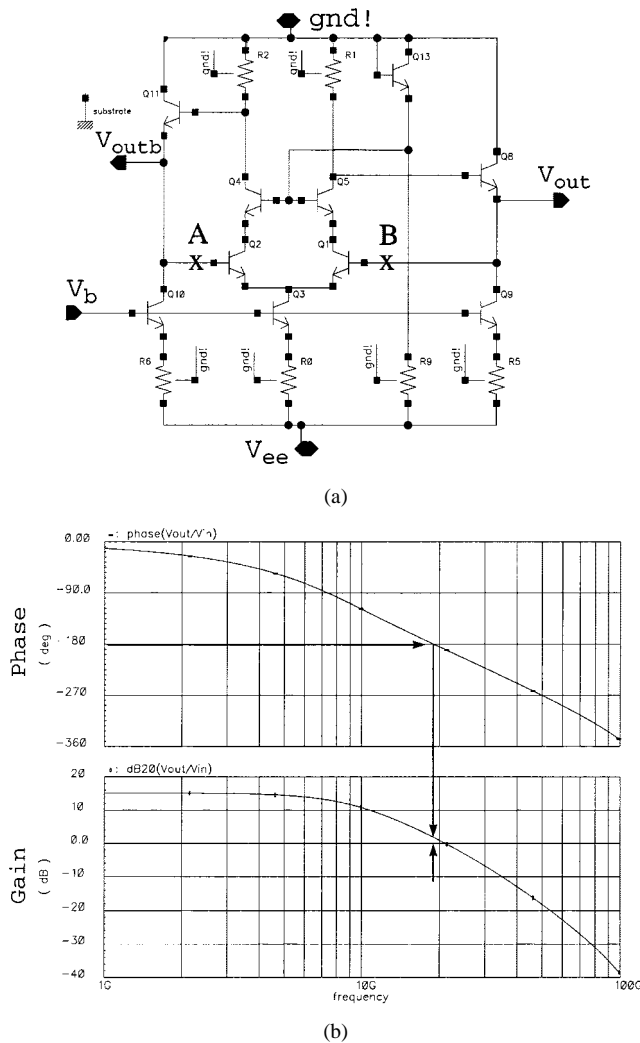


Fig. 3. (a) Differential cascode core oscillator. (b) Open-loop phase plot (top) and gain plot (bottom) of the differential cell in (a).

A. Core Oscillator

The selected core oscillator, shown in Fig. 3(a), consists of a differential common-emitter followed by common-base (cascode configuration) and an emitter-follower buffer pair. The simulated open-loop frequency response of such a differential cell for a midband control voltage is shown in Fig. 3(b). In the simulation, the differential cell is opened at points A and B [cf. Fig. 3(a)] and the outputs are loaded by a similar stage (in a feedback configuration, the cell is loaded by its own inputs). The loading effect of an output buffer stage is also included in the simulation. Fig. 3(b) reveals that a frequency-dependent phase shift of -180° occurs at about 19 GHz, while the small-signal gain at this frequency is around $+2$ dB. Therefore, the gain-phase conditions are achieved for oscillation startup around this frequency. Additional simulations indicate that when control voltage ($V_b - V_{ee}$) is swept from 0.9 to 1.1 V, the gain magnitude is increased and the 180° crossing point in the phase plot is shifted toward higher frequencies. The gain-bandwidth product is also increased.

The operation of the differential cell of Fig. 3(a) as an oscillator is guaranteed by the gain-phase condition. An increase in tail current increases f_T and the charging current of the parasitic

capacitances, thus increasing the frequency of the oscillation. This is achieved by increasing the control voltage that simultaneously boosts the tail current of the differential cascode, as well as the bias currents of the emitter-follower pair. The oscillator stabilizes at a frequency where *large-signal* gain is 0 dB. The oscillation frequency is determined through transient simulations that take into account large-signal nonlinear effects. For this circuit, the oscillation frequency in transient simulation is about 20 GHz.

B. Complete VCO Circuit

The complete VCO circuit, shown in Fig. 4, includes an input voltage-to-current (V/I) converter, the core oscillator, and a differential output driver stage. The input V/I converter, consisting of resistors and a diode-connected HBT, creates a reference current proportional to input control voltage. The reference current is mirrored to the tail current of the differential pair and to the bias current of the emitter-follower feedback HBTs. The output driver is a differential common-emitter amplifier with emitter degeneration driving $50\text{-}\Omega$ resistors both on- and off-chip (double-termination scheme). Thus, an equivalent load on the collector terminal of each HBT output driver is $25\ \Omega$. All capacitors shown in Fig. 4 are parasitics, backannotated from the layout, except for two MIM capacitors bypassing the power supply and the base of the cascode HBTs.

C. Layout and Simulations

The layout of the InP VCO consists of a symmetrical configuration of 13 HBTs, 13 NiCr resistors, and 2 MIM capacitors. The transistor count is one-third of that in a three-stage InP ring oscillator [8]. The VCO cell layout shown in Fig. 5(a) has a physical size of $620\ \mu\text{m} \times 318\ \mu\text{m}$, or about $0.2\ \mu\text{m}^2$. The effect of parasitic interconnect capacitors, i.e., metal1-substrate (M1-S), metal2-substrate (M2-S), and metal1-metal2 (M1-2) with or without an air bridge, is taken into account by extracting the area and perimeter of overlap geometries. The dominant component in most cases is the fringe (perimeter) capacitance. Through preliminary transient simulations of the VCO, those nodes with maximum *sensitivity to parasitic capacitance* (maximum $\Delta f/\Delta C$) were identified in the feedback loop and ranked accordingly. The physical layout was then optimized to minimize capacitance at the most sensitive nodes. Cross-coupling capacitance, especially important between adjacent nodes with 180° phase difference, was reduced by allowing enough distance ($d > 5\ \mu\text{m}$) between nodes on the same metal layer. Air-bridge structures were used as much as possible to minimize overlap capacitance between M1 and M2.

Fig. 5(b) shows the simulation testbench of the VCO. The output drivers are connected via on-chip wide (low-impedance) transmission lines (T-lines) to the output signal pads. The $50\text{-}\Omega$ resistors in the testbench represent external terminations, e.g., spectrum analyzer or power meter, while on-chip $50\text{-}\Omega$ NiCr resistors are included in the VCO on the collector of the output HBTs. The final circuit was characterized via backannotated (postlayout) transient simulations. A robust oscillation was sustained under all simulated process models (nominal, fast, slow) and control voltages varying from -2 to 0 V. Fig. 6 shows the simulated output frequency of the InP VCO versus control

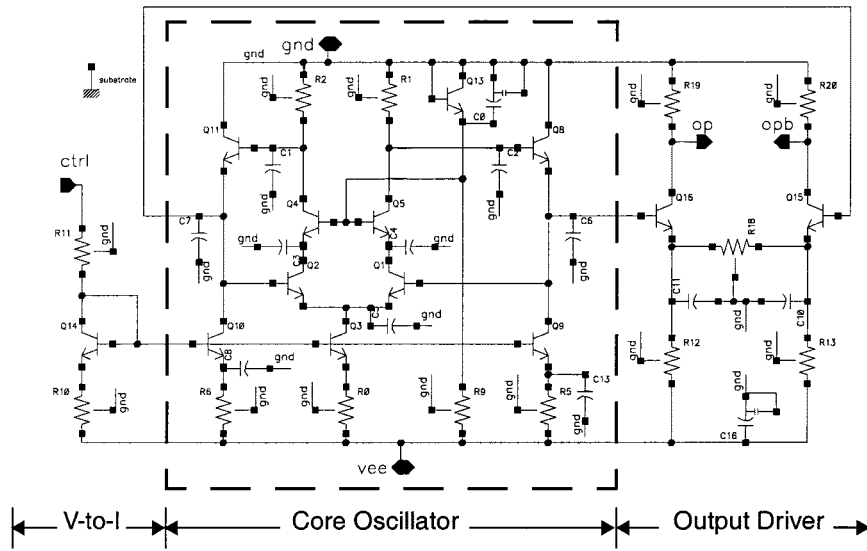
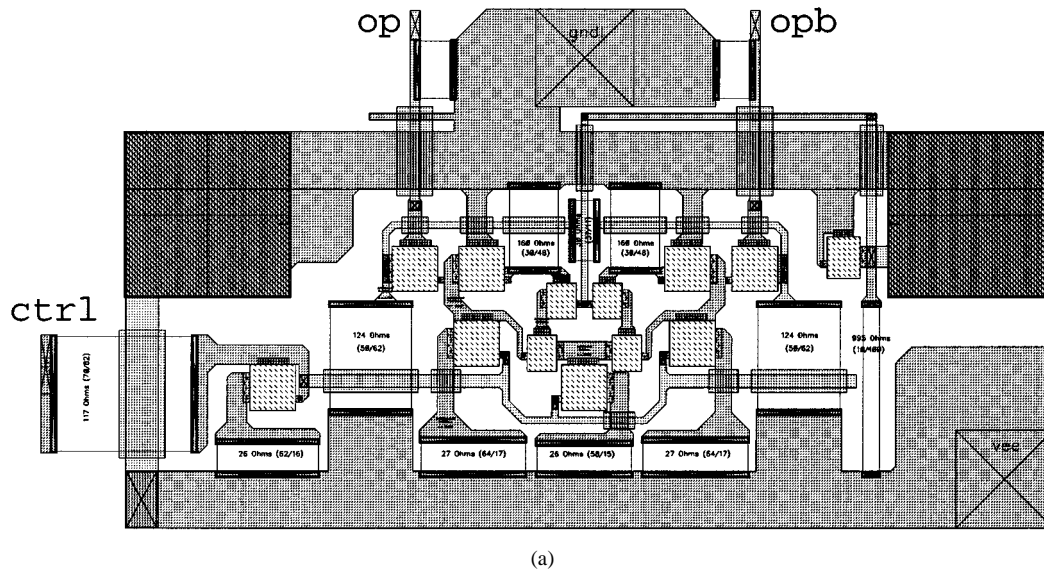
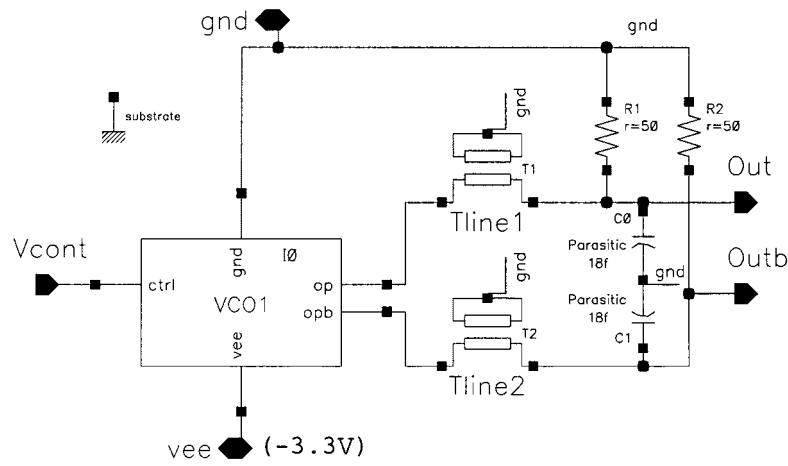


Fig. 4. Implemented differential VCO with cascode configuration.



(a)



(b)

Fig. 5. (a) Cell layout of the InP VCO. (b) Simulation testbench.

voltage based on nominal and corner models. Temperature simulations were performed in a range from 0 °C to 100 °C. While a

temperature rise decreases the output frequency, the oscillation is maintained at a fairly constant output amplitude. Peak-to-peak

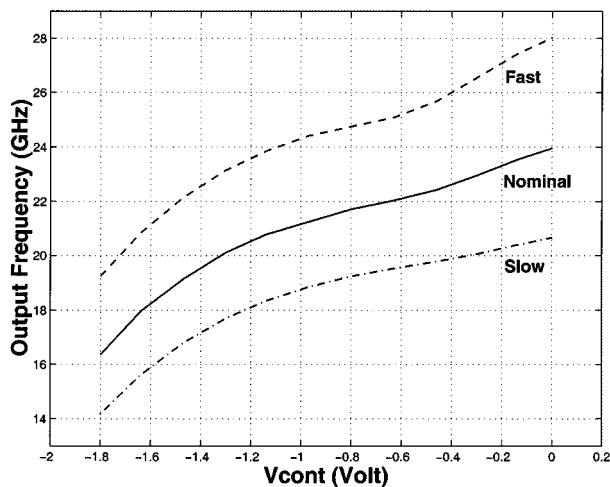


Fig. 6. Simulated frequency characteristics of the VCO over process models.

amplitude of an output node at midband varied from 460 to 425 mV when the temperature parameter (TEMPDC) was increased from 0 °C to 100 °C.

III. IMPLEMENTATION AND CHARACTERIZATION

The proposed wide-range VCO circuit was implemented using the InP-HBT process described in Section I. Fig. 7 (top) shows the die photomicrograph of the InP VCO. The implemented test chip contains two VCO circuits per die (with slight design variations in bias and supply), high-frequency signal pads, and standard pads for supply, ground, and control input. The signal pads have smaller size ($60 \times 60 \mu\text{m}^2$) and exhibit a capacitive loading under 20 fF. The die size is $1.2 \times 1.2 \text{ mm}^2$. A close-up view of an implemented InP VCO is shown in Fig. 7 (bottom). The testing was performed on-wafer using a $50\text{-}\Omega$ RF prober. Maximum frequency of oscillation of the VCO, measured on different InP wafers, varied from 18 to 23 GHz at a supply voltage of -3.3 V . Detailed measurements are presented here for an average die with maximum VCO frequency of 21.5 GHz. With a larger supply voltage of $V_{ee} = -4 \text{ V}$, a maximum frequency of 30 GHz was obtained.

Fig. 8 shows the measured output frequency (solid line) and output power (dashed line) of the InP VCO versus input control voltage. The measured output frequency was adjustable from 13.75 to 21.5 GHz using a control voltage of -1.8 to 0 V . The average gain of the VCO was about 4.3 GHz/V. The VCO exhibits a wide tuning range of 45% around its midband frequency, as compared to tuning ranges of 1%–15% reported for VCOs with LC-tuned [9] or multivibrator oscillators [3]. The two outputs have 180° phase difference. The measured power obtained at each output varied from to over the input control range, as compared to a typical midrange simulation of -3 dBm .

Fig. 9 shows the output spectrum of the VCO for a midband oscillation frequency of 18.56 GHz. The measured phase noise, as indicated on the spectrum, was -87.6 dBc/Hz at 1-MHz offset frequency [10] and with a slightly enhanced test setup, even better phase noise was obtained. Fig. 10 shows a plot of output phase noise versus offset frequency obtained while the

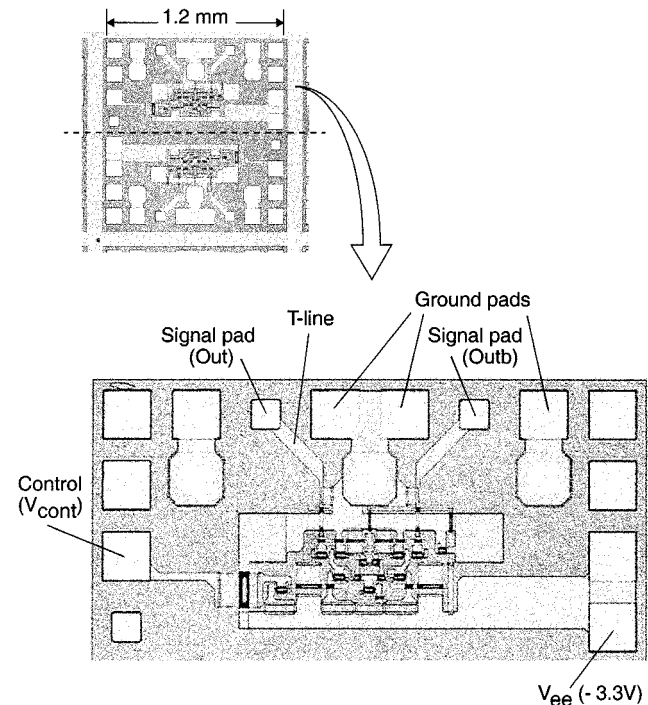


Fig. 7. Photomicrograph of the InP die (top). Close-up view of a VCO (bottom).

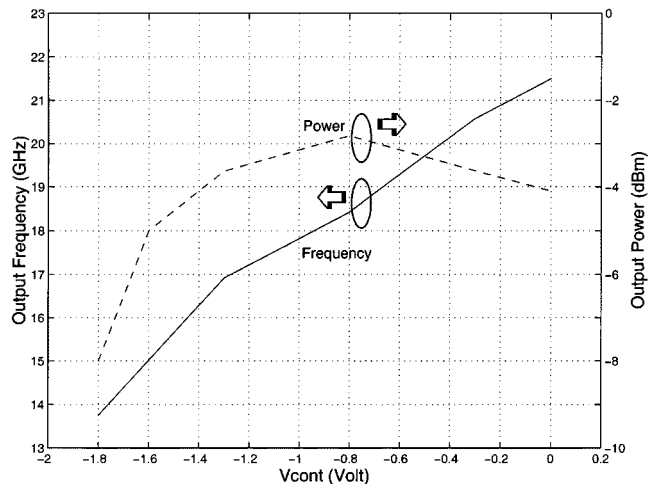


Fig. 8. Measured frequency of the VCO; measured power level (dBm) at each output.

VCO was running at 18.69 GHz. The measured phase noise at 1-MHz offset to the carrier was -90.0 dBc/Hz ; i.e., 2–3-dBc/Hz improvement in the phase noise. At 10-MHz offset frequency, the phase noise was -109.5 dBc/Hz . The phase noise is comparable to those reported for ring oscillators. A comparison between measurements and simulations indicates that the measured results lie between nominal and slow models.

The design proposed in this paper consists of 13 HBTs and dissipates 130 mW of power from a -3.3-V supply. The measurement done at 18.56 GHz includes power dissipation in the input control circuit, the VCO core, and the output drivers. The differential core has an approximate power consumption of 80 mW at center frequencies. By comparison to conventional

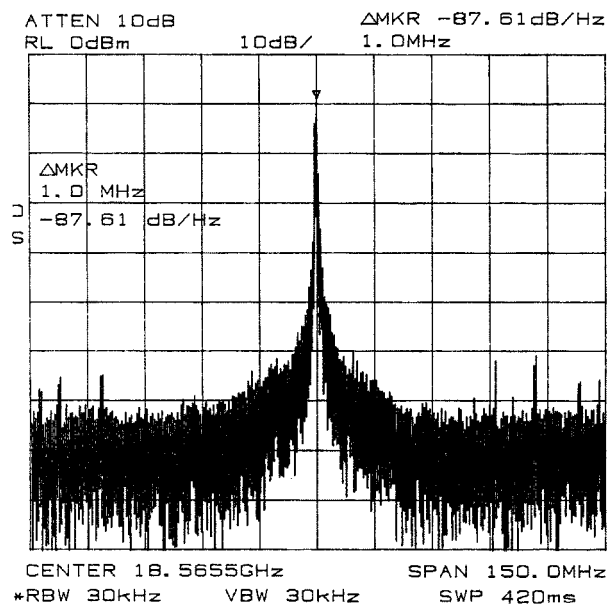


Fig. 9. Output spectrum of the VCO at 18.6 GHz.

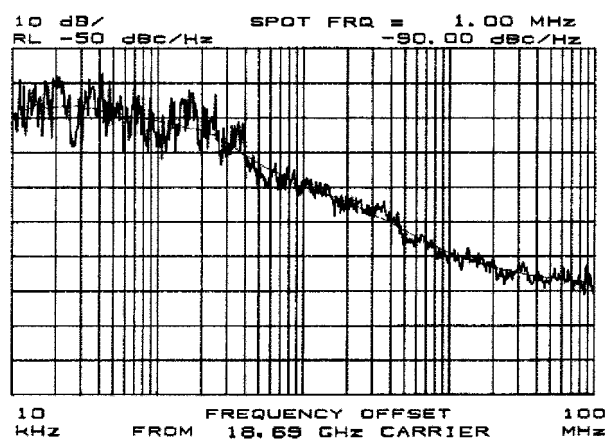


Fig. 10. Measured phase noise of the InP VCO versus frequency offset.

(multistage) ring oscillators, the proposed VCO is advantageous in terms of power consumption and transistor count. For instance, a three-stage ring oscillator with 10- or 26-GHz frequency options consists of 40 InP HBTs and consumes 250-mW power [8].

IV. CONCLUSION

The design and implementation for fiber-optic applications of a 20-GHz-band differential InP VCO was presented. The design is based on positive feedback on a single-stage differential amplifier. The main advantage of the proposed VCO is the wide tunable frequency range, which can be used to compensate for process or temperature variations when used within a PLL. Other features include low power, low transistor count, and, hence, area efficiency compared to conventional ring oscillators. The implemented InP VCO has an adjustable frequency range of 45% around its midband frequency. A typical VCO on implemented wafers operates from 13.75 to 21.5 GHz. The proposed InP VCO provides two complementary outputs each

delivering a measured power level of -2.8 to -8 dBm. Total power consumption is 130 mW at 18.6 GHz and increases with the output frequency. At 1-MHz offset to the carrier, the measured phase noise is -90.0 dBc/Hz and has a slope of about -20 dBc/Hz per decade.

ACKNOWLEDGMENT

The authors would like to thank TRW for providing access to the InP HBT technology and, in particular, A. Gutierrez-Aitken, TRW, Redondo Beach, CA, for his technical assistance.

REFERENCES

- [1] B. Jalali and S. J. Pearton, Eds., *InP HBTs: Growth, Processing and Applications*. Norwood, MA: Artech House, 1995.
- [2] M. Wuzer, J. Bock, H. Knapp, W. Zirwas, F. Schumann, and A. Felder, "A 40-Gb/s integrated clock and data recovery circuit in a 50-GHz f_T silicon bipolar technology," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1320–1324, Sept. 1999.
- [3] M. Yung, J. Jensen, R. Walden, M. Rodwell, G. Raghavan, K. Elliott, and W. Stanchina, "Highly integrated InP HBT optical receivers," *IEEE J. Solid-State Circuits*, vol. 34, pp. 219–227, Feb. 1999.
- [4] K. W. Kobayashi, J. C. Cowles, L. T. Tran, A. Gutierrez-Aitken, M. Nishimoto, J. H. Elliott, T. R. Block, A. K. Oki, and D. C. Streit, "A 44-GHz-high IP3 InP HBT MMIC amplifier for low DC power millimeter-wave receiver applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1188–1195, Sept. 1999.
- [5] A. Gutierrez-Aitken, A. Kaneshiro, B. Tang, J. Notthoff, P. Chin, D. Streit, and A. Oki, "69 GHz frequency divider with a cantilevered base InP DHBT," in *IEDM Tech. Dig.*, 1999, pp. 779–782.
- [6] S. Voinescu, D. Marchesan, J. Showell, M. Maliepaard, M. Cudnoch, M. Schumacher, M. Herod, D. Walkey, G. Babcock, P. Schvan, and R. Hadaway, "Process- and geometry-scalable bipolar transistor and transmission line models for Si and SiGe MMIC in the 5–22 GHz range," in *IEDM Tech. Dig.*, 1998, pp. 307–310.
- [7] B. Razavi, "A 2-GHz 1.6-mW phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 32, pp. 730–735, May 1997.
- [8] R. Montgomery, D. Humphrey, R. Hamm, F. Ren, R. Malik, R. Kopf, A. Tate, P. Smith, R. Ryan, J. Lin, and Y. Chen, "10 and 26 GHz differential VCO's using InP HBTs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, 1996, pp. 1507–1510.
- [9] M. Soyuer, J. Burghartz, H. Ainspan, K. Jenkins, P. Xiao, A. Shahani, M. Dolan, and D. Hame, "An 11-GHz 3-V SiGe voltage-controlled oscillator with integrated resonator," in *Proc. IEEE BCTM*, 1996, pp. 169–173.
- [10] H. Djahanshahi, N. Saniei, S. P. Voinescu, M. C. Maliepaard, and C. A. T. Salama, "20-GHz InP-HBT voltage-controlled oscillator with wide tuning range," in *IEEE RFIC Symp. Dig.*, 2001, pp. 161–164.



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