SiGe BiCMOS Topologies for Low-Voltage Millimeter-Wave Voltage Controlled Oscillators and Frequency Dividers

Timothy O. Dickson and Sorin P. Voinigescu

Edward S. Rogers, Sr. Department of Electrical and Computer Engineering, University of Toronto, 10 King's College Road, Toronto, ON, Canada M5S 3G4 E-mail: tod@eecg.toronto.edu

***Abstract* — BiCMOS topologies for mm-wave voltage-controlled oscillators and frequency dividers are presented. The topologies, based on a MOS-HBT cascode configuration, enable low-voltage operation without compromising speed. A 37-GHz Colpitts VCO with 8% tuning bandwidth is reported with a phase noise of -97 dBc/Hz at a 1-MHz offset. For the first time, experimental evidence confirms that the bias condition for optimal VCO phase noise coincides with the bias point for minimum noise figure. Additionally, frequency division up to 70 GHz is reported, which is believed to be a record for dividers employing n-channel MOSFETs.**

***Index Terms* — BiCMOS, SiGe HBT, mm-wave, VCO, frequency divider**

I. Introduction

Recently, silicon-based technologies have emerged for a number of millimeter-wave (mm-wave) applications. The potential for highly-integrated transceivers makes silicon a low-cost alternative to III-V technologies for these applications. However, reducing building block power consumption remains an obstacle due to the high V_{BE} of the SiGe HBT, which ultimately limits the supply voltage.

The SiGe BiCMOS cascode stage consisting of n-channel MOSFET common-source and SiGe HBT common-base transistors has recently been demonstrated as an ideal low-voltage, low-power topology for high-speed digital circuits as well as analog building blocks [1, 2]. In this work, the applicability of this topology is demonstrated in mm-wave building blocks. Novel BiCMOS frequency dividers and a VCOs are presented which enable low-voltage operation for mm-wave applications.

II. BiCMOS Voltage-Controlled Oscillator

The Colpitts topology is a common choice for low-phase noise, high-frequency voltage oscillators. Figure 1 shows the schematic of a BiCMOS implementation of the Colpitts topology. An n-MOS transistor generates negative resistance to sustain oscillation in the tank, while the cascode HBT transistor improves isolation between the tank and the output. The oscillation frequency of the VCO is given by

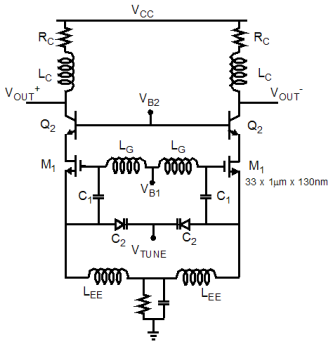

Fig. 1. Schematic of BiCMOS Colpitts differential VCO.

$$\omega_0 = \frac{1}{\sqrt{L_G C_{EFF}}} \quad . \tag{1}$$

Here, the effective tank capacitance is determined largely by C_1, C_2, and the parasitic capacitances of the MOSFET.

$$C_{EFF} \approx C_{GD} + \frac{(C_1 + C_{GS1})(C_2 + C_{SB1})}{C_1 + C_2 + C_{GS1} + C_{SB1}} \quad . \tag{2}$$

In MOS Colpitts oscillators, the parasitic source-to-bulk capacitance C_{SB1} shunts the varactor C_2 and degrades the tuning range. This is less of a concern for bipolar Colpitts oscillators, as modern HBTs have no appreciable emitter-to-substrate capacitance. Finally, negative resistance seen into the gate of M1 is needed to overcome losses in the tank. This resistance is given by

$$R_{NEG} = R_G - \frac{g_{m1}}{\omega^2 (C_1 + C_{GS1})(C_2 + C_{SB1})} \quad . \tag{3}$$

The gate resistance R_G can be made negligible through layout techniques [1].

To gain insight on methods for improving the phase noise of the VCO, we turn to Leeson's formula [3].

$$L(\Delta\omega) = \frac{FkT}{P}\left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1 + \frac{\omega_{corner}}{\Delta\omega}\right). \tag{4}$$

It is well known that the phase noise at offset $\Delta\omega$ from the carrier ω_0 can be improved by maximizing both the carrier power (P) and the quality factor of the tank (Q). The former implies that tank swing should be maximized,

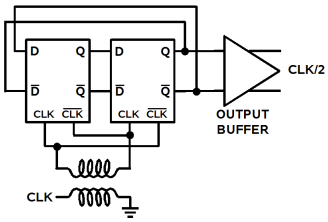

Fig. 2. Block diagram of frequency divider with transformer input.

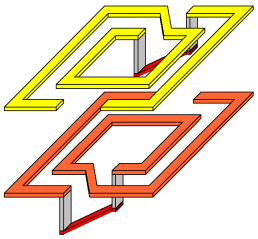

Fig. 3. Conceptual 3-D diagram of mm-wave stacked transformer for single-ended-to-differential conversion.

while the latter dictates careful design of passive components. Minimizing footprint over the silicon substrate is critical to improve inductor quality factor in the mm-wave regime [4]. The Q of an nMOS accumulation-mode varactor is highly dependent on its layout [5]. Using minimum gate length devices reduces the channel resistance, while employing multifinger layout techniques diminishes the impact of the gate resistance. Note that excessively-small unit finger widths will degrade the tuning range due to added parasitic interconnect. In this design, 1-μm unit finger widths are used, with the gate contacted on two sides of the transistor to lower the gate resistance. Further reduction in phase noise can be achieved by minimizing the noise figure (F) of the amplifier. For a fixed power consumption, the cascode transistors can be sized such that they are biased at the optimal noise figure bias condition. This allows for low-noise operation without degrading the tank swing.

III. Frequency Dividers

The frequency divider block diagram is presented in Fig. 2. Frequency division is accomplished through the use of a toggle flip-flop, which consists of two latches in a feedback configuration. At mm-wave frequencies, generating differential clock signals from single-ended external signal generators becomes increasingly difficult. While off-chip phase shifters have been used in the testing of recently-reported mm-wave dividers [6], their prohibitive cost makes them an expensive solution. Instead, an on-chip transformer placed at the input to the divider obviates the need for such external testing components. By making use of the multi-layer backends

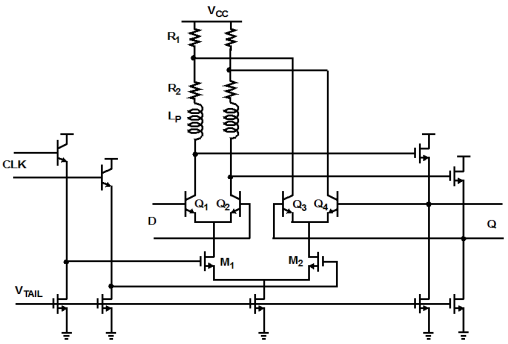

Fig. 4. BiCMOS latch with source follower output buffers.

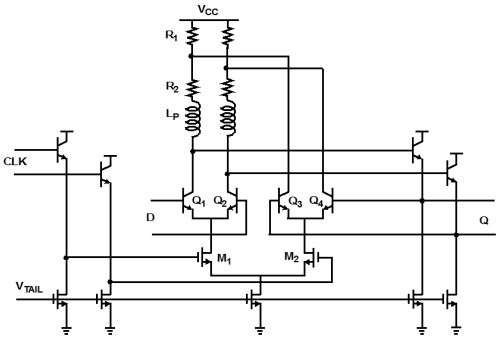

Fig. 5. BiCMOS latch with emitter follower output buffers.

available in modern BiCMOS technologies, stacked transformers such as the one presented in Fig. 3 can be realized due to coupling between adjacent metal layers. The primary and secondary turns are implemented as symmetrical inductors to minimize the phase error between the differential outputs. This stacked structure yields higher coupling while occupying less area than conventional planar transformers [4]. Note that, although the frequency divider topology is static, the addition of the transformer limits the lowest frequency at which the divider can be tested.

The schematic for the BiCMOS implementation of this latch is shown in Fig. 4. The latch core is based on a BiCMOS cascode due to its superior frequency response, which even exceeds that of a bipolar cascode while operating from a lower supply voltage [1]. Unlike other low-voltage high-speed logic topologies which reduce supply voltages at the expense of increased current [7], BiCMOS logic results in low-voltage, low-power, and high-speed operation. MOSFET transistors are used to switch the input clock signal due to their lower input time constant, which can be rendered insignificant by using multi-finger layout techniques. To improve the operating speed of the frequency divider, capacitance at the resistively-loaded node must be minimized. HBTs are used for the upper-level transistors Q1-Q4 in the latch due to their lower output capacitance as compared to n-channel MOSFETs. To reduce capacitive loading from subsequent stages, emitter followers (EF) or source

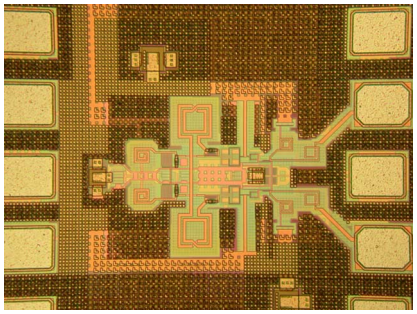

Fig. 6. Die microphotograph of 35-GHz BiCMOS Colpitts VCO.

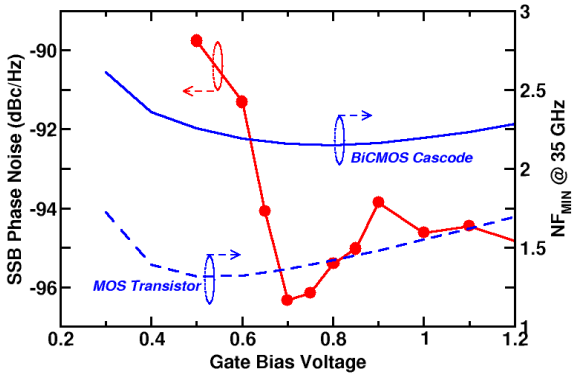

Fig. 7. Measured phase noise as a function of MOSFET bias. The lowest phase noise coincides with the bias condition for optimal NF_{MIN} of the BiCMOS cascode.

followers (SF, Fig. 5) can be employed along the feedback path within the latch. While the former yields better frequency response, the latter allows for a reduction in the supply voltage from 3.3V to 2.5V. In this work, dividers with both types of latches have been implemented. Further improvement in speed can be achieved by employing a split-resistor load, which lowers the Miller capacitance seen by the holding pair Q3-Q4 [6], and through the use of inductive peaking.

IV. Fabrication and Measurements

The VCO and frequency dividers were fabricated in a production 130-nm SiGe BiCMOS technology with 150-GHz f_T/f_{MAX} SiGe HBT [8]. For all circuits, measurements were performed on-wafer with 67-GHz GSGSG GGB probes.

A. Voltage-Controlled Oscillator

The die microphotograph of the 37-GHz VCO is shown in Fig. 6. The circuit occupies an area of 360µm x 270µm, excluding bond pads. Figure 7 presents the measured phase noise as a function of the bias point of the tank transistors. Furthermore, the simulated minimum noise figures at 35-GHz for both the nMOSFET and the

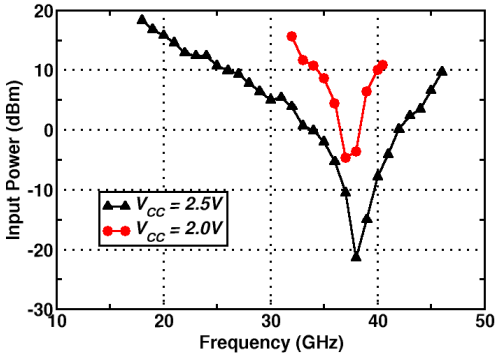

Fig. 8. Sensitivity curves for various supply voltages of the 2.5-V divider implemented with the BiCMOS latches of Fig. 4.

BiCMOS cascode are also included on the opposite axis of Fig. 7. The minimum VCO phase noise of -97 dBc/Hz is obtained when the MOSFET bias coincides with the bias condition for minimum phase noise of the BiCMOS cascode. Note that this bias point is different from that of the nMOSFET due to added collector shot noise from the HBT cascode transistor. To the authors' best knowledge, this presents the first experimental evidence of optimal biasing conditions of VCO transistors for best phase noise performance. The VCO core and output buffer consume 20mA and 30mA, respectively, from a 2.5V supply, and deliver -4.5dBm output power to a 50Ω load (cable and probe losses are not de-embedded). By adjusting the varactor bias, the VCO frequency can be tuned from 33.8GHz to 36.7GHz, which corresponds to an 8.2% tuning range. The oscillation frequency is within 5% of that predicted by hand analysis from equations (1) and (2), where the parasitic MOSFET capacitances are determined based on the geometry of the device and scalable 130-nm RF-CMOS models [9]. Interestingly, this proved to be more accurate than SPECTRE simulations, which predicted an oscillation frequency of 40 GHz for the VCO.

B. Frequency Dividers

Frequency dividers were tested by applying a single-ended clock signal to the circuit from an Agilent E8257D PSG signal source. Although the source is specified for operation up to 67-GHz, CW signals up to 70-GHz were obtained albeit with slightly higher phase noise. The output of the divide-by-2 circuit was monitored on an Agilent E4448A PSA spectrum analyzer from one side of the differential output, with the other side terminated in 50Ω.

Sensitivity curves for the divider with SF's in the latch feedback path are shown in Fig. 9. While operating from the nominal 2.5-V supply, the circuit divides up to 46-GHz. If the supply voltage is lowered to 2.0-V, division of up to 41-GHz is achieved, representing the lowest

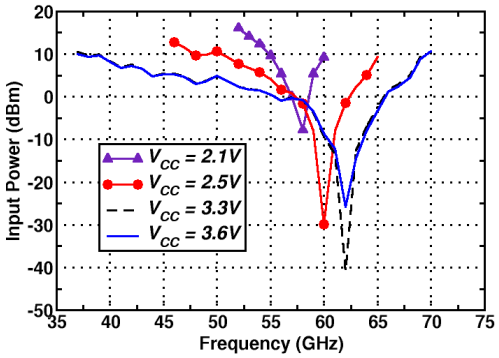

Fig. 9. Sensitivity curves for various supply voltages of the 3.3-V divider implemented with the BiCMOS latches of Fig. 5.

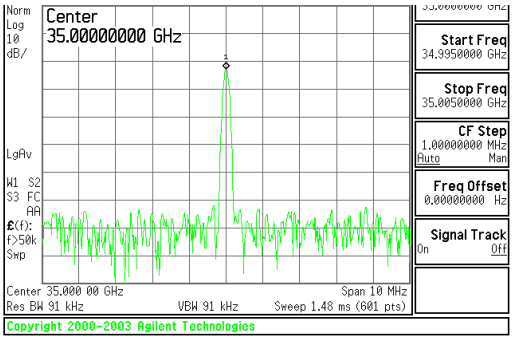

Fig. 10. Divider output spectrum at 35-GHz for an input of 70-GHz.

voltage for a 40-GHz static frequency divider reported to date [10]. The divider and output buffer consume 84mW and 14mW, respectively, from the nominal 2.5-V supply voltage.

Similarly, sensitivity curves were measured for the nominal 3.3-V divider with EF's in the latch feedback path, and are presented in Fig. 9. With the nominal supply voltage, the divider operates with an input frequency of 69 GHz. By increasing the supply voltage to 3.6V, the operating frequency can be increased to 70 GHz and is limited by the test equipment. The output spectrum for a 70 GHz input is shown in Fig. 10. Moreover, operation at 60 GHz and 65 GHz is observed for supply voltages of 2.1V and 2.5V, respectively. As the 70 GHz input signal is applied to the gates of MOSFETs, this is the fastest frequency divider reported to date which employs MOSFETs on high-speed paths. The die photograph of the divider is shown in Fig. 11, and occupies an area of 300µm x 170µm, excluding bond pads. The divider and output buffer consumes 124mW and 18mW, respectively, from a 3.3-V supply voltage.

V. Conclusion

BiCMOS low-voltage topologies for mm-wave VCOs and frequency dividers have been presented. For the first time, experimental evidence of optimal biasing conditions to minimize VCO phase noise is reported. Additionally, low-power mm-wave frequency dividers have been demonstrated operating up to 70-GHz. The BiCMOS divider topology presents an alternative to recently-reported power-intensive mm-wave dividers [11].

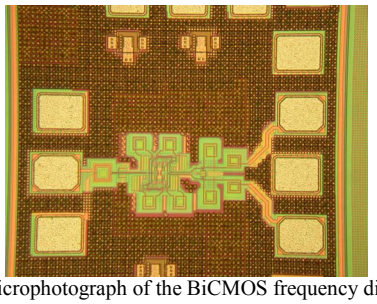

Fig. 11. Die microphotograph of the BiCMOS frequency divider with transformer input.

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