

A 2-GHz Direct Sampling Delta-Sigma Tunable Receiver with 40-GHz Sampling Clock and on-chip PLL

T. Chalvatzis¹, T. O. Dickson^{1,2}, and S. P. Voinigescu¹

¹The Edward S. Rogers Sr., Department of ECE, University of Toronto, Toronto, ON, Canada

²now with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA

Abstract

This paper presents a 2-GHz tunable direct sampling $\Delta\Sigma$ receiver with 40-GHz sampling clock and on-chip PLL, fabricated in a production 130-nm SiGe BiCMOS process. The measured SFDR and SNDR are 59 dB and 59.84 dB, respectively, over a bandwidth of 60 MHz, and the effective number of bits (ENOB) equals 9.65. Compared to the case where an external low-noise 40-GHz clock was used, no SNDR degradation was observed when the on-chip VCO and PLL were employed. The entire receiver with PLL occupies an area of 1.58x2.39 mm² and consumes 2.19 W when powered from a 2.5-V supply.

Introduction

We have recently demonstrated a continuous-time band-pass $\Delta\Sigma$ ADC with external 40-GHz clock and a center frequency of 2 GHz [1]. As a follow-up, this paper describes the first direct sampling 2-GHz receiver with on-chip 40-GHz VCO and PLL. In addition to the increased functionality compared to [1], the circuit features a modified bandpass filter topology leading to lower noise and higher linearity. As a result, the receiver resolution is improved by approximately 1 bit, approaching 10 bits over 60 MHz and exceeding 11 bits over a 10-MHz band centered at 2 GHz. More importantly, by testing the chip with clock signals generated both on-chip and externally, it is demonstrated that the jitter of the on-chip VCO and PLL does not limit performance.

$\Delta\Sigma$ Receiver Circuit Design

Figure 1 illustrates the block level diagram of the digital receiver, including the $\Delta\Sigma$ ADC and PLL. All circuit blocks are fully differential. The 4th order ADC consists of two 2nd order resonators implemented as G_m -LC filters with MOS-HBT cascode amplifiers [1]. The first stage serves as both the LNA of the receiver and the first transconductor stage of the loop. The G_m -LC filters are biased at the peak- g_m current density of 0.4 mA/ μ m to achieve maximum input linearity with little degradation of noise figure [1]. The single-bit quantizer is realized as a Master-Slave-Master D-type flip-flop, which

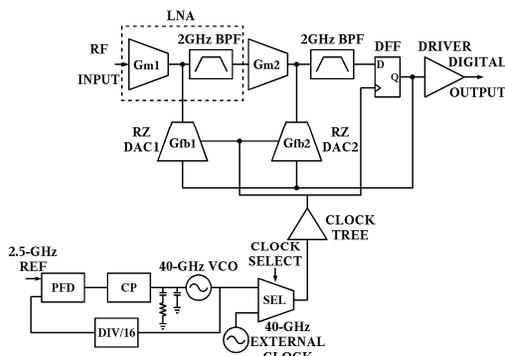


Fig. 1. System level block diagram of the digital receiver with $\Delta\Sigma$ ADC and PLL.

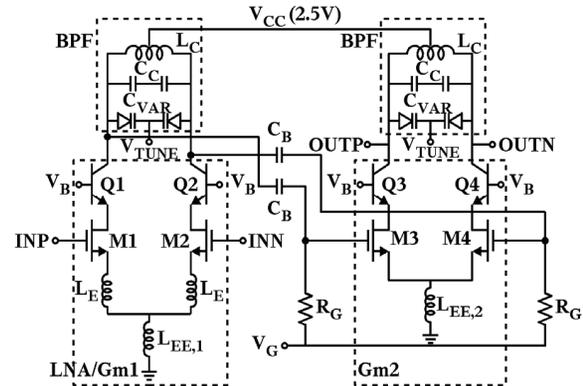


Fig. 2. Circuit schematic of 4th order loop filter.

also provides the feedback signal to the Return-to-Zero D/A converters [1].

The transistor-level filter schematic is shown in Fig. 2. Compared to the topology of [1], the linear voltage swing at the output of the second differential stage, and the overall noise figure and dynamic range of the filter are improved by removing the emitter followers between stages and the current source in the second stage. To ensure common mode rejection in the absence of a current source, a 2.7-nH inductor $L_{EE,2}$ is implemented with series stacked windings in the top three metals of the process and occupies an area of 47x47 μ m².

The 40-GHz sampling clock is generated by an integer-N PLL, with $N=16$, and employing a Colpitts VCO [2] and a 2.5-GHz external reference. Figure 3 reproduces the schematics of the phase frequency detector (PFD), charge pump (CP) and asynchronous resettable latch. A selector allows the chip to be operated either with the internal or with an external clock in order to study the impact of PLL jitter on receiver resolution.

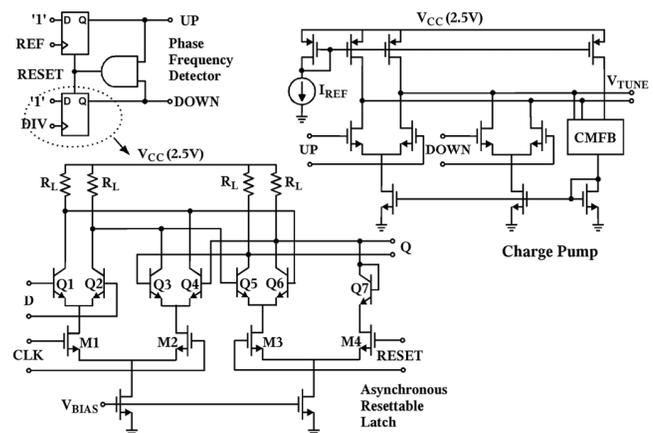


Fig. 3. Circuit schematic of the PFD, CP and asynchronous resettable latch in the PLL.

Measurement Results

The digital receiver was implemented in a production 130-nm SiGe BiCMOS technology with 150-GHz f_T HBTs. The chip shown in Fig. 4 occupies an area of $1.58 \times 2.39 \text{ mm}^2$ including the pads. All measurements were performed on wafer. The measured spectrum at the receiver output is reproduced in Fig. 5 for a -10 dBm input signal at 2 GHz. The 2.5-GHz feedthrough signal poses no problems because it falls outside the receiver bandwidth and is an artifact of the wafer probing setup where the external PLL reference is applied through a pad adjacent to the receiver output pads. The PLL phase noise is -80 dBc/Hz at 100 kHz offset from the 39.7-GHz clock (Fig. 6). The SNDR and DR of the receiver were found by integrating the noise around the carrier. The DR is defined at the output as the range from the P_{1dB} to the integrated noise. A comparison of the integrated noise power over 60 MHz when the receiver is clocked from the on-chip PLL, and when the PLL is turned off and an external clock is applied from a low-noise Agilent E8257D signal source, shows that the noise floor is the same in both cases (-65 dBm/60MHz), proving that clock jitter does not have an measurable impact on performance at this resolution. Quantization noise due to low filter Q is the dominant noise contributor in the band suggesting that further performance improvement is possible with Q-enhancement techniques. The receiver has a peak-SNDR of 59.84 dB, a DR of 58.5 dB (Figs. 7 and 8a) and a SFDR of 59 dB for a bandwidth of 60 MHz. The $FoM = 2^{ENOB} \times 2BW/P$ is 65.5 GHz/W including the power dissipated by the VCO and PLL. Figure 8b summarizes the performance of state-of-the-art $\Delta\Sigma$ ADC's with GHz clocks [3-5].

Conclusion

The first 2-GHz $\Delta\Sigma$ digital receiver with on-chip mm-wave VCO and PLL was demonstrated. The circuit achieves a SNDR of 59.84 dB over 60 MHz and consumes 2.19 W from a 2.5-V power supply. The 40-GHz on-chip VCO and PLL jitter does not appear to degrade receiver performance, indicating that a direct digitization receiver for software-defined radio can be realized in silicon. The overall FoM improve-

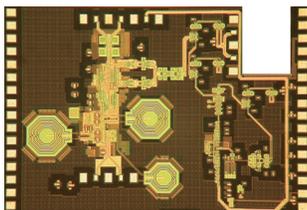


Fig. 4. Die photo of $\Delta\Sigma$ digital receiver.

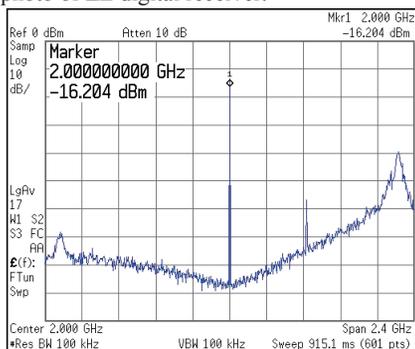


Fig. 5. Measured spectrum of digital receiver for a -10 dBm input tone at 2 GHz and on-chip 40-GHz clock. The tone at 2.5 GHz is the feedthrough from the external reference signal for the PLL.

ment over that of the ADC in [1] is 34% and 58% respectively, with and without the power dissipated by the 40-GHz VCO and PLL.

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References

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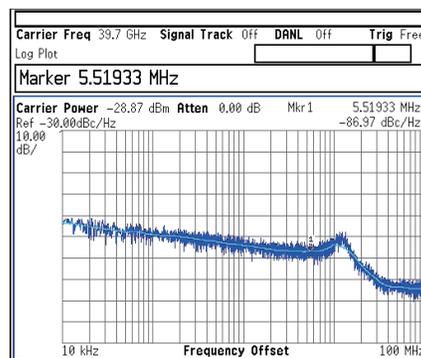


Fig. 6. Measured phase noise of PLL at 39.7 GHz.

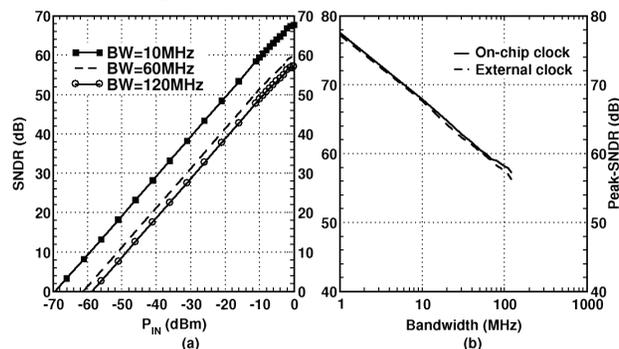


Fig. 7. Measured receiver (a) dynamic range with on-chip clock, and (b) peak-SNDR vs bandwidth with on-chip and external clock.

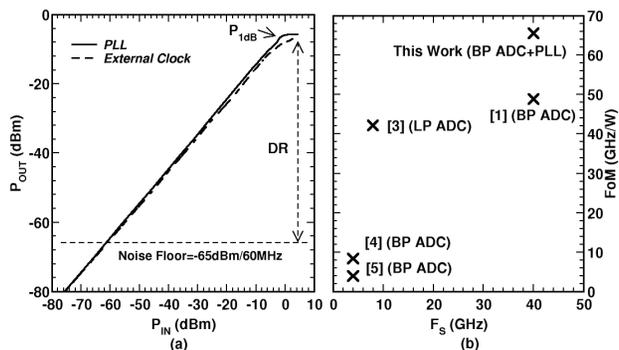


Fig. 8. (a) Measured receiver linearity with on-chip and external clock for a 2-GHz single tone input, and (b) FoM comparison with recently published ADC's.