Linear Large-Swing Push–Pull SiGe BiCMOS Drivers for Silicon Photonics Modulators

Alireza Zandieh, *Member, IEEE*, Peter Schvan, *Member, IEEE*, and Sorin P. Voinigescu, *Fellow, IEEE*

***Abstract*— The analysis, design, and experimental characterization of a novel class of large-swing low output-impedance push–pull SiGe BiCMOS drivers are discussed. The circuits, which employ single- and series-stacked emitter follower (EF) and MOS-HBT cascode topologies, are intended to drive optical modulators with high-order m-pulse-amplitude modulated (PAM) signals, while maximizing energy/bit efficiency. The series-stacked EF version, implemented in a 55-nm SiGe BiCMOS technology with 370 GHz f_{MAX}, achieved the highest linearity with 4.8-V_{pp} differential output swing, 57.5 GHz bandwidth, and an output compression point of 12 dBm per side. Four-PAM and eight-PAM eye diagrams were measured at 56 GBd for a record data rate of 168 Gb/s. Four-PAM 64-GBd eye diagrams were also demonstrated. The circuit consumes 820/600 mW with/without the predriver and has an energy efficiency of 4.88/3.57 pJ/b.**

***Index Terms*— Linear modulator driver, push–pull output stage, series-stacked EF, SiGe BiCMOS.**

I. Introduction

RESEARCH is underway in many industry and academic groups for the next generation of 400–1000-Gb/s fiber-optic systems. Given the exponential increase in data communication and bandwidth usage, energy and bandwidth efficiency have become critical design constraints. Some of the most promising solutions require complex modulation formats, such as four-pulse-amplitude modulation (PAM) and 16-quadratic-amplitude modulation (QAM), at 56–64-GBd symbol rates. To implement the higher order modulations, three system architectures are considered, as illustrated in Fig. 1.

The most common, transmitter architecture [1]–[3], but also with the lowest level of integration, shown in Fig. 1(a), consists of a DSP, a 6–8-b (CMOS) digital-to-analog converter (DAC) with 300–400-mV_{pp} output swing per side, followed by a linear large-swing driver and an optical modulator. Circuit-level examples of this transmitter architecture are reported in [3] at 56 GBd, where a linear distributed amplifier with 2 V_{pp} differential swing is monolithically integrated with the serializer in 130-nm SiGe BiCMOS, and at lower symbol rates, in [2], which uses a lumped driver InP-HBT driver with 3-V_{pp} differential output swing. The main benefit of this architecture is that the low-swing DAC and the DSP can be moonolithically integrated on a separate chip, typically in the most advanced highest density CMOS node, and only one high-bandwidth analog (differential) signal is sent to the higher voltage-swing SiGe BiCMOS or III-V driver chip, and from the driver chip to the optical modulator die. Since most III–V and silicon photonics (SiPh) optical modulators with over 30 GHz of bandwidth, as needed for 56-GBd operation, require more than 2 V_{pp} drive per side, the linear driver becomes one of the most challenging blocks to design. It must be operated with back-off and predistortion compensation, similar to a wireless PA, but with over 50 GHz of bandwidth. So far, only distributed drivers have been reported that achieved both the required bandwidth and more than 4 V_{pp} differential output swing [4], [5].

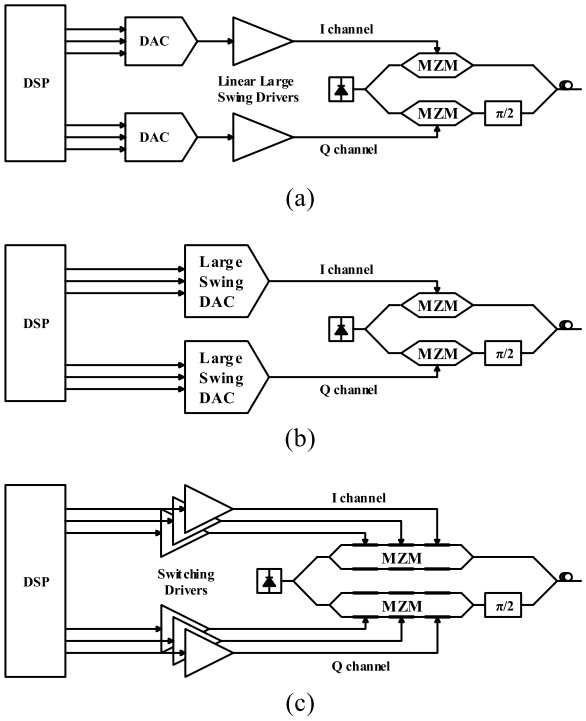


Fig. 1. Block diagram of typical transmitter architectures for optical communication systems.

A second transmitter block partitioning combines the DAC and the driver onto a single chip, as shown in Fig. 1(b). In this case, the DAC-driver combination must be implemented as a large-swing DAC, either distributed [6] or lumped [7]. The challenges here are that: 1) the DSP often needs the most advanced CMOS node, which is typically unreliable for operation above 1 V swing unless an SOI substrate is used,

Manuscript received July 1, 2017; revised September 3, 2017; accepted September 15, 2017. Date of publication November 16, 2017; date of current version December 12, 2017. This work was supported in part by MITACS and in part by Ciena. *(Corresponding author: Alireza Zandieh.)*

A. Zandieh and S. P. Voinigescu are with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: alireza.zandieh@mail.utoronto.ca).

P. Schvan is with the Ciena Corporation, Ottawa, ON K2K 0L1, Canada.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2017.2768028

and 2) solutions with separate DSP and DAC chips require a multilane >400-Gb/s digital interface between ICs, in addition to the high-bandwidth analog signal link from the DAC to the modulator.

The third approach, as depicted in Fig. 1(c), is an electro-optical DAC based on a segmented optical modulator and an array of switching drivers each driving an optical modulator section [8], [9].

In the latter two architectures, the output stage that drives the optical modulator operates in limiting mode, therefore with higher energy efficiency. The main issue for both is synchronizing the high-speed digital signals from the DSP chip to the driver/optical DAC, which can be very costly in terms of power consumption. However, if the DSP is not very large, does not dissipate much power, and can be monolithically integrated with the DAC electronics, this approach can show significant benefits in terms of speed and power efficiency.

SiPh modulators show promise for optical communication systems because of cost and also the fact that the driver can be flip-chipped on top of the optical modulator die to reduce the interconnect parasitics. The latter is feasible if thermal issues can be mitigated. It is also hoped that such a 3-D module can reduce the overall power consumption and improve the energy efficiency by eliminating the need for on-chip termination in the driver or DAC.

Until now, both SiPh modulators and silicon drivers have lacked the necessary bandwidth suitable for 56-GBd operation. Although a 56-Gb/s photonics module consisting of a 55-nm SiGe BiCMOS driver and a SiPh Mach–Zehnder modulator (MZM) has been reported recently [10], the switching driver is not suitable for linear operation as needed for m-PAM or 16-QAM systems, and its output swing is only 1.6 V_{pp} differential.

Implementation of large-swing drivers in CMOS is very challenging because only sub-28-nm CMOS with sub-1-V MOSFET safe operating voltage can potentially reach 64 GBd symbol rate with large swing. Although series stacking of n- and p-MOSFETs can be employed in SOI technologies to create a composite transistor with effective large breakdown voltage and high f_{MAX} [11], only a large-swing switching driver has been reported to date at > 56 Gb/s [12]. The low breakdown voltage of bulk FinFET technologies and the absence of an insulating layer separating the transistor channel and the bulk of the silicon wafer make stacking schemes problematic to achieve more than 2-V swing.

In this paper, we report a novel topology for a linear modulator driver that was manufactured in 55-nm SiGe BiCMOS technology [13]. It achieved higher symbol rates, with larger output swing and three times the data rate of that in [10], the highest ever reported for a modulator driver in any technology. Compared with [14], Section II provides a background on SiPh modulators and traditional driver circuits. Section III discusses the proposed driver topology in detail and provides an analytical model that describes its small-signal gain and frequency response, as well as its large-signal operation. Finally, the measurement results are presented in Section IV.

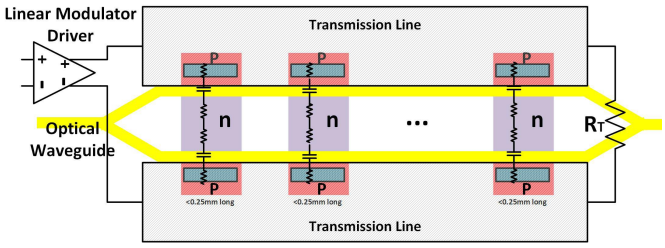


Fig. 2. Traveling wave Mach–Zehnder SiPh modulator structure.

II. Background

A. Silicon Photonics Modulator

Although it could be used with other types of optical modulators, the proposed driver is specifically designed for a SiPh MZM. Therefore, it is important to understand the electrical equivalent circuit of the SiPh optical modulator and its limitations, which must be compensated by the electronic driver.

From the electrical point of view, the modulator can be described as a distributed circuit. Each short section of the MZM arm is a reversed-biased p-n junction. In the small-signal equivalent model of the MZM, this diode can be represented by its junction capacitance in series with parasitic resistances associated with the anode and cathode contact regions. The junction capacitance per modulator arm length, C_m, is typically ~220 fF/mm [15]. The length of the MZM is dictated by $V_\pi \times L$, typically 3–4 V × cm [15]. This value is fairly high and, therefore, a long modulator with relatively high driving voltage and large capacitance is needed to create enough phase shift for high extinction ratio, as needed for higher order modulation formats.

Two MZM structures are commonly encountered, as described below.

1) Modulator With Traveling Wave Electrodes: A sketch of this type of modulator is shown in Fig. 2. It is realized as a transmission line in the top metal layer of the back-end, periodically loaded with p-n junction sections whose depletion width is modulated by the applied voltage and translates into optical phase shift: the longer the p-n junction section, the bigger the phase shift for a given voltage swing. Due to the large area of the p-n junction, a large capacitance shunts the transmission line to ground, reducing its characteristic impedance and significantly increasing its loss at high frequency because of the parasitic series diode resistance. The electrical signal also experiences higher propagation delay. The characteristic impedance of the loaded line depends on its fill ratio with p-n junction sections, the characteristic impedance of the unloaded line, Z_o, and C_m. For a certain SiPh technology, C_m is fixed and, therefore, only Z_o and the fill ratio are available as design parameters. For a typical value of Z_o and a fill ratio of one, the loaded line shows 30-Ω characteristic impedance. Since MZM SiPh modulators are typically longer than 4 mm, to avoid reflection, the electrodes must be terminated on matched 30-Ω resistors per side, 60 Ω differentially. Because of the relatively low characteristic impedance, this type of structure needs a driver with both large output current and large output voltage swing, and suffers

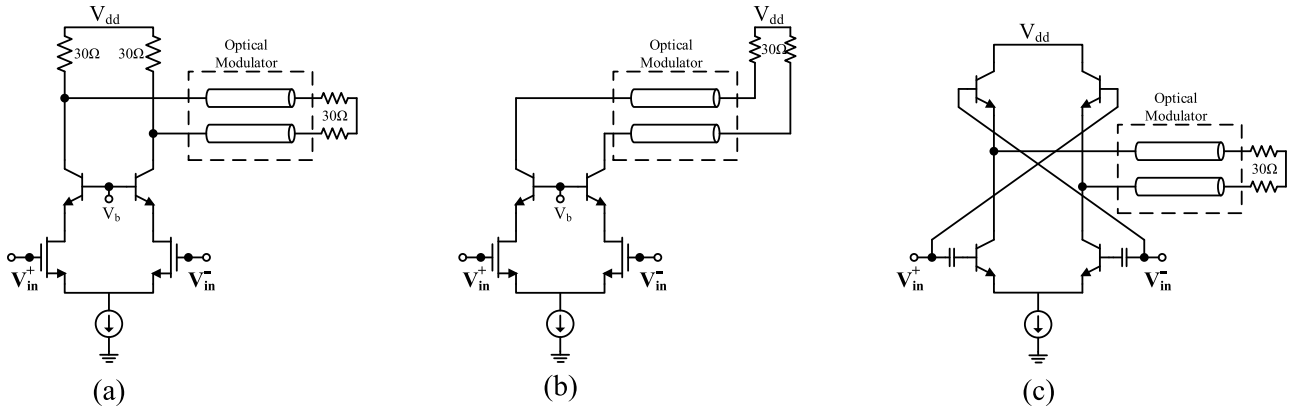


Fig. 3. Traditional driver topologies. (a) Matched current-steering differential pair. (b) Open-collector current-steering differential pair. (c) SEF.

from limited bandwidth because of the lossy transmission line. Some sort of driver pre-emphasis is needed for operation at 56 GBd and beyond.

2) Segmented Modulator: Another option is to break a long modulator into smaller sections and drive each section with a separate smaller driver circuit. Such a linear segmented driver modulator with 16 sections was recently monolithically integrated in a SiGe BiCMOS SiPh technology [16]. Since the modulator sections are short, they can be left unterminated, saving current in the output stage. The load seen by the driver is effectively a lumped capacitor whose value depends on the length of the modulator section. Unlike the traveling wave electrode (TWE) modulator, there is, in theory, no speed limit since the length of the modulator sections can be reduced by increasing their number. Ultimately, the power consumption may increase significantly as the size and bias current of the individual drivers can no longer be scaled down. A more immediate challenge though is to synchronize the signals arriving at the input of each driver to be matched with the optical signal propagation, especially if the input signal is already m-PAM and the drivers have to be linear.

B. Traditional Driver Circuits

Traditional driver topologies, loaded by a differential optical modulator, are compared in Fig. 3. The optical modulator is modeled as 30-Ω transmission lines terminated on 30-Ω resistors, as discussed in the previous section. Fig. 3(a) shows a current-steering differential MOS-HBT cascode stage that allows for larger output swings and can be operated in switching mode or as a linear driver, depending on the bias current density in the MOSFETs and on the input voltage swing. This topology is suitable for situations where the driver and the modulator are placed far apart. Its main drawback is very low power efficiency due to the fact that the effective resistance seen by the driver is only 15 Ω per side and half of the power is dissipated on the on-chip load resistors in the driver.

A more efficient alternative is the open-collector topology shown in Fig. 3(b), where the entire tail current of the driver flows through the modulator, generating the required voltage swing on the termination resistors in the optical modulator. This driver is more efficient than the previous one, requiring half of the tail current and power consumption to generate the same voltage swing [17]. However, it suffers from reflections if the modulator is long or placed more than a wavelength away from the driver. Second, the dc current flowing through the modulator can cause heating, electromigration, and reliability issues.

Finally, Fig. 3(c) depicts the switched emitter follower (SEF) driver topology [18]. Unlike the previous two, it can operate only as a switching driver. Because of its very low output impedance, it can be a good candidate to efficiently drive long or large-capacitance SiPh modulators, being less sensitive to reflections. However, it suffers from relatively low output voltage swing. In addition, it has larger input capacitance than the other two circuits because the emitter follower (EF) and the input common-emitter devices are connected together to the input node, albeit the latter through a series capacitor. This increases the load capacitance seen by the predriver stage that must operate with even larger voltage swing, since the output stage has no voltage gain.

III. Circuit Design

A. Proposed Linear Large-Swing Output Stage Topologies

The circuit consists of a broadband linear predriver and a large-swing linear output stage. This section discusses the output stage, which is intended to drive a TWE push–pull MZM whose electrodes can be treated as lossy transmission lines with low characteristic impedance, typically 30 Ω per side, 60-Ω differential. The performance of the driver with capacitive loads (unterminated modulator section) is also studied.

To save power, it is preferred that the driver output impedance be very low, rather than matched to the characteristic line impedance of the modulator. The low output impedance helps to minimize the impact of reflections due to impedance mismatch and drive larger load capacitances, and can be realized with an EF stage. However, unlike the switched-EF output stage, which is nonlinear, a linear large-swing version is needed to be invented, as described next.

Fig. 4 shows the steps taken to derive the proposed driver topology. First, as illustrated in Fig. 4(a), to increase the output

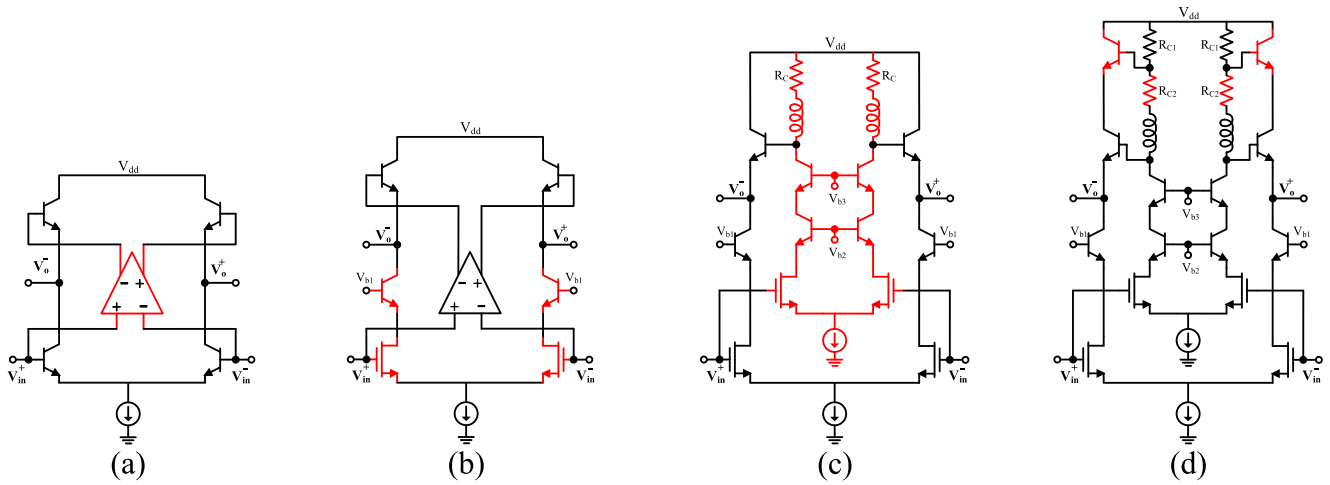


Fig. 4. Steps to create the proposed driver circuit. (a) Adding the linear amplifier. (b) Replacing the common-emitter HBTs with MOS-HBT cascodes. (c) Using a MOS-HBT double cascode for the linear amplifier. (d) Adding the second set of EFs and splitting the collector resistor in the gain stage.

voltage, a linear amplifier is added in the crossing path of the SEF stage. The input signal is thus amplified by this stage before it reaches the output through the EFs. Importantly, adding the amplifier does not increase the input capacitance compared with the original SEF stage since, again, two devices (typically smaller) are connected in parallel at the input node.

Next, to linearize the output stage, the HBT transistors are replaced with MOSFETs biased at the peak-f_{MAX} current density, as shown in Fig. 4(b). Another option is to add degeneration emitter resistors to the common-emitter differential HBT pair. However, besides requiring higher voltage headroom, further increasing power consumption, the emitter resistors would have to be over 50 μm wide to satisfy reliability rules, adding significant parasitic capacitance. At the same tail current, MOSFETs have smaller input capacitance and require a predriver stage with smaller bias current for the same overall bandwidth.

The MOS-HBT double cascode pair with resistive load and inductive peaking, shown in Fig. 4(c), is employed for the linear amplifier. A second common-base HBT is added in the linear amplifier stack to compensate for the extra voltage drop on the EF in the output stage and ensure that the V_{CE} and V_{DS} of all transistors remain in the safe range for this technology. The collector load resistor in the gain stage has two purposes: 1) it creates the required voltage swing for the output stage and 2) it sets the base–collector voltage and linearity of the EF in the output stage. This circuit topology can be considered a lower voltage-swing version of the proposed linear large-swing driver and shall be labeled single EF push–pull (SEFPP) topology.

For larger output swing, another EF can be added in the output stage on top of the original EF, resulting in a series-stacked EF push–pull (SSEFPP) driver as depicted in Fig. 4(d). The collector resistor in the gain stage, R_C, is split in two, R_{C1} and R_{C2}, to properly bias the series-stacked EFs and distribute the output voltage swing on two EFs. This helps to satisfy transistor reliability requirements and also improves linearity, as will be explained later.

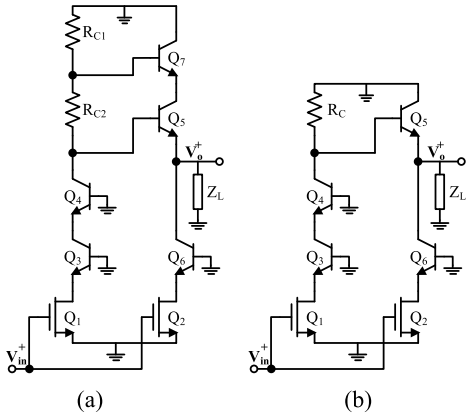


Fig. 5. Small-signal half-circuit. (a) SSEFPP output stage. (b) SEFPP output stage.

B. Small-Signal Analysis

This section derives the approximate small-signal transfer function for the driver circuit. Through this analysis, the effect of different loads on the small-signal performance will be examined. In addition, the critical parameters that affect the bandwidth of the circuit will be discussed. For small-signal analysis, the differential half-circuits of the SEFPP and SSEFPP drivers are illustrated in Fig. 5. To keep the derivation tractable and to gain insight, the analysis is performed for the SEFPP version. It also remains valid for the SSEFPP version as long as R_{C1} is a (small) fraction of R_{C2} and, therefore, the node at the base of Q7 will have little impact on the small-signal transfer function. Given that there are two parallel paths from the input to the output, the voltage gain of the driver can be derived using superposition

$$A_v = A_{v1}A_{v2} + A_{v3} \tag{1}$$

where $A_{v1}A_{v2}$ is the voltage gain through the linear amplifier and A_{v3} is the voltage gain through the bottom differential pair. The expression can be expanded as a function of the

transistor small-signal parameters

$$A_{v1} = -g_{m1}(R_c||1/sC_c||Z_{\text{inef}}) \quad (2)$$

$$A_{v2} = Z_L/(Z_L + 1/g_{m5}) \quad (3)$$

$$A_{v3} = -g_{m2}((1/g_{m5})||Z_L) \quad (4)$$

where g_{m1}, g_{m2}, and g_{m5} are the effective transconductances of Q1, Q2, and Q5, respectively. The effective transconductance includes the parasitic resistance in the emitter/source of the HBT/MOSFET and is always smaller than the intrinsic transconductance of the transistor [19]. R_c is the equivalent resistor at the collector node of the gain stage, and C_c is the total capacitance to ground at this node, including C_{bc4}, C_{cs4}, and C_{bc5}, but excluding C_{be5}. Z_L represents the load impedance (the optical modulator) and can be either resistive or capacitive. Z_{inef} is the impedance seen toward the base of the EF Q5. At moderate and high frequencies, it is given by

$$Z_{\text{inef}} = (1 + g_{m5}/sC_{be5})Z_L + 1/sC_{be5} \quad (5)$$

where C_{be5} is the base–emitter capacitance of Q5 and can be expressed as [19]

$$C_{be5} = \tau_f g_{m5} + C_{je}\text{AE}_5 \approx \tau_f g_{m5} \quad (6)$$

where τ_f is the total transit time of the HBT and is few hundred femtoseconds. C_{je} and AE_5 are the junction capacitance per area and the emitter area of Q5, respectively. The junction capacitance is negligible when the HBT is biased at the peak-f_T or peak-f_{MAX} current densities. Therefore, the second term can be neglected [19].

Equation (4) is strictly valid only at low frequency and ignores the impact of the base resistance of Q5, R_b(Q5), and of the collector resistance in the gain stage, R_C, which are relatively small. Since $g_{m5} \gg g_{m2}$, the gain through the second path is negligible at low and moderate frequencies. At higher frequencies, because the current gain of Q5 decreases, R_b(Q5) and R_C may contribute some peaking to A_{v3} and to the overall gain of the driver. Therefore, to first order, the first path basically determines the small-signal performance of the driver. To proceed with the analysis, the two different cases for the output load are considered separately.

1) Resistive Load ($Z_L = R_L$): This corresponds to the scenario where the circuit drives a TWE optical modulator or test equipment in a 50-Ω environment. Z_{inef} becomes

$$Z_{\text{inef}} = \frac{1 + g_{m5}R_L}{sC_{be5}}(1 + s/\omega_{z1}) \quad (7)$$

$$\omega_{z1} = \frac{g_{m5} + 1/R_L}{C_{be5}} \approx \frac{1}{\tau_f}\left(1 + \frac{1}{g_{m5}R_L}\right). \quad (8)$$

Using (3) and (6), the expression of the voltage gain becomes

$$A_v = \frac{-g_{m1}R_c\frac{R_L}{R_L+1/g_{m5}}(1+s/\omega_{z1})}{R_cC_c/\omega_{z1}s^2+(R_cC_C + R_CC_{be5}/(g_{m5}R_L)+1/\omega_{z1})s+1}. \quad (9)$$

The zero at ω_{z1} is introduced through the EF stage. However, for the resistive-load case where $R_L = 30 - 50\ \Omega$, $\omega_{z1} \approx \omega_T(HBT) \approx 330$ GHz and does not affect the small-signal transfer function. Therefore, to extend the bandwidth, inductive peaking is required to add an effective zero to the transfer function. Although A_{v2} is close to one, it decreases at large input voltage swing, reducing the maximum output swing of the driver. If the circuit has a dominant pole ($\omega_{p1} \ll \omega_{p2}$), a valid assumption for the resistive-load scenario, its expression is given by [20]

$$\omega_{p1} = \frac{1}{R_cC_c + \frac{(R_c+R_L)C_{be5}}{g_{m5}R_L}} \approx \frac{1}{R_cC_c + \tau_f\frac{(R_c+R_L)}{R_L}}. \quad (10)$$

The dominant term in the denominator is R_cC_c, which is the time constant at the collector of the gain stage. Therefore, particular attention should be paid to the layout of this very sensitive node, as any parasitics would affect the transfer function directly. The other interesting point is that, although the second term is not significant for large R_L values, a small value of the load resistance can be detrimental to the circuit bandwidth.

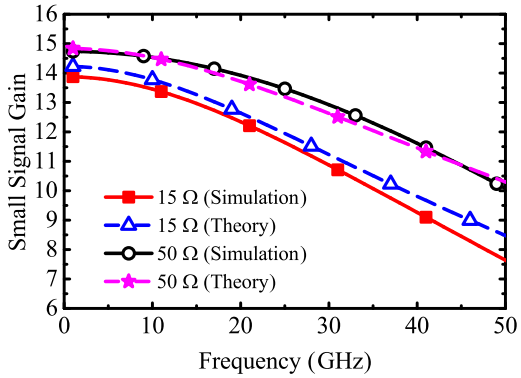


Fig. 6. Comparison of the small-signal gain predicted by (9) with that simulated using the design kit models. Different resistive loads are considered.

To validate the theoretical analysis, the small-signal response predicted by (9) is compared with simulations using the design kit models in Fig. 6. These simulations and analytical predictions refer to the circuit without inductive peaking and therefore show smaller bandwidth than that of the final circuit. The HBTs are biased at 1 mA/μm while the MOSFETs are biased at 0.25 mA/μm, for a total transistor current of 25 mA. The small-signal equivalent circuit parameters were extracted from the simulated S-parameters using the methodology described in [21] with g_{m1}, g_{m5}, and R_c of 0.11 S, 0.6 S, and 52 Ω, respectively. The base–collector capacitance per emitter length and collector–substrate capacitance per emitter length were extracted to be 1.06 and 0.875 fF/μm, respectively, resulting in $C_c = 74.875$ fF. Excellent agreement can be observed between the analytical model and design kit simulations for R_L values of 15 and 50 Ω.

2) Capacitive Load ($Z_L = 1/sC_L$): This is the case where the circuit drives short unterminated optical modulator sections. The expression of Z_{inef} becomes

$$Z_{\text{inef}} = \frac{g_{m5}}{s^2C_{be5}(C_{\text{out}} + C_L)}(1 + s/\omega_{z2}) \quad (11)$$

$$\omega_{z2} = \frac{g_{m5}}{C_{be5} + C_{\text{out}} + C_L} \quad (12)$$

where C_{out} is the parasitic capacitance at the output node of the driver, including C_{bc6} and C_{cs6}. By inserting (11) into (2), the following expression is obtained for the small-signal voltage gain of the driver circuit with capacitive load:

$$A_v = \frac{-1}{1+s/\left(\frac{g_{m5}}{C_{\text{out}}+C_L}\right)} \times \frac{g_{m1}R_c(1+s/\omega_{z2})}{\left(R_cC_{be5}\frac{C_{\text{out}}+C_L}{g_{m5}}+R_cC_c/\omega_{z2}\right)s^2+(R_cC_c+1/\omega_{z2})s+1}. \quad (13)$$

A zero now appears in the transfer function at ω_{z2}. In contrast to the resistive load scenario, the zero for capacitive load is at low frequency and contributes additional peaking to the small-signal transfer function. The value of the zero is proportional to the load capacitance and moves to lower frequencies for larger C_L. Therefore, if inductive peaking is added in series with R_C, the inductor value must be adjusted for each value of the load capacitance. For the modulator sections with very large capacitance, significant peaking will occur even in the absence of a peaking inductor in the gain stage. In these situations, the solution is to increase g_{m5} by increasing the emitter length of the EF HBT and the current in the output stage, thus moving the zero to higher frequencies.

Again, assuming that there is a dominant pole in the second-order expression in the denominator, the expressions of the poles of the driver transfer function are

$$\omega_{p1} = \frac{1}{R_cC_c+\frac{C_{\text{be}}+C_{\text{out}}+C_L}{g_{m5}}} \approx \frac{1}{R_cC_c+\frac{C_{\text{out}}+C_L}{g_{m5}}+\tau_f} \quad (14)$$

$$\omega_{p2} = g_{m5}/(C_{\text{out}}+C_L). \quad (15)$$

Similar to the resistive-load case, ω_{p1} is dominated by the R_cC_c term, which represents the time constant at the collector of the gain stage. However, the second term in ω_{p1} also has some impact, causing bandwidth degradation due to the load capacitance. By examining the expressions of the poles, it is immediately apparent that the size of the EF HBT has a crucial effect on bandwidth. In fact, an optimal size exists for Q5. Having a large EF with large transconductance reduces the second term in ω_{p1} and also increases the value of ω_{p2}, pushing the poles to higher frequencies. At the same time, a larger Q5 increases C_c through C_{bc5}. The EF stage should be biased at the peak-f_T current density to maximize its speed and linearity. Finally, unlike in the resistive-load scenario, there is no dc gain degradation through A_{v2} and higher output voltage swing is expected for a capacitive load.

As illustrated in Fig. 7, there is excellent agreement between the analytical model given by (13) and the design kit model simulations for different capacitive loads. The large capacitive load adds a low frequency zero and improves the bandwidth of the small-signal response. In these simulations, C_{out} is 48.375 fF. All the other transistor parameters used for these simulations are the same as in the previous section.

C. Large-Signal Analysis

The small-signal analysis alone is not sufficient for the design of broadband drivers. The large-signal analysis helps to set the dc current and transistor sizes in the output stage and the collector resistor values for the gain stage. The SSEFPP stage is considered for large-signal analysis.

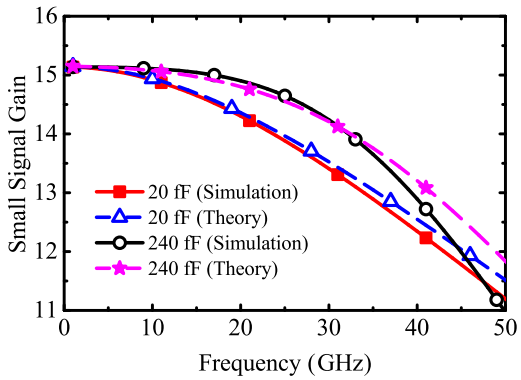


Fig. 7. Comparison of the small-signal gain predicted by (13) with that simulated using the design kit models. Different capacitive loads are considered.

For the resistive-load scenario, the minimum tail current, $I_{\text{dc,min}}$, needed in the output stage can be found as follows:

$$I_{\text{dc,min}} = \frac{V_{\max}-V_{\min}}{2R_L} = \frac{2.5\text{ V}}{60} = 42.5\text{ mA}. \quad (16)$$

In the capacitive-load case, the load capacitance and the tail current of the output stage set the slew rate, maximum output swing, and, therefore, the large-signal symbol rate of the driver. The large-signal fall time, τ_f, is inversely proportional to the dc current in the output stage

$$\tau_f = \frac{V_{\max}-V_{\min}}{I_{\text{TAIL}}}C_L. \quad (17)$$

However, the small-signal rise time, τ_r, depends on the time constant at the collector of the gain stage, as well as on the dc current through the EFs. Therefore, the EF size is the result of the tradeoff between the speed of the collector node in the linear amplifier stage and how much current it can provide to the base of the EF HBT during the rising transition.

The other important aspect of the design is the value of the resistors in the gain stage. It should be noted that the output voltage swing is also limited by the dc voltage drop on the total collector resistance $I_CR_C = I_C(R_{C1}+R_{C2})$, which should be at least 60% of the desired peak-to-peak differential output swing. The dc voltage drops V_{CE5} and V_{CE7} on the series-stacked EF HBTs are set by the values of R_{C1} and R_{C2} in the gain stage. They change dynamically as follows:

$$v_{\text{CE5}}(t) = R_{C2}i_{R_2}(t)+v_{\text{BE5}}(t)-v_{\text{BE7}}(t) > V_{\text{CEsat}} = 0.3\text{ V} \quad (18)$$

$$v_{\text{CE7}}(t) = R_{C1}i_{R_1}(t)+v_{\text{BE7}}(t) > V_{\text{CEsat}} = 0.3\text{ V}. \quad (19)$$

From (18), since $V_{\text{BE5}} \approx V_{\text{BE7}}$, V_{CE5} is equal to $R_{C2}I_{R2}$. Therefore, when the voltage waveform at the output of the gain stage goes high ($i_{R_2}(t) \to 0$), $v_{\text{CE5}}(t)$ approaches V_{CEsat}. This is not an issue in the case of the capacitive load as there is no current in the EF branch when the output voltage is at high level. However, for a resistive load, the current flows from the supply to the load resistor through the EF when the signal is at high level [minimum $v_{\text{CE5}}(t)$]. To alleviate this problem,

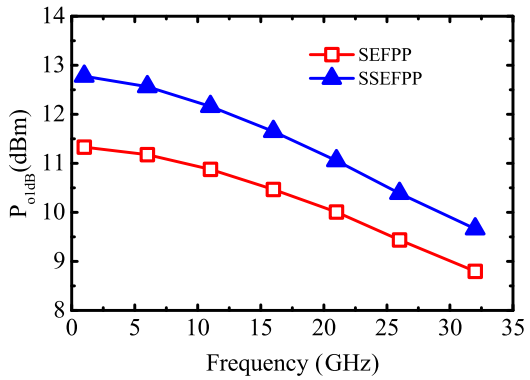


Fig. 8. Simulated 1-dB output compression point per side of the SEFPP and SSEFPP stages as a function of input sinusoid frequency.

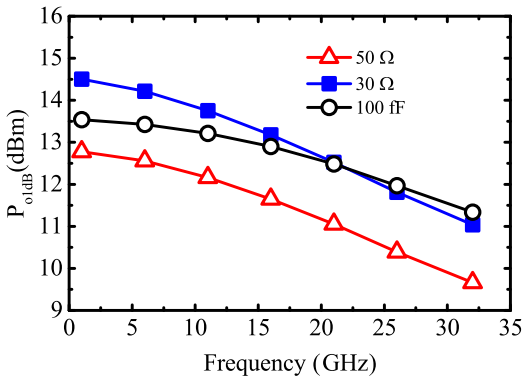


Fig. 9. Simulated output 1-dB compression point per side of the SSEFPP stage for different loads.

two measures can be taken. First, R_{C2} should be designed such that maximum possible portion of the voltage swing is applied to Q5 and only a small fraction to Q7. Second, Q5 should be large enough to be capable of providing large current even when $v_{CE5}(t)$ approaches V_{CEsat}.

This is not a problem for Q7 because $v_{CE7}(t)$ is large and can be further increased by connecting the collector of Q7 to a larger supply voltage. Therefore, Q7 in the SSEFPP driver and Q5 in the SEFPP driver must be biased at the peak-f_T current density in order to reduce the capacitance and time constant at the collector node of the gain stage. In fact, this is one advantage of the SEFPP topology compared with the SSEFPP driver.

The SSEFPP output stage shows superior linearity. When a high voltage swing is applied on an EF stage, a significant dynamic current flows through the base–emitter capacitance of the HBT, degrading the linearity of the preceding stage. This issue can be mitigated at the expense of higher power consumption by increasing the current in the preceding stage. As a result, the SEFPP driver operates with limited output voltage swing. In contrast, the SSEFPP circuit avoids this problem by distributing the voltage swing on two series-connected EFs. The linearity of both circuit topologies was simulated to illustrate this point. The 1-dB output compression point per side, $P_{o1\ \mathrm{dB}}$, is plotted in Fig. 8 as a function of the input sine-wave frequency. The maximum swing at the output of the gain stage is 3 V_{pp} per side in both topologies, but the SSEFPP driver shows higher $P_{o1\ \mathrm{dB}}$ by more than 1.5 dB. This driver topology needs a 6-V supply voltage while the SEFPP version works with two supply voltages of 5 V for the EF and 5.6 V for the gain stage, respectively. As a consequence of its higher supply voltage, the SSEFPP driver consumes more power than the SEFPP version. It should be noted that the $P_{o1\ \mathrm{dB}}$ of the SEFPP topology cannot be improved by increasing the swing at the output of the gain stage beyond 3 V_{pp}. On the contrary, the $P_{o1\ \mathrm{dB}}$ of the SSEFPP driver continues to improve as the voltage swing in the gain stage increases beyond 3 V_{pp}. Therefore, the SSEFPP topology is preferable for driving large swing optical modulators while the SEFPP version is more power efficient if an optical modulator with smaller voltage swing is available.

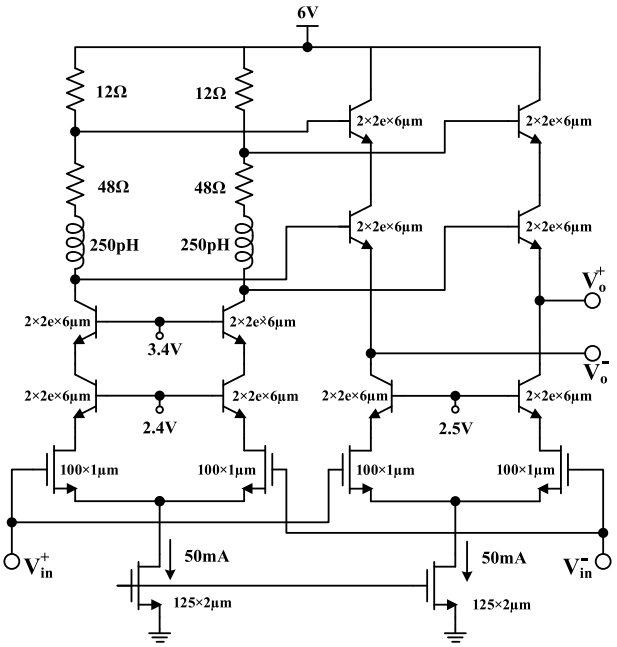


Fig. 10. Schematic of the proposed output stage.

Finally, Fig. 9 illustrates the simulated $P_{o1\ \mathrm{dB}}$ per side of the SSEFPP stage for different types of loads. The output power depends on the load. For the capacitive load, the measured voltage is converted to the power using a 50-Ω resistor. The $P_{o1\ \mathrm{dB}}$ per side for 30-Ω loads is approximately 2 dBm higher than in the case of 50-Ω loads. This proves that the output voltage swing is almost the same for 30- and 50-Ω loads. Additionally, as expected, the voltage swing on the capacitive load and, hence, $P_{o1\ \mathrm{dB}}$ are higher compared with the resistive load, especially at higher frequencies.

D. Circuit Implementation

The final driver consists of a broadband linear predriver stage and a broadband large-swing linear output stage. The schematic of the output stage is depicted in Fig. 10 and features the series-stacked differential EF for best linearity. The tail current of this stage is 50 mA, adequate for driving 30-Ω or 100-fF loads per side at 64-GBd symbol rate

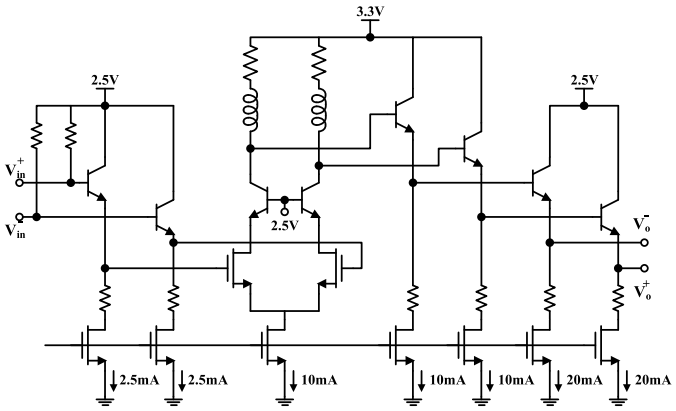


Fig. 11. Schematic of the predriver circuit.

with 5-V_{pp} differential output swing. The gain stage is designed for a swing of 3 V_{pp} per side (6-V_{pp} differential) when a signal of 600 mV_{pp} per side is applied at its input. To meet the bandwidth requirement, the tail current of the gain stage is increased to 50 mA, which makes the total collector resistance R_C small enough for 64-GBd operation.

In this design, 20% of the collector voltage swing in the linear gain stage is applied to the base of Q7 and 80% to the base of Q5. This arrangement improves the 1-dB output compression point of the SSEFPP driver by more than 1.5 dBm compared with the SEFPP version. Furthermore, since R_{C1} is small compared with R_{C2}, adding the second EF has negligible contribution to the bandwidth of the circuit. Peaking inductors are added to the double cascode gain stage primarily to compensate for the losses of the transmission lines in the optical modulator.

All HBTs are biased at the peak-f_{MAX} current density of 1 mA/μm for maximum gain and linearity. The maximum emitter length is limited to 6 μm to minimize self-heating effects. Therefore, two HBTs, each with two 100 nm $\times$ 6 μm emitter fingers, are connected in parallel. All MOSFETs have 55-nm gate length and 1 μm finger width and are biased at the peak-f_{MAX} current density of 0.25 mA/μm, which results in high gain and linearity.

The predriver schematic is shown in Fig. 11. The minimum number of stages and maximum interstage fanout were chosen, which allow to meet the bandwidth and input reflection coefficient requirements. It consists of a small-size and small bias-current input EF stage to minimize the input capacitance and maximize the input matching bandwidth, followed by a linear MOS-HBT cascode gain stage, which also provides common-mode rejection, and two cascaded EF stages needed to drive the output stage. To maximize the bandwidth while simultaneously minimizing power consumption, the transistor sizes and bias currents of each stage are scaled up by a factor of two from the input toward the output. The transistors in the cascode stage are biased at the peak-f_{MAX} current density for maximum linearity with input linear voltage swing of at least 400 mV_{pp} per side.

To verify the performance of the driver when loaded by the optical modulator, electro-optical simulations were conducted

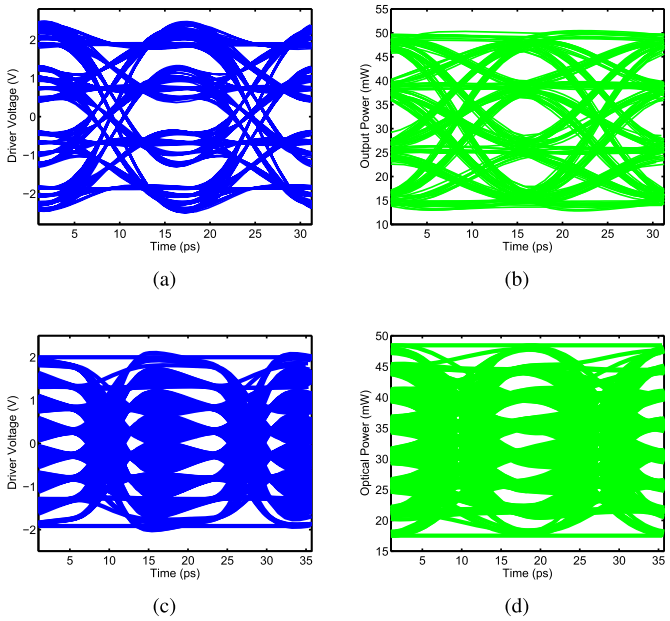


Fig. 12. Electro-optical simulations. (a) Voltage eye diagram for PAM4 at 64 GBd. (b) Optical power eye diagram for PAM4 at 64 GBd. (c) Voltage eye diagram for PAM8 at 56 GBd. (d) Optical power eye diagram for PAM8 at 56 GBd.

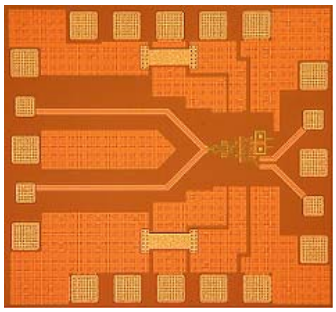


Fig. 13. Driver chip microphotograph.

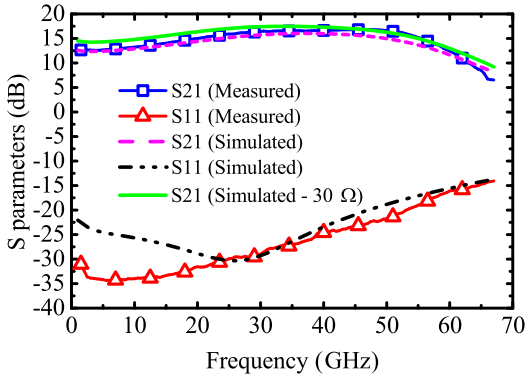


Fig. 14. Comparison of the measured and simulated single-ended S-parameters of the SSEFPP driver.

in a combined electronics-SiPh design kit. The optical modulator has the same structure as in Fig. 2 and was designed in a technology with $V_\pi L$ of 2.7 V cm. The simulated overall electro-optical bandwidth of the driver-modulator combination is 40 GHz. It was assumed that driver would be flip-chip

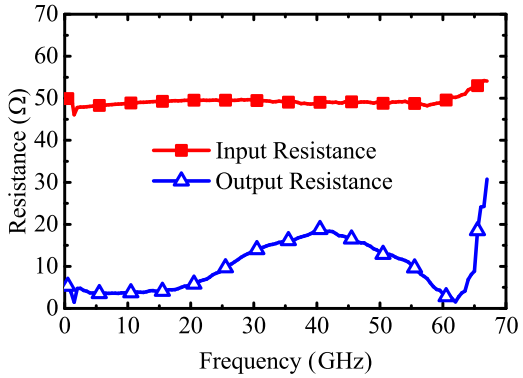


Fig. 15. Measured single-ended input and output resistance of the driver.

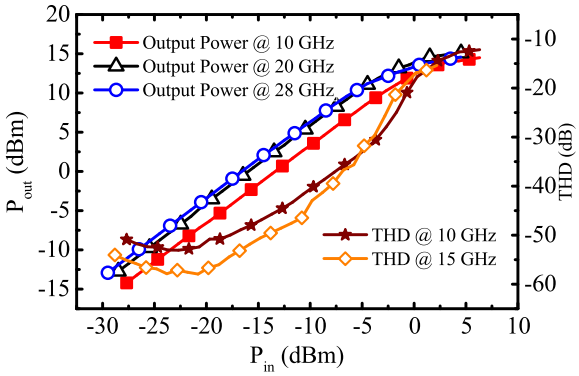


Fig. 16. Single-ended measured output power and THD as a function of input power. The circuit is driven single-endedly with the other port terminated to 50 Ω.

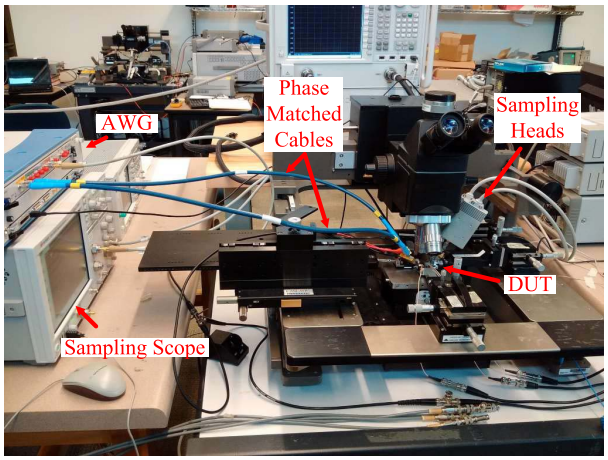


Fig. 17. Eye diagram measurement setup.

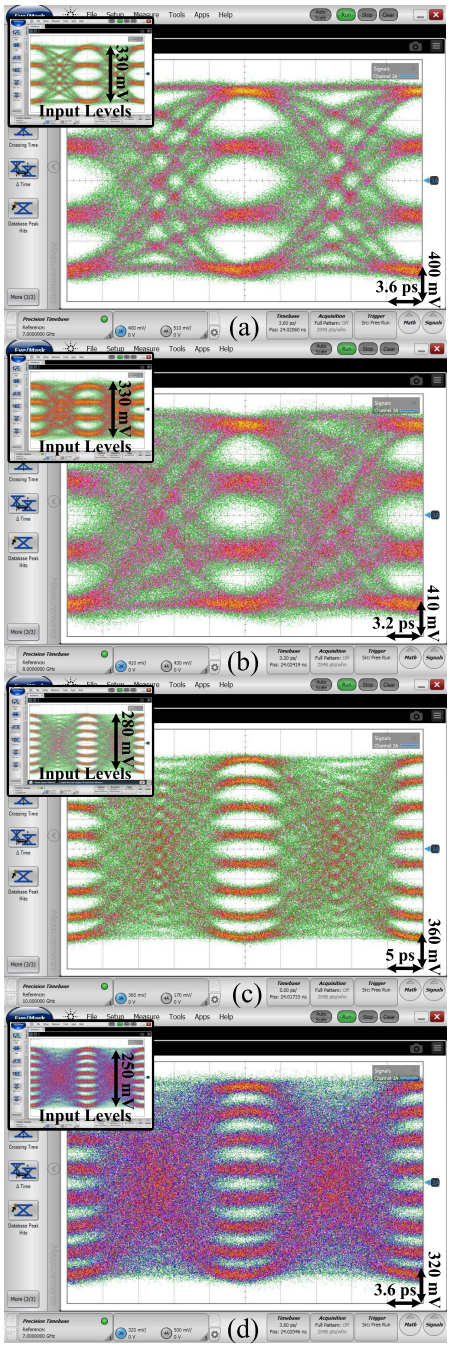


Fig. 18. Measured eye diagrams. (a) 56-GBd four-PAM. (b) 64-GBd four-PAM. (c) 40-GBd eight-PAM. (d) 56-GBd eight-PAM.

mounted on top of the optical modulator die. The interconnect and flip-chip bumps were modeled by a T-network where the total shunt capacitance is 25 fF and the total series inductance is 20 pH. Simulated electrical and optical eye diagrams are reproduced in Fig. 12 for four-PAM signals at 64 GBd and eight-PAM signals at 56 GBd. It should be noted that pre-emphasis was intentionally added at the output of the driver to compensate for the loss of the SiPh modulator electrodes. In the final fiber-optic transmitter system, the DSP and DAC will also be able to generate adequately predistorted signals at the input of the linear driver to equalize the loss of the optical modulator and compensate for driver nonlinearity.

IV. Experiment

The SEFPP and the SSEFPP chips were fabricated in a production 55-nm SiGe BiCMOS process with nine-metal back-end of line, several flavors of 55-nm MOSFETs, and SiGe HBTs. The fully wired highest speed HBTs have measured 300 and 330 GHz f_T and f_{MAX}, respectively. The die microphotograph of the fabricated SSEFPP driver is shown in Fig. 13 and occupies 0.75 mm × 0.8 mm. The die size is

TABLE I
COMPARISON WITH THE STATE OF THE ART

	This work	[4]	[5]	[16]	[10]	[12]	[2]	[22]	[23]
Technology	55-nm SiGe BiCMOS	55-nm SiGe BiCMOS	0.13-μm SiGe:C BiCMOS	0.25-μm SiGe:C BiCMOS	55-nm BiCMOS	28-nm FDSOI	0.5-μm InP HBT	0.25-μm BiCMOS	0.13-μm BiCMOS
Driver Type	Lumped, Linear, Differential	Distributed, Linear, Differential	Distributed, Linear, Differential	Lumped, Linear, Differential	Lumped, Switching, Differential	Lumped, Switching, Single-ended	Lumped, Linear, Differential	Lumped, Switching, Differential	Lumped, Linear, Differential
Bandwidth (GHz)	57.5	>70	90	32	---	17	37.8	33.7	43
Data Rate (Gb/s)	168 (56 GBaud 8-PAM)	168 (56 GBaud 8-PAM)	60 (30 GBaud 4-PAM)	50 (25 GBaud 4-PAM)	56 (NRZ)	60 (NRZ)	56 (28 GBaud 4-PAM)	40 (NRZ)	56 (28 GBaud 4-PAM)
Output Swing (Vpp)	3.8 @168 Gb/s 4.8 @128 Gb/s	3 @168 Gb/s 4.8 @120 Gb/s	3	4	1.6	4.2	3	6	0.32
P_{DC} (mW)	820/600*	1100	550	1500	300	360	730	1350	115
Area (mm^2)	0.015	1.34	1.2	-	0.38	0.22	0.7	0.72	0.056
Efficiency (pJ/bit)	4.88/3.57*	6.54	9.17	30	5.35	6	13	33.75	2.05
FOM (pJ/bit/V)	1.28/0.94*	2.18	3.06	7.5	3.34	1.42	4.33	5.63	6.41

* with/without predriver

determined by the number of pads used for on-die testing and the active are is only 0.015 mm^2.

All reported measurements were conducted on the die using mm-wave probes in a 50-Ω environment. Only the results for the SSEFPP version, which had the best linearity, are reported below. It should be noted though that the SEFPP driver had the highest bandwidth. The measured single-ended S_{11}, lower than −13 dB up to 67 GHz, and S_{21} are reproduced in Fig. 14 for the SSEFPP driver. The low-frequency gain is 12.8 dB (18.8 dB differential) with a peak value of 17 dB (23 dB differential) at 47 GHz and a 3-dB bandwidth (from dc to the frequency where the gain is less than 3 dB of the peak value) of 57.5 GHz. The peaking helps to compensate for the loss of the 50-cm-long input cables used in the eye-diagram measurement setup. The simulated S parameters of the entire driver after layout parasitics extraction are also plotted in Fig. 14, showing very good agreement with measurements. The simulated S_{21} when the driver is terminated on 30-Ω loads per side is also shown for comparison. The gain is slightly higher (14.5 dB at low frequencies) while the 3-dB bandwidth, 56 GHz, remains practically the same as for 50-Ω loads. The latter suggests that the driver can provide the same performance when loaded by the optical modulator, which typically features 30-Ω transmission lines.

The input and output resistances were also extracted from the S-parameter measurements and are reproduced in Fig. 15. The input resistance is close to 50 Ω over the entire measurement bandwidth. As expected, the output resistance is very low, between 5 and 20 Ω, making the driver suitable of driving the optical modulator with 30-Ω transmission lines without the need for on-chip matching resistors.

Fig. 16 shows the measured output power and total harmonic distortion (THD) at different input sine-wave frequencies as a function of the input signal amplitude. The measured input and output compression points at 10 GHz are −0.3 and 12 dBm per side, respectively. THD remains better than 30 dB up to −5-dBm inputs and is less than −15 dB up to an input power of 0 dBm.

Large-signal eye diagram measurements were performed with a 92-GS/s arbitrary waveform generator (AWG) and a 70-GHz bandwidth sampling oscilloscope, as shown in Fig. 17. The differential signal from the AWG was connected to the circuit through two 50-cm-long phase-matched coaxial cables. The differential output signal from the circuit was connected through series capacitors and 20-dB attenuators to the 70-GHz bandwidth remote heads of the sampling oscilloscope. The remote heads and the attenuators were mounted directly on the probe to minimize the output loss. The 20-dB attenuators are needed to avoid damaging the remote heads. In order to determine the exact output swing at the circuit pad, the losses at the output of the test setup were measured using a two-tier VNA calibration and then removed. The output eye diagrams were measured with PRBS-15 patterns at 40–64 GBd. Fig. 18 shows the measured output eye diagrams for 56-GBd four-PAM, 64-GBd four-PAM, 40-GBd eight-PAM, and 56-GBd eight-PAM signals with single-ended output voltage swings of 2.4, 2.4, 2.1, and 1.9 V_{pp}, respectively. The 64-GBd and 56-GBd eight-PAM eye diagrams are jitter-limited by the ENOB of the AWG used to generate the input signals. The driver operates in its linear region at the input levels shown as insets in Fig. 18. Some linear predistortion was applied to the input signal to compensate for the losses of the input cable and probe used in the measurement setup. In the final system, where the optical modulator is integrated with driver, this linear predistortion would be applied by the DSP and DAC to optimize the optical eyes at the output of the modulator.

The total power consumption of the driver is 820 mW, of which 220 mW is consumed by the predriver, resulting in an output stage energy efficiency of 3.57 pJ/b at a data rate of 168 Gb/s.

Finally, bit error rate (BER) measurements were performed for NRZ signals using a 64-Gb/s BERT. The BER measurement was conducted for PRBS15 patterns and is illustrated in Fig. 19 for 40-, 56-, and 64-Gb/s data rates. The measured BER is better than 10^{-12} up to 64 Gb/s, the

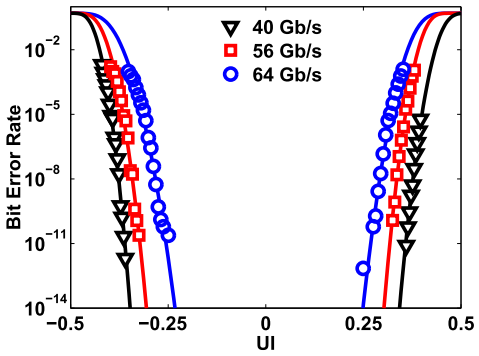
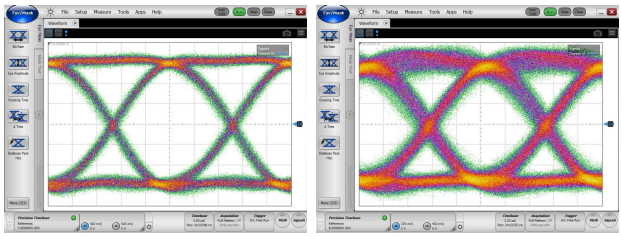


Fig. 19. Measured BER for NRZ modulation at 40, 56, and 64 Gb/s.



(a) (b)

Fig. 20. Measured eye diagrams. (a) Voltage eye diagram for NRZ at 56 Gb/s. (b) Voltage eye diagram for NRZ at 64 Gb/s.

maximum range of the BERT. The corresponding measured eye diagrams at 56 and 64 Gb/s are shown in Fig. 20.

V. Conclusion

A new linear push–pull large-swing driver topology was proposed based on series-stacked EF and MOS-HBT cascode topologies. Detailed small-signal and large-signal analyses, supported by analytical equations and transistor-level simulations, were conducted to illustrate the advantages of the new stage compared with more tradition linear and switching driver topologies. Two versions of the proposed driver, with single-EF and with series-stacked EF topologies, were designed and manufactured in a production 55-nm SiGe BiCMOS technology. The SSEFPP circuit achieved record 4.8 V_{pp} differential output swing with 56- and 64-GBd four-PAM signals, and eight-PAM 56-GBd operation for a record aggregate data rate of 168 Gb/s.

Table I summarizes the performance and compares it with the state of the art. Although the linear distributed driver in [4] has larger bandwidth and can operate at 120 Gb/s with NRZ signals, the lumped driver topology proposed in this paper occupies significantly smaller area and achieves the same maximum data rate and output swing with lower power consumption and better linearity, which results in higher output swing for m-PAM formats. Therefore, the proposed driver shows the best figure of merit (FOM) defined as energy efficiency per bit per output swing.

Acknowledgment

The EMX simulation software was provided by Integrand Software, Inc. The authors would like to thank J. Pristupa and CMC for CAD tools and CAD support.

References

[1] C. Laperle, N. Ben-Hamida, and M. O'Sullivan, "Advances in high-speed DACs, ADCs, and DSP for software defined optical modems," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2013, pp. 1–4.

[2] M. Nagatani, Y. Bouvier, H. Nosaka, and K. Murata, "A 3-Vppd 730-mW linear driver IC using InP HBTs for advanced optical modulations," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2013, pp. 1–4.

[3] S. Shahramian *et al.*, "A 112Gb/s 4-PAM transceiver chipset in 0.18 μm SiGe BiCMOS technology for optical communication systems," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2015, pp. 1–4.

[4] R. J. A. Baker, J. Hoffman, P. Schvan, and S. P. Voinigescu, "SiGe BiCMOS linear modulator drivers with 4.8-V_{pp} differential output swing for 120-GBaud applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 1–4.

[5] P. Rito, I. G. López, A. Awny, A. C. Ulusoy, and D. Kissinger, "A DC-90 GHz 4-Vpp differential linear driver in a 0.13 μm SiGe:C BiCMOS technology for optical modulators," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1–4.

[6] A. Balteanu, P. Schvan, and S. P. Voinigescu, "A 6-bit segmented DAC architecture with up to 56-GHz sampling clock and 6-V_{pp} differential swing," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 881–891, Mar. 2016.

[7] T. Kishi *et al.*, "56-Gb/s optical transmission performance of an InP HBT PAM_4 driver compensating for nonlinearity of extinction curve of EAM," *J. Lightw. Technol.*, vol. 35, no. 1, pp. 75–81, Jan. 1, 2017.

[8] A. Shastri *et al.*, "Ultra-low-power single-polarization QAM-16 generation without DAC using a CMOS photonics based segmented modulator," *J. Lightw. Technol.*, vol. 33, no. 6, pp. 1255–1260, Mar. 15, 2015.

[9] I. G. López *et al.*, "High-speed ultralow-power hybrid optical transmitter module with InP I/Q-SEMZM and BiCMOS drivers with 4-b integrated DAC," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4598–4610, Dec. 2016.

[10] E. Temporiti *et al.*, "Insights into silicon photonics Mach–Zehnder-based optical transmitter architectures," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3178–3191, Dec. 2016.

[11] I. Sarkas, A. Balteanu, E. Dacquay, A. Tomkins, and S. Voinigescu, "A 45 nm SOI CMOS class-D mm-wave PA with >10 V_{pp} differential swing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 88–90.

[12] S. Shopov and S. P. Voinigescu, "A 3×60 Gb/s transmitter/repeater front-end with 4.3 V_{pp} single-ended output swing in a 28 nm UTBB FD-SOI technology," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1651–1662, Jul. 2016.

[13] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT/370 GHz fMAX HBT and high-Q millimeter-wave passives," in *IEDM Tech. Dig.*, Dec. 2014, pp. 3.9.1–3.9.3.

[14] A. Zandieh, P. Schvan, and S. Voinigescu, "57.5 GHz bandwidth 4.8 V_{pp} swing linear modulator driver for 64 GBaud m-PAM systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1–4.

[15] G. Denoyer *et al.*, "Hybrid silicon photonic circuits and transceiver for 50 Gb/s NRZ transmission over single-mode fiber," *J. Lightw. Technol.*, vol. 33, no. 6, pp. 1247–1254, Mar. 15, 2015.

[16] P. Rito *et al.*, "A monolithically integrated segmented linear driver and modulator in EPIC 0.25-μm SiGe:C BiCMOS platform," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4561–4572, Dec. 2016.

[17] N. Wolf *et al.*, "Electro-optical co-design to minimize power consumption of a 32 GBd optical IQ-transmitter using InP MZ-modulators," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2015, pp. 1–4.

[18] K. M. Sharaf and M. I. Elmasry, "Active-pull-down nonthreshold logic BiCMOS circuits for high-speed low-power applications," *IEEE J. Solid-State Circuits*, vol. 30, no. 6, pp. 691–695, Jun. 1995.

[19] S. Voinigescu, *High-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 2013.

[20] P. R. Gray, P. J. Hurst, R. G. Meyer, and S. H. Lewis, *Analysis and Design of Analog Integrated Circuits*. Hoboken, NJ, USA: Wiley, 2001.

[21] S. P. Voinigescu *et al.*, "Characterization and modeling of an SiGe HBT technology for transceiver applications in the 100–300-GHz range," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4024–4034, Dec. 2012.

[22] C. Knochenhauer, J. C. Scheytt, and F. Ellinger, "A compact, low-power 40-GBit/s modulator driver with 6-V differential output swing in 0.25-μm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1137–1146, May 2011.

[23] G. Belfiore, L. Szilagyi, R. Henker, U. Jörges, and F. Ellinger, "Design of a 56 Gbit/s 4-level pulse-amplitude-modulation inductor-less vertical-cavity surface-emitting laser driver integrated circuit in 130 nm BICMOS technology," *IET Circuits, Devices Syst.*, vol. 9, no. 3, pp. 213–220, 2015.

Alireza Zandieh (GS'12–M'13) received the B.A.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2010, and the M.A.Sc. degree from the University of Waterloo, Waterloo, ON, Canada, in 2013. He is currently pursuing the Ph.D. degree under the supervision of Prof. S. Voinigescu at the University of Toronto, Toronto, ON, Canada, where he is involved in silicon photonics front-end circuits.

From 2013 to 2015, he was with TeTechS, Inc., Waterloo, where he was responsible for projects in high-frequency sensors and imaging systems. His current research interests include the design of high-speed and millimeter-wave integrated circuits.

Peter Schvan (M'89) received the M.S. degree in physics and Ph.D. degree in electronics in 1985.

He then joined Nortel, where he was involved in device modeling, CMOS, and BiCMOS technology development followed by circuit design for fiber-optic and wireless communication using SiGe, BiCMOS, InP, and CMOS technologies. Currently, he is the Director of analog design with Ciena, Ottawa, ON, Canada, where he is involved in the development of broadband amplifiers and high-speed A/D and D/A converters. He has authored or co-authored over 40 publications and has given several workshop presentations.

Sorin P. Voinigescu (M'90–SM'02–F'17) received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, toronto, ON, Canada, in 1994.

He holds the Stanley Ho Chair in Microelectronics and is the Director of the VLSI Research Group in the Electrical and Computer Engineering Department at the University of Toronto, which he joined in 2002. During the 1984-1991 period, he worked in microwave and quantum semiconductor device and circuit research, and as an Assistant Professor in Bucharest. Between 1994 and 2002, he was first with Nortel and later with Quake Technologies in Ottawa, ON, Canada. In 2008–2009 and 2015–2016, he spent sabbatical leaves at Fujitsu Laboratories of America, Sunnyvale, CA, at NTT's Device Research Laboratories in Atsugi, Japan, at UNSW in Sydney, Australia, and at Robert Bosch GmbH in Germany, exploring technologies and circuits for 128 GBaud fiber-optic systems, 300Gb/s mm-wave radio transceivers, imaging and radar sensors. He co-founded and was the CTO of two fabless semiconductor startups: Quake Technologies and Peraso Technologies. He was a member of the International Technology Roadmap for Semiconductors RF/AMS Committee between 2008 and 2015, served on the TPC and ExCom of the IEEE CSICS from 2003 until 2013, and is a member of the ExCom of the IEEE BCTM. He received NORTELs President Award for Innovation in 1996 and is a corecipient of the Best Paper Award at the 2001 IEEE CICC, the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won several Best Student Paper Awards at IEEE VLSI Circuits Symposium, IEEE IMS, IEEE RFIC, and IEEE BCTM. In 2013 he was recognized with the ITAC.