Channel Equalizer in 0.13 SiGe BiCMOS

By

Andreea Balteanu

A thesis submitted in conformity with the requirements

for the degree of Master of Applied Science

Graduate Department of Electrical and Computer Engineering

University of Toronto

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Abstract

Double spaced.

Acknowledgements

Foremost, I would like to thank Professor Sorin Voinigescu for his guidance and supervision. His knowledge, dedication and hands-on approach to research have taught me a great deal throughout these past two years.

I would like to thank all my colleagues and friends in BA4182 who made thing bearable during the all nighters: Ricardo Aroca, Adam Hart, Mehdi Khanpour, Ekaterina Laskin, Sean Nicolson, Ioannis Sarkas, Shahriar Shahramian, Alexander Tomkins and Kenneth Yau. I would especially like to thank Ricardo and Ken for helping me measure and Ioannis for moral support.

This work would not have been possible without the generous support of the National Science and Engineering Research Council (NSERC), STMicroelectronics and Gennum Corporation. I also thank Canadian Microelectronics Corporation (CMC) for providing the CAD tools and Jaro Pristupa for his impeccable support. I would also like to thank Professors XX, XX and XX for serving on the supervising committee for this thesis.

Most of all, I would like to thank my fabulous parents, Liliana and Florinel for their love and support.

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1 Introduction

1.1 Motivation

Consumer demands have fuelled the growth in high speed communications while scaling of semiconductor technologies have allowed for rapid grown in computing and data transmission capabilities. The bottleneck now is the limitations of the channel bandwidth. Future generations of the HDTV standard at 6 Gbps and beyond have triggered the need to transmit increasingly higher data rates over existing coaxial cable connections originally designed for 1.5-Gbps operation. When several 6-Gbps HDTV signals are multiplexed, the aggregate serial data rate can quickly rise up to 50 Gbps. Many physical effects such as skin effect, dielectric loss and reflections associated with impedance mismatches severely limit the ability of the channel to function in the GHz range. Although optical links can be used to increase communication speeds, it is more cost effective to improve the operation of the currently installed coaxial cable infrastructure.

It has been shown that equalizers can be used to improve transmission rates over bandwidth limited channels when placed in the transmitter [Aroca, Katya], receiver [Balteanu, Altan, Dickson, Nakamura, Garg], or in both the transmitter and receiver [Bulzacchelli]. Since the exact channel characteristics are not known, using an adaptive equalizer in the receiver is desirable in order to compensate for actual channel characteristics.

1.2 Outline

The thesis concentrates on the design and measurement of a receive equalizer and retimer which were fabricated as separate chips for testing purposes. In Section 2, the equalizer architecture is presented followed by measurement results in Section 3. The retimer design is described Section 4 while the test circuit and measurement results can be seen in Section 5. Conclusions are offered in Section 6.

1.3 Background

The finite bandwidth of the transmission mediums such as copper interconnects gives rise to a phenomenon called intersymbol interference (ISI) in which the signal level of the current bit is affected by the values of the previously transmitted bits (postcursor ISI) and the values of the succeeding bits (precursor ISI). A transmission system typically has a latency of many bits, hence precursor ISI does not violate causality. A graphical depiction of non-return to zero (NRZ) signal transmitted over an infinite and a finite bandwidth channel can be seen in Figure 1.1. The ISI degrades the eye at the receiver and depending on the severity, the eye can even be closed making data recovery impossible.

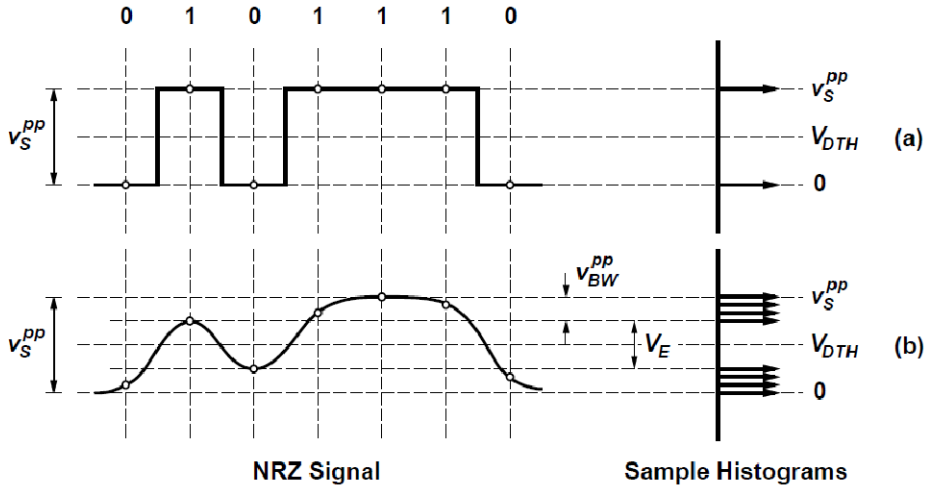


Fig. 4.21 NRZ signal at the decision circuit of (a) an infinite-bandwidth receiver and (b) a finite-bandwidth receiver.

Figure 1.1: A NRZ signal after (a) an infinite bandwidth channel and (b) a finite-bandwidth receiver. (Make own picture and add eyes)

Unlike noise which is unpredictable, ISI depends on the data as well as the transmission medium, making it deterministic and hence reversible. An equalizer can be used to mitigate the ISI and improve the effective bandwidth for a channel. It is well established that the highest theoretical performance can be achieved using maximum likelihood sequence estimation (MLSE) [Forney, MacPerson, Sackinger]. The continuous time approach requires an analog to digital convertor

(ADC) at the receiver after which a digital signal processor (DSP) is used. Although ADCs functioning at above 40 GSamples/s [Cheng] exist and such a system has been proven to work at 10 Gbps [Kupfer], designing the high speed ADCs is complex and requires a large chip area making this approach not suitable for high speed communication. In the alternate, discrete time approach, the signal is sampled using a track and hold amplifier and then the data is processed using analog techniques. High speed track and hold amplifiers have been proven to work at above 40 GSamples/s [Shahramian], however their power and size requirements also make this approach undesirable.

A more common approach is the use of a filter before the decision circuit. The filter must be adaptive in order to be able to function without foreknowledge of the channel. A common implementation is a feed-forward equalizer (FFE), also known as a transversal filter or finite impulse response (FIR) filter. In this implementation, the input is feed into a series of delay lines the output of which is multiplied by a pre-determined coefficient after which all the outputs are summed together and passed to the decision circuit. The coefficients are determined based on the transmission channel. When the delay lines are equivalent to one bit period, the system is known as a synchronous equalizer. A fractional equalizer is when the delays are less than one bit period, the advantage of is that is also improves the horizontal eye opening, not just the vertical eye opening as is the case with the synchronous equalizer [Sackinger]. The FFE can be used to mitigate precursor ISI while a decision-feedback equalizer (DFE) can be used to mitigate postcursor ISI without amplifying noise. The DFE consists of a feedback path from the output of the decision circuit back to the summation node. If the previous bit was a one, the current bit under consideration is reduced by α_4 and if the previous bit was a zero, the current bit is increased by α_4. Non linear effects associated impedance mismatches due to chip packages and connectors can be corrected using the DFE. The combination a FFE and DFE can address both precursor and postcursor intersymbol interference. A system consisting of a three tap FFE and a two tap DFE can be seen in Figure 1.2. The weighting coefficients for the FFE and DFE can be controlled using algorithms such as Least-Mean-Square and Recursive Least Square [Kim]. The adaptive equalizer approximates the inverse characteristic of the channel, restoring the high frequency signal and reducing ISI.

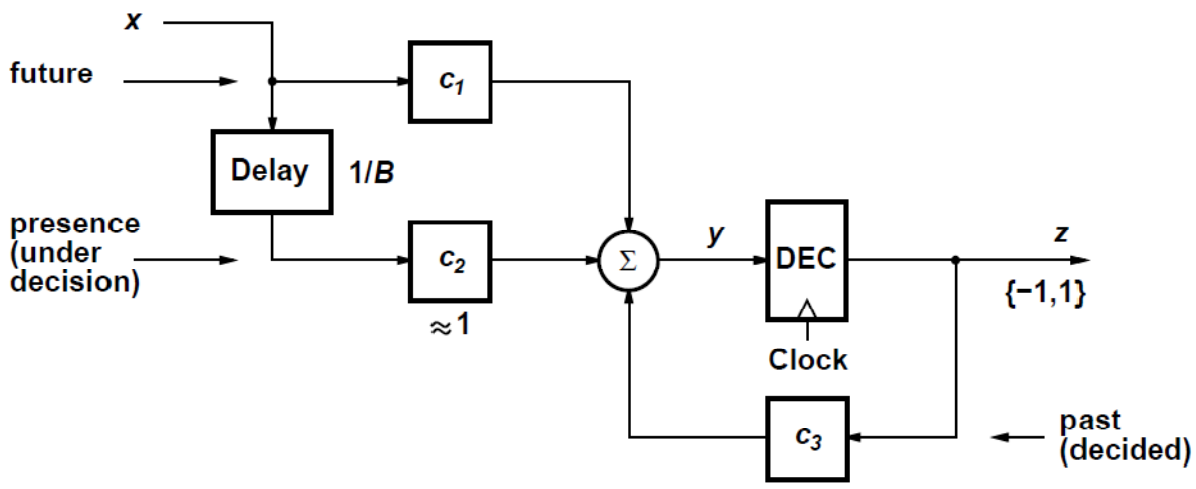


Figure 1.2: An equalizer system consisting of a three tap FFE and a two tap DFE. (make!!!)

The FFE can be implemented using either a digital or an analog architecture. The digital implementation however suffers from the same short falls as the MLSE architecture, namely the difficulty in creating a high speed ADC or track and hold amplifier. For high speed applications, the FFE is commonly implemented using a continuous time analog architecture. In [MacPerson], a continuous time approach consisting of an automatic gain control (AGC) stage followed by a FFE and a DFE is employ to achieve 10 Gbps data rates. The most challenging part in designing an analog FFE is creating wide-bandwidth delay structures. Often, and as is the case in [MacPerson, Altan, Ricardo], the delays are implemented using microstrip transmission lines. When compared to transistor based implementations, the microstrip delay elements have higher bandwidth, zero power dissipation, less group delay, however they occupy a large area, sometime much bigger than the area occupied by the actual transistors. In order to minimize area, the lines are often bent making them harder and less accurate to model. In addition, they introduce frequency dependent loss and group delay variation. Nevertheless a transversal filter operating at 49 Gbps was reported in [Altan] using a SiGe BiCMOS technology.

One impediment to high speed operation for the DFE is the feedback propagation time. In [Katsturia] a look-ahead architecture is proposed which relaxes the timing constraints. The architecture makes a tentative decision assuming the previous bit was “zero” and another decision assuming that the previous bit was a “one”. The correct result is then selected using a

shorter feedback look. This architecture however employs three flip flops in order to make the correct decision. At high frequencies, this becomes quite taxing on the distribution network. In [Garg] two of the flip flops are replace with a cascade of three ECL buffers that act as slicers thus reducing the complexity of the clock path. Data rates of up to 40 Gbps were achieved using this architecture.

In order to alleviate the large area requirements due to the microstrip delay lines in the FFE and the timing constraints due to the feedback path in the DFE, a frequency domain adaptive equalizer is proposed, also known as Bode equalizer. The equalizer functions by providing the inverse of the channel response, namely by providing peaking at high frequencies in order to alleviate the channel losses. Several such equalizers have been published. In [Yasumoto] a Cherry Hopper topology was employed to realize the adjustable equalizer. The high frequency peaking was constant while the low frequency gain can be adjusted in order to generate the required inverse channel response as seen in Figure 1.3.a. The adjustment in gain is done by changing the tail current which is undesirable since the transistors would no longer be biased at their peak f_T current density thus degrading the amplifier bandwidth. Another approach [Zhang] is to have a flat response amplifier in parallel with a tuned amplifier as seen in Figure 1.3.b. The difficulty in such an approach is to match the delay between the flat response path and the tuned path. Mismatches in these delays can cause jitter and further reduce the eye horizontal opening and thus decrease the maximum achievable bandwidth. A better approach is to combine the flat response path and the tuned path into one stage as seen in Figure 1.3.c [Balteanu, Oshito, Shakiba, Cordell, Kiaei]. This approach is further developed in Section 2.

As is the case with many equalizer, the output eye exhibits significant jitter and therefore a retimer should be used at the output of the equalizer to reduce jitter. The retimer can also be used in a feedback configuration in order to implement a one tap DFE as seen in Figure 1.4. This decreases the bandwidth due to the feedback path and the addition of the summation node at the input of the retimer. A look-ahead topology as proposed in [Adesh] can be used to further increase the bandwidth. The DFE provides further equalization without amplifying the noise while the retiming reduces the jitter of the signal. If the clock signal is recovered from the transmitted signal using a clock and data recovery system (CDR), the jitter is further reduce by ensuring that the retimer is triggered at the center of the eye, regardless of drift in the transmitter

frequency. In order to measure the effect of the Bode equalizer and the maximum operating frequency of the retimer, the two circuits were fabricated separately.

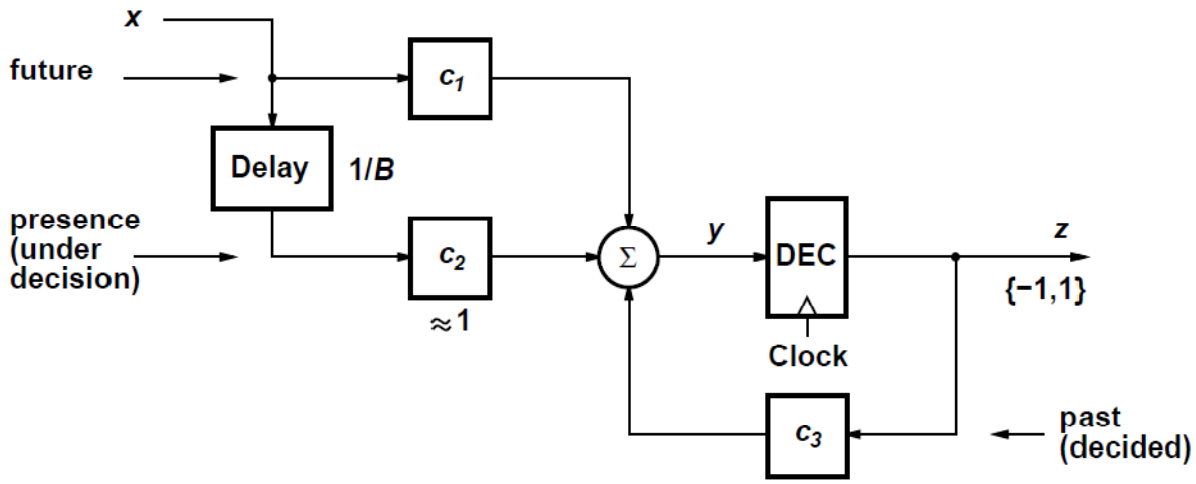


Figure 1.3: PALCEHOLDER Examples of Bode Equalizers (a), (b) (c).

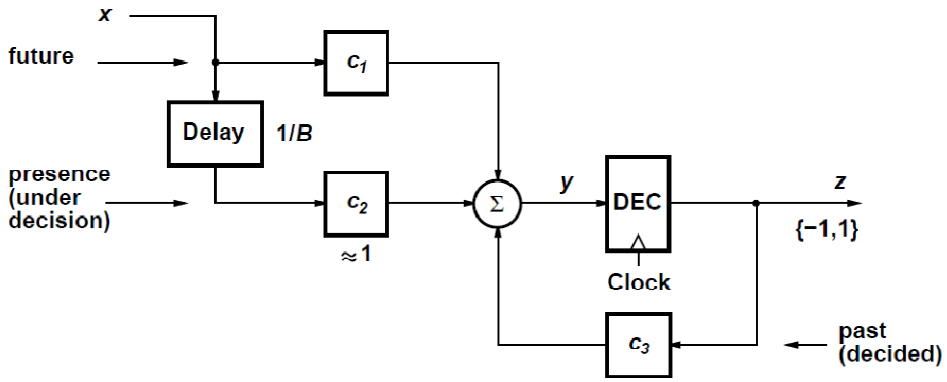


Figure 1.4: PALCEHOLDER Proposed equalizer with a one tap DFE.

2 Equalizer Design

The first step in designing a channel equalizer is to characterize the transmission medium. For a wireline transceiver the cable electrical characteristic dictates the equalization requirements. After the transmission cable is characterized, the equalizer and system can then be designed.

2.1 Cable Characteristics

It is not known before hand what cable length or type the user will employ, therefore several cables must be measured. For the purpose of this experiment, three cables of different qualities and lengths were measured: a 10-m Belden cable with two BNC-to-K transitions and two K-to-V transitions, a 1.8-m SMA cable consisting of two cascaded 90-cm SMA cables with K-to-V transitions on each side and one K-to-K connector, and a 1-m long V cable. The cable frequency response can be seen in Figure 2.1. As expected, the cable exhibits a linear loss with frequency.

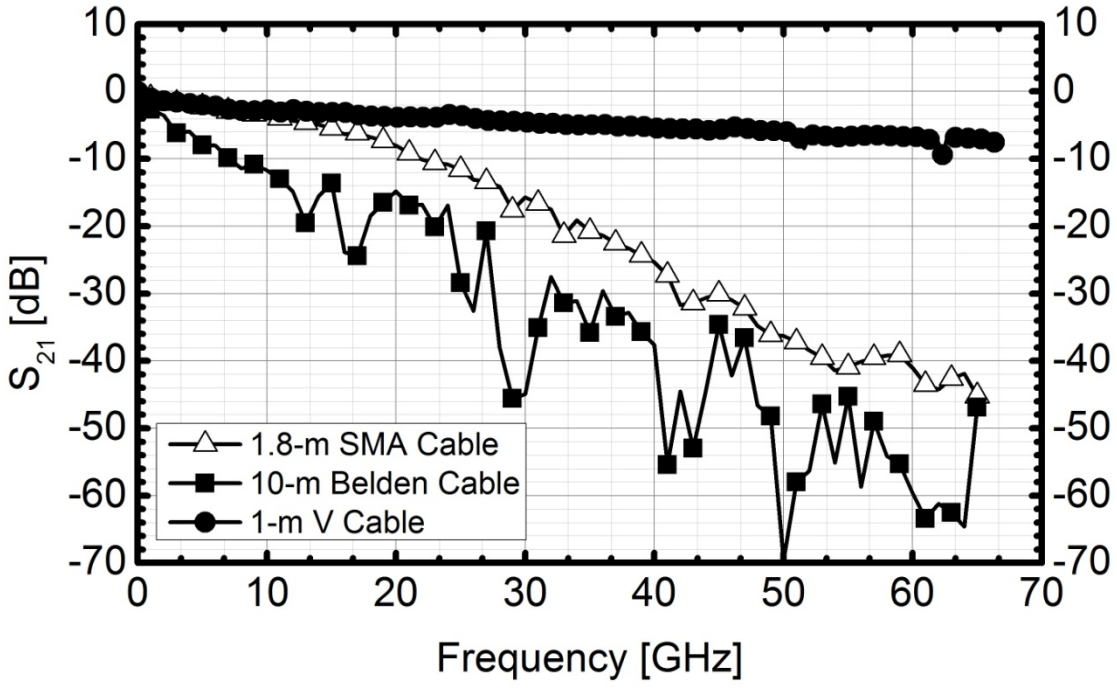


Figure 2.1: Measurements of the cables used in the equalization experiments.

While the cable bandwidth causes vertical distortion in the eye diagram, horizontal distortion in the form of data-dependent jitter occurs when the cable is not phase linear. Phase linearity is the variation in group delay with frequency given by [Sackinger]:

$$\tau(\omega) = -\frac{d\Phi}{d\omega} \tag{2.1}$$

Where $\tau(\omega)$ is the frequency dependent group delay, Φ is the phase in radians and ω is the radian frequency. For a given cable length, the group delay can be approximated using [Pozar]:

$$Group\ Delay \approx \frac{l \times \sqrt{\varepsilon_r}}{c} \tag{2.2}$$

where l is the cable length, c is the speed of light and $\sqrt{\varepsilon_r}$ is the relative permittivity of the dielectric. For the 1-m V cable, the dielectric is low density polytetrafluoroethylene (PTFF), therefore $\varepsilon_r = 1.5$ [www.micro-coax.com] corresponding to a group delay of 4.1 ns. The 1.8-m cable has a dielectric filled with Teflon, hence $\varepsilon_r = 2.08$ [Pozar] corresponding to a group delay of 8.7 ns. The 10-m cable uses polyethylene as the dielectric corresponding to a permittivity of 2.25 and a group delay of 50 ns. The group delay for the cables was calculated using the measured S parameters which were taken at 4 MHz intervals from 1 GHz to 50 GHz. The S_{21} phase was unwrapped and then the derivative with respect to frequency was taken. The cable group delay is plotted in Figure 2.2. Due to the limitations of the test equipment, the group delay for the 10-m cable could not be measured. At low frequencies, the group delay for the 1-m V cable is roughly 4.1 ns and the group delay for the 1.8-m SMA cable is 7.85 ns. These measurements vary slightly from the hand calculations because the dielectric is not constant throughout the entire cable and hence the relative permittivity varies. After 25 GHz, the group delay measurements for the 1.8 cm SMA cable are no longer accurate due to the high loss of the cable, and the sensitivity of the equipment. In addition, as the frequency and cable length increase, measurements have to be taken at much finer interval steps for the group delay to be accurate.

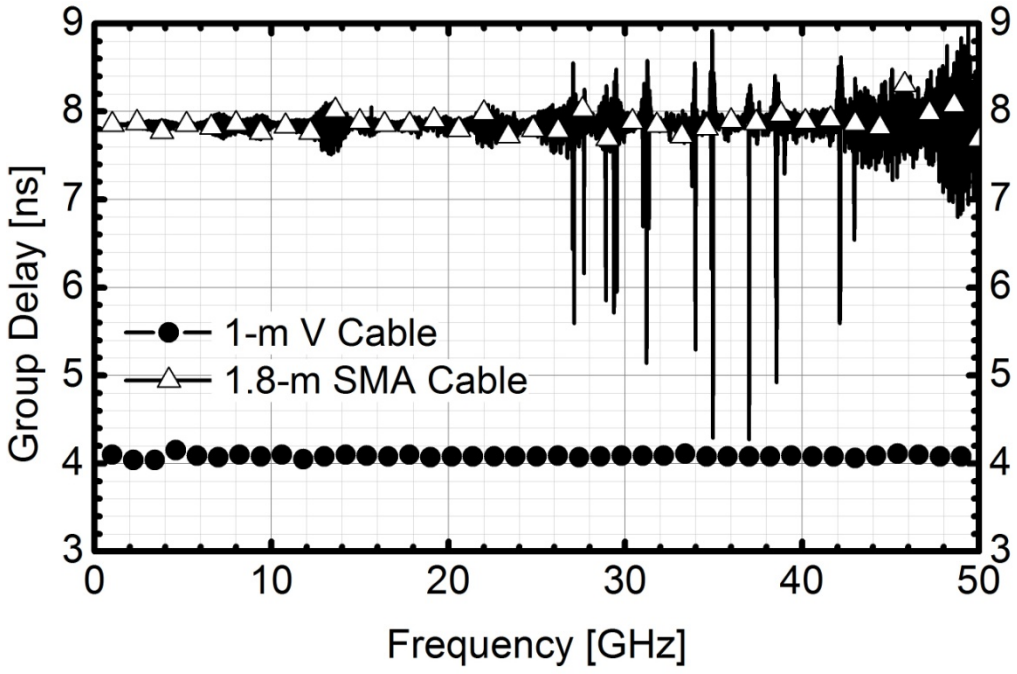


Figure 2.2: Group delay for cables used in equalization experiment.

In order the limit the data dependent jitter, a group delay variation of less than 10% of the bit period (UI) over the desired bandwidth is needed [Sakinger]. The group delay variation ($\Delta\tau$) for the 100cm V cable is 435 ps (which corresponds to 230 GHz when using the 10% rule) up to 50 GHz hence there is no need for phase equalization at data rates below 50 GHz. The 180cm SMA cable has a $\Delta\tau$ of 600 ps (167 GHz using the 10% rule) up to 25 GHz.

2.2 Equalizer System

The cable loss characteristics can be modeled as a function of frequency [Shakiba]:

$$C(f) = e^{-k_s l(1+j)\sqrt{f} - k_d f} \tag{2.3}$$

where k_s is the skin effect constant, k_d is the dielectric constant and l is the cable length. Equalization can be achieved by implementing a circuit whose frequency response is the inverse of (2.3). The latter can be described by the superposition of two functions, one that has constant gain over frequency and one whose gain increases exponentially with frequency:

$$\mathrm{H}(s) = G_{DC} + G_{HF} \frac{(s+\alpha_1)(s+\alpha_2)\cdots(s+\alpha_n)}{(s+\gamma_1)(s+\gamma_2)\cdots(s+\gamma_n)(s+\gamma_{n+1})} \tag{2.4}$$

where G_{DC} is the DC gain, G_{HF} is a scaling constant for the frequency dependent gain term, and α_n and γ_n are the zeros and poles of the frequency dependent term, chosen to best match the inverse of the cable response.

The equalizer bandwidth must be made sufficiently wide so that it does not further distort the signal, however too large a bandwidth results in too much noise getting passed to the decision circuit reducing the signal-to-noise ratio (SNR) of the system. The optimum 3-dB bandwidth is between 60% and 70% of the bit rate [Sackinger] meaning that a 50 GHz bandwidth equalizer can be used for up to 70 Gbps data. By adding 30 dB of adjustable peaking at roughly 50 GHz, the 3 dB bandwidth can be extended to above 40 GHz for the 100 cm cable and above 30 GHz for the 180 cm cable.

2.3 Equalizer Stage

A gain of 30 dB cannot be obtained from a single stage, however the effort can be broken over multiple equalization stages. The equalization function was realized physically with the circuit illustrated in Figure 2.3 where all transistors have 0.13µm emitter width and $Q_{1\text{-}4}$ are each 0.13 µm x 2 µm. The equalizer stage consists of two differential transconductor stages and two Gilbert cells which act as a weighted current adder.

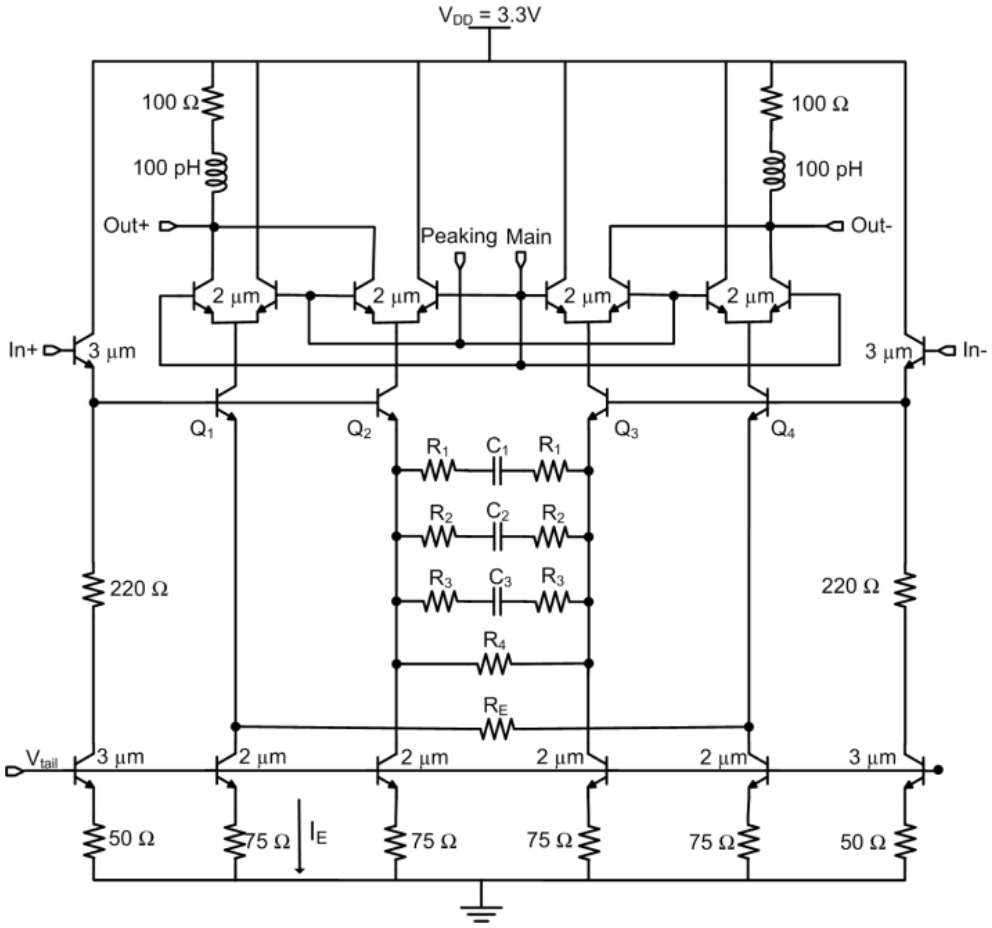


Figure 2.3: Equalizer stage schematic.

The current per side at the output of the first transconductor (Q_1, Q_4) is given by:

$$i_1 = \frac{g_m}{(Z_{CS} \parallel \frac{R_E}{2})g_m + 1} v_i \tag{2.5}$$

while the current at the output of the second transconductor (Q_2, Q_3) is described by:

$$i_2 = \frac{g_m}{(Z_{CS} \parallel \frac{Z_E}{2})g_m + 1} v_i \tag{2.6}$$

where g_m is the transconductance of $Q_{1\text{-}4}$, Z_{CS} is the impedance of the current source (ideally much larger than R_E and Z_E), R_E is the emitter degeneration resistance in the first transconductor and Z_E is the frequency dependent emitter degeneration impedance in the second transconductor.

It must be noted that, in this implementation:

$$Z_E \rightarrow R_4 \; as \; f \rightarrow 0 \; Hz \tag{2.7}$$

As the frequency increases, Z_E decreases thus producing peaking at high frequencies which compensates for the cable loss. R_4 is equal to R_E (200 Ω) to ensure that the gains of the two paths are equal at DC, regardless of the equalizer settings. In order to maximize the bandwidth, the capacitors are set to 27 fF, the smallest value allowed by the technology. The remaining resistors R_1, R_2 and R_3 are chosen to be 100 Ω, 1 kΩ, and 10 kΩ, respectively.

The voltage at the output of the equalizer stage can now be expressed as:

$$v_o = -[\beta i_1 + (1 - \beta) i_1] Z_L \tag{2.8}$$

where β, which varies between 0 and 1, is controlled by the differential voltage applied at the bases of the Gilbert cells and Z_L is the load impedance per side at the output of the equalizer stage. The DC gain obtained from (6) by setting β to 1 is approximately:

$$Gain_{DC} = -\frac{2R_L r_e g_m}{2r_e + R_E} = 0.86 \tag{2.9}$$

where $g_m = \frac{I_C}{V_T}$. $Gain_{EF}$ is the gain of the emitter follower stage, equal to one at DC, and r_e is the emitter resistance of the transistor. For a 0.13 µm × 2 µm device, this is about 12 Ω. The simulated gain at DC is -0.71 (-3 dB). The maximum peaking gain is obtained when β is zero and reaches its maximum value when Z_E is at its minimum. The measured transistor MAG at 52 GHz is 12 dB leading to a maximum theoretical gain of 4 in the absence of emitter degeneration.

However, at 52 GHz, the gain of the emitter follower stage is simulated to be 0.9. The non-zero emitter degeneration impedance Z_E, further reduces the gain at 52 GHz to be:

$$Gain_{\,52GHz} = -\frac{2R_L r_e g_m}{2r_e + Z_E} \times \mathrm{Gain}_{\mathrm{EF}\,52GHz} \approx -1.37 \tag{2.10}$$

The simulated gain at 52 GHz is -1.4 (3 dB) which results in a total gain peaking from DC to 52GHz of 6 dB.

The linear peak-to-peak input voltage swing per side is given by $I_E \times R_E$ and is equal to 400 mV_{pp} in this design. All differential pair transistors are biased at 8 mA/um^2. The minimum bias current is limited by the minimum transistor size, the parasitic capacitance of the current source and the required bandwidth. The latter consideration is dominant in this case and imposes the minimum usable bias current of 2 mA and transistor emitter length of 2 µm.

Since 30 dB of peaking is needed and each stage provides 6 dB of peaking, 5 equalizer stages must be cascaded to obtain the desired frequency response. The block diagram of the equalizer is shown in Figure 2.4 and consists of five identical equalizer stages with adjustable peaking control and 50-Ω input and output buffers.

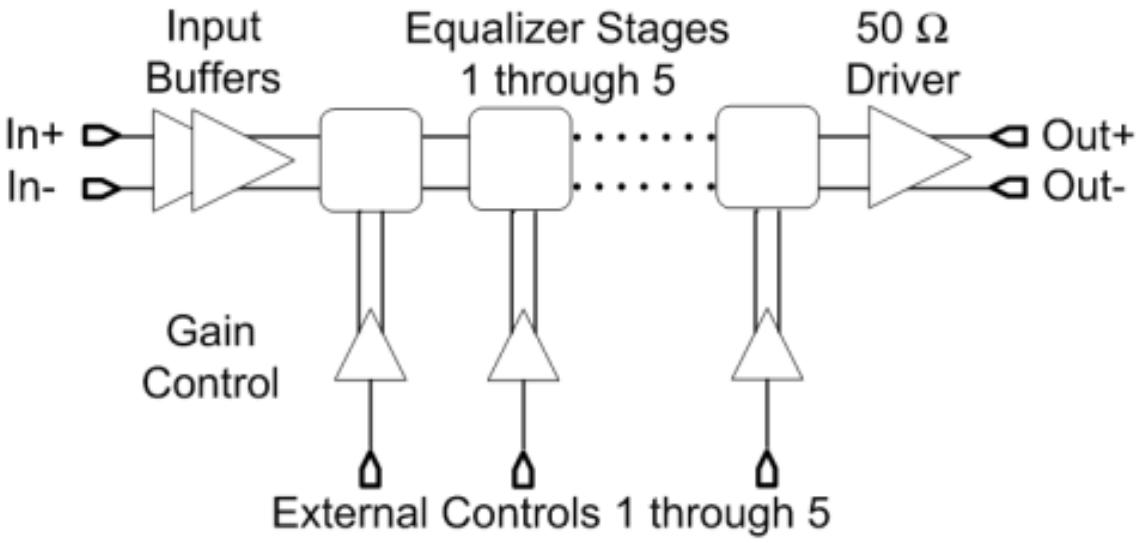


Figure 2.4: Equalizer block diagram (make picture sharper 50-ohm driver)

2.4 Retimer Input Buffers

The circuit schematic of the input buffers can be seen in Figure 2.5. Two cascaded differential stages are used to provide adequate common-mode rejection at high frequency, needed to restore a single ended input to a differential signal.

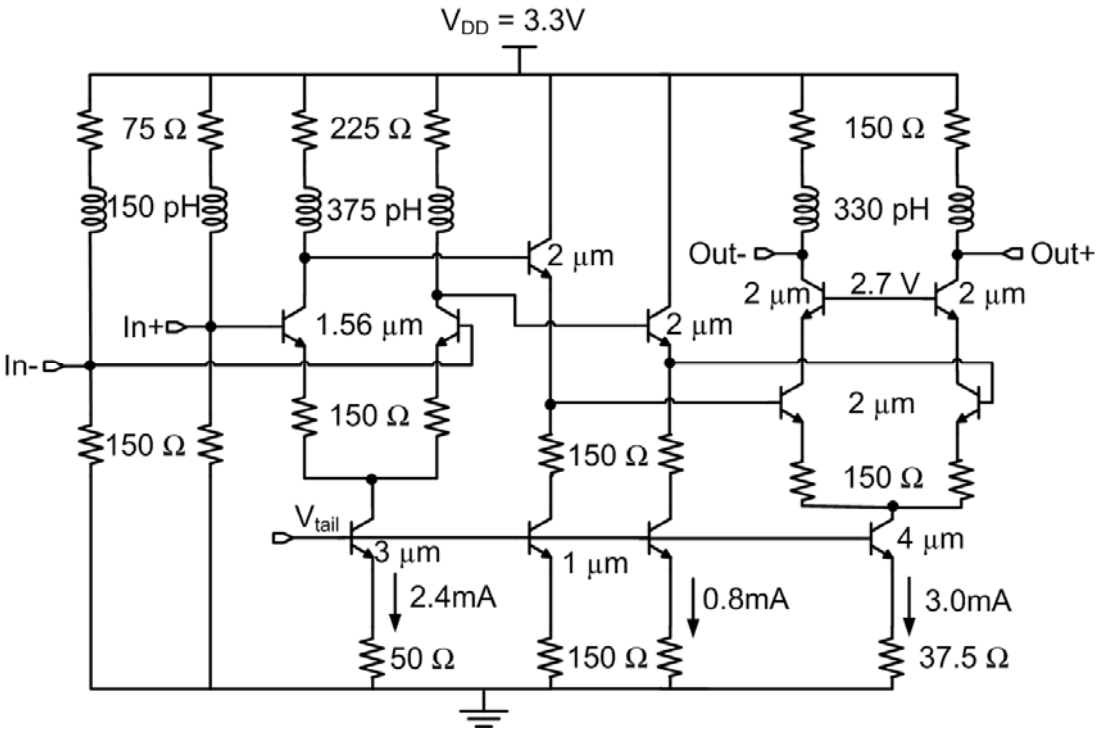


Figure 2.5: Circuit schematic of the input buffers. (add outp inp, 2.9V not 2.7)

The HBT exhibits a finite input impedance due to its finite β. In order to increase the input impedance and reduce the signal distortion, an emitter degeneration resistance is introduces. This increases the linear voltage range to 360 mV however the trade off is gain. The gain for a differential pair with emitter degeneration is given by:

$$A_v = \frac{-R_L}{\frac{2V_T}{I} + R_E} \tag{2.11}$$

where R_L is the load resistance, R_E is the emitter degeneration, V_T is the thermal voltage and I is the tail current. The purpose of the system is to test the equalization stages; hence the buffers

were designed to have unity gain. The cascaded gain for the two buffers is calculated to be 1.17 V/V which is slightly higher than unity in order to combat the loss introduced by the emitter followers that separate them.

A simulation of the buffers AC response can be seen in Figure 2.6 bellow. Slight peaking is introduced at 40 GHz in order to account for layout parasitic capacitances and interconnects.

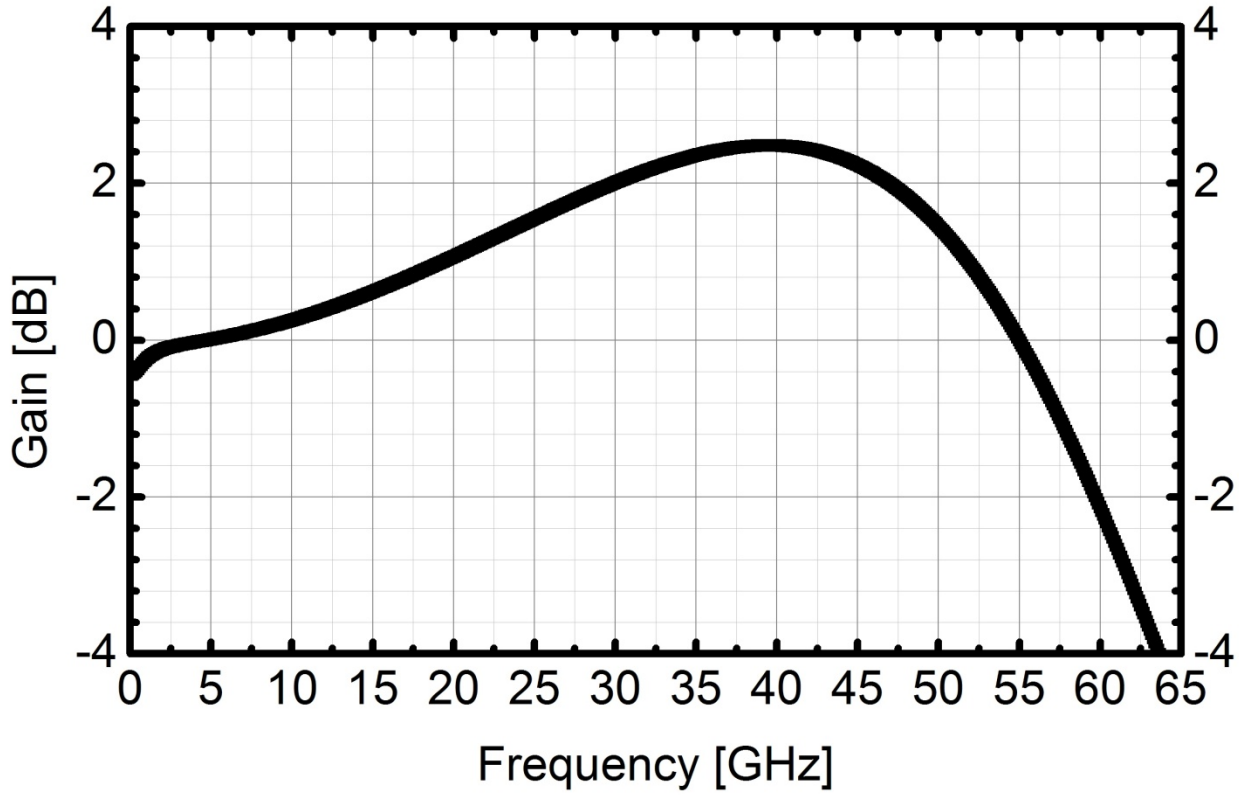


Figure 2.6: Input buffers AC response.

2.5 Equalizer Input Matching

The channel to be equalized as well as the measurement equipment has a characteristic impedance of 50 Ω, hence input to the equalizer is matched to 50 Ω using a resistive divider and an inductor as seen in Figure 2.7.

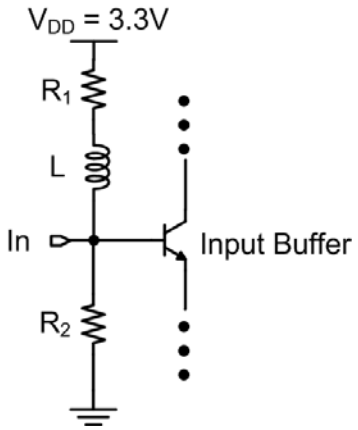


Figure 2.7: Input 50 Ω matching.

At low frequencies, the characteristic input impedance of this system is given by:

$$R_{in} = R_1 \parallel R_2 \parallel R_{\text{inv}} \approx R_1 \parallel R_2 \approx \frac{R_1 R_2}{R_1 + R_2} \tag{2.12}$$

where R_1 and R_2 are labelled in Figure 2.7, R_{in} is the equalizer input resistance, and R_{inv} is the input resistance to the inverter in the following stage. R_{inv} is composed of r_{be}, the base emitter resistance of the HBT, in series with a 150 Ω emitter resistance and the output resistance of the current source. It is safe to assume that R_{inv} is much larger then R_1 and R_2; thus R_{in} can be simplified to $R_1 \parallel R_2$ as seen in (2.12). The input to the equalizer is AC coupled, hence this resistive decider also serves to set the input DC level, V_{in}, for the input buffer. V_{in} is given by:

$$V_{in} = \frac{R_2}{R_1 + R_2} V_{DD} \tag{2.13}$$

Rearranging the equations as seen in (2.12) and (2.13) and setting R_{in} to 50 Ω and V_{in} to be the necessary 2.2 V results in a R_1 75 Ω and R_2 of 150 Ω.

$$R_1 = \frac{R_{\text{in}}}{V_{\text{in}}} V_{DD} = \frac{50\ \Omega}{2.2\ \text{V}} (3.3\ \text{V}) = 75\ \ \Omega \tag{2.14}$$

$$R_2 = \frac{R_1 R_{\text{in}}}{R_1 - R_{\text{in}}} = \frac{(75\ \Omega)(50\ \Omega)}{(75\ \Omega) - (50\ \Omega)} = 150\ \Omega \tag{2.15}$$

At high frequencies, the input impedance Z_{in} can be approximated as:

$$Z_{in} = \mathrm{R_2} \parallel (\mathrm{sL} + \mathrm{R_1}) \parallel \left(\frac{1}{\mathrm{sC_{bc}}} + \mathrm{R_C}\right) \tag{2.16}$$

where $\mathrm{C_{bc}}$ is the base-collector capacitance of the HBT and $\mathrm{R_C}$ is the collector resistance. For first order approximation, the base emitter capacitance can be ignored because of the large output resistance of the current source in the inverter. As the frequency increase, the $\frac{1}{\mathrm{sC_{bc}}}$ term decreases and the overall input impedance decreases. The inductor L is introduced to mitigate this term and extend in 50-Ω input matching. Simulations show that the optimum inductor value is 150 pH.

2.6 Equalizer Output Buffers

The output of the equalizer must be matched to 50 Ω hence the last stage is a 50-Ω output driver seen in Figure 2.8. It consists of an emitter follower stage and a differential pair with resistive degeneration and consumes 13.4 mA from 3.3 V. The first consideration when designing the output stage is that the output must be matched to 50 Ω. The simplest way to achieve this is to use a CML inverter with a 50-Ω load. In order to achieve a 300 mV swing across the output load and to maintain a unity gain, a tail current of 6 mA was chosen for the buffer. The previous equalizer stages attenuate the DC component of the signal, therefore the input to the buffer is not large enough to fully switch the HBTs. For this reason, they are biased so that the current density flowing thorough each is $J_{peak\ f_T} = 2\frac{mA}{\mu m}$ when Inp and Inn are equal. The small input signal to the buffer also relaxes the linearity requirement and lowers the value required for the degeneration resistor to 22-Ω in this case. Peaking inductors were used order to maximize the bandwidth. The emitter followers were used in order to provide the proper common mode voltage for the buffer. The 100-Ω resistor was introduce in order to reduce the capacitance seen at the emitter as well as to match the current tail V_{ce} to that of the current mirror and provide better matching. (Need to check current and calculate gain using the expression again)

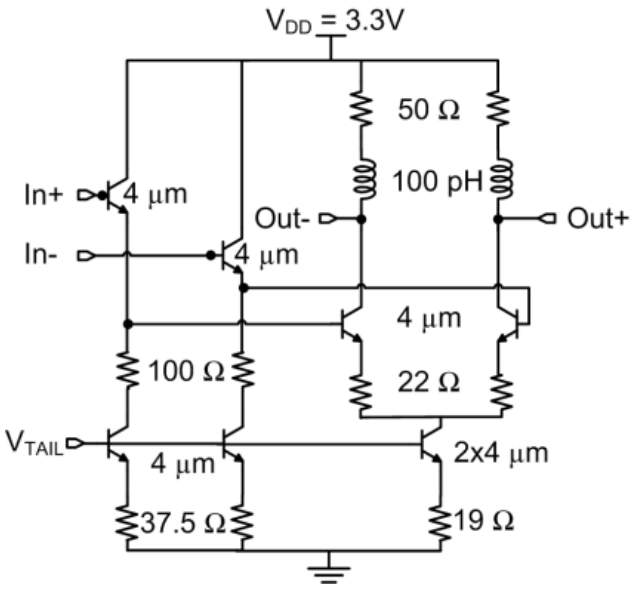


Figure 2.8: 50-Ω output driver (add currents, remove dots, change to Inp and Outp)

There is 3.9 mA current for each 4 um device.

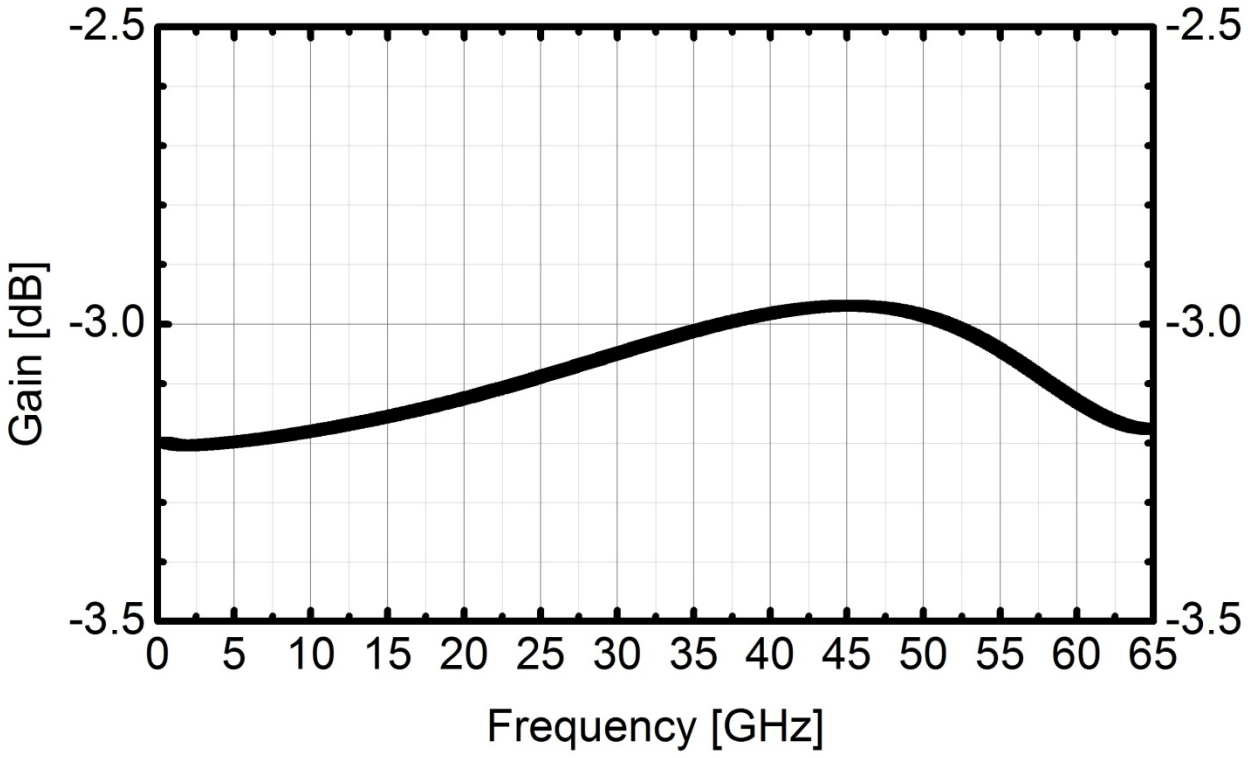


Figure 2.9: Output buffer AC response.

2.7 Equalizer Simulation Results

The simulated gain of the equalizer for the different equalization settings is shown in Figure 2.10. A peak gain of X dB is observed at X GHz for a total of X dB of adjustable gain.

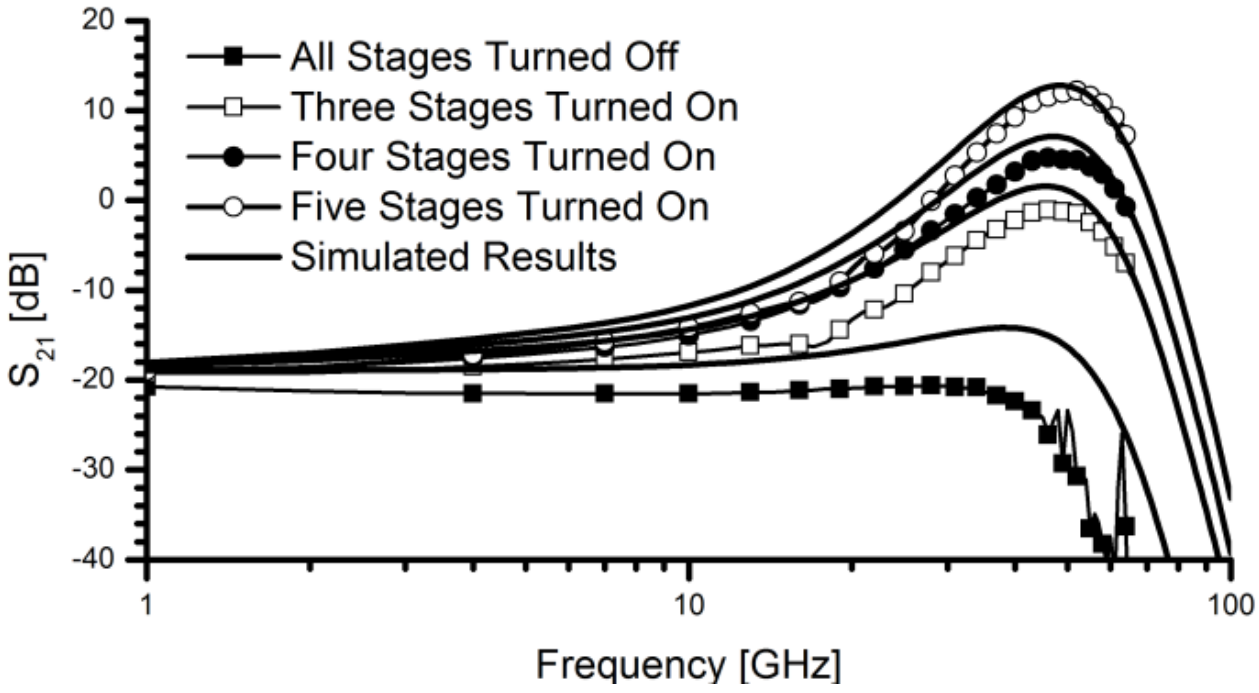


Figure 2.10: Simulated S_{21} of the equalizer. (Add grid, remove measurements)

In the case of a good quality cable, all the equalizer stages will be turned to the main path in order to not disturb the signal. Such a situation was simulated using an ideal 500 mV_{p-p} single ended PRBS signal at 40 Gbps in Figure 2.11 and 80 Gbps Figure 2.12.

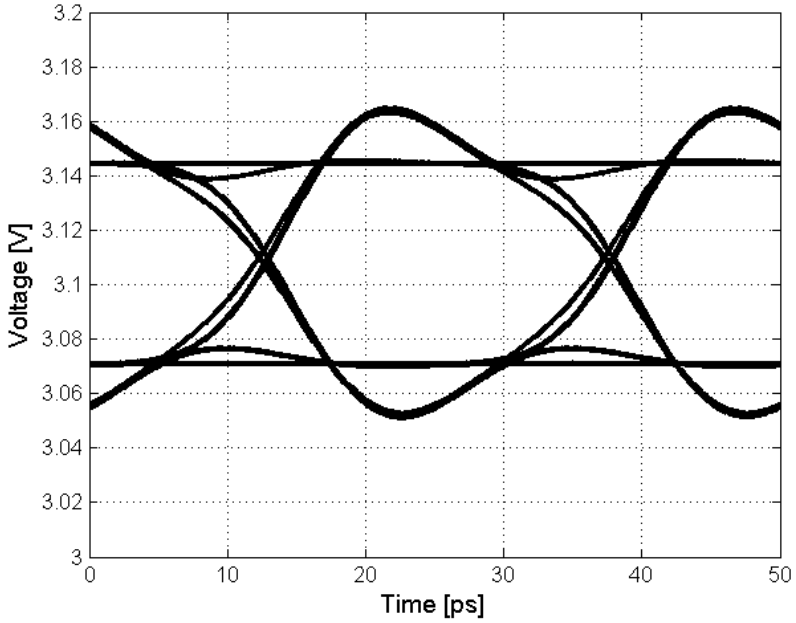


Figure 2.11: Simulated output eye using a 40-Gbps PRBS input sequence.

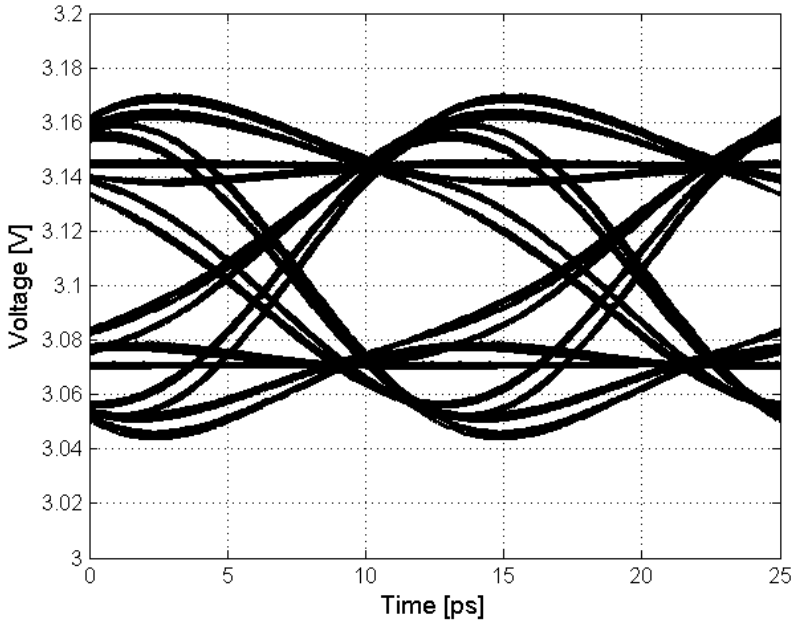


Figure 2.12: Simulated output eye using an 80-Gbps PRBS input sequence.

3 Equalizer Fabrication and Experimental Results

This chapter describes the experiments carried out in order to measure the performance of the equalizer as well as providing the measurement results. A photomicrograph of the chip is shown in Section 3.1. Section 3.2 and Section 3.3 detail the test setup and results for S-parameter measurements and time domain measurements respectively. A performance comparison is given in Section 3.4.

3.1 Test Chip

The test chip was designed in STMicroelectronics' 0.13-µm SiGe BiCMOS9MW technology with HBT transistors having an f_T of 240 GHz and f_{MAX} of 270 GHz [Chevalier]. A photomicrograph of the fabricated test chip can be seen in Figure 3.1. The pad limited area of the chip is 990-µm x 895-µm while the equalizer circuit occupies 680-µm x 170-µm.

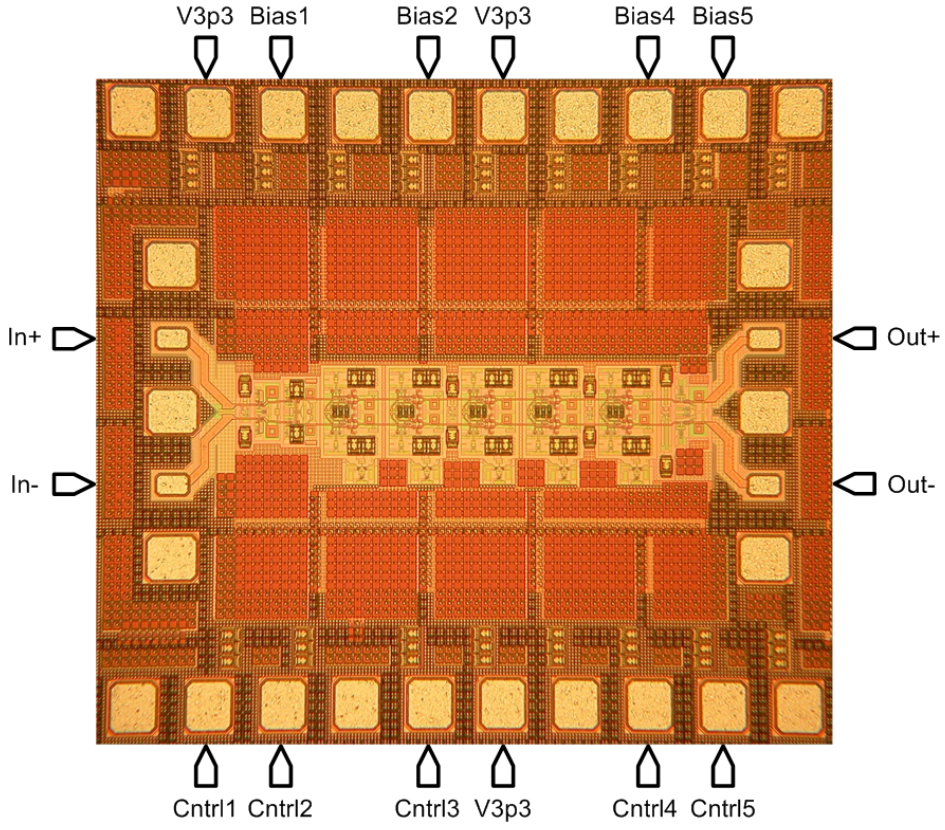


Figure 3.1: Photomicrograph of the equalizer.

The circuit has five control pads (Cntrl1...5), one for each of the equalizer stages. The biasing for the input stages is provided using Bias1. The bias for the first three equalizer stages is provided using Bias2, while the bias current for the final two stages of the equalizer is provided using Bias3. The current through the output stages can be independently controlled using Bias4. In order to minimize IR drop across the cables supplying the power, it is desirable to keep the current drawn per pad to less than 100 mA. The circuit consumes 336.6 mW hence three DC pads (V3p3) were used to provide the power. The unlabeled pads are connected to ground. All measurements were conducted on wafer using 67-GHz GGB probes for input and output.

3.2 S Parameter Measurements

The S-parameter measurements were performed up to 65 GHz using a Wiltron 360B Vector Network Analyzer (VNA). A picture of the test setup can be seen in Figure 3.2.

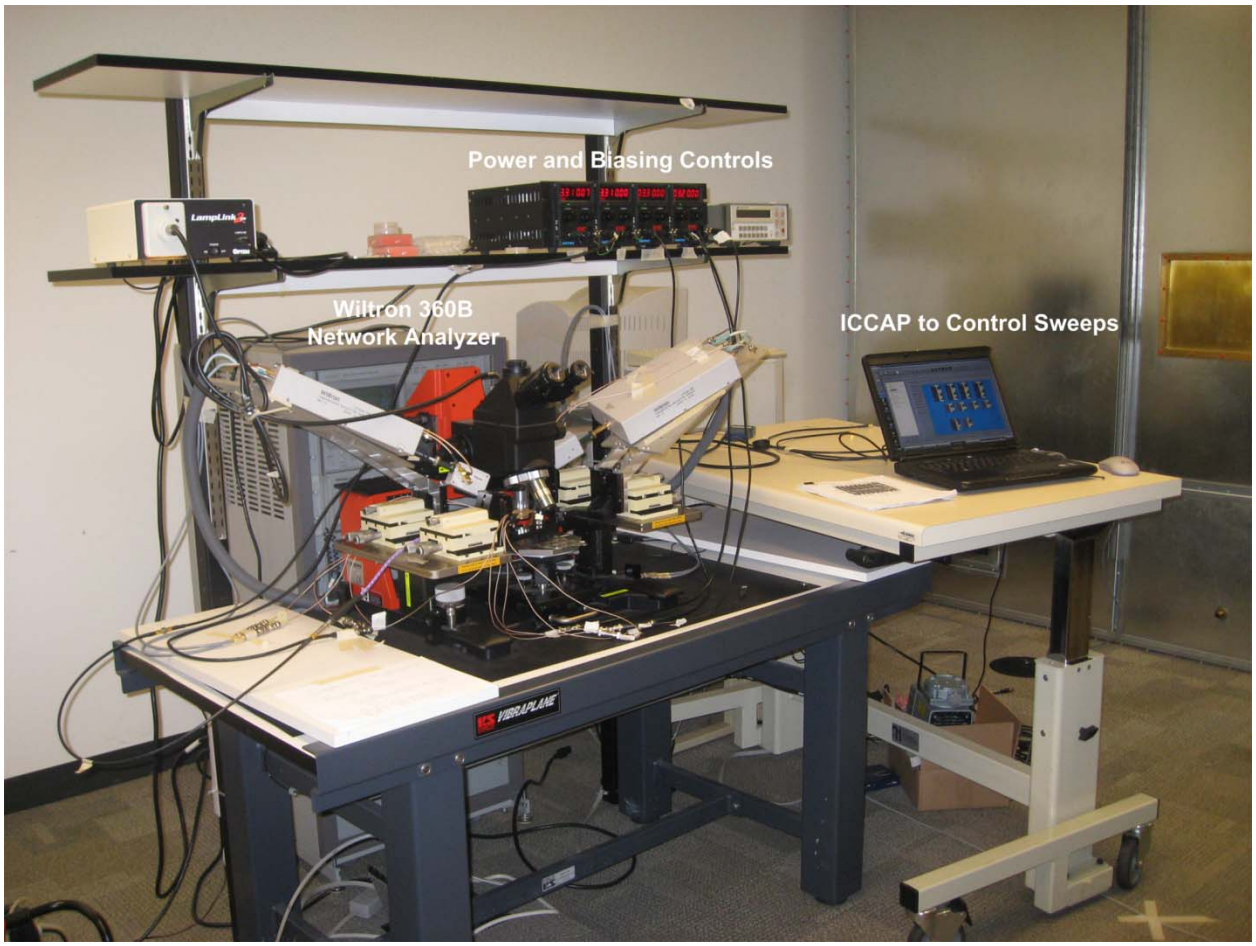


Figure 3.2: Test setup for S-parameter measurements. (Add ports)

A comparison of the measured and simulated single-ended gain (S_{21}) is shown in Figure 3.3. With the control voltage in all stages set for maximum peaking, a gain of 12.2 dB (18.2 dB differentially) is observed at 52 GHz, 0.4 dB lower than the simulated value. The DC "gain" is -19 dB, giving a total of 31 dB of adjustable peaking between DC and 52 GHz. For differential gain, 6 dB should be added to the measured values.

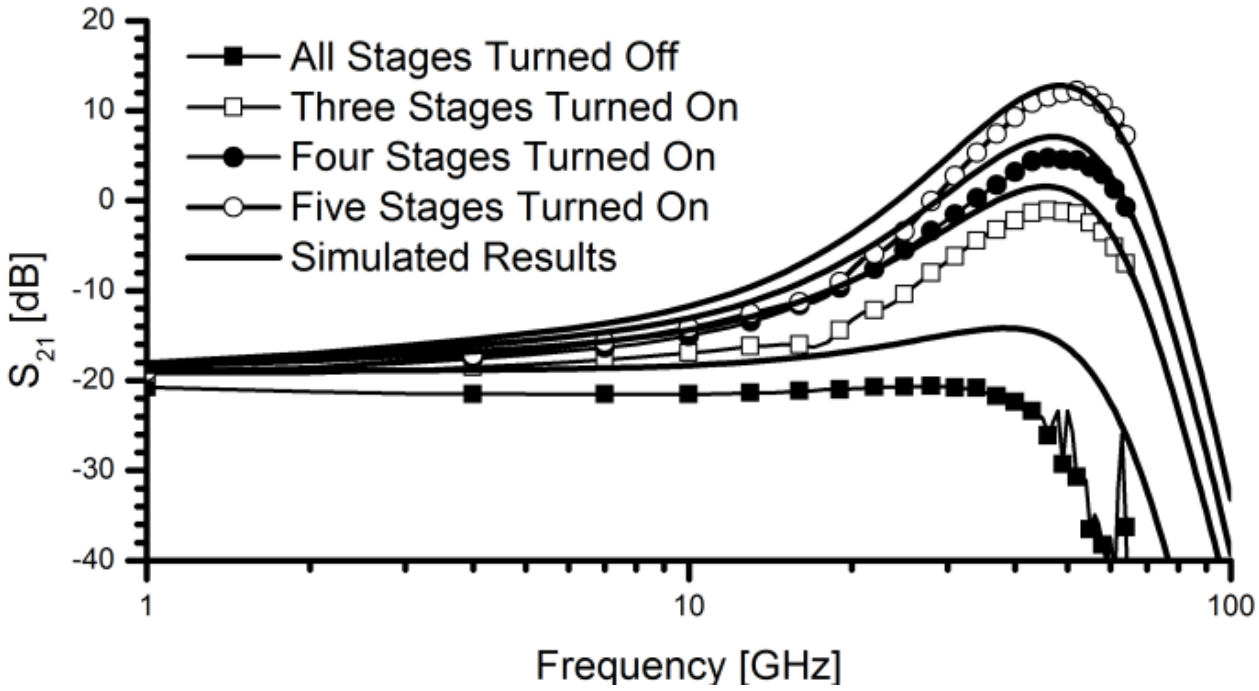


Figure 3.3: Measured and simulated S_{21} of the equalizer. (Add grid)

The simulated and measured input (S_{11}) and output (S_{22}) return loss are plotted in Figure 3.4. S_{11} is less than -16.1 dB and the S_{22} is below -9.3 dB up to 65 GHz. At low frequency, S_{11} and S_{22} are both better than -29 dB indicating less than 3% deviation of the 50-Ω input and output resistors from the nominal value.

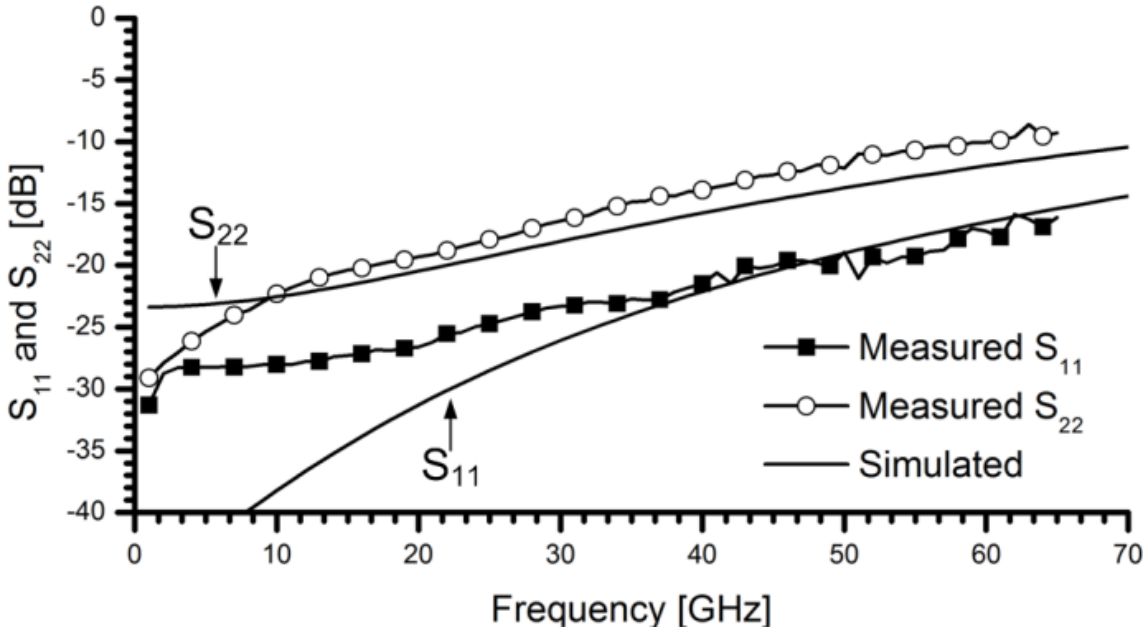


Figure 3.4: Measured and simulated S_{11} and S_{22} of the equalizer. (Add grid)

In order to measure the equalization capabilities, the three cables whose frequency responses are shown in Figure 2.1 are inserted at the input of the equalizer. The old and new test setups are illustrated in Figure 3.5.

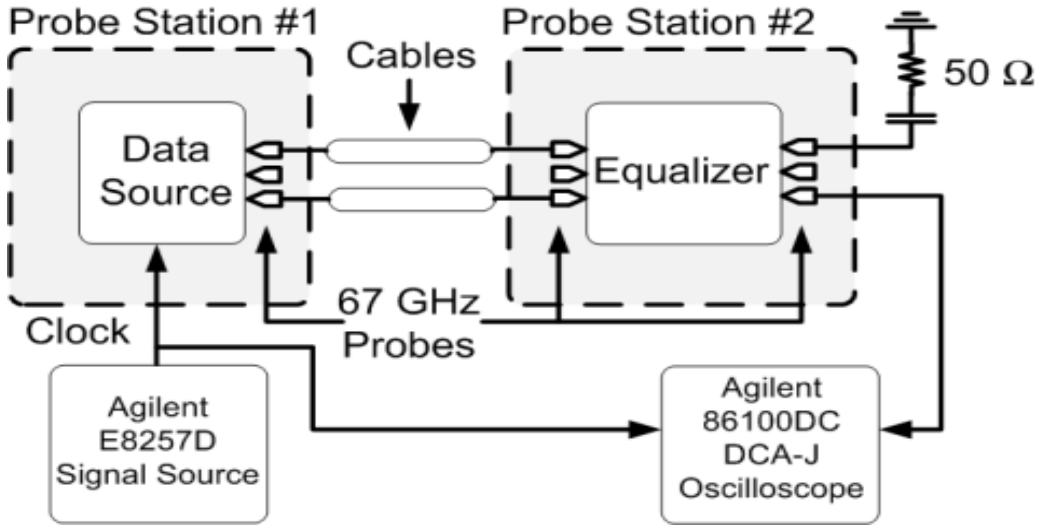


Figure 3.5 Test setup for S parameter measurements. (change picture, do before and after)

The equalizer is capable of improving the 3-dB bandwidth from 16 GHz to 43 GHz for the 1-mV cable as shown in Figure 3.6.

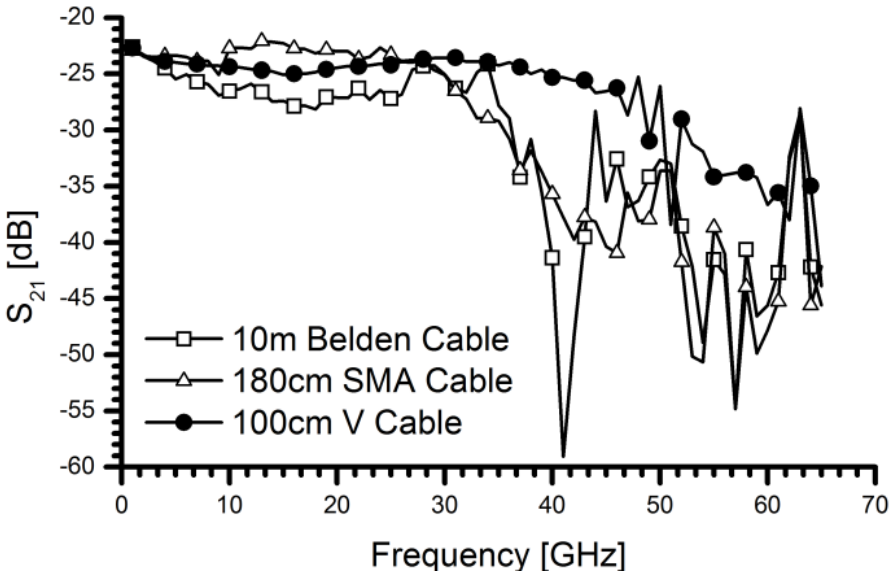


Figure 3.6 S_{21} measurements using the V cable. (Add boxes, change symbols)

The 3dB bandwidth for the SMA cable is improved from 11 GHz to 30 GHz as seen in Figure 3.7.

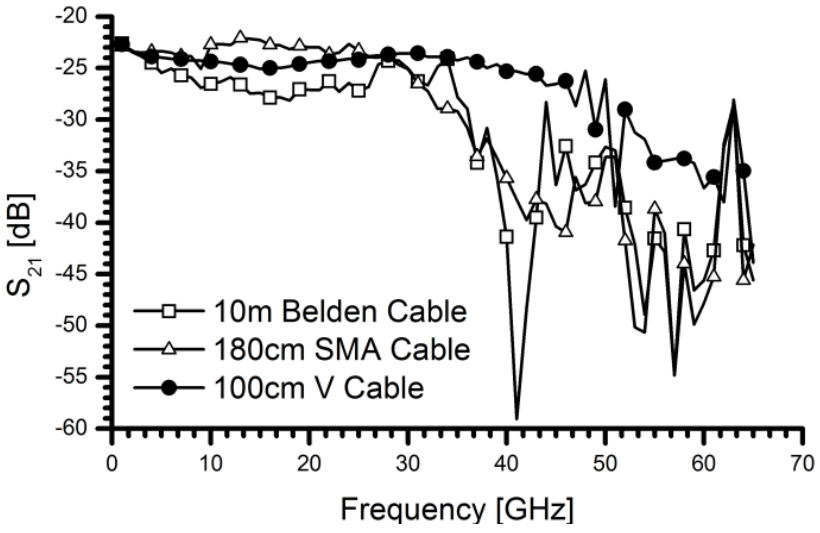


Figure 3.7 S_{21} measurements using the SMA cable. (Add boxes, change symbols)

The 3dB bandwidth for the 10m Belden cable is improved and from 3 GHz to 7 GHz. This is illustrated in Figure 3.8.

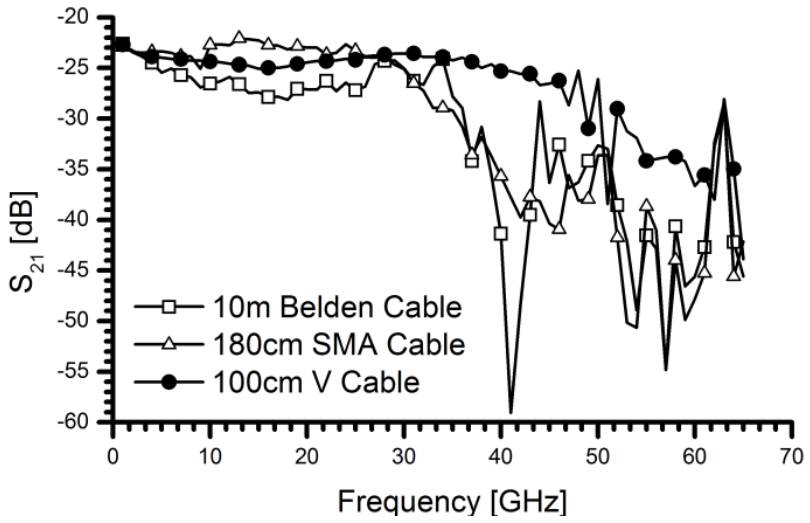


Figure 3.8 S_{21} measurements using the Belden cable. (Add boxes, change symbols)

When measuring the performance of the equaliser alone, the calibration of the equipment was performed using Line Reflect Match (LRM). This allows the effect of the probes to be extracted from the performance results. The same calibration was performed when measuring the ensemble formed by the cable and the equalizer, however, following the calibration, the cable to be equalized was inserted between Port 1 of the VNA and the probe attached to the input of the equalizer. This created a less accurate calibration. This reason along with the low gain results in an increasingly non-smooth S_{21} measurement at high frequencies.

3.3 Time Domain Measurements

Large signal equalization experiments were performed on the three cables. All measurements were conducted on wafer using 67 GHz GGB probes for input and output. Each probe has a loss of up to 1.1 dB hence the channel loss consists of the channel loss plus up to 2.2 dB of probe loss. The test setup for the time domain measurements is shown in Figures Figure 3.9 and Figure 3.10. The input signal is provided by an 80-Gbps 2^7-1 PRBS Generator described in [Tod] which produces an eye amplitude of 400 mV_{pp} per side.

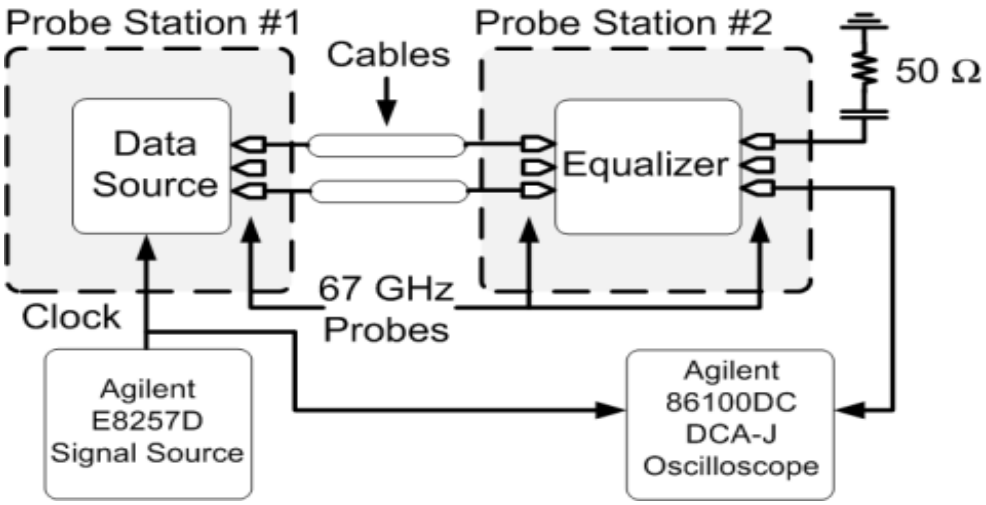


Figure 3.9 Schematic of the test setup for time domain measurements. (flip to match photo)

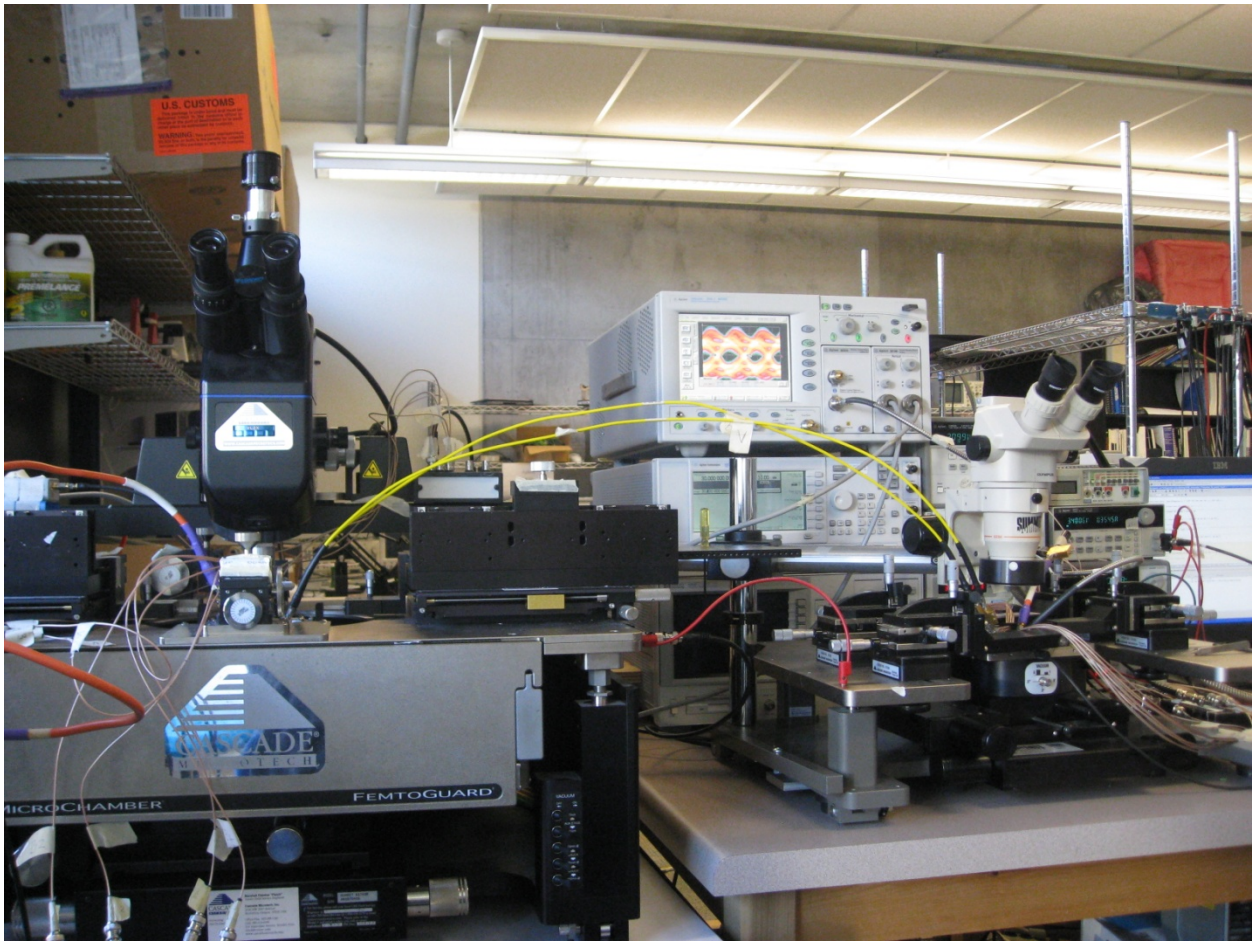


Figure 3.10: Picture of the test setup for time domain measurements. (label)

Equalization of the 1.8-m SMA cable at 59.2 Gbps is shown in Figure 3.11. The right hand side shows the S parameter response of the channel, the cable and the channel plus cable system. The channel loss at 30 GHz for the probes and cables is 17.9 dB. On the left hand side, the eye diagrams are shown for the signal at the output of the transmitter, after the cable and after the equalizer. Maximum gain settings were applied to the equalizer in order to achieve the cleanest eye diagram.

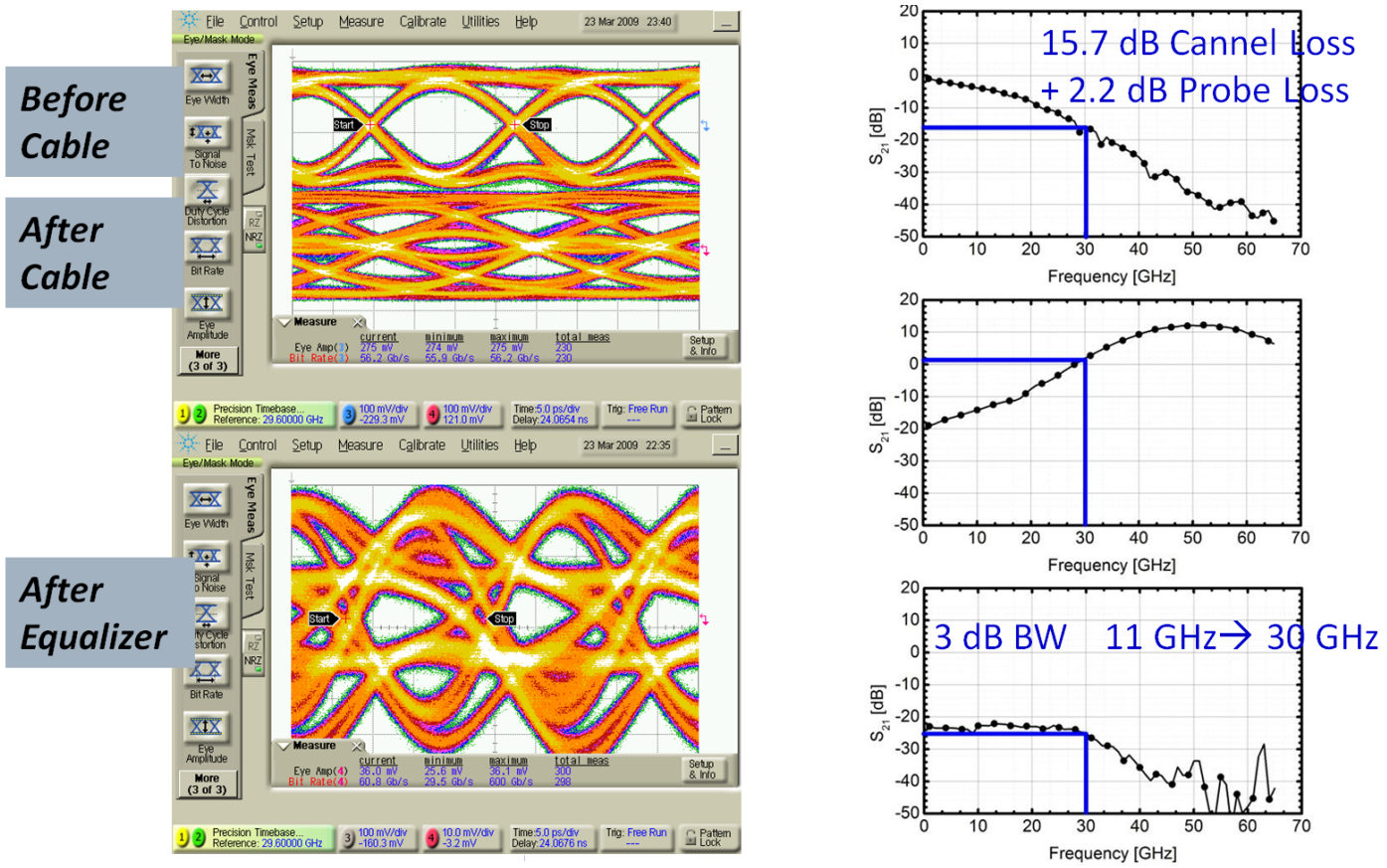


Figure 3.11: Measurement at 59.2 Gbps showing the transient and S parameter response. (fix)

Equalization of the 1-m V cable at 50.6 Gbps is shown in Figure 3.12. In this case, only two of the equalizer stages need to be turned on in order to equalize -3.6 dB of channel loss at 25 GHz. The channel loss at 30 GHz is 1 dB higher at -4.6 dB, which requires all stages to be turn on in order to equalize the 60 Gbps data seen in Figure 3.13.

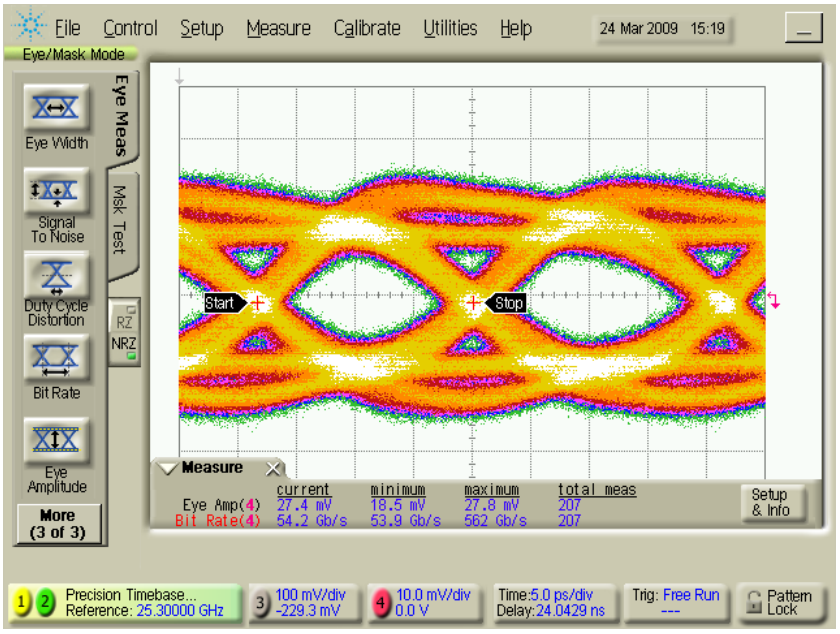


Figure 3.12: Output of the equalizer at 50.6 Gbps when equalizing a 1-m long V cable.

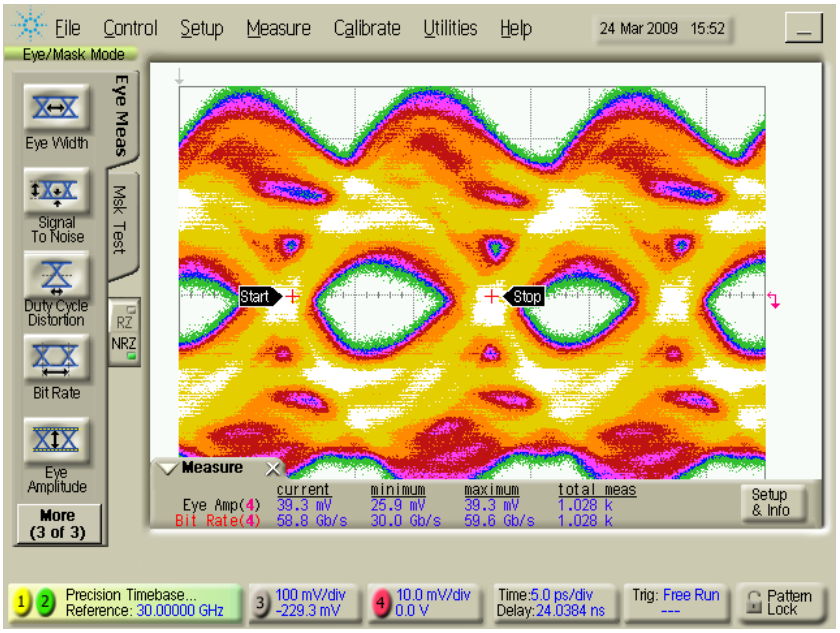


Figure 3.13: Output of the equalizer at 60 Gbps when equalizing a 1-m long V cable.

The output of the equalizer for a 70 Gbps data is seen in Figure 3.14. The channel loss at 35 GHz is 7.2 dB causing a significant deterioration in the eye diagrams. All stages needed to be turned on in order to achieve an open eye which in turn causes excessive peaking. Another problem is the miss-alignment of the differential signals at the input of the equalizer as can be seen in Figure 3.15. This miss-alignment is attributed to the slight length difference of the two V cables that were used causing excessive jitter at the input of the Equalizer. It can be conclude that due to the high quality of the cable and the difficulty in matching between the two cables, the Equalizer should not be used at data rates below 70 Gbps.

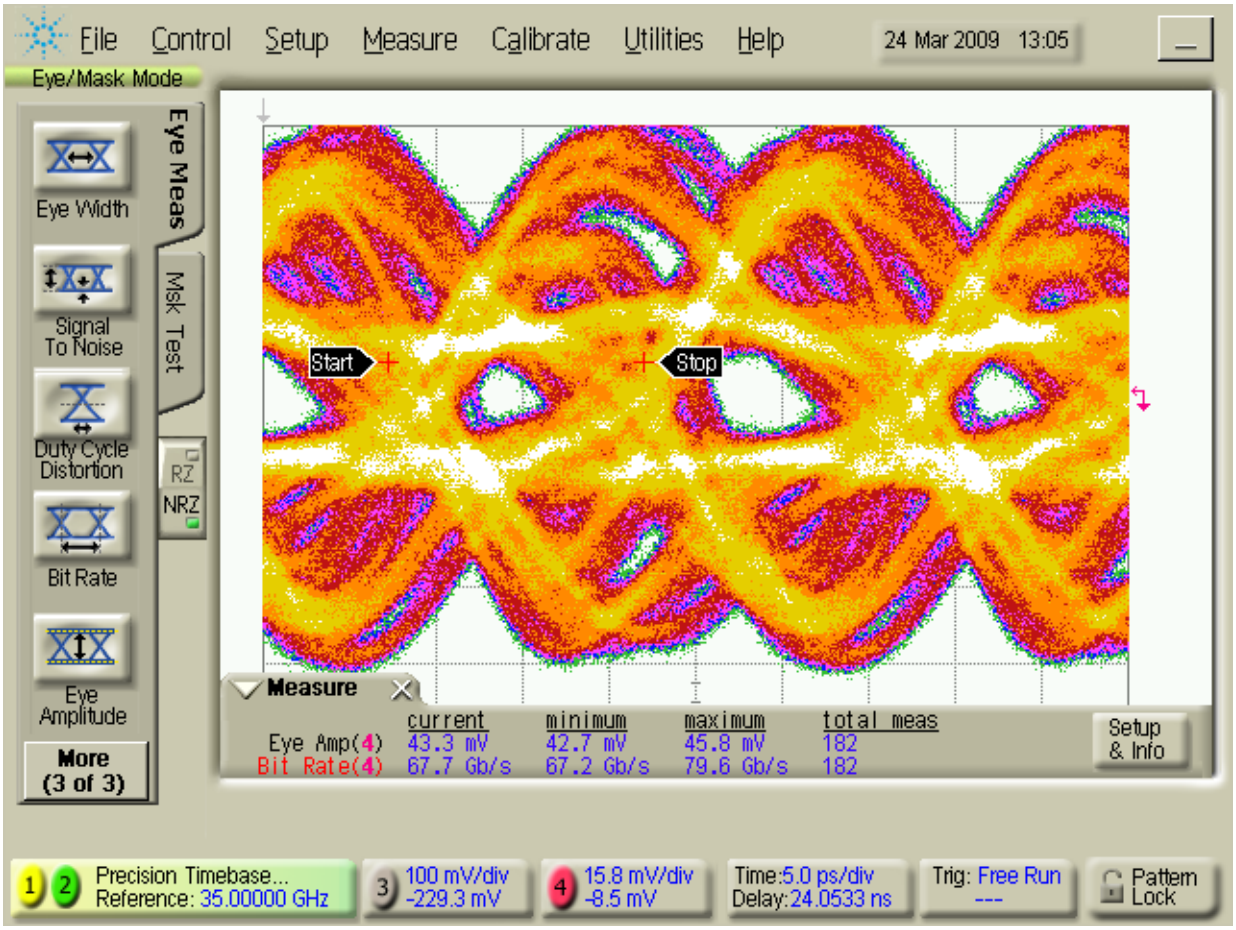


Figure 3.14: Equalizer output at 70 Gbps after a 1m long V cable.

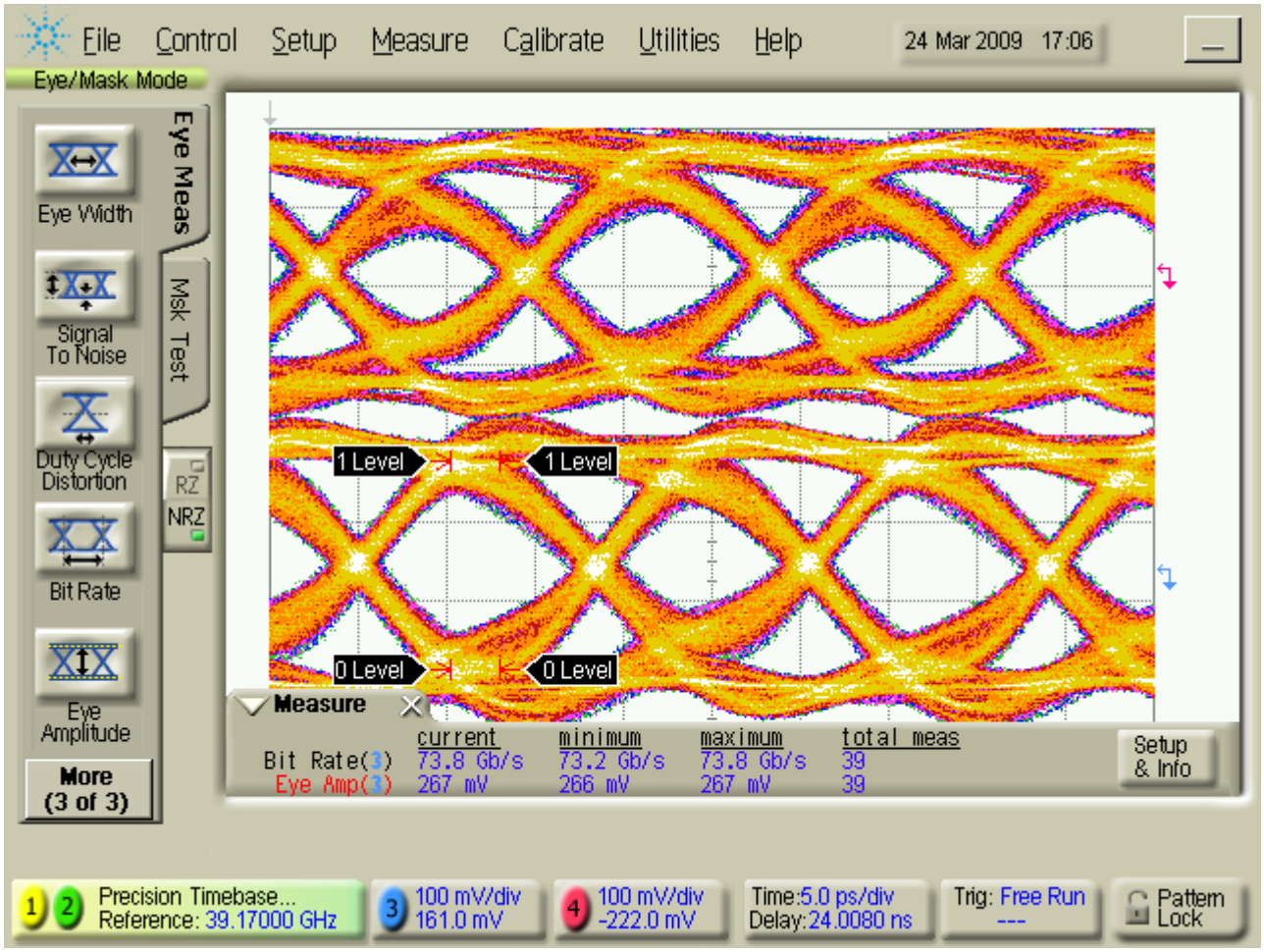


Figure 3.15: The differential input to the equalizer after a 1-m V cable.

The high loss of the 10-m Belden cable causes the signal to be too small for the input of the Equalizer. A 40-Gbps driver described in [Ricardo] capable of producing a signal with adjustable amplitude from 1-V_{pp} to 3.6-V_{pp} was used in order to generate a large enough input for the Equalizer. The 2^{31}-1 PRBS input pattern was generated by an external Centelax board. The new measurement setup can be seen in Figure 3.16 and Figure 3.17. It should be noted that in this situation the input to the equalizer was single ended and that the 10-m Belden cable and driver are matched to 75 Ω while the Equalizer input is matched to 50 Ω.

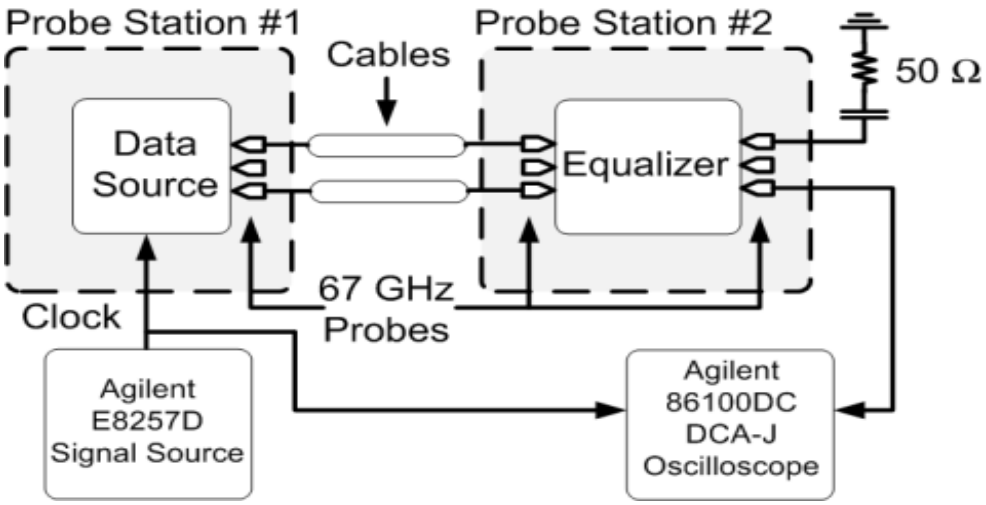


Figure 3.16: Test setup for time domain measurements using the driver. (change!!!!)

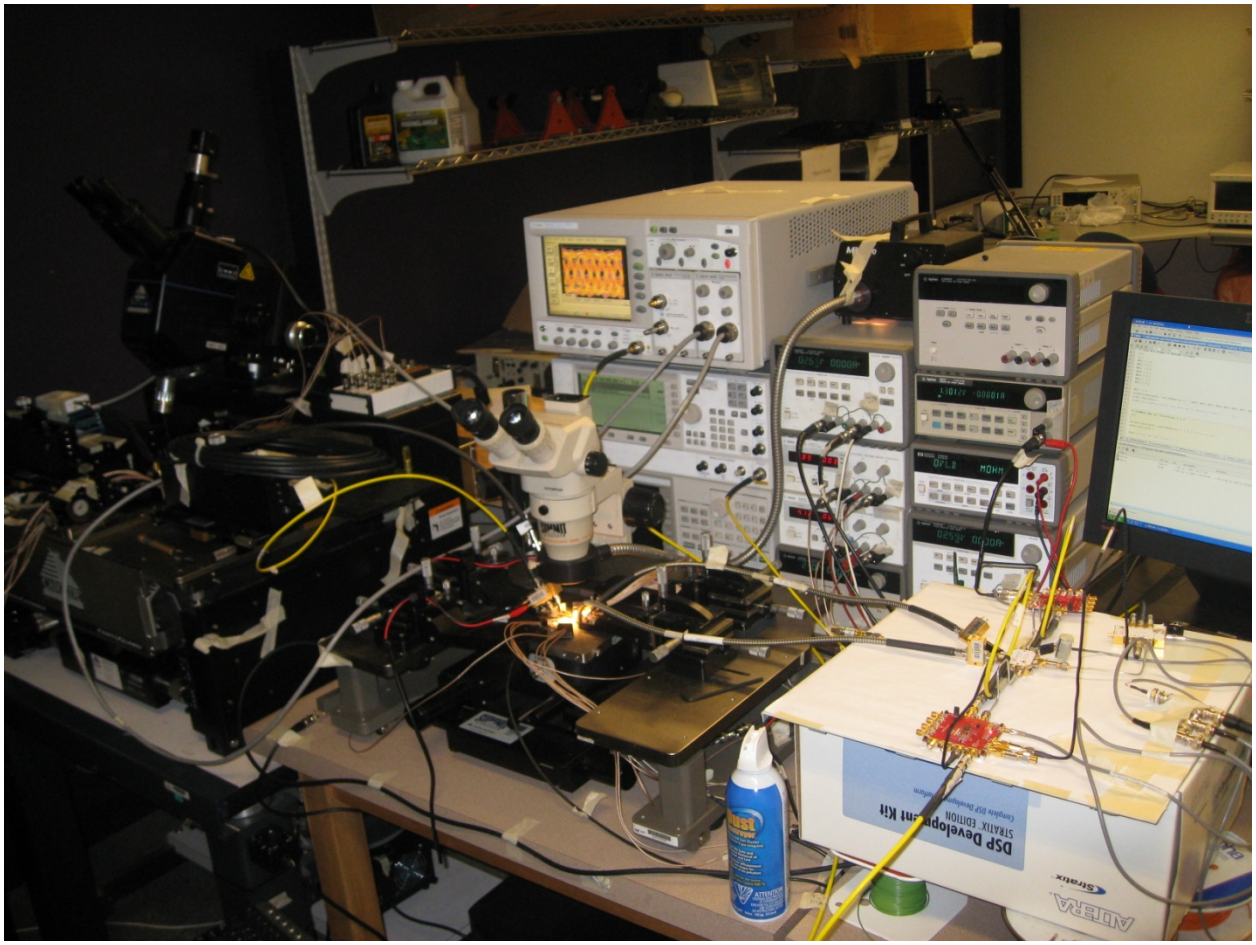


Figure 3.17: Picture of the test setup for time domain measurements using the driver. (label)

A 30-Gbps signal after the 10-m cable and after equalization is shown in Figure 3.18 and Figure 3.19. A clear improvement in the eye opening when compared to the signal amplitude can be observed. The signal jitter can be further improved by using the retimer described in Section 4 at the output of the Equalizer.

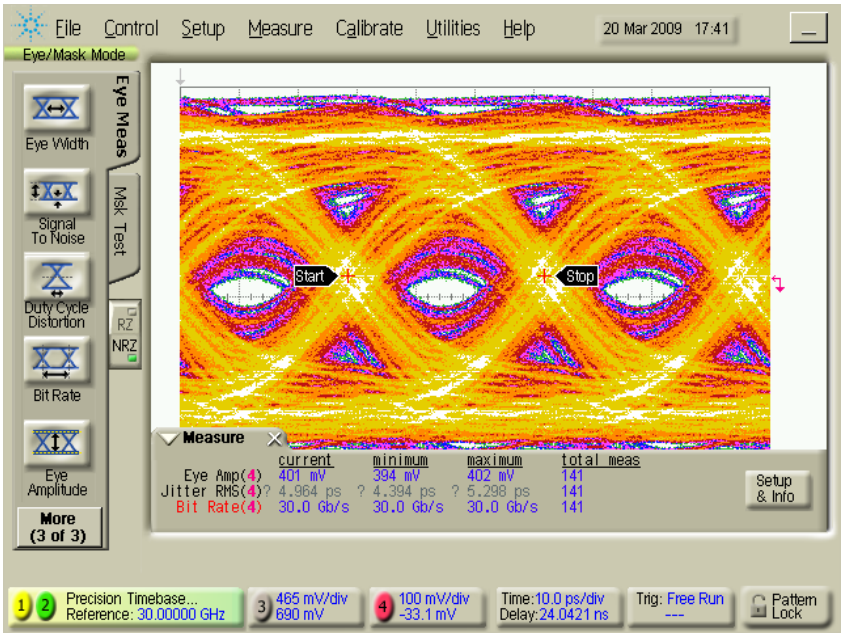


Figure 3.18: A 30-Gbps signal after a 10 m cable. The channel loss at 15 GHz is -15.8 dB.

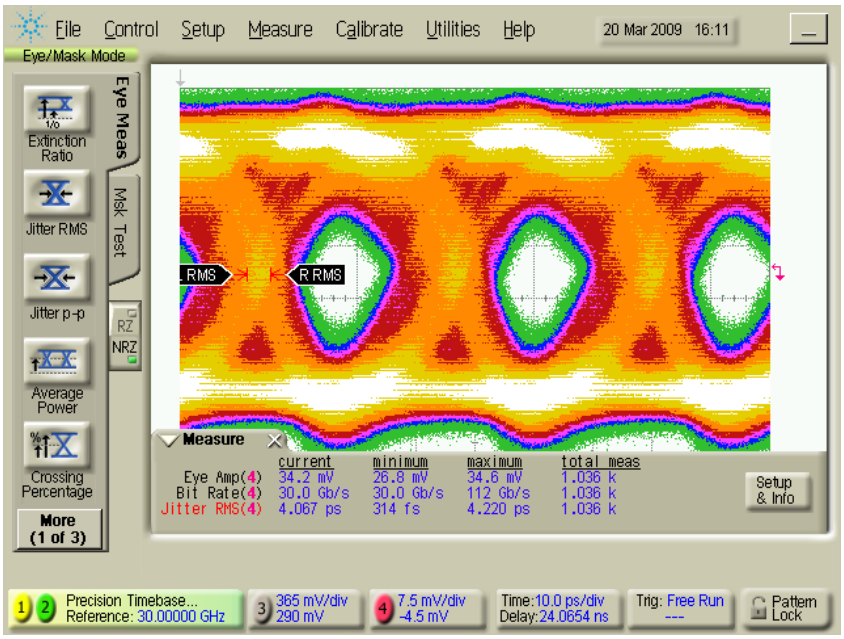


Figure 3.19: The 30-Gbps signal after the Equalizer.

At 34.6 Gbps, the channel loss of 26.4 dB causes the eyes to be fully clothes after 10 m as seen in Figure 3.20, however, after the equalizer the eyes are now open again as seen in Figure 3.21.

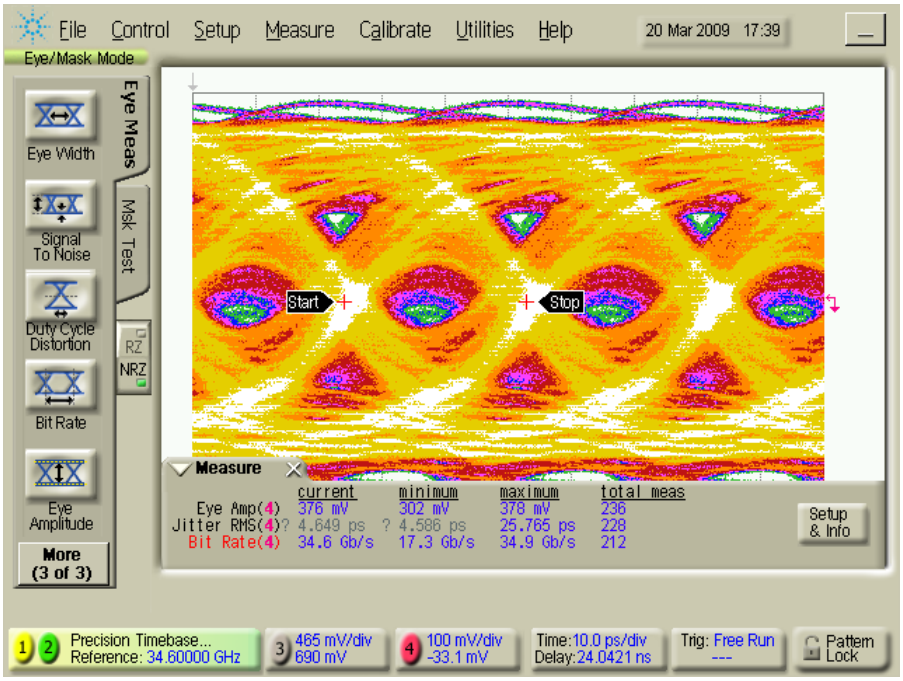


Figure 3.20: A 34.6 Gbps signal after a 10m cable with channel loss of 26.4 dB at 17 GHz.

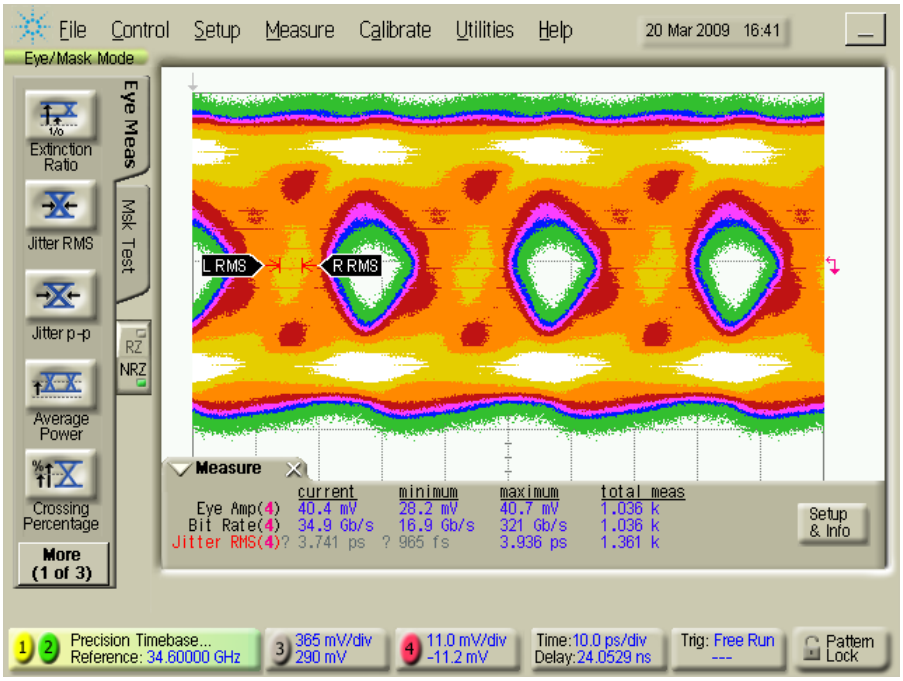


Figure 3.21: A 34.6 Gbps signal after the Equalizer for a channel loss 26.4 dB of at 17 GHz.

The cable was replaced with the 1-m V cable and the same experiment was performed. The effect of turning different stages of the equalizer was observed at 38.3 Gbps when the channel loss is 5.9 dB at 19 GHz. An improvement in eye opening is observed in Figures 3.22 thru 3.25 as the equalizer stages are gradually turned from non-peaking mode to peaking mode.

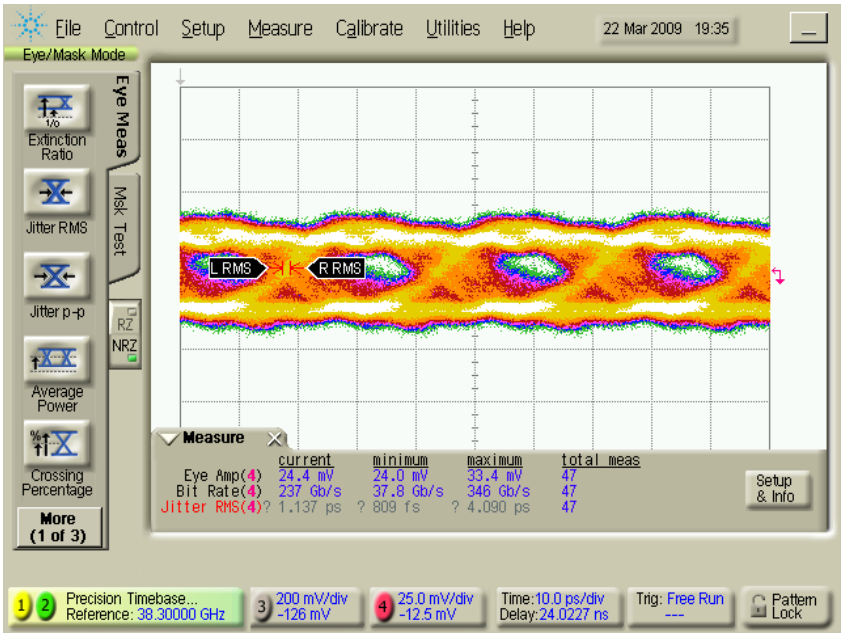


Figure 3.22: Equalizer output at 38.3 Gbps when all stages are set to non-peaking mode.

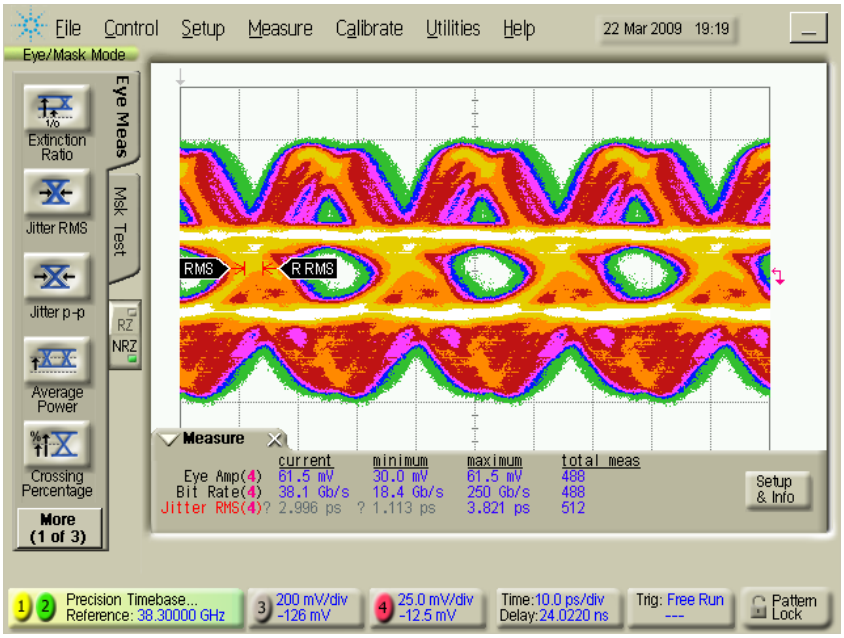


Figure 3.23: Equalizer output at 38.3 Gbps when three stages are set to non-peaking mode.

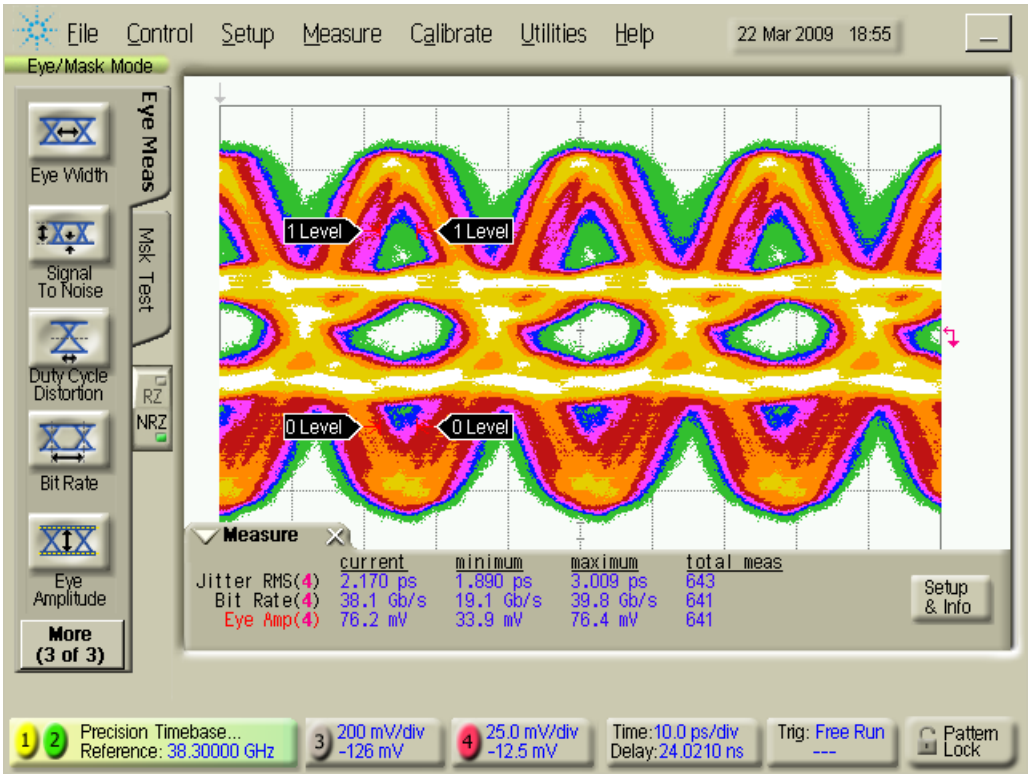


Figure 3.24: Equalizer output at 38.3 Gbps when two stages are set to non-peaking mode.

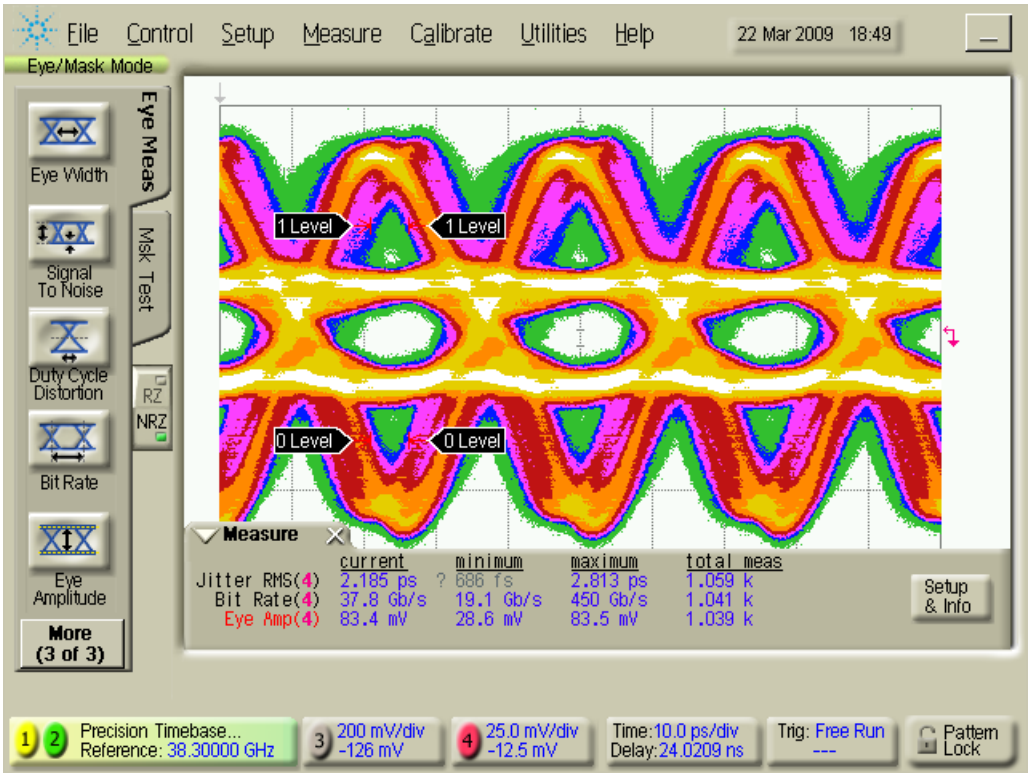


Figure 3.25: Equalizer output at 38.3 Gbps when two stages are set to non-peaking mode.

3.4 Performance Comparisons

The equalizer is capable of providing a peak gain of 12.2 dB at 52 GHz with 31 dB of adjustable ain peaking from DC to 52 GHz. Operation up to 70 Gbps was shown making this the fastest receive equalizer published to date. A comparison of this work with previously published channel equalizers is given in Table 3-1.

Table 3-1: Comparison of Equalizer with previously published work. (add more)

Ref.	**Description**	**Technology**	**Power**	**Performance**
Aroca CSICS'07	Cable driver with adaptive pre-emphasis	0.18 µm SiGe BiCMOS f_T = 160 GHz, f_{MAX} = 160 GHz	3.6 W from 4 V, 6 V, and 8 V	40 Gbps
Garg JSSC'06	1-Tap Decision Feedback Equalizer	0.18µm SiGe BiCMOS f_T = 160 GHz, f_{MAX} = 160 GHz	759 mW from 3.3 V	40 Gbps
Haznec i CSICS'04	7-Tap Transversal Filter	0.18µm SiGe BiCMOS f_T = 160 GHz, f_{MAX} = 160 GHz	750 mW from 5 V supply	49 Gbps
Laskin CISCS'08	2:1 MUX with FFE	SiGe8HP f_T = 210GHz, f_{MAX} = 260GHz	1.94 W from -3.3V	90 Gbps
Shakiba, JSSC'99	Receive Equalizer	0.5 µm Bipolar f_T = 14 GHz	12.7 mW from -3 V and -2 V	2.5 Gbps
This Work	Receive Equalizer	0.13µm SiGe BiCMOS f_T = 230 GHz, f_{MAX} = 280 GHz	336.6mW from 3.3 V	70 Gbps

4 Retimer Design

4.1 Background

The rapid and continual grown in multimedia services has created an ever increasing demand for high data rate communication systems. Flip flops are the most critical digital blocks and have several uses in today communication systems. They can be used as retimers in transmitters, as phase detectors in clock and data recovery circuits (CDR), and as decision circuits when placed at the front of a receiver. In a full-rate transceiver, the flip-flop must operate at a clock frequency equal to the data rate making this one of the highest frequency block in the system. Their maximum operating frequency can limit the system operating frequency hence the flip flop performance is critical for high speed data communication.

Several variations on the classical CML latch have been proposed in literature in order to extend the bandwidth. Double emitter followers (E^2F) are used in order to extend the operating frequency to 51 GHz in [Rylyakov]; this however requires the use of a higher supply voltage of -5.2 V. In [Dickson] MOSFETs replace the clock transistors and only one set of source followers are used instead of E^2F in order to reduce the supply voltage to 2.5 V, the trade off being an operating frequency of 43 GHz.

Many low voltage latch topologies have been proposed in literature. In [Razavi], a triple-tail cell is proposed in which the differential data pair is controlled using clamp transistors whose base is connected to the clock signal and its emitter is connected to the emitters of the differential pair. When a high voltage is applied to the clamping clock transistor, it starves the current flowing through the corresponding differential pair. Unfortunately large clock signals are required in order to properly turn off the differential pair. In [Kishine], the clock differential pair is replaced by current mirror controlled logic in order to lower the supply voltage. The increase delay on the clock path due the current mirror makes this not suitable for high frequency operation. Low voltage topologies were implemented in CMOS by removing the tail current source [Theo]. This however is not an option when using an HBT implementation due to the fact that the current through the HBT varies exponentially with V_{BE}. Small variations in the base voltage due to process variations lead the transistors to no longer be biased at $J_{peak\ f_T}$ thus diminishing

performance. Another method for lowering the supply voltage is to use a transformer to couple the signal between clock differential pair and the data transistors. This however leads to a limited operating range due to the tuned nature of the transformer.

4.2 Retimer Architecture

The classical retimer architecture consists of two latches arranged in a master slave configuration that form a standard CML Flip Flop. When the retimer is intended as part of the transmitter, it is placed as the last element in the chain so that the system transmits with the lowest possible jitter. However, the system must be matched to the cable impedance. Although the latch can be designed to be matched to 50 Ω, or 75 Ω as the case may be, this reduces the maximum operating frequency. In order to achieve the fastest latch possible, it should be designed without matching consideration after which a series of buffers can be added to achieve the necessary output matching. This project was targeting the highest achievable operating frequency hence the output buffers were added at the expense of extra power consumption, added jitter and increased area. The retimer block diagram can be seen Figure 4.1. A cascade of two buffers is used after the retimer in order to achieve an output matching of 50 Ω. The emitter followers (EF) are necessary in order to provide the required DC operating level for the subsequent stage. The transistor level description for each block is detailed in Sections 4.3 and 4.4. The full chip used to test the retimer is discussed in Section 5.1.

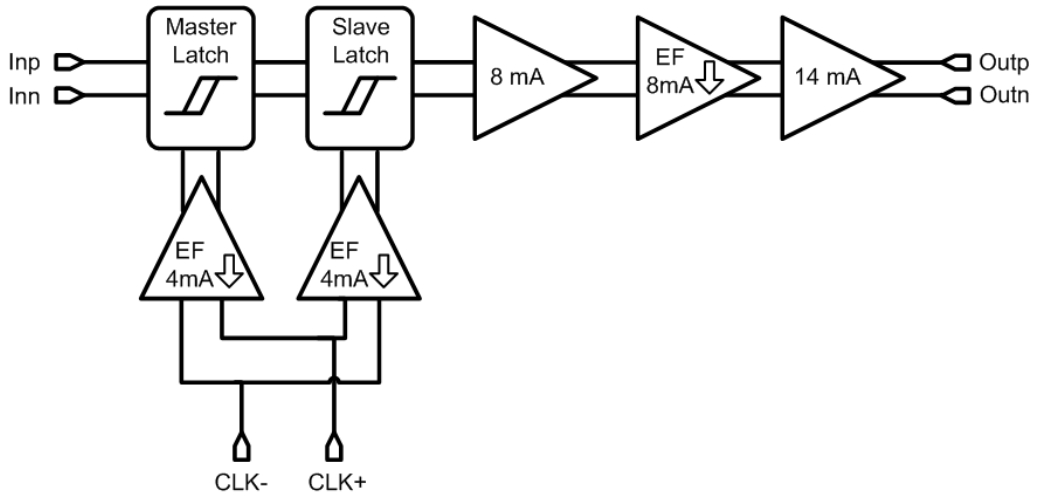


Figure 4.1: Retimer block diagram consisting of the Master – Slave D Flip – Flop and output buffers.

4.3 Retimer Latch Design

Due to the availably of both MOSFET and Bipolar transistors, BiCMOS technologies allow for numerous latch topologies several of which were discussed in Section 4.1. The topologies most suited for high speed operation, and the ones analyzed here are seen in Figure 4.2.

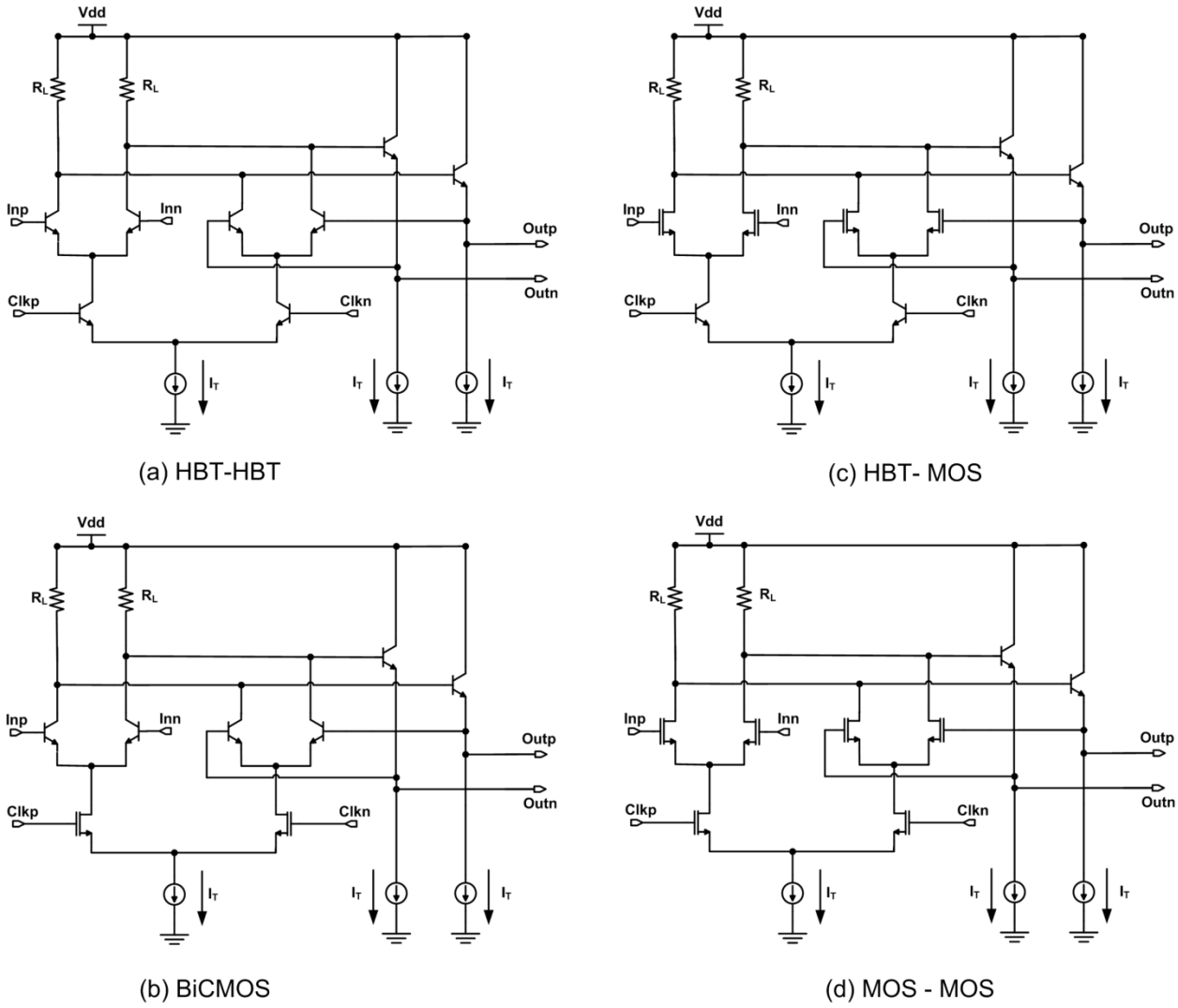


Figure 4.2: Latch topologies in BiCMOS technology.

In order to simplify the analysis, the load resistance (R_L) and tail current (I_T) are kept constant for each design while the MOSFETS and HBTs, with the exception of the emitter followers, are sized so that they function at their respective peak f_T current density ($J_{peak\ f_T}$). The emitter followers are primarily used as signal buffers for the preceding stage due to their high input

impedance and low output impedance. In the feedback path, they also allow for a higher V_{DS} (or V_{CE}) for the data path MOSFETs (or HBTs) thus maximizing their f_T. The main obstacle of lowering the power dissipation of the latch is due to the of the SiGe HBT which is nearly 1V when the device is biased at $J_{peak\ f_T}$. Emitter followers in the feedback path further increase the supply voltage hence only one set of emitter followers will be used in order to maintain the supply voltage at 3.3 V and reduce power consumption.

The maximum operating speed of each topology can be compared by examining the open-circuit time constants of each of the latches. The processed used for cascode inverters outlined in [Tod] can applied to these latches. It can be noted that each latch is loaded by the same emitter follower stage, hence it is sufficient to compare the time constants at the input of the emitter followers to be able to compare the relative speeds of the different topologies. For this analysis, it can be assumed that the data input has already settled, ΔV_{MOS} (ΔV_{HBT}) is the voltage swing needed to switch the MOSFET (HBT) clock pairs and C_{in} is the input capacitance to the emitter follower stage. The time constants at the input of each emitter followers are given by:

$$\tau_{HBT-HBT} = \Delta V_{HBT}\frac{2C_{bc}+2C_{cs}+C_{in}}{I_T} + \left(1+\frac{R_b}{R_L}\right)\Delta V_{HBT}\frac{C_{be}+2C_{bc}}{I_T} + \frac{C_{be}+C_{cs}+C_{bc}}{g_{m,HBT}} \tag{4.17}$$

$$\tau_{BiCMOS} = \Delta V_{MOS}\frac{2C_{bc}+2C_{cs}+C_{in}}{I_T} + \left(1+\frac{R_g}{R_L}\right)\frac{\Delta V_{HBT}}{I_T}\left\{C_{gs}+(1+\frac{g_{m,MOS}}{g_{m,HBT}})C_{gd}\right\} + \frac{C_{be}+C_{db}+C_{gd}}{g_{m,HBT}} \tag{4.18}$$

$$\tau_{HBT-MOS} = \Delta V_{HBT}\frac{2C_{gd}+2C_{db}+C_{in}}{I_T} + \left(1+\frac{R_b}{R_L}\right)\frac{\Delta V_{MOS}}{I_T}\left\{C_{be}+(1+\frac{g_{m,HBT}}{g_{m,MOS}})C_{bc}\right\} + \frac{C_{gs}+C_{cs}+C_{bc}}{g_{m,MOS}} \tag{4.19}$$

$$\tau_{MOS-MOS} = \Delta V_{MOS}\frac{2C_{gd}+2C_{db}+C_{in}}{I_T} + \left(1+\frac{R_g}{R_L}\right)\Delta V_{MOS}\frac{C_{gs}+(1+2)C_{gd}}{I_T} + \frac{C_{gs}+C_{db}+C_{sb}+C_{gd}}{g_{m,MOS}} \quad (4.20)$$

Each equation is of the form:

$$\tau = \tau_{OUT} + \tau_{IN} + \tau_{MID} \quad (4.21)$$

The first term of the equation, τ_{OUT}, represents the time constant at the output of the cascode pair and input of the emitter follower stage. The second term τ_{IN} represents the time constant at the input of the clock transistors while τ_{MID} represents the time constant seen at the drain (or collector) of the clock transistor.

When carrying the same current, and sized so that they are each biased at their respective $J_{peak\ f_T}$, the parasitic capacitances are much higher for the MOSFET than for the HBT, while the g_m of an HBT is much higher that of the MOSFET. The lower MOSFET gain has the advantage of reducing the Miller effect.

The intrinsic and extrinsic components of the base resistance for the SiGe HBT can be reduced by using multiple emitter stripes. This however increase the base-to-collector capacitance making R_bC_{bc} approximately constant for a given technology node [Tod]. The gate resistance for MOSFETS however can be reduced through layout minimization while the while the gate-drain overall area is kept constant thus C_{gd} remains constant. For these reasons and the equations (4.17) through (4.20), it is expected that the HBT-HBT topology has the lowest τ_{MID} followed by the BiCMOS, HBT-MOS and then the MOS-MOS topology.

For a 0.130 µm MOSFETs, the required swing ΔV_{MOS} is roughly 400mV and reduces by a factor of $\sqrt{2}$ for each technology node [Tod]. For HBT gates, the required voltage swing ΔV_{HBT} is slightly lower at 300 mV [Tod] regardless of technology node. It is therefore expected that the HBT-HBT topology has the best τ_{OUT} while the MOS-MOS topology has the slowest τ_{OUT}. Given that $\Delta V_{MOS} > \Delta V_{HBT}$ and $g_{m,HBT} > g_{m,MOS}$ the slowest τ_{IN} is expected for the HBT-MOS case.

Setting the tail current to 8 mA results in a load resistance, R_L, of 50 Ω in the case of MOSFET data pairs and 37.5 Ω in the case of HBT data pairs. In order to be biased at $J_{peak\ f_T}$, the HBTs are sized to 2 µm emitter lengths while the MOSFETs are realized using 14 fingers each of 1µm. The tail current is set using a MOSFET current mirror with gate width of 32 µm. The HBTs in the emitter pairs are sized at $0.5 \times J_{peak\ f_T}$. Simulation results for the four different topologies using an 80-Ghz clock frequency are shown in Figure 4.3 .

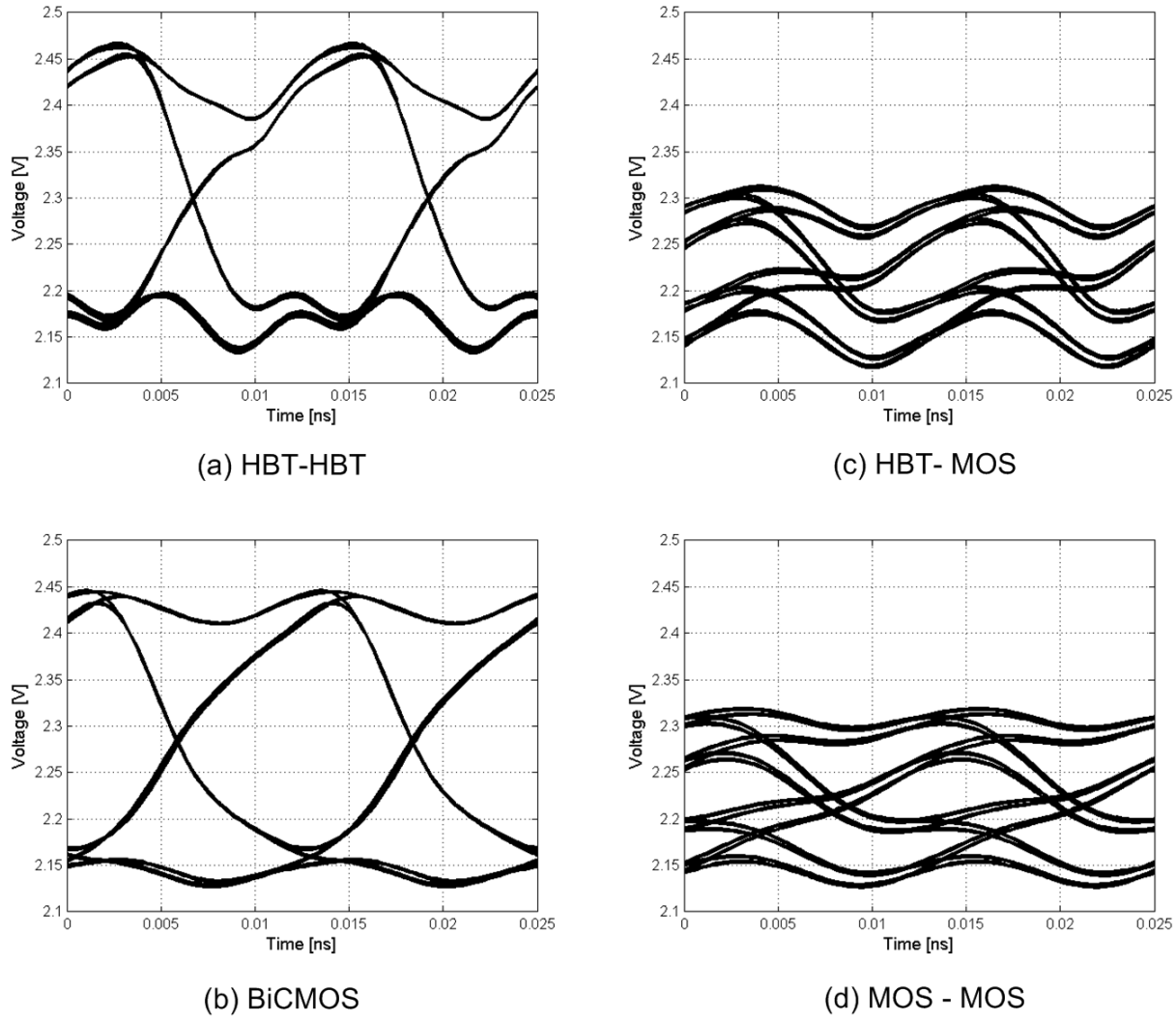


Figure 4.3: Simulated 80 Gbps eye diagrams for the (a) HBT-HBT (b) BiCMOS (c) HBT-MOS and (d) MOS-MOS latch topologies.

As expected, the best performance was observed for the HBT-HBT topology with the BiCMOS technology coming in a close second. This contradicts the findings in [Katay PRBS, TOD] where the BiCMOS topology slightly outperformed the HBT-HBT topology. This is due to the fact that [Katay PRBS, TOD] used a similar 0.13 um SiGe BiCMOS topology which had slower HBTs with f_T of 150 GHz compared to the 240 GHz for this technology [Chevalier] while the MOSFETs remained the same. The 60% increase in HBT performance was enough to make the HBT-HBT outperform the BiCMOS topology.

The HBT-HBT topology requires the smallest voltage swing to be applied on the clock pair, lowering the strain on the clock buffers, which is a major consideration when operating with above 100 GHz signals. Taking the hand calculations and simulation results into account, the HBT-HBT topology was chosen for fabrication. The transistor level schematic of the manufactured latch is shown in Figure 4.4.

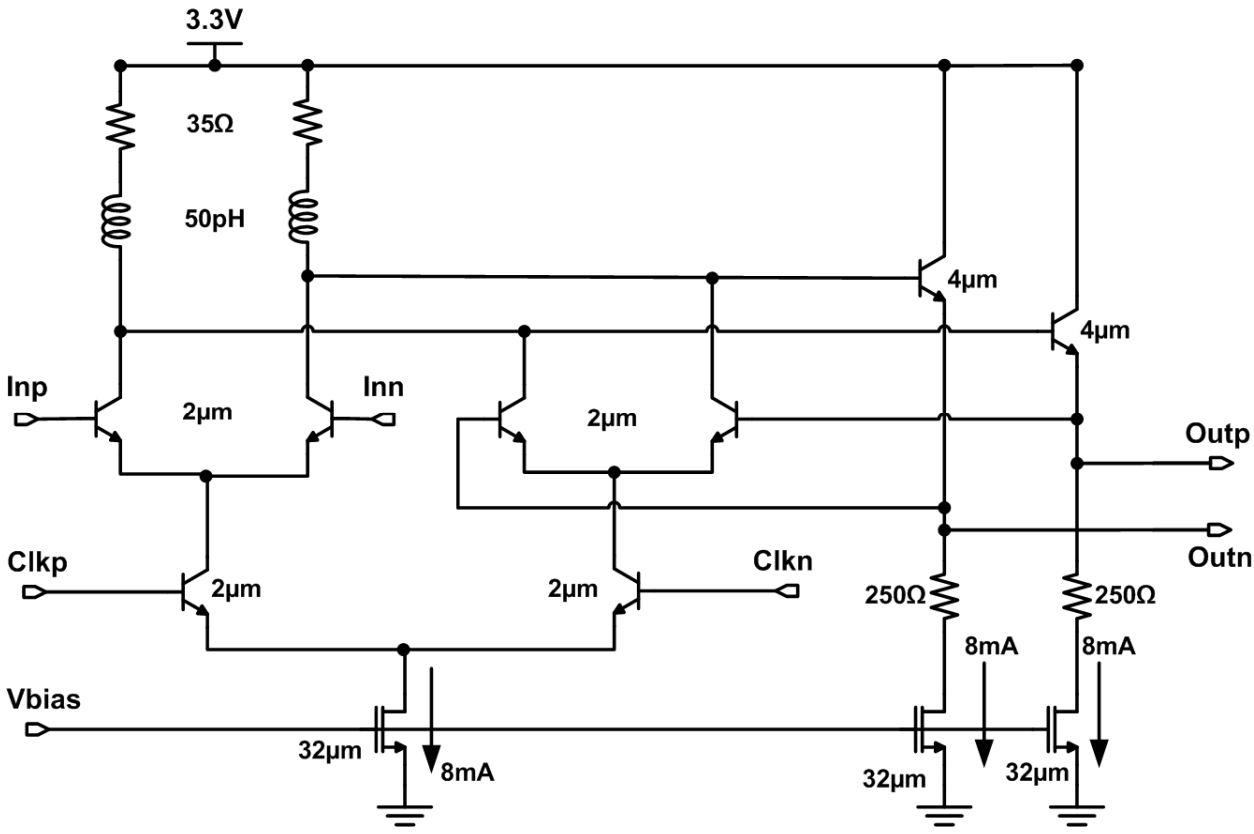


Figure 4.4: Fabricated latch using the HBT-HBT topology.

The first design step is choosing the tail current, which is 8 mA in this case. From this it follows that the load resistance should be 37.5 Ω in order to allow for a 300 mV swing. In order to account for contact and metal resistances in the inductor, the load resistor was slightly reduced to 35 Ω. A 20% variation in the resistor size corresponds to a 60 mV difference in the ΔV_{HBT} still leaving enough margin to switch the HBTs.

In order to be biased at $J_{peak\ f_T}$ of 2 mA/µm [] when balanced, 2 µm emitter lengths are chosen. The emitter followers are sized at $0.5 \times J_{peak\ f_T}$. The tail currents is are implemented using MOSFET current mirrors and a 220 Ω resistor is inserted in the emitter follower in order to reduce the MOSFET V_{DS} to approximately 300 mV and provide better matching with the bias distribution as well as lower the capacitance seen at the emitter of the HBT.

The latch bandwidth can be improved by up to 60% by using inductive peaking [33] and sizing the inductor using:

$$L = \frac{{R_L}^2 C_L}{3.1} \tag{4.22}$$

From the above equation it becomes obvious that a small load resistor is desirable in order to reduce the inductor size and save area. Decreasing the resistor however increases the power consumption since the tail current must be increased in order to maintain the same voltage swing. The increase in tail current also entails an increase in device size so that the HBTs are still biased at $J_{peak\ f_T}$ thus leading to larger parasitic capacitance and hence larger load capacitance C_L.

$$C_L \approx\ 2C_{bc} + 2C_{cs} + C_{bc,EF} + \ C_{be,EF} \approx 126\ fF \tag{4.23}$$

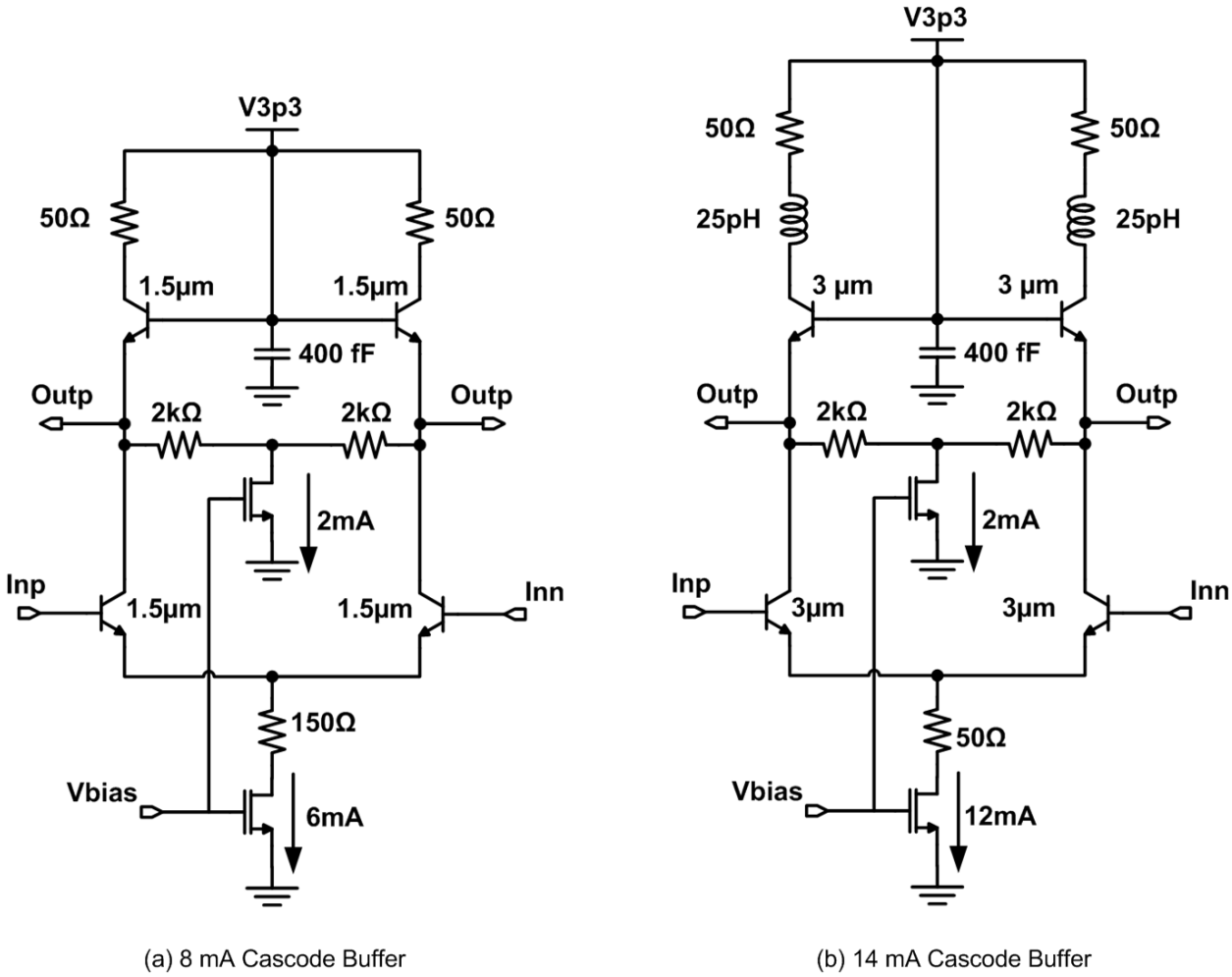
Using Equation (4.22), this leads to a peaking inductor if roughly 50 pH. This extends the -3 dB bandwidth BW_{3dB} [9] to:

$$BW_{3dB} \approx\ 1.6 \times \frac{1}{2\pi R_L C_L} \approx 57.7\ GHz \tag{4.24}$$

which is sufficient for 110 Gbps operation. The inductor is implemented as a spiral inductor employing the copper Metal 5 and Metal 6 layers of the millimetre-wave back end. The Q factor of this inductor is not highly important since its resistance can be absorbed by R_L.

4.4 Retimer Output Buffers

In order to match to the 50-Ω system output load, two buffers are cascaded after the retimer as depicted in Figure 4.1. The cascode buffer schematics can be seen in Figure 4.5.



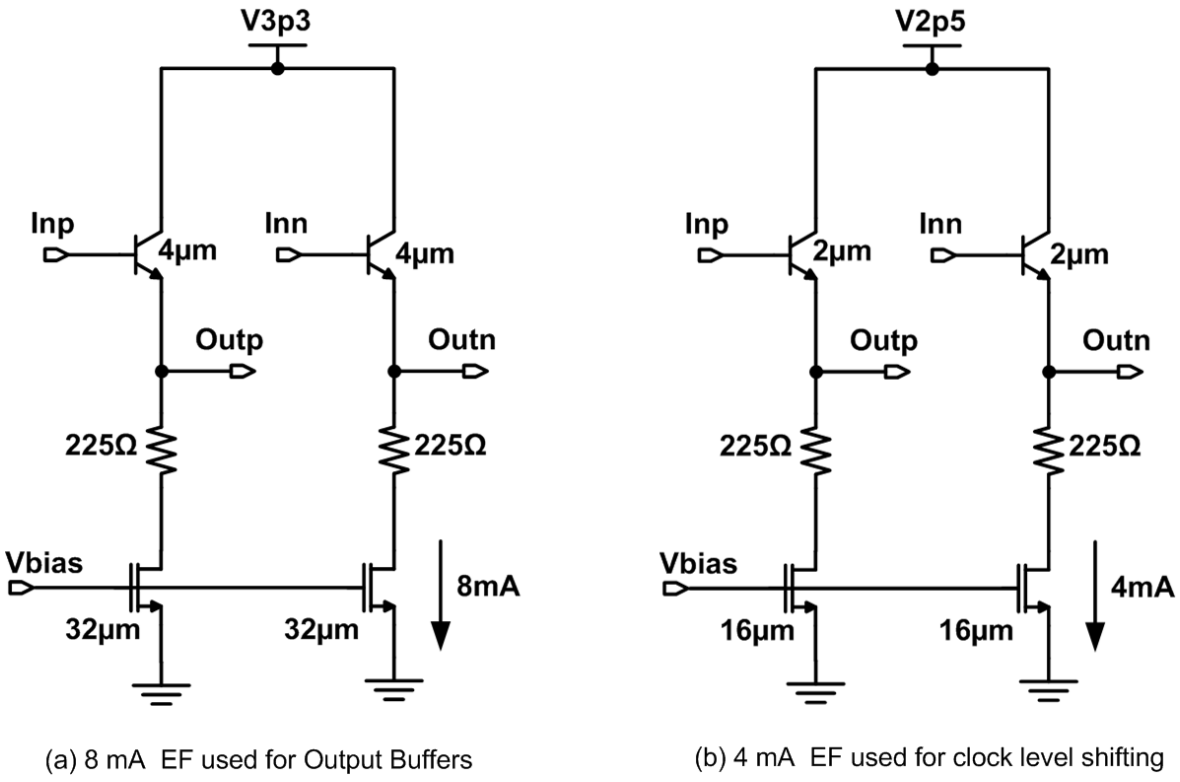
(a) 8 mA Cascode Buffer (b) 14 mA Cascode Buffer

Figure 4.5: Retimer output buffers: (a) first buffer and (b) final 50-Ω buffer.

The input HBTs are biased at $J_{peak\,f_T}$ while the common base HBTs are biased at slightly higher current density. The role of the 2 mA current is to allow for the proper input DC bias for the next stage. One approach would have been to keep the same bias current but increase the load resistance; this however would have deteriorated the frequency response of the cascode. Another approach is to increase the tail current, however this would have required bigger HBTs in order to maintain $J_{peak\,f_T}$ biasing. Introducing the 2-mA current source produces the same effect for the same power consumption, without the need for bigger devices at the input. In addition, the

common base transistors are never current starved hence are faster when switching from the "off" state to the "on" state. The resistor sizes are chosen so that the voltage swing is 300 mV. The 12-mA output buffer is AC coupled to a 50-Ω load making the effective load 25-Ω at high frequencies. The output buffer has an additional 25-pH inductor in order to account for parasitic in the test circuit and pads.

In order to provide the proper DC biasing between the stages, the buffers are separated by an 8-mA per side emitter follower seen in Figure 4.6 (a). The emitter follower has the benefit of extending the bandwidth of the 8-mA buffer without the need for peaking inductors which occupy a large area. Two other 4-mA emitter followers seen in Figure 4.6 (b) are used to provide the proper DC levels for the latch clock inputs. The preceding clock buffers are biased from 2.5 V, therefore, in order to save power and due to the availability of the power supply, the emitter follower stage was also biased from 2.5 V. The HBTs in the emitter followers are biased at $J_{peak\ f_T}$ while the role of the resistor is to provide set the MOSFET V_{DS} for proper current mirror matching as well as decreasing the capacitance seen at the emitter and thus increasing stability.



(a) 8 mA EF used for Output Buffers

(b) 4 mA EF used for clock level shifting

Figure 4.6: Emitter Followers used to (a) cascade output buffers and (b) provide proper DC levels for latch clock inputs.

4.5 Simulation Results

The Retimer was first simulated using an ideal 300-mVpp, 125-Gbps differential input signal. The output eye after the retimer and after the final output buffers can be seen in Figure 4.7 and Figure 4.8 respectively. It can be seen that the output buffers deteriorated jitter seen after the retimer.

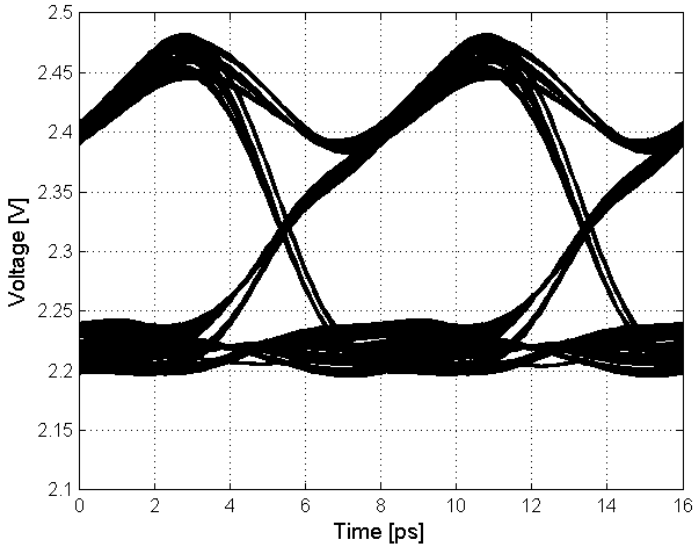


Figure 4.7: A 125-Gbps signal at the output of the Retimer when retimed at 125GHz.

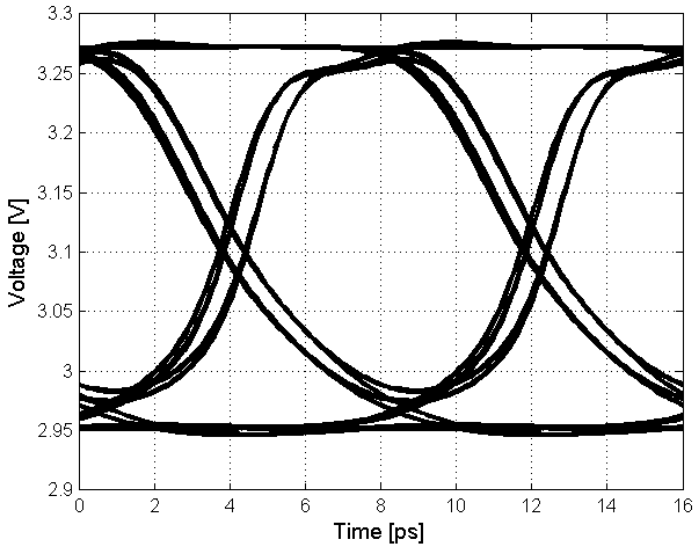


Figure 4.8: A 125-Gbps signal after the 50-Ω output buffer when retimed at 125GHz.

The Retimer can also be used to retimer half rate data. A 62.5-Gbps input data stream retimer at 125 GHz can be seen at the output of the Retimer in Figure 4.9 and at after the 50-Ω output buffer in Figure 4.10.

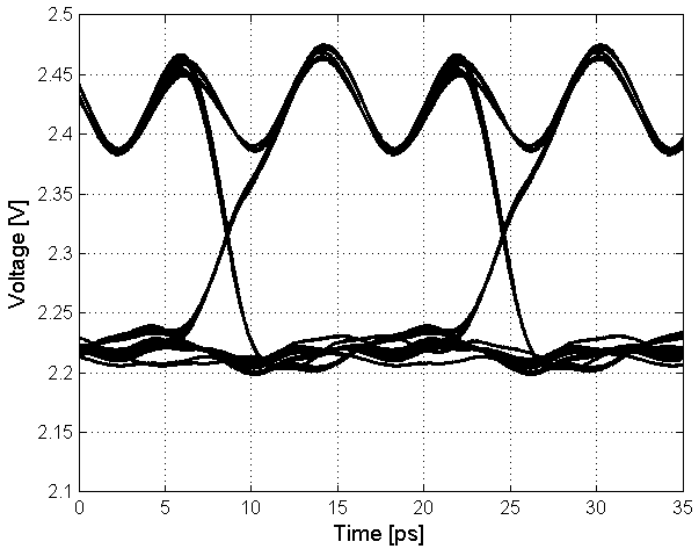


Figure 4.9: A 62.5-Gbps signal at the output of the Retimer when retimed at 125GHz.

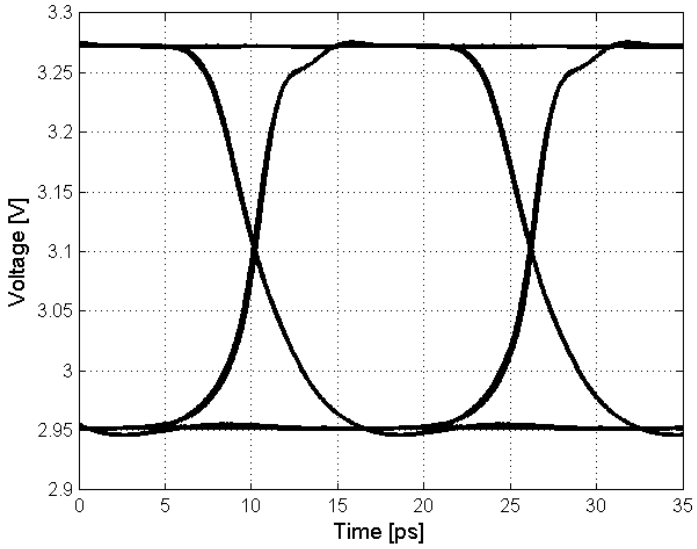


Figure 4.10: A 62.5-Gbps signal after the 50-Ω output buffer when retimed at 125GHz.

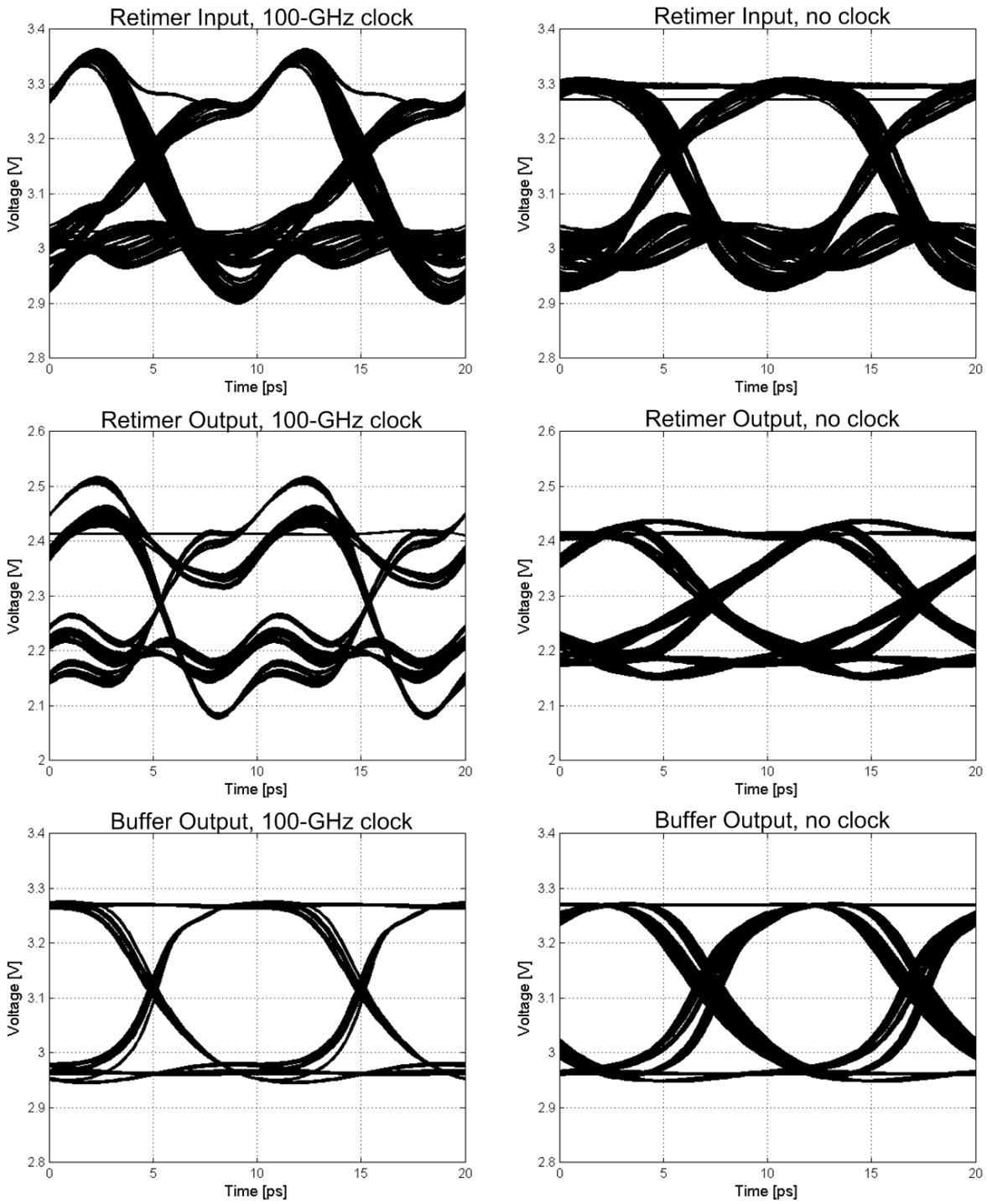


Figure 4.11: Retimer simulations with 100-Gbps input data and 100-GHz Retimer clock.

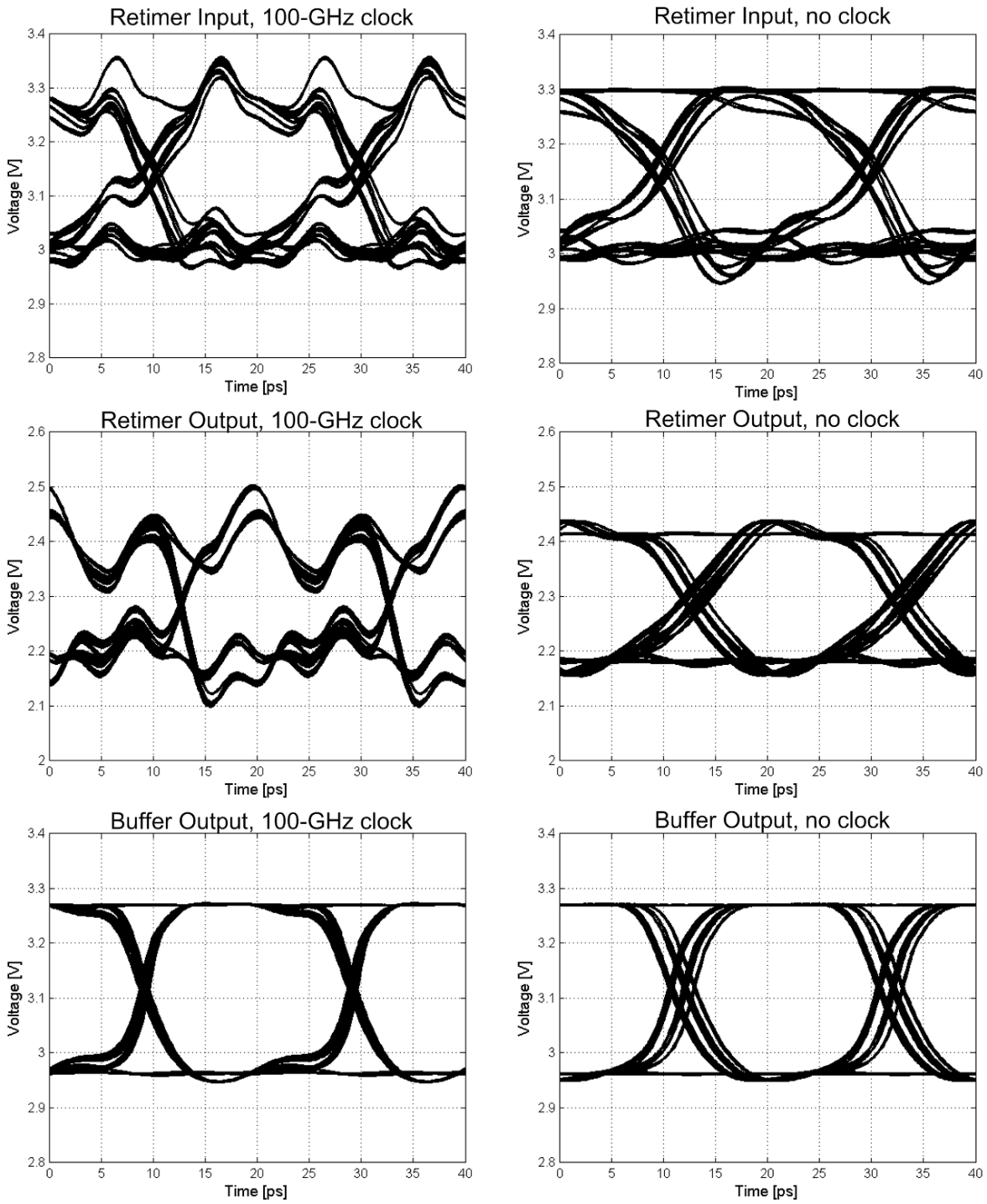


Figure 4.12: Retimer simulations with 50-Gbps input data and 100-GHz Retimer clock.

5 Retimer Fabrication and Experimental Results

5.1 Test Chip

In order to test the Retimer, a test circuit was fabricated that has an on-chip PRBS generator. A diagram of the Retimer test circuit can be seen Figure 5.1. The work discussed in this thesis, the Retimer and output buffers, is highlighted in the diagram while the other blocks were previously designed and published.

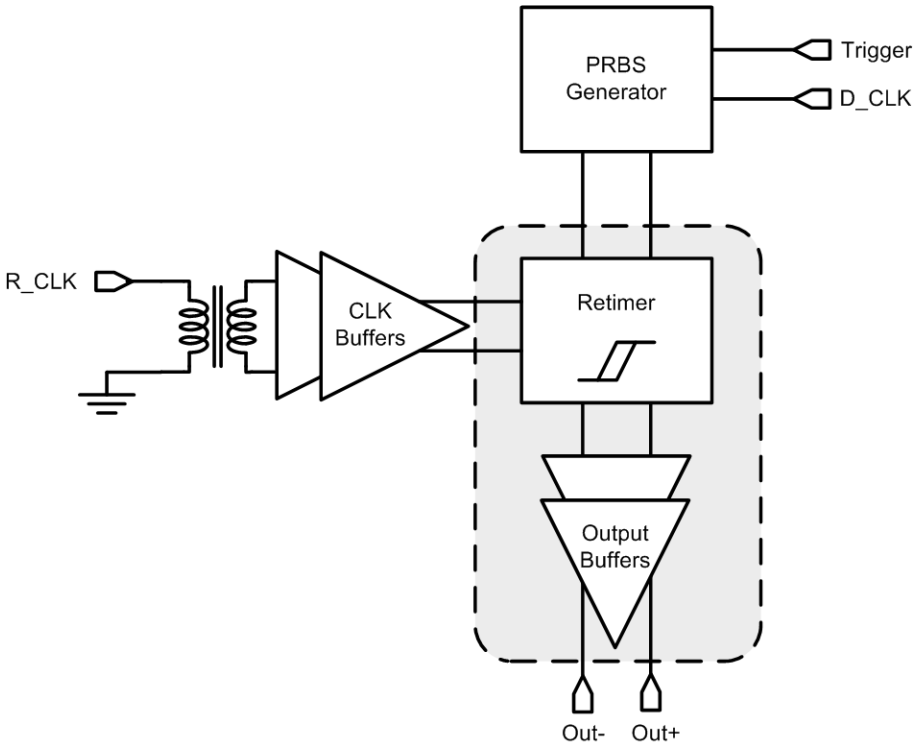


Figure 5.1: System Architecture of the Retimer Test Chip

In order to eliminate the need for an on-chip VCO and thus reduce space, the Retimer clock signal (R_CLK) is provided by an external source as a single ended input. In order to generate the differential signal needed by the retimer, a transformer balun followed by two tuned buffers are used. The transformer, previously designed by Ioannis Sarkas, has primary and secondary inductances of 100 pH and a coupling factor of 0.8. The two clock buffers, designed by Shahriar Shahramian, each consist of an HBT cascode with emitter followers. The clock buffers are tuned for 110 GHz using 40-pH inductive loading. Each buffer consumes 20 mA from a 2.5-V supply

for a total of 100 mW for the pair. A chain of these buffers could have been used to transform the single ended clock input into a differential signal, however their high power consumption along with their low common mode rejection at 110 GHz made the use of the transformer balun at the input the preferred choice.

The PRBS generator was originally designed by Tod Dickson and published as an 86 Gbps 2^7 -1 PRBS Generator in [28]. It produced an eye amplitude of 300 mVpp per side and RMS jitter of 582 fF. A re-spin of the circuit for this tapeout was made by Katya Laskin and Ricardo Aroca. A separate clock is used for the PRBS generator in order to be able to align the PRBS data provided at the input of the retimer with the retimer clock. Two external clock signals allows for a phase shift to be introduce between the two.

The Retimer test chip was designed using the same technology that was used for the Equalizer, this being STMicroelectronics' 0.13µm SiGe BiCMOS9MW technology with HBTs having a f_T of 240 GHz and f_{MAX} of 270 GHz [30]. A photomicrograph of the fabricated test chip can be seen in Figure 3.1. The unlabelled pads are connected to ground. The pad limited area of the chip is 1055µm x 1290µm. A description of the each pad is given in Table 5-1.

Table 5-1: Pad Description for the Retimer Test Circuit

Pad Name	Description
R_CLK	High speed clock input.
Out-	High speed differential retime output.
Out+	High speed differential retime output.
I_Retimer	Retimer bias current with nominal value of 2 mA.
V3p3	Retimer Vdd with nominal value of 3.3 V.
D_CLK	High speed data input clock.
Trigger	Output signal used to trigger the oscilloscope pattern capture function.
I_MUX	Mux bias current with nominal value of 1.2 mA.
Reset	PRBS data reset function.
M_CLK_Bias	Bias current for the MUX clock buffers with nominal value of 1.2 mA.
V2p5	Data Generator Vdd with nominal value of 2.5 V.
I_PRBS	Bias current for the PRBS with nominal value of 2 mA.
R_CLK_Bias	Bias current for the retime clock buffers with nominal value of 2 mA.

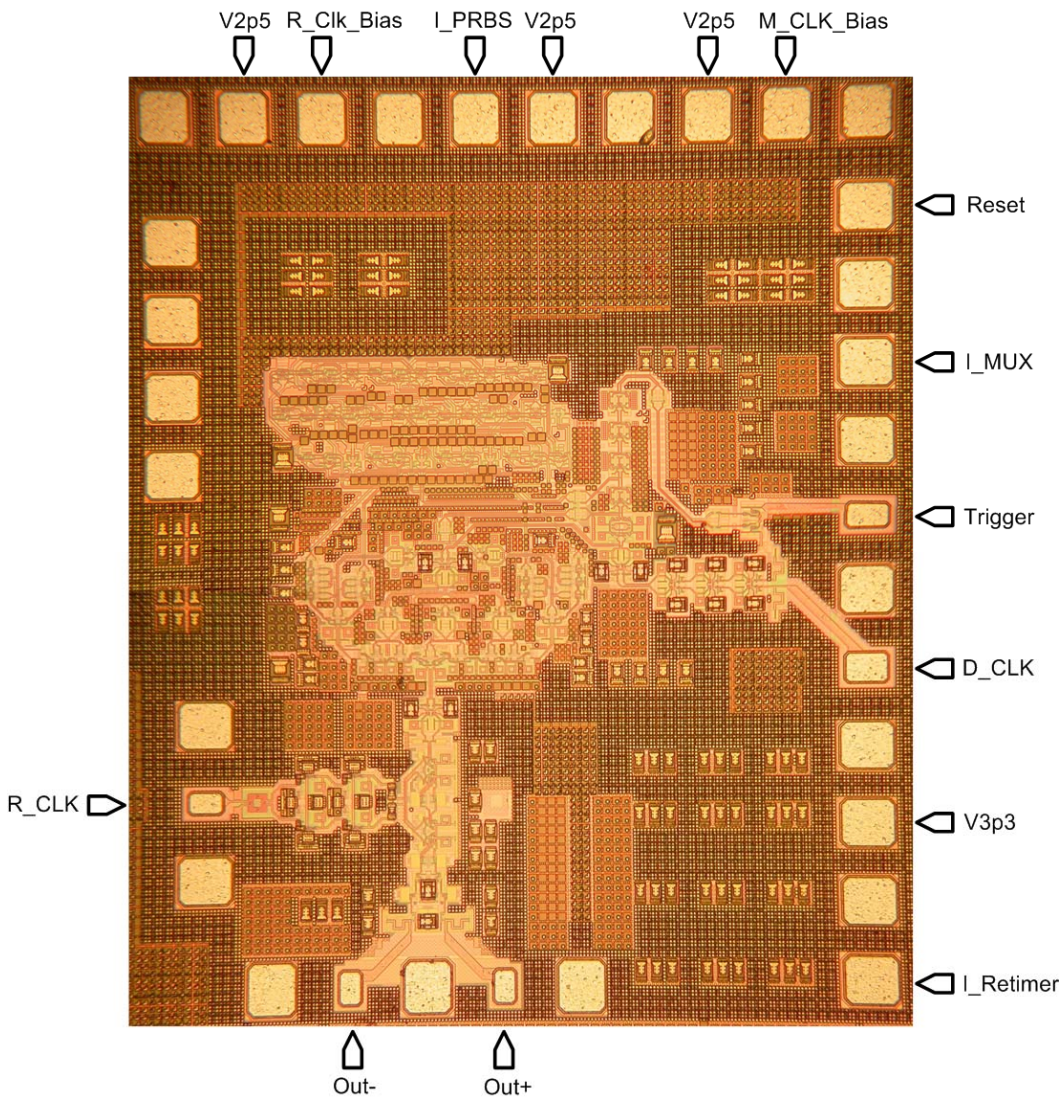


Figure 5.2: Photomicrograph of the retime test chip.

The circuit consumes 457 mA (1143 mW) from a 2.5-V supply hence three DC pads (V2p5) were used to provide this power. An additional 94 mA (310 mW) is consumed from a 3.3-V supply which is provided using only one DC pad. The 94 mA supply the retimer, output buffers and the required bias circuitry.

5.2 Measurement Setup

All measurements were conducted on wafer and diagram of the test setup can be seen in Figure 5.3. The DC power supplies and sources are not shown in the diagram. A single ended 110 GHz GGB probe was used for the high speed Retimer clock input. A low speed clock signal was provided by the Agilet E8257D PSG Analog Signal Generator. This device can only provide signals up to 67GHz. In order to produce higher speed clock, the signal was fed to a Militech 236 multiplier which produced a signal equivalent to 6 times the input signal frequency thus producing the high speed R_CLK. The data clock was generated using the Hewlet Packard 83650B Series Swept Signal Generator. In order to prevent phase drift, these two signal sources were synchronized using a 10 MHz signal produced by the Agilent source. In order to trigger the scope, the Agilent signal is split using an Anritsu V240 Power Divider, one signal is used to feed the multiplier while the other is used for the scope trigger.

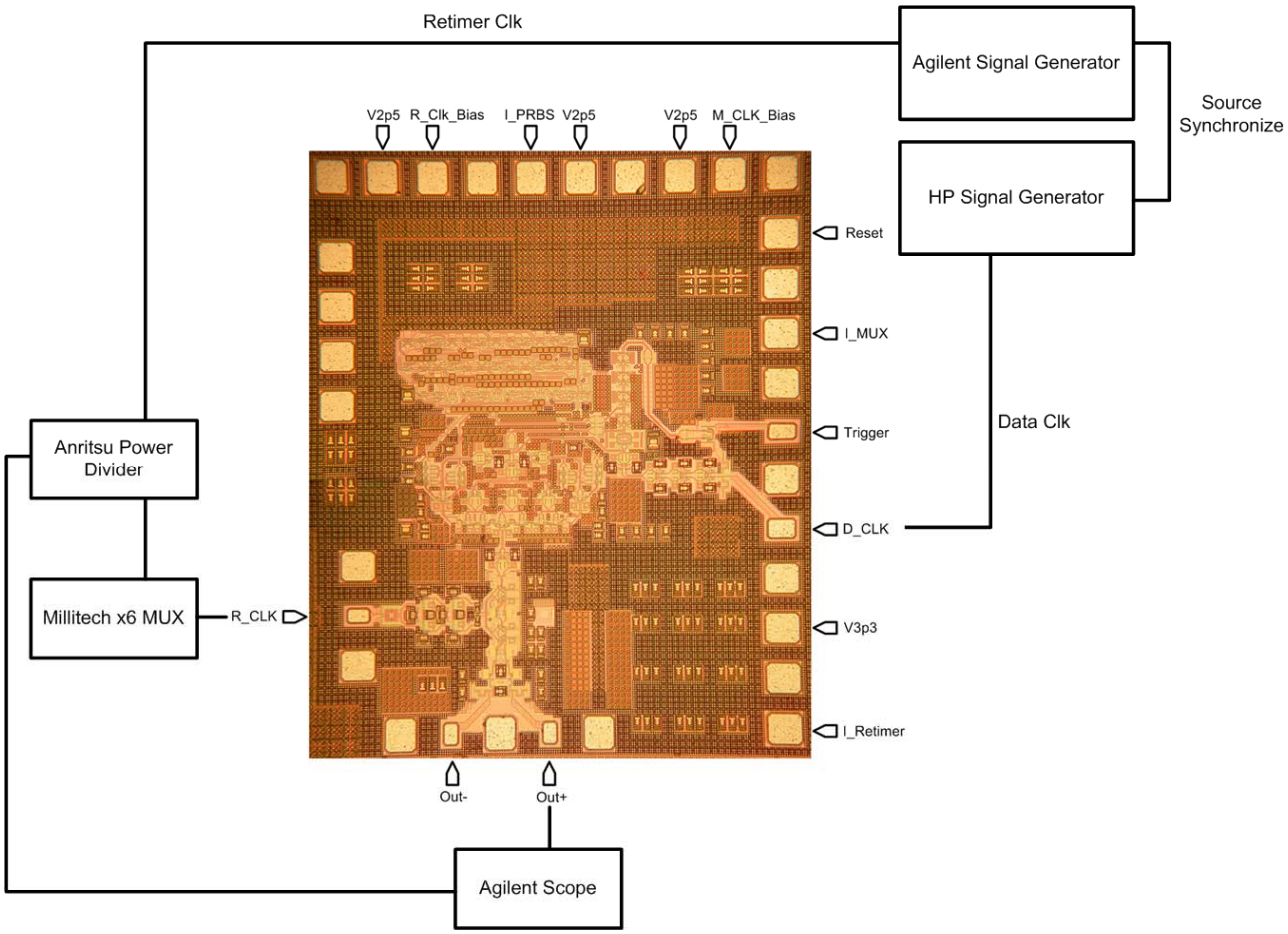


Figure 5.3: Retimer Test Setup Diagram.

The design required that the output be measured using a differential 110 GHz probe in order to provide symmetrical loading for the output buffer. When the measurements were performed however, it was discovered that there was not enough space for the differential 110 GHz output probe due to the proximity of the composite probe. Two different experiments were therefore performed, first a differential 67 GHz probe was used, and then a single ended 110 GHz probe was used. The data was captured using an Agilent Infinium DCA-J 86100C Digital Communication Analyzer with an Agilent 86107A Precision Timebase Module. When using the differential probe, the second output was terminated using a capacitor and 50-Ω load. In the case of the single ended probe, the second output was left floating. A picture of the measurement setup can be seen in Figure 5.4.

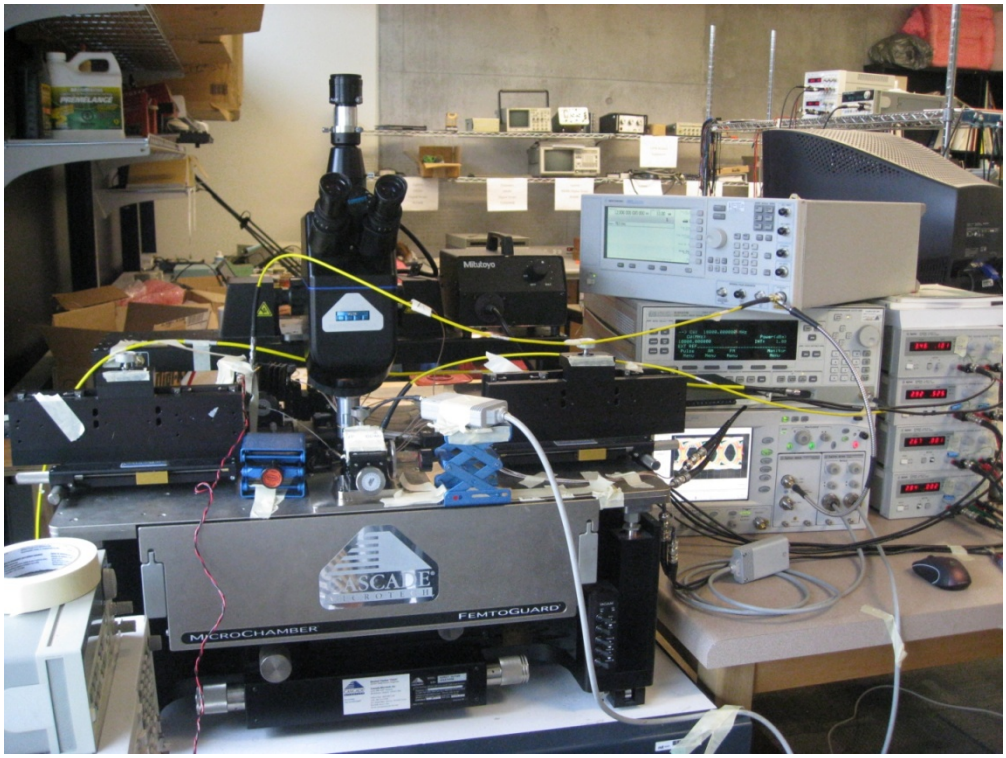


Figure 5.4: Picture of the Retimer Measurement Setup. (Label Components)

5.3 Measurement Results

When the chip was fabricated, it was discovd that the PRBS generator only functioned up to 72 Gbps. The clock path to the Retimer, however, is tuned at 110 GHz and therefor cannot generate a strong enough signal at 72 GHz to retime the 72 Gbps data. The Retimer functionality can still be tested by retiming half rate data. For example, a 50 Gbps signal can be retimed using a 100 GHz clock. In order to test the Retimer performance, the system as first measured with the retimer clock off to get a base jitter measurement. In this situation, the Retimer let input data thru without actually retiming it. The Retimer clock was then turned on by turning on the power to the external multiplier and the impovement in jitter was measured and plotted in Figure 5.5. The captured eye diagrams used to generate this data are attached in Appendix A. Measurements were pefromed up to 118 GHz after which the Militech multiplier was no longer able to prove a strong enough clock for the Retimer. When using the 110GHz probes, the measured phase margin at 72 GHz was 48° (1.85 ps), at 90 GHz it was 38° (1.17 ps), and at 105 GHz it was 25° (0.66 ps).

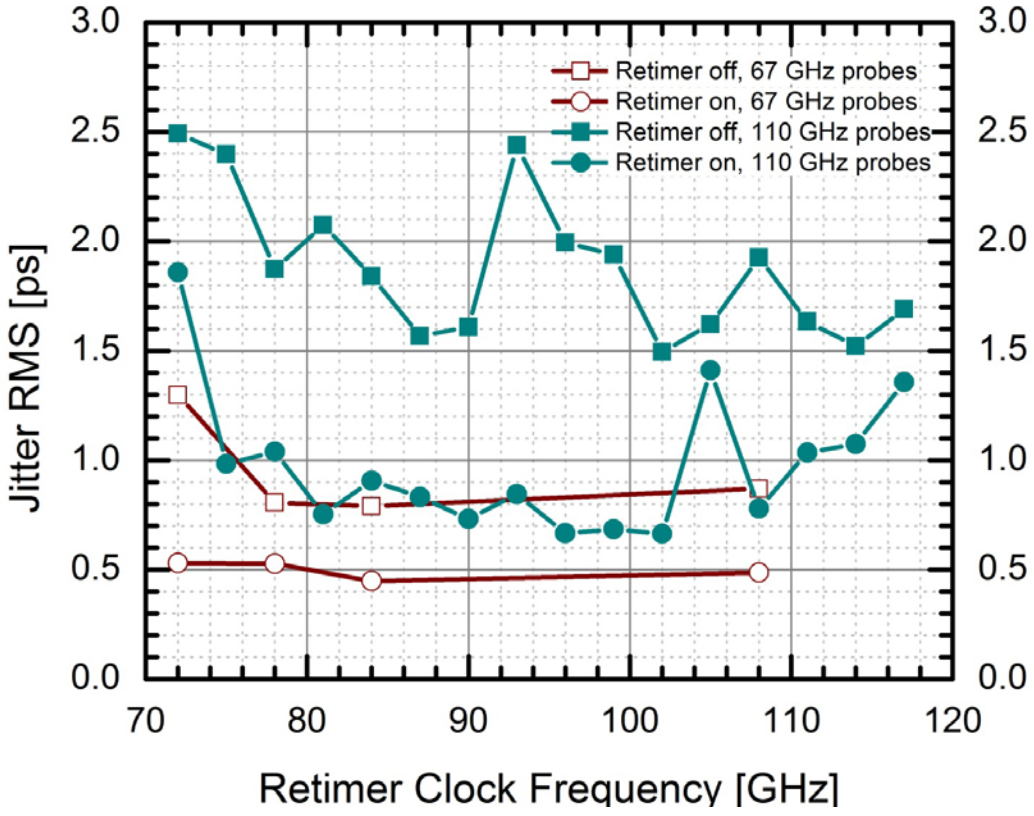


Figure 5.5: Improvement in jitter performance due to retiming.

Clearly an improvement in jitter can be observed then the Retimer clock signal is turned on. The lower quality 67 GHz probes also produce a much sharper signal then the 110 GHz probe. This is due to the fact that the 67 GHz probes are differential and provide a symmetrical load to the circuit while the 110 GHz is single ended and one output is left floating. This phenomenon is clearly observed in the eye diagrams for a 39 Gbps signal retimed using a 78 GHz clock in Figure 5.6. The measurements performed using the 110 GHz single ended probe are on the right hand side show a degradation in RMS jitter in both the retimed and not retimed case when compared the measurements on the left hand side which were performed using a differential 67 GHz probe.

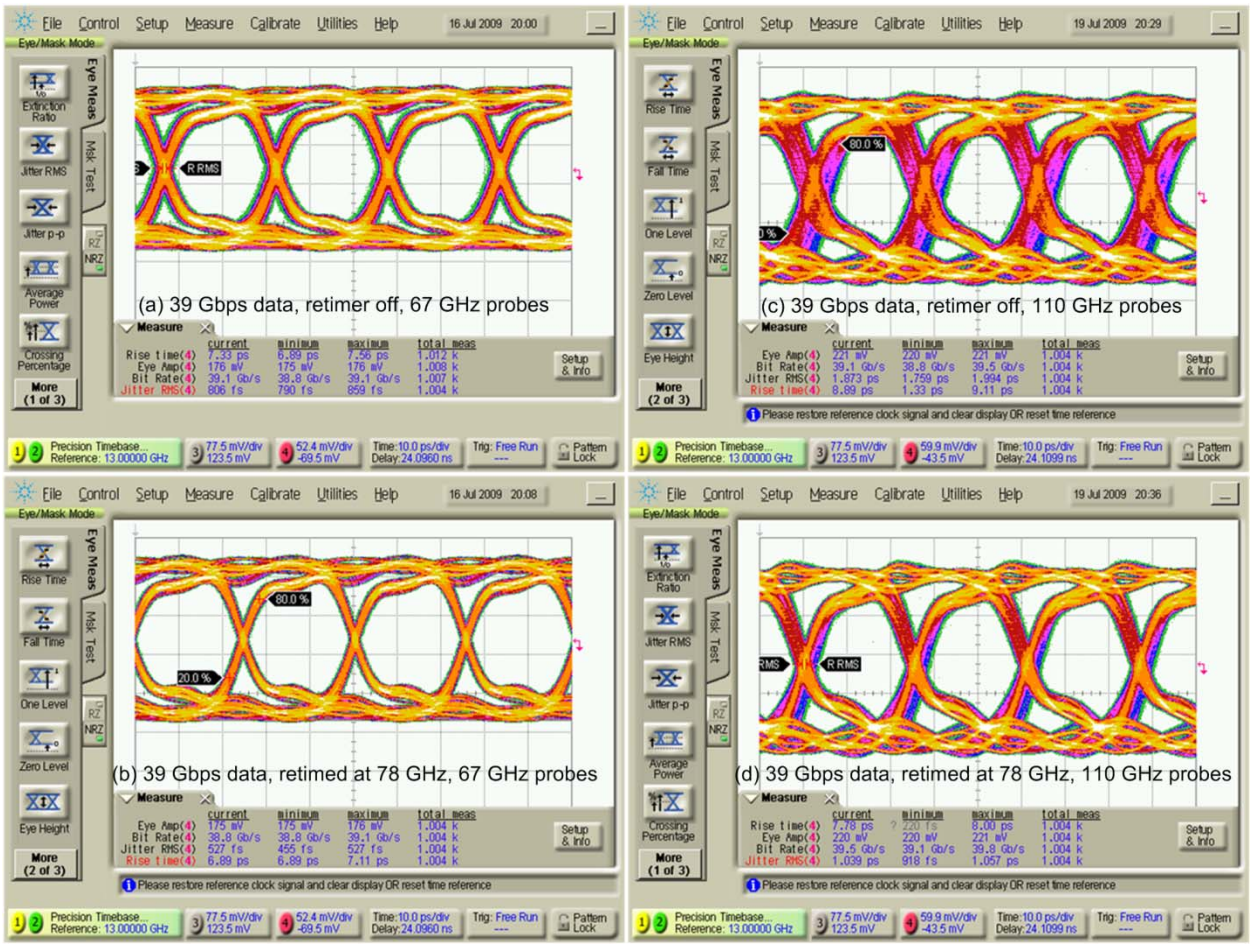


Figure 5.6: Eye diagrams for a 39 Gbps signal when measured with 67 GHz and 110 GHz probes.

5.4 Performance Comparisons

The Retimer described in this section has the faster operating clock frequency when compared with previously published work, as seen in Table 5-2. When compared with an InP HEMT technology with similar f_T [Suzuki], an almost 50% improvement in clock frequency is observed while the supply voltage is significantly lower. An improvement from 45 GHz [Dickson] to 118 GHz in clock frequency is observed over the previous 0.13µm SiGe BiCMOS technology node. Although part of the frequency increase can be attributed to the improvement in f_T from 150 GHz [Dickson] to 240 GHz [30]. The use of HBTs for the clock transistors, emitter followers on the feedback path and increased supply from 2.5 V to 3.3 V all contributed to more the double the clock frequency.

Table 5-2: Retimer performance comparison with previously published work.

Technology	Ref.	Technology Node	Power Consumption per Latch	Performance
BiCMOS	This work	0.13µm SiGe BiCMOS $f_{T,\ SiGe\ HBT}$ = 240 GHz	52.8 mW, 16mA per latch from 3.3V	59 Gbps data with 118 GHz clock, 25° phase margin at 105 GHz
	[Rylyakov]	0.18µm SiGe BiCMOS $f_{T,\ SiGe\ HBT}$ = 120GHz	156 mW; 30 mA per latch from -5.2 V	40 Gbps, 152° phase margin; 25.5 Gbps data with 51 GHz clock
	[Kucharski]	0.18µm SiGe BiCMOS $f_{T,\ SiGe\ HBT}$ = 120GHz	2.5 V, current not given	45.6 Gbps
	[Dickson]	0.13µm SiGe BiCMOS $f_{T,\ SiGe\ HBT}$ = 150 GHz	27.5 mW; 11 mA per latch from 2.5 V	45 Gbps
CMOS	[Shariar]	65 nm CMOS f_T = 170 GHz	9.6 mW; 8 mA per latch from 1.2 V	81 Gbps
	[Chalvatzis]	90 nm CMOS f_T = 125 GHz	10.8 mW; 9 mA per latch from 1.2 V	40 Gbps, 163° phase margin

Technology	Ref.	Technology Node	Power Consumption per Latch	Performance
InP	[Suzuki]	0.1µm InP HEMT f_T = 245 GHz	-5.7 V, current not given	80 Gbps
	[Amamiya]	InP HBT f_T = 150 GHz	20 mW, 13 mA per latch from 1.5V	50 Gbps
	[Yasuhiro]	0.13µm InP HEMT f_T = 150 GHz	-5.2 V, current not given	50 Gbps, 70° phase margin
	[Krishnamu]	InP DHBT f_T = 150 GHz	-4.2 V, current not given	43.2 Gbps, 190° phase margin

6 Conclusions

Table 6-1: Equalizer Performance

		3dB Bandwidth		
Cable	Length	Before equalization	After equalization	% improvement
V cable	1 m	16 GHz	43 GHz	269 %
SMA cable	1.8 m	11 GHz	30 GHz	273 %
Belden Cable	10 m	3 GHz	7 GHz	233 %

Although equalization has been proven for data travelling over long coaxial cables, the same principle can be extended for other copper media used in backplanes and twisted pair cables as well as for fiver optic cables all of which suffer from frequency dependent signal degradation.

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Appendix