Tunable RF Bandpass Delta-Sigma Digital Receivers with Millimetre-Wave Sampling Clocks

by

Theodoros Chalvatzis

A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy
Graduate Department of Electrical and Computer Engineering
University of Toronto

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Abstract

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This thesis presents the design and implementation of direct digitizing analog-to-digital converters for software-defined radio receivers. A new design methodology in the s-domain for continuous-time ∆Σ ADCs is presented. The system level design is carried out entirely in continuous-time by appropriately linearizing the digital components of the loop. A new circuit topology is introduced in the loop filter, which provides higher linearity and lower noise than previously reported filters. The filter is based on the combination of a MOSFET and HBT transistor, which also allows for low power operation.

The feasibility of mm-wave sampling is investigated in both SiGe BiCMOS and nanoscale CMOS technologies. The critical building blocks of the mm-wave analog-to-digital converter are implemented in SiGe BiCMOS and nanoscale CMOS. New topologies for the single-bit quantizer and clock distribution network are proposed in CMOS. The CMOS transimpedance amplifier proves the best solution for broadband amplification in nanoscale technologies, where the power supply must be kept lower than 1.2 V. A novel latch topology employing devices with low and high $V_T$ allows for operation at 40-Gb/s from 1.2 V with a record low power dissipation per latch.

The design techniques presented in this work lead to the first analog-to-digital converter operating at mm-wave frequencies in any semiconductor technology. The 40-GHz continuous-time ∆Σ ADC centered at 2 GHz achieves 59.8 dB of SNR over 60 MHz of signal bandwidth. The integration of the ADC with a 40-GHz PLL results in the world’s
first direct sampling mm-wave receiver. A comparison of measured receiver performance when external and on-chip clock source is employed shows no significant degradation for SNR of 60 dB. Furthermore, experimental results on a tunable digital receiver centered at 5 GHz and clocked at 40 GHz prove that the resolution of a continuous-time bandpass ΔΣ modulator is a strong function of the filter quality factor.
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<th>Description</th>
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<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic gain control</td>
</tr>
<tr>
<td>BER</td>
<td>Bit-Error Rate</td>
</tr>
<tr>
<td>B</td>
<td>Number of bits</td>
</tr>
<tr>
<td>BiCMOS</td>
<td>Bipolar complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>BPF</td>
<td>Bandpass filter</td>
</tr>
<tr>
<td>CDMA</td>
<td>Code division multiple access</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock</td>
</tr>
<tr>
<td>CML</td>
<td>Current-mode logic</td>
</tr>
<tr>
<td>CP</td>
<td>Charge pump</td>
</tr>
<tr>
<td>∆ΣM</td>
<td>∆Σ modulator</td>
</tr>
<tr>
<td>DCA</td>
<td>Data communication analyzer</td>
</tr>
<tr>
<td>DFF</td>
<td>D-type flip-flop</td>
</tr>
<tr>
<td>EF</td>
<td>Emitter follower</td>
</tr>
<tr>
<td>F</td>
<td>Noise factor</td>
</tr>
<tr>
<td>$F_{MIN}$</td>
<td>Minimum noise factor</td>
</tr>
<tr>
<td>$f_T$</td>
<td>Unity gain frequency</td>
</tr>
<tr>
<td>$f_{MAX}$</td>
<td>Maximum oscillation frequency</td>
</tr>
<tr>
<td>FoM</td>
<td>Figure of merit</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction bipolar transistor</td>
</tr>
<tr>
<td>ITRS</td>
<td>International technology roadmap for semiconductors</td>
</tr>
<tr>
<td>LNA</td>
<td>Low noise amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local oscillator</td>
</tr>
<tr>
<td>LPF</td>
<td>Lowpass filter</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
</tr>
<tr>
<td>--------------</td>
<td>------------</td>
</tr>
<tr>
<td>NF</td>
<td>Noise figure</td>
</tr>
<tr>
<td>NF&lt;sub&gt;50&lt;/sub&gt;</td>
<td>Noise figure in 50Ω</td>
</tr>
<tr>
<td>NF&lt;sub&gt;MIN&lt;/sub&gt;</td>
<td>Minimum noise figure</td>
</tr>
<tr>
<td>nMOSFET</td>
<td>n-channel metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>NRZ</td>
<td>Non-return to zero</td>
</tr>
<tr>
<td>P&lt;sub&gt;1dB&lt;/sub&gt;</td>
<td>1-dB compression point of power gain</td>
</tr>
<tr>
<td>PFD</td>
<td>Phase frequency detector</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-locked loop</td>
</tr>
<tr>
<td>pMOSFET</td>
<td>p-channel metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>PRBS</td>
<td>Pseudo-random binary sequence</td>
</tr>
<tr>
<td>PSA</td>
<td>Power spectrum analyzer</td>
</tr>
<tr>
<td>PSG</td>
<td>Power signal generator</td>
</tr>
<tr>
<td>Q</td>
<td>Quality factor</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RZ</td>
<td>Return to zero</td>
</tr>
<tr>
<td>SAW</td>
<td>Surface-Acoustic Wave</td>
</tr>
<tr>
<td>SDR</td>
<td>Software defined radio</td>
</tr>
<tr>
<td>SERDES</td>
<td>Serializer-Deserializer</td>
</tr>
<tr>
<td>SF</td>
<td>Source follower</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-free dynamic range</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon germanium</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-noise and distortion ratio</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
</tr>
<tr>
<td>SRF</td>
<td>Self resonant frequency</td>
</tr>
<tr>
<td>TIA</td>
<td>Transimpedance amplifier</td>
</tr>
<tr>
<td>V&lt;sub&gt;T&lt;/sub&gt;</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-controlled oscillator</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector network analyzer</td>
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</table>
Chapter 1

Introduction

1.1 Background and Motivation

The evolution of IC technology and the need for high data rates supporting voice, video and data applications has created a plethora of wireless standards. To meet all requirements for wireless connectivity the entire frequency band from a few MHz up to about 6 GHz has been allocated. The need for a versatile radio being able to process any signal in this range has increased in the last decade, as applications require larger bandwidths and wireless handsets must assume a larger role than that of just a voice terminal. A modern cellular phone must be able to process low bandwidth signals (voice), while having the capability to connect to the Internet via wireless access points and handle high bandwidth video applications, such as high-definition TV.

To handle the different requirements for signal bandwidths and data rates of each application, regulating organizations (ITU, IEEE, ETSI, 3GPP) have published specifications in the form of protocols, that any commercially available chip must satisfy. These regulations describe the main characteristics of the wireless link, e.g. frequency allocation, channel bandwidth, receiver sensitivity, maximum transmit power and bit-error rate (BER). Due to existence of numerous frequency bands, these specifications are difficult to meet on the same chip and, as a result, the circuits cannot satisfy all standards. Moreover, the coexistence of these bands in close proximity creates interference that must be dealt with inside the receiver. The common approach to this problem is to reduce each receive path to a single radio channel and apply highly selective filtering. As a consequence, the entire band of each standard cannot be covered by one chip. One could argue that many parallel transceivers integrated in the same package would ad-
address this problem. Indeed, cellular basestations are developed as a parallel combination of individual receivers. This solution, however, increases the cost and complexity of the system. A flexible receiver should consist of as few analog components as possible, while capitalizing on high-speed digital signal processing for filtering and channel selection. To understand why a traditional receiver lacks flexibility, one can investigate the existing topologies from a system level point of view.

The dominant architecture in RF engineering has been for many decades the superheterodyne receiver of Fig. 1.1(a). This topology consists of at least two downconversion stages with analog mixers. The RF signal is filtered by the duplexer and then amplified by the low-noise amplifier (LNA). Selectivity is ensured by external bandpass filters (BPF) with sharp roll-off, such as the Surface Acoustic Wave (SAW) filters. The role of each mixer is to downconvert the signal of interest by multiplying the RF and local oscillator (LO) frequencies. The signal at the mixer output appears at a lower frequency, where analog and digital processing is easier to perform. In the last stage, the signal is located in baseband. The analog-to-digital converter (ADC) then converts this analog signal to its digital equivalent. External filtering can provide much higher Q than on-chip filters, thus attenuating interfering signals, which are located near the band of interest and degrade the quality of the wireless link. Although superheterodyne receivers are well understood and have proved successful in numerous products, they suffer from two main disadvantages. First, the selectivity of the receiver relies on external filters, thus making integration difficult. Second, the two mixing stages have the inherent problem of image signals, which requires extra image reject filters. The number of image signals aliasing in the signal band is directly proportional to the frequency translation steps in the receiver.

To alleviate the problem of image rejection, one of the downconversion stages can be removed. If the frequency of the voltage-controlled oscillator (VCO) is the same as that of the incoming RF signal, then the signal is downconverted to DC, thus having no images present in band. The zero-IF receiver of Fig. 1.1(b) was developed as an implementation of this concept. The LO signal is divided into two parts being 90° out of phase. This allows for selection of the RF signal above or below the LO frequency. The proposed topology of Fig. 1.1(b) has fewer blocks than the superheterodyne receiver, but this flexibility comes at a price. The main drawbacks are the $1/f$ noise of the frequency synthesizer, which is directly translated into the signal band, the DC offsets that are particularly detrimental for low bandwidth signals such as GSM with 200 kHz channel bandwidth and the LO-RF leakage caused by inadequate filtering before the mixer. A
compromise between cost and performance is achieved with the low-IF topology that employs a frequency near DC. This topology still employs fewer components than the superheterodyne receiver, but requires a filter with sharp roll-off to attenuate the image signals.

1.2 Direct Sampling Receivers for Radio Systems

The maximum flexibility and lowest cost for a receiver can be realized if the analog filters and mixer stages following the LNA are removed altogether. In the scenario described in Fig. 1.1(c), the ADC is placed after the antenna and directly samples the RF signal. Such a concept was described in [1] in a software-defined radio (SDR) receiver comprising of just an antenna, a circulator as duplexer and an ADC. The ADC will replace all the analog processing by converting the RF signals to baseband digital data that will then be processed by the digital channelizer and demodulator. It should be noted that the ADC must have sufficient dynamic range and handle both low and high power signals, in the absence of any narrowband filtering. This remains one of the most demanding tests that radio receivers are subjected to and proves the ability of a circuit to operate in the presence of large interfering signals (also called blockers) near the band of interest. The
major drawback of a direct sampling receiver is the high power dissipation associated to digital signal processing at higher frequencies compared to Figs. 1.1(a) and 1.1(b).

From the previous discussion, it is clear that to avoid aliasing, the analog signal is sampled by an ADC clocked at a speed that is at least twice its maximum input bandwidth. However, this is not always necessary according to the Nyquist sampling theorem, which states that the sampling rate must be higher than twice the sampled bandwidth.

\[ F_S > 2 \times BW \]  

This means that the ADC can sample the analog signal at a rate lower than the RF frequency. In bandpass sampling or subsampling, the sampling rate is lower than the maximum frequency of the signal, but higher than twice its bandwidth. To prevent aliasing from distorting the signal, the band of interest must fall in one of the bandpass aliasing zones

\[ \left( f_0 - \frac{BW}{2}, f_0 + \frac{BW}{2} \right) \in \left( (n-1)\frac{F_S}{2}, n\frac{F_S}{2} \right) \text{ or } \left( n\frac{F_S}{2}, (n+1)\frac{F_S}{2} \right), n \in \mathbb{Z}. \]  

Figure 1.2 illustrates the spectrum of the signal before and after sampling. The signal of interest is located in a Nyquist zone, whose frequency is much higher than the sampling rate. After sampling, the signal appears at the first Nyquist zone. The first SDR receiver of this type was demonstrated in [2] for a dual GPS (Global Positioning System) and GLONASS (GLObal NAvigation Satellite System) satellite receiver. These two were the only operational radio-based satellite navigation systems at the time of [2]. Proper selection of the sampling rate allowed for simultaneous reception of both bands. Two major drawbacks limit the applicability of this technique. First, the ADC front end must have a bandwidth higher than the maximum input frequency at the sampling point, which is not always possible if the ADC sampling rate is a few hundred MS/s. Second, not only does the ADC subsample the RF signal, it also downconverts the noise from all Nyquist bands down to DC. Therefore, this technique can only work in systems with relaxed specifications for dynamic range and noise, such as GPS receivers.

To be able to perform RF sampling and handle the adjacent interference to the channel of interest with sufficient attenuation, one can combine analog decimation and
1.2. Direct Sampling Receivers for Radio Systems

Figure 1.2: Spectrum before and after subsampling. The signal of interest is located between the Nyquist zones \( nf_s/2 \) and \((n+1)f_s/2\) to avoid aliasing.

filtering after the mixing stage (Fig. 1.3). In a number of recent publications, it has been demonstrated that RF sampling can be merged with built-in anti-aliasing and analog decimation to provide a means of filtering after the mixing stage and to lower the signal frequency before the ADC. Various groups have reported receivers that operate with windowed integration, either immediately after the sampling switch [3, 4], or after the mixing stage [5, 6]. All the above topologies are based on a finite impulse response (FIR) filter, having a \textit{sinc} transfer function

\[
|H(f)| = C\left|\frac{\sin(\pi f / F_s)}{\pi f / F_s}\right|,
\]

where \( f \) is the input signal frequency, \( F_s \) is the rate of the sampler and \( C \) is a gain constant. The analog decimation with built-in anti-aliasing uses the nulls of the FIR filter to attenuate any adjacent channels and interference. With a proper combination of filtering, all interference can be removed such that the ADC does not saturate. Moreover, the nulls can be tuned by changing the sampling frequency \( F_s \), resulting in a flexible receiver across many frequency bands. The authors of [6] claim functionality for any standard from GSM (\( BW_{\text{channel}} = 200kHz \)) to 5.8 GHz 802.11 (\( BW_{\text{channel}} = 20MHz \)).

All the previously mentioned schemes [3, 4, 6, 7] rely on a mixer to relax the requirements on the ADC and tunable filters to adjust to any signal bandwidth. Despite their flexibility, these designs cannot handle more than one receive channel. If the bandwidth of the FIR \textit{sinc} filter is increased, adjacent channel interferers will overload the ADC. Most importantly of all, all the previously mentioned efforts can be seen as zero-IF receivers with tunable analog baseband filtering [8] and wideband digitally controlled VCOs to
cover all the bands. But the problem has shifted from improving the ADC, as in Fig. 1.1(c), to performing extra analog filtering to be able to accommodate today’s ADCs. The question is how much the ADC can improve in order to process the entire receive bandwidth and realize a true SDR.

1.3 Continuous-Time $\Delta\Sigma$ ADCs

As advances in silicon technologies have led to transistors having $f_T$ and $f_{MAX}$ in excess of 150 GHz, it becomes feasible to directly digitize the RF carrier, as in Fig. 1.1(c). If more than one receiver channel can be digitized simultaneously, the direct sampling receiver will have the flexibility to process the entire system bandwidth in the digital domain, while replacing most of the analog circuitry used for downconversion and filtering. Channel selection can be performed by digital filters, which are relatively easy to implement in sub-100 nm technologies. This topology achieves direct digitization without using subsampling mixing [3, 4], which is known to increase the receiver noise figure (NF) [9], and without analog downconversion [5]. In comparison to Fig. 1.1(c), the receivers of [3, 4], and [5] support only a single radio channel.

Since the power supply voltage follows the ever-decreasing breakdown voltage of transistors in advanced technology nodes, one must take advantage of the faster response of transistors and compensate for the reduced signal amplitude by exploiting timing information. $\Delta\Sigma$ modulators ($\Delta\Sigma$M) are an attractive solution for direct sampling receivers, because they trade-off resolution in amplitude for resolution in time, while having high resolution, low power and low complexity compared to other ADC types. They can
potentially replace the analog blocks (except the VCO/PLL generating the LO signal in Fig. 1.1) of a wireless receiver, including the LNA, and directly digitize the RF signal. Although, flash ADCs can also operate at GS/s rates, they cannot provide the required resolution at twice the Nyquist rate for a radio signal. For example, a direct sampling flash ADC would need more than 12 bits of resolution at 4 GS/s sampling rate, which is not realistic with state-of-the-art semiconductor technology. Other architectures (pipelined, subranging, successive approximation) cannot operate in the GHz range with today’s semiconductor technology due to their complexity. The state-of-the-art pipelined ADC of [10] in a silicon bipolar technology is limited to a rate of 125 MS/s while dissipating 1.8 W. Despite achieving more than 74 dB of SNR over the 62.5 MHz Nyquist bandwidth, the power dissipation of the ADC, if designed for GHz rate would be prohibitive.

A representation of the $\Delta\Sigma$ topology is illustrated in Fig. 1.4. It consists of a filter (lowpass or bandpass), quantizer and feedback DAC. The filter attenuates all signals outside the band of interest, while simultaneously shaping the quantization noise. The quantizer converts the analog input to a digital output. The DAC is employed as the feedback element inside the ADC. The $\Delta\Sigma$ analog-to-digital conversion is based on the use of feedback to minimize in-band quantization noise. In Fig. 1.4, the input signal is sampled by the quantizer at a rate $F_S$. The digitized output is then fed back and subtracted from the input. This results in two different transfer functions for the input and quantization noise signals. For the purpose of demonstrating the $\Delta\Sigma$M operation, one can assume that the quantizer does not affect the dynamics of the loop. The behaviour of the ADC when the quantizer is considered in the design will be presented in chapter 2 in more detail. For a filter transfer function $H(z)$, the signal transfer function for unity
feedback is

$$STF(z) = \frac{H(z)}{1 + H(z)} \approx 1$$  \hspace{1cm} (1.4)

assuming that the filter gain is larger than one. To understand what happens to quantization noise, one can model the quantizer as a linear block that adds some error $e(n)$ to the analog input. The output of the quantizer can be approximated as the sum of the error $e(n)$ due to finite quantization and the signal that is converted to digital. The power of $e(n)$ is proportional to the quantizer step size $\Delta$. Multi-bit quantizers have less quantization noise at the expense of extra complexity in the design. The relationship between quantization noise power $P_{QN}$ and quantizer step $\Delta$ is [11]

$$P_{QN} = \frac{\Delta^2}{12}.$$  \hspace{1cm} (1.5)

Equation (1.5) has a flat power spectral density from DC to $F_S/2$ equal to

$$S_{QN} = \frac{\Delta^2}{12F_S}.$$  \hspace{1cm} (1.6)

If this noise power is removed from the signal band and somehow moved to higher frequencies, then the resolution of the ADC can improve significantly. This is made possible through the application of feedback. Using the linear model approximation of the quantizer, the noise transfer function $NTF(z)$ can be found. By setting the input signal to zero, it can be easily shown that quantization noise is filtered by

$$NTF(z) = \frac{1}{1 + H(z)} \approx \frac{1}{H(z)}.$$  \hspace{1cm} (1.7)

Equation (1.7) means that quantization noise effectively sees a bandstop transfer function with the notch being at the filter resonance (Fig. 1.5). The total quantization noise over the signal bandwidth is

$$P_{QN, total} = \int_{f_o - \frac{BW}{2}}^{f_o + \frac{BW}{2}} S_{QN}(f) |NTF(f)|^2 df = \frac{\Delta^2}{12F_S} \int_{f_o - \frac{BW}{2}}^{f_o + \frac{BW}{2}} |NTF(f)|^2 df.$$  \hspace{1cm} (1.8)

It should be noted that quantization noise in the $\Delta \Sigma M$ is not canceled, but moved to frequencies outside the useful signal band. Also, thermal noise is not shaped by the
loop because it appears at the input of the ΔΣM. The major advantage of the topology is the ability to have an arbitrarily high resolution with even a single-bit quantizer, but not better than the limits set by circuit noise. This ability is particularly useful in deep submicron circuit design where power supplies scale to lower levels. It is also the main reason why the ΔΣM have been very popular in CMOS circuits which operate traditionally from lower power supplies than bipolar implementations.

In general, the resolution of the ADC is a function of its order (higher order filters produce deeper notches in the bandstop response of Fig. 1.5), the number of physical bits in the quantizer (more bits means smaller quantization step) and the OSR ratio. All these dependencies are summarized in the following expression, which gives the maximum achievable SNR for any ΔΣ ADC with ideal filters and loop components [12]

\[
SNR_{\text{max}} = \frac{3\pi}{2} (2^{B_q - 1})^2 (2n + 1) \left( \frac{OSR}{\pi} \right)^{2n+1}
\]

(1.9)

where \(B_q\) the number of physical bits in the quantizer, \(n\) the order of the loop filter and \(OSR\) the oversampling ratio defined as

\[
OSR = \frac{F_S}{2 \times BW}.
\]

(1.10)

For a second order ΔΣ loop with a single-bit quantizer, (1.9) predicts an SNR increase by 15 dB for each octave of OSR.
The ∆ΣM can be either discrete-time or continuous-time depending on the type of filter used. The former circuits are built with switched capacitor filters, while the latter are realized with analog filters. Compared to its discrete-time counterpart, the continuous-time architecture is more suitable for high sampling rates. In a discrete-time ∆ΣM, the opamps forming the switched capacitor filter must operate at the clock speed, which puts limitations in the maximum frequency that the discrete-time ADC can operate at. Designers tend to prefer discrete-time implementations for low frequency applications and continuous-time loops when the sampling rate exceeds a few MHz. In the direct sampling receiver, the continuous-time ADC is more suitable since the signal frequency is in the GHz range. Since we are not interested for any signals outside the radio bands, a bandpass topology is the appropriate choice.

1.4 State-of-the-art

The benefits of continuous-time bandpass ∆Σ ADCs were recognized early on by RF designers. Table 1.1 summarizes all the circuits that have been recently published in literature in the area of GHz ∆Σ ADCs. It does not include circuits clocked below 1 GHz, because they require a mixer to perform the frequency translation. The table comprises data on center frequency $f_O$, sampling rate $F_S$, bandwidth $BW$, signal-to-noise ratio (SNR), power and figure-of-merit (FoM). To FoM is calculated on the combination of SNR and BW that result in the best performance using the International Technology Roadmap for Semiconductors (ITRS) definition on ADCs [13,14]

$$FoM = \frac{2^B \times 2BW}{P},$$

(1.11)

where the number of bits (B) equals

$$B = \frac{SNR - 1.76}{6.02}.$$  

(1.12)

Most of the bandpass designs in Table 1.1 employ a 1:4 ratio between the center and sampling frequencies. This makes the digital downconversion easier since the output bit stream is multiplied by $+1, 0, -1, 0, \ldots$ [15]. Although this approach simplifies post-processing of the data, it limits performance because of the small OSR. If the center frequency is set to 2 GHz with the system bandwidth being 60 MHz, the sampling rate
of 8 GHz results in an OSR of 67. To sample the entire system bandwidth with high OSR, the clock rate should be larger than four times the center frequency.

Another common characteristic in these designs is the order of the modulator. Almost all references are based on fourth order bandpass filters, with the reason simply being the complexity and size of higher order filters when realized on chip. Continuous-time bandpass $\Delta \Sigma$ ADCs centered between 0.8 to 1 GHz were reported in the 1990’s, but insufficient transistor speed resulted in inadequate circuit performance [16–18]. Historically, the authors of [17] were among the first ones to show a functional ADC in these frequencies. They use a bandpass LC filter with tunable $Q$ and two feedback DACs with modified RZ pulse shape. A similar feedback topology can be also found in [19], implemented in a faster III-V technology. The quantizer has three bits, whereas the $G_m$-LC filter is tuned at 1.3 GHz. In [18], the authors opt for an architecture with a single DAC and a feedforward path inside the 0.8-GHz bandpass loop. Reference [20] describes a topology with $G_m$-C biquad filters and a transconductor designed for extra linearity. The authors also provide a comparison of feedforward and feedback modulator topologies with respect to linearity. What is different in [21] compared to the previous designs, is the combination of a standard DAC and an integrator to realize the feedback. Despite being lowpass types, the designs of [22] and [23] were the first to use a sampling rate above 4 GHz. Their FoM is better than the bandpass ADCs, since their filters do not have to be tuned to high frequencies. In addition to all the semiconductor ADCs, GHz-sampling $\Delta \Sigma$M have been reported in superconductive technologies, as well. A bandpass $\Delta \Sigma$M clocked at 42.6 GHz has been demonstrated in [24] and was implemented in a Nb technology with Josephson junctions, being the fastest $\Delta \Sigma$M to date.

1.5 Thesis Objectives and Outline

This thesis describes the analysis, design and implementation of a direct digitizer for RF systems realized as a continuous-time bandpass $\Delta \Sigma$ ADC in SiGe BiCMOS. The target application is basestation receivers that process a large number of channels simultaneously. Unlike all previous $\Delta \Sigma$ ADCs, the proposed architecture in this thesis incorporates the LNA in its main path, as the input stage of the loop filter and the PLL as an on-chip clock source. Compared to other bandpass ADC designs with GHz clocks [16–20] and operating from 3.3 V or higher supplies, this work employs a new, highly linear and low-noise MOS-HBT cascode filter topology, which is powered from a
<table>
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<th>Ref/Year</th>
<th>Technology</th>
<th>Type</th>
<th>$f_o$ (GHz)</th>
<th>$F_S$ (GHz)</th>
<th>BW (MHz)</th>
<th>SNR (dB)</th>
<th>Power (W)</th>
<th>FoM (GHz/W)</th>
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<tr>
<td>[17] 1998</td>
<td>50-GHz SiGe HBT</td>
<td>BP</td>
<td>0.8</td>
<td>3.2</td>
<td>25</td>
<td>41</td>
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<tr>
<td>[18] 1997</td>
<td>40-GHz GaAs</td>
<td>BP</td>
<td>1</td>
<td>4</td>
<td>60</td>
<td>47.4</td>
<td>3.2</td>
<td>7.18</td>
</tr>
<tr>
<td>[20] 2004</td>
<td>130-GHz InP</td>
<td>BP</td>
<td>1</td>
<td>4</td>
<td>4</td>
<td>53</td>
<td>0.35</td>
<td>8.34</td>
</tr>
<tr>
<td>[21] 2007</td>
<td>47-GHz SiGe BiCMOS</td>
<td>BP</td>
<td>0.95</td>
<td>3.8</td>
<td>1</td>
<td>59</td>
<td>0.075</td>
<td>19.4</td>
</tr>
<tr>
<td>[22] 2006</td>
<td>200-GHz SiGe HBT</td>
<td>LP</td>
<td>-</td>
<td>20</td>
<td>312.5</td>
<td>30.5</td>
<td>0.49</td>
<td>34.9</td>
</tr>
<tr>
<td>[25] 2006</td>
<td>130-GHz InP</td>
<td>BP</td>
<td>1.4</td>
<td>4</td>
<td>180</td>
<td>40.2</td>
<td>7.7</td>
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<td>[23] 2003</td>
<td>205-GHz InP</td>
<td>LP</td>
<td>-</td>
<td>8</td>
<td>62.5</td>
<td>57.4</td>
<td>1.8</td>
<td>42.1</td>
</tr>
<tr>
<td>[26] 2003</td>
<td>150-GHz InP HBT</td>
<td>BP</td>
<td>0.1</td>
<td>2.5</td>
<td>12.5</td>
<td>84.2</td>
<td>6</td>
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</table>

Table 1.1: Comparison of state-of-the-art $\Delta\Sigma$ ADCs
2.5-V supply. The 40-GHz clock frequency in the present thesis is two times larger than in any previously reported semiconductor ΔΣ ADCs, marking the first use of mm-wave clocks in silicon ΔΣM. The system level design methodology developed for bandpass ΔΣ ADCs is demonstrated for two center frequencies, 2 GHz and 5.2 GHz corresponding to CDMA and WLAN standards, respectively. The 5.2-GHz frequency can also be the IF of a 60-GHz radio system. To investigate low power alternatives for mm-wave analog-to-digital conversion, the quantizer and low-noise broadband clock distribution amplifiers were also designed, fabricated and tested in 90-nm and 65-nm CMOS. The comparison of these building blocks in SiGe BiCMOS and CMOS platforms allows for the analysis of tradeoffs between these advanced technologies.

The thesis is organized as follows. Chapter 2 presents the new system level design methodology of the loop in s-domain and sets the link between resolution (SNR) and center frequency in continuous-time bandpass ΔΣ ADCs. Circuit design of all building blocks used in this work is discussed in chapter 3, where the filter, feedback DACs, quantizer and clock distribution network are analyzed in depth. At the core of all SiGe BiCMOS circuits is the MOS-HBT cascode topology, which provides the best combination of noise figure and linearity, and the best frequency response in both the analog and digital parts of the chip. A comparison between SiGe BiCMOS and CMOS implementations is conducted in chapter 4 based on simulated and measured performance. Finally, measurement results of the entire ADC are summarized in chapter 5 along with a comparison to state-of-the-art GHz-sampling ΔΣ ADCs. Two ADC versions were developed in SiGe BiCMOS in the course of this work. One is clocked by an external clock and the other has an on-chip 40-GHz VCO/PLL. The measured performance of two digital receivers centered at 2 GHz and 5 GHz, while employing the same 40-GHz clock, is presented in chapter 5. The contributions of this thesis and suggestions for future work are summarized in chapter 6.
Chapter 2

System Level Design of Continuous-Time $\Delta\Sigma$ ADCs

This chapter presents the design methodology for high-speed $\Delta\Sigma$ ADCs employed in direct sampling receivers. First, the requirements of the ADC are discussed in the case of the ADC sampling a 2-GHz RF signal. The order, OSR, SNR and clock jitter specifications of the modulator are derived from analytical expressions and simulations. The second part of this chapter presents a new design methodology for continuous-time bandpass $\Delta\Sigma$ ADCs. A linear approximation of the quantizer and DAC is used to design the fourth order modulator and derive the gain coefficients in the forward and feedback components of the loop.

2.1 System Level Design Considerations for Direct Sampling ADC

2.1.1 Signal-to-Noise Ratio Requirements

To be able to replace all analog downconversion stages by the combination of the LNA and ADC of Fig. 1.1, the digital receiver must meet all the specifications of the wireless standard. As stated in the previous chapter, the most demanding test case of a receiver remains the operation in the presence of adjacent channel interference. The direct sampling receiver, and eventually a software-defined radio, must handle both low and high power signals of different types. The blocking signal can be a continuous-wave tone leaking from the PA of the same chip or a modulated signal from another cellular
standard. The desensitization scenario is graphically reproduced in Fig. 2.1, where a single-tone falls near a channel. To understand what happens in reality, we will assume the specifications for the CDMA system IS-95, currently in use in North America. The entire receive system bandwidth is 60 MHz ranging from 1850 to 1910 MHz. The SNR of the CDMA signal with 1.23 MHz of bandwidth must be at least $E_b/N_0 = 6.7 dB$ for a frame error rate less than 1% with 95% confidence. As in any spread spectrum system, the baseband voice/data information is coded into a signal occupying more bandwidth than the original signal. This ensures immunity against interference from other users and allows for the reuse of frequencies in one cell. In the case of IS-95 the data rate is 9.6 $kb/s$, which is coded by the pseudo random sequence to the chip rate of $1.2288 M b/s$. The processing gain (PG) or decoding gain is defined as the ratio of the chip to data rate

$$PG = 10 \log_{10} \frac{1.2288 M b/s}{9.6 k b/s} = 21 dB.$$ \hfill (2.1)

A single channel must have a receive sensitivity of -119 dBm at the antenna input bringing the signal at 5.8 dB below the thermal noise floor, typical for a spread spectrum system ($-119 dBm - 10 \log_{10} 60 MHz = -179.9 dBm/Hz$). The total NF of the receiver can then be found.
To calculate the ADC requirements in a direct sampling system, one can follow a similar approach to the analysis of [27]. In the basestation receiver section, the standard sets the maximum power level of the interference to be $\Delta P = 80\text{dB}$ above the minimum value of the signal. The blocking tone is located 1.25 MHz offset from the CDMA signal. Assuming an LNA gain of $G_{LNA} = 25\text{dB}$, one can find the blocker power at the ADC input

\[
P_{bl} = S_r + \Delta P + G_{LNA} + A_{P-A} = -5\text{dBm}
\]

where $A_{P-A}$ the peak-to-average ratio. This term describes the difference between the peak and average power levels of a signal. The value of $A_{P-A}$ can be 3 dB for sinusoidal signals ($10\log_{10}2 = 3\text{dB}$) or 9 dB for spread spectrum signals. We will use the latter for these calculations. The full-scale power level of the ADC depends on the voltage levels of the logic family. It is feasible to use a MOS-HBT CML logic in 0.13-\text{$\mu$m} SiGe BiCMOS technology [28] with 0.4 V single-ended peak-to-peak amplitude, as will be shown in chapter 3. The full scale power of the ADC for $V_{FS} = 0.4V$ will then become

\[
P_{FS} = \frac{V_{FS}^2}{2 \times 50\Omega} = 2\text{dBm}
\]

The ADC will not saturate as long as the LNA does not amplify the blocker near the ADC full-scale power. From (2.3), (2.4) and allowing for 6 dB headroom,

\[
P_{bl} = -5\text{dBm} \leq P_{FS} = -4\text{dBm}.
\]

To estimate what kind of dynamic range we need for the ADC, let’s assume that the resolution is $N$ bits. The quantization noise power $P_{QN}$ of the ADC can be calculated from its SNR.
\[ SNR = \frac{P_{FS}}{P_{QN}} \]

\[ SNR = 6.02 \times N + 1.76 \quad (2.6) \]

From (2.4) and (2.6), we have

\[ P_{QN} = P_{FS} - (6.02 \times N + 1.76) \quad (2.7) \]

or equivalently the quantization noise density is

\[ P_{QN,d} = P_{FS} - (6.02 \times N + 1.76) - 10 \log_{10}(BW). \quad (2.8) \]

This amount of power must be at least equal to the thermal noise at the ADC input

\[ P_{TN,d} = -174 dBm/Hz + G_{LNA}. \quad (2.9) \]

We define \( \Delta N \) as the difference between quantization and thermal noise densities at the ADC input.

\[ \Delta N = P_{TN,d} - P_{QN,d} \quad (2.10) \]

From (2.8), (2.9) and (2.10) we can solve for the required effective number of bits \( N \)

\[ N = \frac{P_{FS} - 10 \log_{10}(BW) - 1.76 + 174 - G_{LNA} + \Delta N}{6.02}. \quad (2.11) \]

Assuming \( P_{FS} = -4 dBm \), \( BW = 60 MHz \) and \( G_{LNA} = 25 dB \), the last equation estimates that \( N \) equals 10.9 bits for \( \Delta N = 0 dB \). If we design the receiver for \( \Delta N = 6 dB \), then the effective number of bits must be 11.9. The system level technique to find the number of bits that are necessary in a direct sampling system is not limited to a single standard only. Once the specifications of the system in use are known, one can apply this approach and find the ADC requirements.
2.1.2 Selecting the Oversampling Ratio and Clock Frequency of ADC

After finding the ADC resolution required for direct sampling, one must select the oversampling ratio (or clock frequency), number of quantizer bits, filter order and topology of the ΔΣ modulator. As discussed in chapter 1, the SNR is a function of all the above parameters [12] as summarized in (1.9) and repeated below

\[
SNR_{\text{max}} = \frac{3\pi}{2} (2^B - 1)^2 (2n + 1) \left(\frac{OSR}{\pi}\right)^{2n+1}
\]  

(2.12)

To improve SNR, one has three parameters to optimize: number of bits \( B \), filter order \( n \) and oversampling ratio \( OSR \). Increasing the physical bits will likely result in the noise floor being limited by the distortion of the DAC, especially at GHz-rates. A single-bit quantizer is the safest way to get the best linearity of the modulator. The modulator order and OSR are usually traded-off against each other by designers such that higher order modulators would need lower OSR. A higher filter order would attenuate quantization noise by a larger amount and the clock frequency could be reduced. Figure 2.2 illustrates the dependence of SNR on OSR for three filter orders. To achieve sufficient SNR either a second or third order loop is required. Due to the difficulty in implementing a stable third order ΔΣM at 2 GHz, a second order loop seems to be a sensible decision. It is clear at this point that the only remaining parameter to improve SNR is OSR, or equivalently the clock rate, since the bandwidth is fixed by the application.

So far in the analysis, the sampling clock jitter has not been taken into consideration in the design. In reality, jitter can be the limiting factor in high-speed ADCs and can set the in-band noise floor. To predict the loop behavior in the presence of clock jitter, one can use the expression that links SNR and clock jitter [15, 29]

\[
SNR = 20 \log_{10} \sqrt{\frac{OSR}{2\pi f_o \sigma_i^2}},
\]

(2.13)

where \( f_o = 2\text{GHz} \) is the center frequency and \( \sigma_i^2 \) is the jitter variance. The SNR as a function of jitter is plotted in Fig. 2.3 for 10, 20 and 40 GHz sampling rates. So long as a low phase noise clock source (VCO/PLL) is available in the technology, a large \( OSR \) helps to reduce the contribution of clock jitter in the band. For the direct sampling ΔΣ ADC, we select the clock at 40 GHz in order to get the maximum performance from the system. It should be noted that (2.13) is only applicable for single-bit quantizers. A
Figure 2.2: SNR of an ideal ∆Σ modulator as a function of oversampling ratio for second \((n = 1)\), fourth \((n = 2)\) and sixth \((n = 3)\) order loop filter.

multi-bit modulator would be less sensitive to clock jitter because the quantization steps are smaller.

## 2.2 Continuous-Time ∆Σ ADC Modelling

The ∆ΣM concept was initially introduced with continuous-time filters in the 1960s. Although digital filters are still derived by transforming the transfer functions of their continuous-time counterparts (e.g. Butterworth, Chebyshev, elliptic), the discrete-time loop design in ∆Σ ADCs has gained more ground. The reason behind this trend can be attributed to the relative simplicity of describing the loop using \(z\)-domain transfer functions and the popularity of switched capacitor ADCs for audio applications in the early days of ∆Σ design. In continuous-time ∆ΣM, the closed loop stability is traditionally analyzed in the \(z\)-domain. The coexistence of analog (loop filter) and digital (quantizer, DACs) components makes the design of such a circuit cumbersome in the \(s\)-domain. The quantizer and DACs in a ∆ΣM are inherently digital blocks and their behavior can be analyzed in discrete-time.

Typically, the design process starts from a discrete-time transfer function that satisfies the requirements in OSR, SNR and SFDR. The loop filter is then transformed to its equivalent in the Laplace domain. With the use of [30], one can find the normalized \(H(z)\) that meets the above requirements. For 2-GHz center frequency, 40-GHz clock frequency and 60 MHz bandwidth, the resulting loop filter transfer function from [30] is
2.2. Continuous-Time ΔΣ ADC Modelling

The continuous-time transfer function can then be found using a filter conversion method. The conversion can be made with one of zero-order hold, bilinear (also known as Tustin transform [31]) and impulse invariance methods. The zero-order hold method assumes that the signal remains constant over the sampling period. The bilinear or Tustin method employs a $z$-to-$s$ frequency transformation, by simply using the approximation

$$z = e^{sT_S} \approx \frac{1}{1 - sT_S/2} \approx 2 + \frac{sT_S}{2 - sT_S}$$

(2.15)

where $T_S$ is the sampling period. The impulse invariant method tries to find the equivalent transfer function by setting equal the impulse responses in the two domains, as in Fig. 2.4. Mathematically, this can be expressed as

$$\mathcal{Z}^{-1}\{H(z)\} = \mathcal{L}^{-1}\{D(s)H(s)\}_{t=nT_S}$$

(2.16)

where $D(s)$ the DAC transfer function. Equation (2.16) states that the discrete-time and continuous-time modulators are equivalent if the inputs of both quantizers are the same when sampled every $T_S$. To find the $s$-domain loop filter, $H(z)$ is usually decomposed into partial fraction expansion and each term is mapped to a continuous-time transfer function. References [32] and [15] provide tables of common impulse invariant transformations.

Figure 2.3: SNR vs clock jitter for $F_S = 10, 20$ and $40$ GHz and $2$-GHz input signal.
Chapter 2. System Level Design of Continuous-Time $\Delta \Sigma$ ADCs

Figure 2.4: Equivalence between discrete-time and continuous-time $\Delta \Sigma$ loops.

Using one of the previously mentioned methods (bilinear transform), the transfer function of the loop filter can be found as

$$
H(s) = \frac{0.66667(s^2 + 0.5538s + 0.1247)(s^2 + 0.2762s + 0.2675)}{(s^2 + 0.09858)(s^2 + 0.1021)}
$$

(2.17)

By substituting $s = sT_S$, the transfer function is denormalized and can be mapped to a feedback or feedforward filter structure (Fig. 2.5 and 2.6). The individual second order transfer functions are either realized as active-RC filters (Fig. 2.7) or $G_m - C$ biquads (Fig. 2.8). Both structures can implement any type of second order filter response. Equations (2.18) and (2.19) give the transfer functions of the active-RC and $G_m - C$ biquad filter, respectively.

$$
H(s) = \left(\frac{C_1}{C_B}\right) s^2 + \frac{1}{R_2C_B} s + \frac{1}{R_1R_3C_A C_B} s^2 + \frac{1}{R_3C_B} s + \frac{1}{R_1R_3C_A C_B}
$$

(2.18)

$$
H(s) = \left(\frac{C_X}{C_X + C_B}\right) s^2 + \frac{G_m5}{C_X + C_B} s + \frac{G_m4}{C_A(C_X + C_B)} s^2 + \frac{G_m3}{C_X + C_B} s + \frac{G_m2}{C_A(C_X + C_B)}
$$

(2.19)

In the final step of the design, one has to calculate the feedback coefficients by using the technique shown in [15] or [33, 34]. These filter implementations are suitable for low frequency ADCs with sampling frequencies up to a few hundred MHz. Although $G_m$-RC
2.2. Continuous-Time ΔΣ ADC Modelling

Figure 2.5: ADC with feedback loop filter.

Figure 2.6: ADC with feedforward loop filter.

filters have been reported with center frequencies above 1 GHz [35–37] these come with the penalty of higher noise than a $G_m - LC$ filter, while having the same linearity and power consumption.

On the other hand, the $G_m - LC$ filter is the most popular approach when the center frequency is in the GHz range. A $G_m - LC$ filter topology, however, cannot implement the $z$-to-$s$ transformation due to the inherent absence of a lowpass term in the transfer function of the bandpass filter. The transfer function of the filter in Fig. 2.9 is

$$H(s) = \frac{G_m}{C} \frac{s}{s^2 + \omega_o^2} \quad (2.20)$$

with

$$\omega_o = \frac{1}{\sqrt{LC}}. \quad (2.21)$$
Figure 2.7: Second order active-RC filter.

Figure 2.8: Second order $G_m - C$ filter.

Figure 2.9: $G_m - LC$ filter topology.
As analyzed in [15], the z and s domain loop filter transfer functions are not mathematically equivalent. This can be shown with the popular $F_S/4$ modulator. Starting from its lowpass loop filter transfer function

$$H_{LP}(z) = \frac{-2z^{-1} + z^{-2}}{(1 - z^{-1})^2} \quad (2.22)$$

one can find the bandpass representation by substituting $z^{-1}$ with $z^{-2}$

$$H_{BP}(z) = \frac{2z^{-2} + z^{-4}}{(1 + z^{-2})^2}. \quad (2.23)$$

The s-domain transfer function can be found by applying a discrete-to-continuous time transformation

$$H_{BP}(s) = -1.0354s^3 + 1.0652s^2 - 1.3210s + 4.5661 \quad (s^2 + (\pi/2)^2)^2. \quad (2.24)$$

This equation must be mapped to the classical topology with two resonators each having

$$H_i(s) = \frac{G_{mi} s}{C s^2 + \omega_i^2}. \quad (2.25)$$

and feedback coefficients $G_{fb1,2}$. The combined transfer function can be shown to be of the form

$$H(s) = [G_{fb2} + G_{fb1}H_1(s)]H_2(s). \quad (2.26)$$

From (2.26) it is clear that the lowpass term $s^0$ is missing, since all factors are multiplied by the numerator of $H_i(s)$ in (2.20).

Historically, this problem has been addressed in two ways. The first approach [33] uses a numerical optimization algorithm that tries to match the impulse response of the z and s-domain filters. The filter and feedback coefficients are optimized such that the noise transfer function (NTF) satisfies Lee’s criterion [38], which states that

$$\left| NTF(e^{j\omega}) \right| \leq 1.6 \quad (2.27)$$

The algorithm also selects the coefficients that give maximum attenuation outside of the band of interest. To verify that the optimized filter results in the same transfer function, the impulse response of the modulator filter is compared in z and s domains, as in (2.16).
Another approach [32] employs a modified quantizer that has two DACs with different delays (Fig. 2.10). The feedback pulses consist of two return-to-zero (RZ) and half-return-to-zero (HRZ). The latter is generated from the quantizer after half a period $T_S$. The resulting loop filter can be made equivalent to its $z$-domain counterpart, due to the extra degrees of freedom inserted into the system by the two DAC pulses. Despite the elegant solution that satisfies the transfer function equivalence of the loop, this scheme poses circuit implementation difficulties when the clock is in the GHz range. At mmwave sampling speeds, it is difficult to maintain the phase delay between the two parallel DAC pulses. Another drawback of the two pulses is the extra amount of jitter injected into the loop filter, since two DACs are connected to each feedback node instead of one. To benefit from the low-noise and high linearity potential of the $G_m – LC$ topology, while keeping a single feedback DAC pulse, one can address the problem from a different perspective. The next section introduces a new design methodology that circumvents the mathematical nonequivalence by addressing the problem in the $s$-domain.

### 2.3 New Method for Transfer Function Design in $s$-domain

Figure 2.11 shows the system level architecture of the $\Delta \Sigma$ ADC. It is based on a classical feedback topology with two resonators and two feedback paths. The bandpass loop filter consists of two $G_m$-LC stages. A Master-Slave-Master D-type flip-flop with 5 ps
A new method that bypasses the $z$-domain analysis is proposed here. The loop filter is directly designed in the $s$-domain using established analog filter design techniques. Stability is verified by employing a linear approximation of the quantizer. The design procedure begins with the derivation of the loop filter transfer function. The loop filter can be chosen to have a flat response in the passband and its transfer function can be derived either from a lowpass prototype [39], or directly in bandpass mode. The filter is centered at 2 GHz and covers the entire 60 MHz bandwidth of the CDMA system. The transfer function of a $G_m$-LC filter with quality factor $Q$, center frequency $\omega_o$ and gain
constant $A$ is

$$H(s) = \frac{A\omega_0 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}. \quad (2.28)$$

Ideally, the two poles of each resonator should be placed close to the $j\omega$-axis to achieve large suppression of quantization noise. The ADC closed loop transfer function with two resonators and two feedback DACs is described by (2.29), where $G_{m1}, G_{m2}$ are the transconductances of the bandpass filters and $G_{fb1}, G_{fb2}$ are the transconductances of the DACs.

$$G(s) = \frac{H^2(s)D(s)}{1 + \frac{H^2(s)D(s)}{s} \left[ \frac{G_{fb2}C}{G_{m1}G_{m2}} s^2 + \frac{G_{fb1}}{G_{m1}} + \frac{G_{fb2}C\omega_0}{G_{m1}G_{m2}Q} \right] s + \frac{G_{fb2}C\omega_0^2}{G_{m1}G_{m2}}} \quad (2.29)$$

For simplicity it has been assumed that the two stages are tuned to the same center frequency. The transfer function of the filter path is described by

$$H^2(s) = \frac{G_{m1}G_{m2}}{C^2} \frac{s^2}{(s^2 + \frac{\omega_0}{Q} s + \omega_0^2)^2}. \quad (2.30)$$

the RZ DAC transfer function is expressed as

$$D(s) = \frac{1 - e^{-sT_s/2}}{s} \quad (2.31)$$

and the feedback can be modeled with the following transfer function

$$F(s) = \frac{G_{fb2}C}{G_{m1}G_{m2}} s^2 + \left( \frac{G_{fb1}}{G_{m1}} + \frac{G_{fb2}C\omega_0}{G_{m1}G_{m2}Q} \right) s + \frac{G_{fb2}C\omega_0^2}{G_{m1}G_{m2}}. \quad (2.32)$$

The two pairs of poles from (2.30) are located at

$$s_{1,2} = -\frac{\omega_0}{2Q} \pm j\omega_o \sqrt{1 - \frac{1}{4Q^2}}. \quad (2.33)$$

If the effect of the quantizer is ignored ($D(s) = 1$), the root locus method for stability analysis shows that the loop is unconditionally stable (i.e. poles do not enter the right half-plane, as can be seen in Fig. 2.12). However, the quantizer must be taken into consideration in the design, because it introduces a variable gain element $K$ in the loop.
2.3. New Method for Transfer Function Design in $s$-domain

Figure 2.12: Root locus of fourth order bandpass $\Delta \Sigma$ ADC if the quantizer is ignored ($D(s) = 1$).

Figure 2.13: Root locus of fourth order bandpass $\Delta \Sigma$ ADC.
For small input signals, the system gain can increase and lead to the generation of limit cycles [40]. To evaluate the stability of the loop, (2.29) cannot be solved analytically due to the exponential term of the DAC transfer function. To overcome this issue, one solution is to estimate the poles and zeros numerically, as shown in [40], with the drawback of adding complexity to the design procedure. Instead, we can employ a rational function to approximate the quantizer/DAC transfer function $D(s)$. By using the Padé approximation [41], a linear system with delay $\tau_d$ can be expressed as

$$e^{-\tau_ds} \approx \frac{1 - \tau_ds/2 + (\tau_ds)^2/12}{1 + \tau_ds/2 + (\tau_ds)^2/12}.$$  

(2.34)

With the Padé approximation, the transfer function of the quantizer followed by a delay element becomes

$$D(s) \cdot e^{-\tau_ds} \approx \frac{T_s}{2} \left( \frac{1}{1 + \frac{\tau_ds}{2}} \frac{1}{1 + \frac{\tau_ds + T_s/2}{2}} \right).$$  

(2.35)

which describes mathematically the combination of the flip-flop and DAC, including the excess loop delay. The root locus of the modulator can now be plotted since the quantizer is approximated by a rational expression. Part of the root locus plot around the filter poles is reproduced in Fig. 2.13. The filter poles move from the values defined in (2.33) when the loop is open, and $K = 0$ (no feedback) to the position of zeros for an infinite gain in the loop as $K \to \infty$ (zero input signal to the modulator). As the gain in the loop increases due to the presence of the quantizer, one pair of the filter poles moves toward the $j\omega$-axis. For certain gain values, the loop can become unstable. This occurs when the poles enter the right half-plane for a maximum gain $K_{max} = 4.3 \cdot 10^4$. In order to ensure the stability of the system for low input signals, the total gain introduced by the quantizer must be smaller than $K_{max}$. If the loop gain for small input signals is comparable to the maximum allowable gain, the feedback transconductances $G_{fb}$ must be adjusted to reduce the closed loop gain.

The design methodology for the continuous-time bandpass ADC can be summarized in the following steps

1. Design a bandpass filter in $s$-domain.

2. Map filter transfer function to circuit parameters ($G_m$, $L$, $C$, $Q$).

3. Select $G_{m1}$ from circuit simulations for sufficient gain in the first stage.
4. Set DAC current of $G_{fb1}$ stage equal to first transconductor stage $G_{m1}$.

5. Select $G_{m2}$ for maximum linearity and $G_{fb2}$ at least equal to $G_{fb1}$.


7. Increase $G_{fb2}$ and $G_{fb1}$ (if necessary) to account for excess loop delay by reducing the forward gain in the loop.

2.4 Simulation Results with Behavioral Model

Following the derivation of the loop parameters, the system level model must be verified in a behavioral simulation. The fourth order $\Delta\Sigma$M model was simulated in Matlab Simulink in order to capture the real effect of the quantizer. The final ADC parameters were $G_{m1} = 22mS$, $G_{m2} = 10mS$, $G_{fb1} = 50mS$ and $G_{fb2} = 150mS$. The frequency response of the loop filter is shown in Fig. 2.14. The ADC achieves an $SNR = 57dB$ over 60 MHz at 2 GHz (Fig. 2.15) and is able to recover its $\Delta\Sigma$ noise shaping after being overloaded with a full-scale (FS) input signal.

One would expect that the quantization noise of an ADC with an OSR of 333 would be insignificant. It is expected from (2.12) that the dynamic range of single-bit $\Delta\Sigma$ modulators increases by 15 dB for every octave of OSR in second order modulators. The previous equation, however, assumes that the modulators are constructed with ideal lossless filters. In reality, a leaky integrator/resonator in a lowpass or bandpass filter
limits the performance. Figure 2.16 illustrates the simulated SNR vs single resonator $Q$ of the designed modulator at the system level. The simulation was performed in Matlab Simulink. The noise was integrated over a bandwidth of 60 MHz. The peak-SNR is a strong function of $Q$ for values below 80. The maximum value of SNR is 76dB. In comparison, the Delta-Sigma Toolbox [30] simulates a peak-SNR of 77dB for the same OSR and RZ DAC with one clock period delay $T_S$.

This behavior of the SNR vs $Q$ can be predicted analytically if the noise transfer function is known. Figure 2.17 shows a linear representation of a single-bit $\Delta \Sigma$ ADC. Quantization noise appears as a signal added to the analog input. The transfer functions of the loop filter, quantizer and feedback DACs are $G(s) = H^2(s)$, $D(s)$ and $F(s)$, as defined in (2.30), (2.31) and (2.32), respectively. From Fig. 2.17 the noise transfer
The magnitude response of (2.37) is plotted in Fig. 2.18 for three values of $Q$. As $Q$ increases from 10 to 20, the noise floor drops by 10 dB, which correlates to the 10 dB increase of SNR in Fig. 2.16. To gain a better insight into the effect of the filter $Q$ on SNR, we can estimate the quantization noise floor at resonance $\omega_o$. For $s = j\omega_o$, (2.37) becomes

$$|NTF(s)|^2_{s=j\omega_o} = \frac{\omega_o^2}{Q^2 \left( \left( \frac{G_{fb1} G_{m2}}{C^2} \right) + \frac{G_{fb2} \omega_o}{CQ} \right) \omega_o^2}$$

(2.38)

which is plotted in Fig. 2.19. The SNR can be also estimated analytically by integration of quantization noise around the center frequency $\omega_o$. From (1.8) and (2.38), the SNR is
Chapter 2. System Level Design of Continuous-Time $\Delta\Sigma$ ADCs

Figure 2.18: Noise transfer function of $\Delta\Sigma$ ADC for three values of resonator $Q$.

Figure 2.19: Magnitude response of $\text{NTF}(j\omega_0)$ vs resonator $Q$ at $f_o = 2\text{GHz}$.

\[
\text{SNR} = P_{FS} - P_{QN, total} \\
= P_{FS} - \frac{4\pi^2 \Delta^2}{12F_S} \int_{f_o - \frac{BW}{2}}^{f_o + \frac{BW}{2}} Q^2 \left( \frac{G_{f21}G_{m2}}{C_2} + \frac{G_{f22}2\pi f}{C_Q} \right) df. \tag{2.39}
\]

The SNR calculation with (2.39) can be carried out with the aid of a symbolic mathematical tool such as Maple. Figure 2.16 shows that the analytical calculation of SNR is in good agreement with the results found in the behavioral simulation for $Q > 10$.

The SNR is also a function of the loop delay, as previously mentioned. As the location
of the poles changes with increasing delay, the noise transfer function is modified and, as a result, the quantization noise is not attenuated sufficiently. The impact of the extra delay around the loop for stable modulators is illustrated in Fig. 2.20 for RZ and NRZ DAC pulses. The RZ pulse offers higher SNR by almost half a bit for small delays and can maintain higher SNR when the delay approaches $2 \times T_S$. These simulations were performed at the system level model with a resonator Q of 10.9 and a quantizer delay equal to $1.5 \times T_S$. The x-axis represents the extra delay in the loop from the quantizer output to the feedback node. This can be caused by transistor and interconnect delay in the feedback path of the modulator. The ADC was designed to operate with delays between $0.25 \times T_S$ and $0.5 \times T_S$.

Figure 2.20: Peak-SNR vs excess loop delay of $\Delta \Sigma$ ADC ($N_{FFT} = 65536$). The total delay is $1.5 \times T_S + \text{Delay}$.
Figure 2.21: Magnitude response of $NTF(j\omega)$ vs resonator $Q$ at $f_o = 2GHz$ and $f_o = 5.2GHz$.

Figure 2.22: System level simulation of ΔΣ ADC at 5.2 GHz ($N_{FFT} = 65536$).

5-GHz WLAN is 20 MHz, we can assume for simplicity that the ADC has the same OSR. This will allow us to quantify the effect of center frequency on the SNR.

The stability analysis with the root locus method of the open loop signal transfer function predicts that the 5.2-GHz ADC is more susceptible to instability than the 2-GHz version. In particular, to obtain the same gain parameter $K_{max}$ as in the 2-GHz modulator, the quantizer must be realized with only two latches, with a total delay of $T_s$. The behavioral simulation supports this observation with the 5.2-GHz ADC being on the verge of stability when three latches are employed. The other limitation stems from the resonator $Q$. The magnitude of the quantization noise floor from (2.38) is plotted in Fig. 2.21 as a function of $Q$. To attenuate quantization noise by the same amount, as at
2.5. CENTER FREQUENCY SCALING OF BANDPASS ΔΣ MODULATORS

2 GHz, one needs to increase the filter $Q$ by the ratio $5.2\text{GHz}/2\text{GHz}$. For example, to reach $|NTF(j2\pi5.2\text{GHz})| = -80\text{dB}$, the filter $Q$ must be greater than 26. Indeed, the system level simulation at 5.2 GHz gives an SNR of 57.14 dB for a $Q$ of 26 (Fig. 2.22). If the $Q$ is 10.9 as before, then the modulator achieves an SNR of only 46.25 dB. Ways to estimate the loop filter $Q$ of a ΔΣ modulator will be discussed in detail in chapter 5.
Chapter 3

Building Block Design

This chapter presents the schematic design of all building blocks used in the 40-GS/s △Σ ADC. After a brief overview of SiGe BiCMOS and CMOS technologies, the loop filter, DAC, single-bit quantizer and clock distribution network are analyzed. Among the various blocks employed in this thesis, the quantizer and clock distribution network were designed and implemented both in SiGe BiCMOS and nanoscale CMOS in order to explore the suitability of CMOS as a low-power alternative for mm-wave A/D conversion.

3.1 Technology Overview

3.1.1 High Frequency Figures of Merit (\(f_T\) and \(f_{MAX}\))

Prior to presenting the building block circuit design, it is instructive to take a closer look at the technologies used in this work. The ADC and digital receiver are realized in a state-of-the-art production 0.13-\(\mu\)m SiGe BiCMOS technology [42]. The study of low-power blocks in CMOS was performed in two 90-nm processes from two different foundries and in a 65-nm process.

The most commonly used device FoMs for high-speed circuit design are the unity gain current frequency, \(f_T\), and the maximum oscillation frequency, \(f_{MAX}\). The former is defined at the frequency where the current gain of the device

\[
h_{21} \equiv \left. \frac{i_2}{i_1} \right|_{v_2=0}
\]  

(3.1)
drops to one, or equivalently,
\[ 20 \log_{10} h_{21}(f_T) = 0. \] (3.2)

In a similar manner to the previous definition, \( f_{MAX} \) is defined as the frequency where the maximum available gain (MAG) of the device equals one. This FoM contains information about input and output impedances of the device, unlike \( f_T \) that is based solely on intrinsic current gain. To determine \( f_{MAX} \), the MAG must be plotted as a function of frequency. By definition [43]

\[ MAG = \left| \frac{S_{21}}{S_{12}} \right| \left( k - \sqrt{k^2 - 1} \right) \] (3.3)

where
\[ k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\text{det}[S]|^2}{2 |S_{12}| |S_{21}|}. \] (3.4)

One can derive analytical expressions for \( f_T \) and \( f_{MAX} \) from the small signal equivalent circuit of HBT and MOSFET transistors. In the case of \( f_T \), it can be shown that

\[ \frac{1}{2\pi f_T,\text{HBT}} = \tau_B + \tau_C + \frac{1}{g_m} (C_{je} + C_{\mu}) + (R_e + R_c) C_{\mu} \] (3.5)

where \( \tau_B, \tau_C \) the transient times of the base and collector, respectively, \( C_{je} \) the base-emitter junction capacitance, \( C_{\mu} \) the base-to-collector capacitance, and \( R_e, R_c \) the parasitic resistances of emitter and collector, respectively. Equation (3.5) shows the strong dependence of \( f_T \) on bias current \( (g_m) \) and the geometry of the device since both transient times are proportional to the base and collector widths.

The \( f_T \) for the MOSFET becomes

\[ \frac{1}{2\pi f_T,\text{MOS}} = \frac{C_{gs} + C_{gd} + C_{gb}}{g_m} + (R_s + R_d) C_{gd} + \left( \frac{C_{gs}}{1 + g_m R_s} + C_{gd} \right) R_d g_{ds} \] (3.6)

where \( C_{gs}, C_{gd}, C_{gb}, R_s, R_d \) are the parasitic capacitances and resistances of the device and \( g_{ds} \) the source-to-drain conductance.

As opposed to \( f_T \), the \( f_{MAX} \) expression contains information about the parasitic resistance in each device. The \( f_{MAX} \) expression for the HBT can be found as a function of \( f_T \)

\[ f_{MAX,\text{HBT}} = \sqrt{\frac{f_T,\text{HBT}}{8\pi R_b C_{\mu}}}, \] (3.7)
3.1. Technology Overview

Figure 3.1: Measured $f_T$ and $f_{MAX}$ of HBT and MOSFET devices available in a 0.13-µm SiGe BiCMOS technology [42].

implying that minimizing $R_b$ is critical for improved device performance.

The $f_{MAX}$ of a MOSFET device exhibits similar dependence on gate resistance. Because $R_g \propto W_f$, the MOSFET $f_{MAX}$ is strongly dependent (unlike HBTs) on layout geometry. Devices with smaller finger widths have larger $f_{MAX}$, but one should not reduce $W_f$ to a large extent, since this would degrade $f_T$. For very small $W_f$ the gate-to-bulk overlap capacitance $C_{gbo}$ dominates and $f_T$ drops. The expression of $f_{MAX}$ in a MOSFET is

$$f_{MAX,MOS} = \frac{f_{T,MOS}}{2 \sqrt{R_g (g_{ds} + 2\pi f_{T,MOS} C_{gd}) + g_{ds} (R_s + R_b)}}$$  \hspace{1cm} (3.8)$$

The relationship between $f_T$ and $f_{MAX}$ vs current density for a production 0.13-µm SiGe BiCMOS process used in this thesis is illustrated in Fig. 3.1. The emitter width $w_E$ in the HBT is 0.17 µm, while the channel length $L$ of the nMOSFET is 0.13 µm. The measured peak-$f_T$ values of the two devices exceed 150 GHz (HBT) and 90 GHz (nMOSFET). As expected, the higher $g_m$ and lower parasitic capacitances of the HBT ($C_{cs}$ vs $C_{db}$ - collector-to-substrate vs drain-to-bulk capacitance) result in higher $f_T$ and $f_{MAX}$. The $f_T$ peaks at 0.3 mA/µm of drain current density for the MOSFET and 6 mA/µm² for the HBT.

As constant-field MOSFET scaling is followed by all foundries, it is expected that
Chapter 3. Building Block Design

$f_T$ and $f_{\text{MAX}}$ of nMOSFETs peak at the same current densities. Figure 3.2 summarizes device measurements for transistors manufactured from different foundries. Each FoM peaks at the same $I_{DS}/W$ irrespective of technology node and foundry (0.3 mA/µm for $f_T$ and 0.2 mA/µm for $f_{\text{MAX}}$). Biasing at the peak-$f_T$ current density guarantees that both analog and digital blocks have the highest speed.

3.1.2 Linearity Performance

The choice of an HBT or MOSFET device is also related to linearity. One has to investigate the linearity performance of each device before selecting the most suitable one for A/D converters. In particular, the analog portion of the ΔΣ ADC must have as high linearity as possible, since this will dictate the full-scale level and, consequently, the SNR of the entire ADC.

Although HBTs follow the exponential $I-V$ law [44] in each technology node, the square law no longer holds for nanoscale CMOS. As shown in [45] and analyzed in [46], constant-field scaling in CMOS technologies results in a linear dependence between drain current and effective voltage $V_{\text{EFF}} = V_{GS} - V_T$ for drain current densities above 0.15 mA/µm. The physical mechanism that causes this behaviour is the degradation of carrier mobility due to the large electric field across the channel. As a result, the classical $I_D$ vs $V_{GS}$ equation of MOSFETs [46]

$$I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_T)^2$$

becomes

$$I_D = \begin{cases} \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_T)^2, & I_D/W \leq 0.15 \text{mA}/\mu\text{m} \\ \mu_n C_{OX} \frac{W}{L} V_{\text{EFF,cr}} (V_{GS} - V_T - \frac{1}{2}V_{\text{EFF,cr}}), & I_D/W \geq 0.15 \text{mA}/\mu\text{m} \end{cases}$$

where $V_{\text{EFF,cr}}$ the effective voltage that gives the maximum transconductance $g_{m,max}$. Figure 3.3 shows the measured DC characteristic of a 90-nm nMOSFET. Current $I_D$ becomes linear for large values of $V_{GS}$ in the strong inversion region. To take full advantage of the linear behaviour in nanoscale MOSFETs, it is preferable to bias the circuit at the point where the linear voltage gate swing is maximum. As can be seen in Fig. 3.4, this occurs at different values of $V_{GS}$ across technology nodes but at a constant drain current density of 0.3 mA/µm irrespective of transistor channel length. It has recently been
3.1. Technology Overview

found that this trend is also independent of foundries [45,47]. Rather than following a $V_{GS}$-centric methodology that makes designs sensitive to process variations of $V_T$, it is advantageous to bias at constant current density for maximum linearity. This bias technique ensures that the design is insensitive in the presence of process variations because under strong inversion the device still operates in the optimum region of 0.3 mA/µm, where linearity is at its maximum.

3.1.3 Noise Performance

It is useful to examine the noise behaviour of the two main devices, HBTs and MOSFETs. This is relevant because the first stage of the ADC operates at GHz frequencies and, as a result, its noise contribution must be minimal. The noise factor $F$ of the a two-port network can be expressed as a function of the device minimum noise factor $F_{MIN}$, the noise resistance of the device $R_n$, the source admittance $Y_S = G_S + jB_S$ and the optimum source admittance $Y_{S,OPT}$.
Figure 3.3: Measured DC transfer characteristics of a 10 × 1 μm 90-nm nMOSFET [45].

Figure 3.4: Measured $f_T$ as a function of gate-to-source voltage $V_{GS}$ for bulk nMOSFETs fabricated with different drawn gate lengths in the 90-nm node [45].
\[ F = F_{\text{MIN}} + \frac{R_n}{G_s} |Y_S - Y_{S,\text{OPT}}|^2. \] (3.10)

From the last expression, it is clear that if the device or circuit is presented a source impedance \(1/Y_{S,\text{OPT}}\), then its \(F = F_{\text{MIN}}\). In all cases, the source should have \(Y_{S,\text{OPT}} = 1/50\Omega\) for a 50-\(\Omega\) testing environment.

The noise resistance \(R_n\) expresses the sensitivity of the device to source admittance mismatch. Based on the small signal equivalent circuit, one can derive the analytical expressions of the basic noise parameters \(F_{\text{MIN}}, R_n\) and \(Y_{S,\text{OPT}}\) [48]. For an HBT device with current gain \(\beta\), base and emitter resistances \(R_b\) and \(R_e\), respectively, we can write

\[ F_{\text{MIN,HBT}} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T} \sqrt{\frac{g_m}{2} (R_e + R_b)} \left(1 + \frac{f_T^2}{\beta f^2}\right) + \frac{f_T^2}{\beta f^2} \] (3.11)

\[ R_{n,HBT} \approx \frac{1}{2g_m} + (R_e + R_b) \] (3.12)

\[ Y_{S,\text{OPT,HBT}} \approx \frac{f}{f_T R_n} \left[ \sqrt{\frac{g_m}{2} (R_e + R_b)} \left(1 + \frac{f_T^2}{\beta f^2}\right) + \frac{f_T^2}{\beta f^2} - j\frac{1}{2} \right] \] (3.13)

For the nMOSFET device with gate and source resistances \(R_g\) and \(R_s\), respectively, the expressions for \(F_{\text{MIN}}, R_n\) and \(Y_{S,\text{OPT}}\) become [48]

\[ F_{\text{MIN,MOS}} \approx 1 + \frac{f}{f_T} \sqrt{ Pg_m (R_s + R_g) } \] (3.14)

\[ R_{n,MOS} \approx \frac{P}{g_m} + (R_s + R_g) \] (3.15)

\[ Y_{S,\text{OPT,MOS}} \approx \frac{f}{f_T R_n} \left[ \sqrt{ Pg_m (R_s + R_g) } - jP \right]. \] (3.16)

The drain noise current parameter \(P\) (also known as \(\gamma\) in some papers) equals approximately \(2/3\) for long-channel devices.

A comparison of (3.11) and (3.14) shows that \(F_{\text{MIN}}\) is proportional to the square root of \(g_m\). A MOSFET device, therefore, has lower \(F_{\text{MIN}}\), provided that its \(f_T\) is comparable to that of an HBT. This not widely-known property of MOSFETs has been also verified in state-of-the-art 65-nm CMOS and 300-GHz SiGe HBT technologies [49]. The low-noise potential of CMOS will be used in the design of low-noise broadband amplifiers, as will
be shown later in this chapter. The better noise performance of MOSFETs, however, comes with a disadvantage. As seen in (3.12) and (3.15), the MOSFET is more sensitive to impedance mismatches between $Y_S$ and $Y_{S,OPT}$ because its $R_n$ is higher. A circuit with MOSFET input stage is more difficult to noise match than one with HBT as the input transistor. It should also be noted that $F_{MIN}$ changes with current density [45] both in HBTs and MOSFETs. At low collector/drain current densities, the main noise contributor is base/gate resistance. At high current densities, $F_{MIN}$ is determined by the collector shot noise or channel noise. The optimum noise figure current density for nMOSFETs is about 0.15 mA/$\mu$m irrespective of technology node, while the HBTs have their optimum noise performance at current densities that increase with each technology generation [45].

3.2 Blocks implemented in SiGe BiCMOS

3.2.1 Loop Filter

The key block in any $\Delta\Sigma$M is the loop filter because it sets the linearity, noise and tunability performance of the entire receiver. Moreover, the filter $Q$ determines the quantization noise floor, as explained in chapter 2. To be able to reduce the power dissipation of a 40-GS/s ADC, one has to design both the analog and digital parts from a power supply lower than 3.3 V. It has been recently shown that a 40-Gb/s retimer can operate from 2.5 V in SiGe BiCMOS [28] with sufficient margin. Therefore, the loop filter of the $\Delta\Sigma$ ADC should operate from the same 2.5-V power supply while having excellent linearity and noise performance.

The circuit schematic of the fourth order loop filter is shown in Fig. 3.5. The first stage serves as both the input transconductor $G_{m1}$ and the receiver LNA. The combination of nMOSFET and HBT transistors in the cascode amplifier provides maximum linearity and isolation allowing for lower power supply than is otherwise possible with an HBT-only implementation. Since the design goal for the filter is linearity rather than gain, we take advantage of the excellent linearity of nMOSFETs when biased at the peak-g$_m$ current density of 0.4 mA/$\mu$m. Under peak-g$_m$ bias, the 0.13-$\mu$m nMOSFET exhibits 0.45V$_{pp}$ linear swing at its gate for 1-dB compression of g$_m$ and does not require inductive or resistive source degeneration for improved linearity. The NF is only slightly degraded from its minimum value at 0.15 mA/$\mu$m [45]. A degenerated HBT-HBT cascode would
increase the NF of the circuit for the same linearity. Furthermore, the linearity is improved over that of a MOS-MOS cascode by the higher output voltage swing and output resistance of the HBT in the MOS-HBT cascode. Another way to examine the suitability of the four basic cascode combination available in a SiGe BiCMOS process (HBT-HBT, MOS-HBT, HBT-MOS and MOS-MOS) is the ratio of $f_T$ over its second derivative with respect to current density [50]. In other words, the linearity of a certain topology is proportional to the peak value of $f_T$ and the flatness of its characteristic. The plot of \( \frac{f_T}{\omega g_m} \) as a function of collector/drain current density clearly shows that the MOS-HBT cascode amplifier has better linearity than all the other combinations [46, 51]. Sizing of transistors at the peak-$g_m$ bias was done such that the transconductance of each cell is as specified in the system level analysis (Fig. 3.6).

The degeneration inductor $L_E$ is employed to make the real part of the input impedance $Z_{in}$ equal to 50 $\Omega$, as in an LNA. It also slightly improves the linearity. The MOS-HBT cascode has an $f_T$ of 80 GHz.

\[
Z_{in} = \frac{1}{sC_{gs}} + sL_E \left( 1 + g_m \frac{1}{sC_{gs}} \right) \\
= \frac{g_mL_E}{C_{gs}} + j \left( \omega L_E - \frac{1}{\omega C_{gs}} \right)
\]

or

\[
\Re(Z_{in}) = \omega_T \cdot L_E \\
L_E = \frac{50\Omega}{2\pi80\text{GHz}} = 100\text{pH}
\]

The common mode inductor $L_{EE}$ suppresses the even order harmonics of the first transconductor with minimal noise contribution. A current source or a resistor could provide common mode rejection, but at the expense of increased noise and lower headroom. Both filter stages are biased at the peak-$g_m$ current density. The resistors at the drains of M5/M7 lower the $V_{DS}$ across these transistors below 1.2 V.

The filter tank consists of an $LC - C_{VAR}$ combination, with $L_C = 3.8$ nH (differential) and $C_C = 2.3$ pF, such that

\[
\omega_0 = \frac{1}{\sqrt{(L_C/2)(C_C + C_{VAR})}}.
\]

(3.17)
Chapter 3. Building Block Design

The varactor was added to provide a means of adjusting the center frequency. Its capacitance $C_{VAR}$ varies between 0.4 and 0.8 pF. It is significantly smaller than $C_C$ in order to maintain a high $Q$ while still providing more than 10% tunability at 2 GHz. The varactor control voltage $V_{TUNE}$ is applied from an external power supply. The S-parameter simulation results of the filter can be found in Fig. 3.7 for $V_{TUNE} = 0$ and 2.5 V. The $Q$ and center frequency depend on the varactor. If its capacitance changes by 15% due to process variations, the total capacitance will change by less than 4%. The process variations on the inductor and MIM capacitor are insignificant (less than 1%), since their values depend on the metals, which are very well controlled in the process. Figure 3.8 reproduces the $S_{21}$ of the filter before and after extraction. Due to parasitic resistance, the gain at the center of the passband drops by about 1.5 dB. An external inductor at the gate is required to cancel out the imaginary part of the input impedance and also perform the noise matching to the 50-Ω source impedance. The input impedance of the circuit would then be matched to 50 Ω, as in Fig. 3.9.

Assuming a NF of 2 dB across a signal bandwidth of 60 MHz and an $SNR = E_b/N_0 = 14dB$ for voice/data signals, the receiver sensitivity at room temperature without accounting for quantization noise is

$$P_S = -174dBm/Hz + NF + 10\log_{10}BW + SNR$$

$$= -80.2dBm$$ (3.20)
3.2. Blocks implemented in SiGe BiCMOS

Figure 3.6: Simulated transconductances $G_{m1}$ and $G_{m2}$ of loop filter.

Based on the measured sensitivity of the flip-flop at 40 Gb/s [28], the minimum signal required at the input of the quantizer is $10mV_{pp}$ per side. The LNA/filter must therefore amplify the minimum input signal up to at least $10mV_{pp}$ at the first stage of the quantizer. The voltage gain of the two-stage filter must be larger than

$$A_V = \frac{V_{out}}{V_{in}} = \frac{5mV}{30.9\mu V} = 162.$$  \hfill (3.21)

Each LC filter tank has a $Q$ of 11 and can be represented at resonance as a parallel RLC network with $R_P = Q\omega_0L = 262\Omega$, resulting in a voltage gain of the first stage $V_{out}/V_{in} = -g_mR_P = -6V/V$. The total gain of both stages is about 36. To reach the required $A_V = 162$, the filter $Q$ must be further improved by a factor of 2. Therefore, we can conclude that the sensitivity of the present design is limited by the $Q$ of the filters.

The linearity of the ADC is also determined by the voltage swing at the output of each amplifier stage. The maximum voltage swing at the collectors of Q1-Q2 should not drive the HBTs into saturation. Assuming a bias current $I_C$ and $V_{CE,SAT} = 0.3V$, the maximum swing is

$$\Delta V_{\text{max}} = \min\{I_C R_P, V_{CC} - (V_B - V_{BE} + V_{CE,SAT})\}$$  \hfill (3.22)

or $2.6V_{pp}$. For a single-ended gain of 6 and 2.6V swing, the maximum allowable input signal is $V_{in,max} = 0.44V_{pp}$, corresponding to an input power of -3dBm. This value is approximately equal to the receiver $P_{1dB}$, as will be shown in chapter 5.
Figure 3.7: Simulation results of the fourth order bandpass loop filter.

Figure 3.8: Comparison of simulated $S_{21}$ before and after extraction of parasitics.
To gain extra linearity from the filter, while reducing its noise contribution, one can modify the second transconductance stage as in Fig. 3.10. Compared to the topology of Fig. 3.5, the linear voltage swing at the output of the second differential stage, and the overall noise figure and dynamic range of the filter are improved by removing the emitter followers between stages and the current source in the second stage. A current source would not contribute to circuit noise in a fully balanced differential circuit operating in small signal. However, the two-stage filter is in large signal mode when the differential circuit is fully switched to one side, therefore the noise of the cascode directly degrades the sensitivity. It is also expected that during the testing phase of the circuit, the input is applied to one side only and the filter will not work in fully differential state. To ensure common mode rejection in the absence of a current source, a 2.7-nH inductor $L_{EE,2}$ is implemented with series stacked windings in the top three metals of the process and occupies an area of $47 \times 47 \mu m^2$.

One can employ a similar filter topology for the 5-GHz ADC as illustrated in Fig. 3.11. Unlike the input stage of the 2-GHz ADC that requires a large external inductor ($> 20nH$) to perform the 50-Ω noise and impedance matching, the transconductance cell of the 5-GHz ADC can be matched to the 50-Ω source impedance with on-chip inductors. This is made possible because the reactance due to $C_{gs}$ of M1-M2 is smaller at 5 GHz. The input impedance matching inductor $L_B$ is 4.6 nH for an input nMOSFET $3 \times 32 \times 1\mu m \times 0.13\mu m$. The filter tank at 5 GHz now consists of a 2.3-nH inductor in
Figure 3.10: Circuit schematic of fourth order modified 2-GHz loop filter for increased linearity.

Figure 3.11: Circuit schematic of fourth order loop filter centered at 5 GHz.
parallel with a 800-fF varactor for higher tunability. The S-parameter simulation showing input noise and impedance matching is shown in Fig. 3.12.

3.2.2 Feedback Digital-to-Analog Converter

Figure 3.13 shows the DAC topology, similar to the one in [23] but implemented with MOS-HBT cascodes which allows it to operate from 2.5 V with improved frequency response. When both M1 and one of Q1-Q2 turn on, $I_{TAIL}$ flows though the nodes DACP or DACN and is subtracted from the feedback node, which is the collector of the MOS-HBT amplifier in the filter. The clock signal switches the differential pair M1-M2 and generates the RZ current waveform. The presence of HBTs Q1-Q2 provides a large $g_{m}/I_{TAIL}$ ratio and reduces the voltage swing that is required at the quantizer output to fully switch the DACs. Transistors Q3-Q4 act as dummy loads to ensure the symmetry of the waveform. The two DACs are designed for a peak current of 18 mA and 54 mA, respectively. Their total power dissipation is 237.5 mW from the 2.5 V power supply. Figure 3.14 shows the transient simulation of the first DAC. The quantizer signal VDFF is applied to transistors Q1 and Q2, while the clock signal VCLK steers $I_{TAIL}$ either through M1 or M2. The current IDAC at node DACP it then subtracted from the collectors of the loop filter in Fig. 3.5. The duration of each quantizer pulse is $4 \times T_s$. The simulation of the DAC was performed in open loop mode.
Figure 3.13: Circuit schematic of RZ DAC.

Figure 3.14: Transient simulation results of RZ DAC when clocked at $F_s=40$GHz and the quantizer signal is applied to its input. Simulation performed after parasitic extraction.
3.2.3 Quantizer

The schematic of the latch used in the Master-Slave-Master flip-flop is illustrated in Fig. 3.15. It is based on the same MOS-HBT cascode and has similar speed from a lower power supply [28] when compared to an HBT-only implementation. The HBTs provide large gain on the data path to reduce the effect of quantizer metastability. To fully switch the DACs and output driver, the voltage swing at the quantizer output must be higher than 300\textit{mV}	extsubscript{pp}. If the Master-Slave-Master latches do not have adequate output swing, the DACs in the feedback loop of the ADC will not operate correctly. For a minimum input data swing of 10\textit{mV}	extsubscript{pp}, this requires a voltage gain of 30, which can only be realized by cascading at least three latches in a Master-Slave-Master configuration.

For an \textit{I}_{TAIL} of 14 mA and a load resistance \textit{R}_{L} of 35Ω, the data path gain of the latch (from the data input to the source follower) is

\[ \text{Gain} = -g_{m}R_{L} = -\frac{I_{TAIL}/2}{V_{T}}R_{L} = -10\text{V/V} \] (3.23)

This value ignores the effect of the parasitic emitter resistance \textit{R}_{E}, typically 3.5Ω for an 8μm × 0.17μm HBT. The effective transconductance then becomes

\[ g_{m,eff} = \frac{g_{m}}{1 + g_{m}R_{E}} \] (3.24)

and considering the 0.8 V/V gain in the source follower, the gain of the latch reduces to about 4. The HBT differential pair produces a voltage swing of 14mA × 35Ω = 490mV\textsubscript{pp}, which is further attenuated to 400mV\textsubscript{pp} by the source follower pair. For this reason a Master-Slave-Master flip-flop is employed with a total voltage gain of 4\textsuperscript{3} = 64. If a Master-Slave flip-flop had been employed, the gain would have been only 16 and the voltage swing before the driver and DACs would have been only 160mV\textsubscript{pp}, which is inadequate to fully switch a bipolar differential pair with some emitter degeneration. This analysis gives a worst-case estimate of the signal gain in the latch. It assumes that the clock differential pair is switched to one side and the latch operates as an amplifier. In reality, the gain can be higher due to the finite regeneration inside the latch. As shown in [28], the flip-flop produces a high swing output for low input signals up to 45 Gb/s. From time domain simulations of the latch at 40 GHz, the large signal gain is 5.9 V/V and the regeneration time is 5.1 ps. Although the three latches have the same topology, the device sizes and tail currents of each stage are scaled by a factor of 1.5 compared
to the preceding stage. This allows for the last master latch to drive the two DACs and output driver. The entire power dissipation of the flip-flop is 512.5 mW from 2.5 V. Figure 3.16 illustrates the 40-Gb/s eye diagram at the output of the flip-flop when simulated with a $2^7 - 1$ pseudorandom input bit pattern.

### 3.2.4 Clock Distribution Network

The external clock signal is distributed to the three latches and two DACs by a broadband clock tree. As depicted in Fig. 3.17, the clock network comprises a chain of MOS-HBT cascode inverters with series and shunt inductive peaking to extend its bandwidth beyond 40 GHz. The number of stages is determined by the load that the clock tree drives. Due to the existence of delay around the loop and accounting for the subsequent adjustment of the tail currents in the feedback DACs, the flip-flop fanout was increased to ensure that the DACs and output driver switch completely. The resulting total tail currents in the flip-flop and DACs are 62 mA and 60 mA, respectively. Figure 3.17 shows the current consumption of each MOS-HBT inverter, including the emitter follower differential pair, for a scaling factor of about 1.5 between successive stages. The clock distribution network is the highest power consuming block in the ADC with 645 mW from 2.5 V.

In order to satisfy the 40-GHz bandwidth condition, the clock distribution network operates as a chain of CML inverters each with a gain of 1.5. The minimum voltage swing to switch the 0.13-µm MOS differential pair biased at maximum speed is $400 mV_{pp}$.
3.2. Blocks implemented in SiGe BiCMOS

Figure 3.16: Simulated 40-Gb/s eye diagram of master-slave-master D-type flip-flop after extraction of parasitics ((2^7 − 1)-bit pattern).

[45]. For a tail current of 3mA, the MOS-HBT inverter (Fig. 3.17) has a swing ΔV = 1.5 × 400mV_{pp} = 600mV_{pp} and a load resistance R = ΔV/I_{TAIL} = 200Ω. The cascode is biased at peak-f\text{f}_T current density when the entire I_{TAIL} is steered through one side. The bandwidth of the MOS-HBT inverter can be estimated if the total capacitance C_T at the collector node of Q_1 is known. For the MOS-HBT inverter of Fig. 3.17 with 10μm × 0.13μm MOSFETs, 1.5μm × 0.17μm HBT in the cascode and 2.9μm × 0.17μm HBT in the emitter follower, C_T can be estimated as

\[ C_T = C_{\mu,Q1} + C_{CS,Q1} + C_L = 32.5fF, \]  

(3.25)

where C_L is the capacitive load of the next stage

\[ C_L = C_{\mu,Q3} + \frac{C_{\pi,Q3}C_{MOS}}{C_{\pi,Q3} + C_{MOS}} \]  

(3.26)

and

\[ C_{MOS} = C_{gs,M1} + C_{gd,M1} + C_{gd,M3} + C_{db,M3} = 38fF \]  

(3.27)

The 3-dB bandwidth BW_{3dB} is 24.5 GHz. With the use of inductive peaking (L = 420pH), the bandwidth is extended to 39.2 GHz. The simulated bandwidth of the clock tree was found to be 38.1 GHz (Fig. 3.18) and it is about the same for both output nodes of the distribution network, i.e. the input to the latch and DACs.
Figure 3.17: Block diagram of clock distribution tree and schematic of emitter follower MOS-HBT inverter.

The output buffer that drives the $\Delta\Sigma$ bitstream to the external 50-\(\Omega\) loads consists of two bipolar inverter stages with inductive peaking [28]. As shown in Fig. 3.19, the second inverter employs an emitter degeneration resistance in order to improve the bandwidth and reduce the impact of distortion in the last stage that drives the signal off chip.

### 3.3 Blocks implemented in CMOS

One of the main advantages of MOSFET scaling to nanometer gate lengths is the ability to reach device speeds exceeding 120 GHz with low supply voltages. Despite the high intrinsic speed of transistors available in these processes, the design of 1.2-V 40-Gb/s digital blocks in CMOS remains a challenge. A CMOS implementation would permit 40-GS/s ADCs to operate with the same performance as in SiGe BiCMOS, while consuming lower power \(^1\). This section presents a 40-Gb/s full-rate D-type flip-flop (DFF) and two transmitters.

\(^1\)Aside from their use as quantizers in mm-wave ADCs, flip-flop circuits are the most critical digital blocks used in high-speed wireline and fiber-optic transceivers and equalizers. In a full-rate transceiver, the flip-flop must retime the data at a clock frequency equal to the data rate, while also removing the jitter. A CMOS implementation would permit 40-Gb/s serializer-deserializer (SERDES) chips to reach the same levels of integration as state-of-the-art 10-Gb/s ICs [52, 53], and to operate from a single 1.2-V power supply. For a 40-Gb/s SERDES to be economically viable, its cost and performance must be competitive compared to a 4×10 Gb/s solution [54]. Typically, a 40-Gb/s SERDES must have less than 2.5 times the cost of a 10-Gb/s system while consuming less than 2.5 times the power. Although a half-rate 40-Gb/s transmitter in CMOS has been reported in [55], it operates from 1.5 V and consumes two times the power of a similar SiGe BiCMOS transmitter operating at 86 Gb/s [56].
3.3. Blocks implemented in CMOS

Figure 3.18: Simulation result of clock distribution network small signal response at the two DAC and quantizer clock inputs.

Figure 3.19: Circuit schematic of 50-Ω output driver.
Figure 3.20: Schematic of traditional latch in CMOS requiring $V_{DD}=1.5$ V for 40-Gb/s operation.

TIA topologies in CMOS. Operation at 40 Gb/s is made possible by combining low-$V_T$ and high-$V_T$ transistors in the latch and optimally biasing, and sizing the transistors at the peak-$f_T$ current density.

3.3.1 Quantizer

Full-rate retiming has been successfully demonstrated at speeds above 40 Gb/s only in III-V [57, 58] and SiGe BiCMOS technologies [28, 59]. However, these circuits operate from 1.5 V or higher supplies and consume at least 20 mW per latch. To truly benefit from the lower power potential of nanoscale MOSFETs, the traditional CML latch topology of Fig. 3.20 must be simplified by reducing the number of vertically-stacked transistors to allow for 1.2-V operation. The availability of low-$V_T$ devices is also a prerequisite. In the past, the low-voltage latch has been implemented either by removing the current source [60] or using transformers [61] to couple the signal between the differential pairs in the clock and data paths. The former solution has been demonstrated in 90-nm CMOS at speeds below 20 GHz. The latter has been used in a 60-Gb/s 2:1 MUX clocked at 30 GHz, but its bandwidth is limited to that of the transformer.

Figure 3.21 illustrates the proposed MOS-CML latch schematic and its placement in a decision circuit. The data and clock signals are applied to the Master-Slave flip-
Figure 3.21: Full transistor-level schematic of decision circuit in 90 nm CMOS. All devices have minimum channel length.
flop through broadband TIAs that will be discussed in the next section. A MOS-CML output buffer drives the 40-Gb/s signal to 50-Ω loads. In the proposed latch topology, the clock signal switches the differential pair transistors M1 and M2 from 0 to \(2 \times I_{BIAS} = 0.3 \text{ mA/µm}\). The latter corresponds to the peak-\(f_T\) current density of nMOSFETs [45]. Equivalently, when the gate voltages of M1 and M2 are equal, the current density through each device is 0.15 mA/µm. To fully switch the 90-nm MOS differential pair, a voltage swing exceeding 300mV per side is required [45]. For a \(30 \times 1 µm \times 0.09 µm\) device with \(I_{BIAS} = 4.5 \text{ mA}\) and a load resistance of \(R_L = 40 \Omega\), the voltage swing at the output of each latch is

\[
\Delta V_{swing} = (I_{M1} + I_{M2})R_L = 360mV
\]

which is sufficient to fully switch the differential pair in the next stage and results in an inverter gain \(A_V = -1.2\). The bandwidth of the latch is extended with shunt inductive peaking. For a fanout of \(k = 1\) and the input capacitance of the next stage equal to \(C_{gs} + (1 - A_V)C_{gd}\), the total capacitance at the drain of M3 is

\[
C_T = C_{d3} + C_{g3} + C_{d5} + C_{g5} + C_{gs3} + (1 - A_V)C_{gd5} + k (C_{gs} + (1 - A_V)C_{gd}) = 197fF
\]

and the inductance \(L = 100pH\) increases the \(BW_{3dB} [9]\) to

\[
BW_{3dB} = 1.6 \times \frac{1}{2\pi R_L C_T} = 32.3GHz
\]

which is adequate for 40-Gb/s operation on the data path.

The second technique that improves the speed of the latch is the choice of devices with different \(V_T\) in the data and clock paths of the latch. As shown in Fig. 3.21, low-\(V_T\) transistors are employed in the data path differential pairs M3-M4 and M5-M6. The clock pair is designed with high-\(V_T\) devices. This approach ensures that transistors in the clock path buffer, immediately preceding the latch, have \(V_{DS} > 0.3V\), as required for operation at 40 GHz. When either M1 or M2 is turned off, its \(V_{GS}\) is equal to \(V_T\). A high-\(V_T\) device (0.34V) on the clock path ensures that the \(f_T\) of M7/M8 remains larger than 80 GHz because their \(V_{DS} = 0.34 \text{ V}\). On the other hand, when M3 or M4 are fully turned off, \(V_X = V_{DS,M1} = V_{DD} - \Delta V_{swing} - V_{T,M3}\). By choosing a low \(V_T\) (0.18V) device for M3-M6, the \(V_{DS}\) and therefore the speed of M1/M2 are maximized.
Figure 3.22: Simulated 40-Gb/s eye diagram of decision circuit in 90 nm CMOS.

The decision circuit was simulated over process and temperature corners after extraction of layout parasitics with a $2^7 - 1$ pseudorandom signal. The corresponding output 40-Gb/s eye diagram at $V_{DD}=1.2V$ is shown in Fig. 3.22.

3.3.2 Transimpedance Amplifiers

To be able sample CMOS circuits at 40-GS/s, a broadband amplifier is required on the clock path of the ADC. Such an amplifier will take advantage of the low-power capabilities of CMOS and reduce the power dissipation of the clock tree, which, in the SiGe version, amounts to $1/3$ of the total ADC power. One attractive solution for broadband amplification is the use of shunt-shunt feedback. Transimpedance amplifiers are extensively used in wireline communications receivers to interface with the photodiode [62]. When the amplifier is placed at the input of the clock tree, it must have 50-Ω impedance. Compared to a typical CML inverter with on-chip resistive matching, transimpedance feedback helps to have lower noise at lower current [45].

A CMOS TIA in a 40-GS/s ADC must be able to operate from 1.2-V supply with more than 40 GHz bandwidth and low noise. Possible TIA topologies are shown in Fig. 3.23. The TIA with resistive load (Fig. 3.23(a)) requires a significant DC voltage drop on $R_D$ in order to achieve adequate open loop gain, making it impractical. One approach to increase the gain, while requiring only 0.6 V of DC headroom, is to replace the resistor $R_D$ with a PMOS active load (Fig. 3.23(b)), as has been shown in [45]. The loop gain of the TIA increases from $g_m \times (R_D//R_F)$ to $g_m \times (r_{o,n}//r_{o,p}//R_F)$. The PMOS load
is needed to increase the gain of the amplifier at low supply voltages, at the expense of higher capacitance at the output node. The latter effect is partially mitigated by adding an inductor in the feedback loop, which resonates out the parasitic capacitance of the NMOS and PMOS transistors.

The gain stages that provide the data and clock signals to the latches in the flip-flop are implemented as fully differential versions of the NMOS TIA with PMOS active load. As illustrated in Fig. 3.21, an on-chip 1:1 vertically stacked transformer converts the single-ended external clock to a differential signal applied to the TIA input for testing purposes. Although the transformer limits the bandwidth of the clock tree at low frequencies to about 20 GHz, it is preferred over applying the clock signal to one side of the amplifier’s differential input. Because the differential amplifier has no common mode rejection, the clock signal would arrive at the latch with amplitude and phase mismatch. However, in a 40-GS/s digital receiver implementation a 40-GHz VCO/PLL would be integrated on chip and the transformer would be removed, as will be described in chapter 5. The TIAs are followed by differential common-source stages with inductive peaking.

To tune out the parasitic capacitance in the feedback loop of the TIA, a 500-pH inductor, realized with vertically stacked windings in the top two metal layers of the process, is inserted in series with the feedback resistor $R_F$. Its self-resonant frequency exceeds 100 GHz when a layout with 35 $\mu$m diameter and 2 $\mu$m conductor width is employed. The relatively large series resistance of the vertically-stacked inductor can be absorbed in the feedback resistor $R_F$. 

Figure 3.23: Circuit schematics of low-voltage TIAs with resistive and inductive feedback: (a) NMOS inverter with resistive load, (b) NMOS inverter with PMOS active load, and (c) CMOS inverter.
Figure 3.24: Measured \( f_T \) vs \( V_{GS} \) (left) and \( I_{DS/W} \) (right) of 90-nm and 65-nm nMOSFETs with low and high-\( V_T \) showing that the peak-\( f_T \) current density and peak-\( f_T \) value do not depend on \( V_T \).

The PMOS current mirrors control the bias currents of the MOSFETs in the TIA stages and in the following common-source amplifiers, making them independent of temperature and power supply variations [63]. The role of the differential common-source stages with inductive peaking is also to provide the proper DC levels to the latches in the flip-flop. The 12-Ω common mode resistor at the clock tree output lowers the DC voltage level at the gates of M1 and M2. The gate voltage must correspond to a drain current density of 0.15 mA/\( \mu \)m, such that the transistors switch from 0 to 0.3 mA/\( \mu \)m. It should be noted that a CML inverter with a tail current source cannot be employed in place of the M7-M8 differential pair due to lack of voltage headroom. More importantly, this bias scheme is robust to supply voltage variation from 1.1 V to 1.3 V. When the supply voltage increases above 1.1 V, the \( V_{GS} \) of the clock pair transistors in the latch increases commensurately. As illustrated in Fig. 3.24, this has little impact on the \( f_T \) of the nMOSFET which remains practically constant at large \( V_{GS} \).

To further improve the TIA performance, while reducing the power dissipation, one can employ a typical CMOS inverter with resistive and inductive feedback (Fig. 3.23(c)). As outlined in [64], the CMOS inverter offers the advantage of smaller size and lower bias current for the same performance. For example, the CMOS inverter with feedback resistor \( R_F \) has a small signal open-loop gain of

\[
A = \frac{g_{m,n} + g_{m,p}}{g_{o,n} + g_{o,p} + 1/R_F} \tag{3.31}
\]

\[
A = \frac{g_{m,n} + g_{m,p}}{g_{o,n} + g_{o,p} + 1/R_F} \tag{3.31}
\]
with an input resistance

\[ R_{IN} = \frac{R_F}{1 + A}. \]  

(3.32)

Due to its higher transconductance, it can achieve the same noise impedance for about 1/3 the transistor size of an NMOS TIA [64]. Compared to the NMOS version, the biasing of the CMOS TIA of Fig. 3.23(c) is sensitive to power supply variations. To overcome this, one can employ a PMOS transistor to bias the CMOS inverter at the source of its PMOS transistor. This can be realized if the \( V_{GS} \) required for 40-Gb/s operation is around 0.5 V as can be seen in Fig. 3.24 for the 65-nm GP nMOSFETs.

To investigate the benefits of switching from SiGe BiCMOS to nanoscale CMOS for 40-Gb/s applications, the NMOS and CMOS TIA circuits were designed in 90-nm GP CMOS and 65-nm LP CMOS. The component values of each implementation are summarized in Table 3.1. The clock amplifier of Fig. 3.21 was designed as a differential (Fig. 3.25) and single-ended test structure for analysis of both large and small signal characteristics.

The measured \( f_T \) of 90-nm GP and 65-nm LP nMOSFETs from two different foundries is summarized in Fig. 3.24. The measured data in Fig. 3.24 clearly indicate that the peak-\( f_T \) value occurs at the same current density irrespective of the device threshold voltage and technology node. As shown in the CMOS technology discussion, this property of submicron MOSFETs can be applied in the design of high-speed digital circuits that are robust to threshold voltage, \( V_{GS} \), and ultimately power supply voltage variation. Another important aspect unveiled by the measured data in Fig. 3.24 is that the threshold voltage of the low-\( V_T \) 65-nm LP MOSFETs is actually higher than that of the high-\( V_T \) 90-nm GP devices. At the same time, the \( f_T \) of the 65-nm LP FETs is slightly lower than that of the 90-nm GP ones. Both effects are due to the thicker gate oxide and slightly longer gate lengths of the 65-nm LP process. This behavior is the result of the requirement to reduce gate leakage in LP processes for digital applications [65]. However, gate and subthreshold leakage pose no problem at mm-wave frequencies and in high-speed digital CML gates, where the tail current far exceeds the leakage currents [66].

The simulated S-parameter of the 90-nm differential NMOS TIA are illustrated in Fig. 3.26. The 3-dB bandwidth of the circuit after extraction of layout parasitics is 29 GHz. The amplifier also has 2 dB of gain at 40 GHz, which is sufficient to deliver the sampling clock at the input of the latches. In comparison to a 40-GHz TIA in 0.18-\( \mu \)m SiGe BiCMOS [67] having 757 \( \mu V_{RMS} \) input referred voltage noise simulated over
3.3. Blocks implemented in CMOS

Table 3.1: Comparison of TIA Topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>90-nm GP NMOS (Fig. 3.23(b))</th>
<th>65-nm LP NMOS (Fig. 3.23(b))</th>
<th>65-nm LP CMOS (Fig. 3.23(c))</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W$ (µm)</td>
<td>80</td>
<td>50</td>
<td>20</td>
</tr>
<tr>
<td>$R_F$ (Ω)</td>
<td>180</td>
<td>200</td>
<td>170</td>
</tr>
<tr>
<td>$L_F$ (pH)</td>
<td>500</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>$I_{DS}$ (mA)</td>
<td>16</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>1.2</td>
<td>1.3</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Figure 3.25: Schematic of 90-nm differential NMOS TIA.

40 GHz, the 90-nm differential NMOS TIA has 442 $\mu V_{RMS}$ noise simulated over the same 40-GHz bandwidth. This is an indication of the lower noise capabilities of the CMOS technology as discussed previously in this chapter. The simulated S-parameter response of the 65-nm TIAs are shown in Fig. 3.27. Simulation predicts 48 GHz and 51 GHz of bandwidth for the NMOS and CMOS TIAs, respectively, but these results were simulated at the schematic level in the absence of a parasitic extraction tool for the 65-nm LP technology. The large bandwidth of the CMOS TIA reflects in the simulated eye diagram of Fig. 3.28. At 40 Gb/s the output voltage swing is 350$mV_{pk−pk}$.

As presented before, the TIA performance is based on low-noise bias with concurrent impedance matching. The design technique can be summarized in the form of a logarithmic design methodology, which gives the lowest NF for any topology. The noise factor of a TIA with resistive feedback can be expressed as [68]
Figure 3.26: Simulated S-parameters of differential TIA in 90-nm CMOS after extraction of parasitics.

Figure 3.27: Simulated S-parameters of (a) NMOS and (b) CMOS TIA in 65 nm CMOS. Extraction of parasitics not available in 65-nm CMOS design kit.
3.3. Blocks implemented in CMOS

Figure 3.28: Simulated output eye diagram at 40 Gb/s of CMOS TIA in 65 nm CMOS with 200 mV_{pp} input and (2^7 - 1)-bit pattern. Extraction of parasitics not available in 65-nm CMOS design kit.

\[
F(Z_O) = 1 + R_n Z_O \left| \frac{Y_{COR}}{Z_O} + \frac{1}{Z_O} \frac{1 - j\omega_{o,TIA}}{R_F 1 + \omega_{o,TIA}^2} \right|^2 + Z_O G_n + \frac{Z_O}{R_F} \frac{1}{1 + \omega_{o,TIA}^2} \quad (3.33)
\]

where

\[
\omega_{o,TIA} = \frac{\omega L_F}{R_F} \quad (3.34)
\]

and \( Z_O \) the source impedance. The NF expression of the TIA depends strongly on the noise parameters of the amplifier, which are a function of the device size and geometry. In (3.33), \( R_n, G_n, \) and \( Y_{COR} = G_{COR} + jB_{COR} \) are the noise resistance, conductance, and correlation admittance, respectively, of the transistor realizing the main amplifier. The four main noise parameters \( (R_n, G_n, G_{COR} \text{ and } B_{COR}) \) depend on technology constants \( G, R, G_C \) and \( B \) as follows [69]

\[
R_n = \frac{R}{W} \quad (3.35)
\]

\[
G_n = G\omega^2 W \quad (3.36)
\]

\[
G_{COR} = G_C\omega W \quad (3.37)
\]

\[
B_{COR} = B_C\omega W. \quad (3.38)
\]
At any frequency $\omega$, (3.33) has an optimum device size $W_{OPT}$ that gives the minimum noise factor. The value of $W_{OPT}$ can be found by solving

$$\left. \frac{\partial F(Z_O)}{\partial W} \right|_{\omega=\omega_{3dB}} = 0.$$  (3.39)

The optimal gate width that gives the minimum noise of the amplifier at frequency $\omega$ is [68]

$$W_{OPT} = \frac{1}{\omega} \left[ \frac{1}{Z_O} + \frac{1}{R_F} \frac{1}{1 + \omega_{o,TIA}^2} \right] \sqrt{\frac{1}{G_R + G_{C}} + B^2}.$$  (3.40)

When $W = W_{OPT}$, the TIA achieves the minimum noise. The previous discussion can be summarized in the following steps:

1. Bias MOSFET at minimum noise current density of 0.15mA/µm.
2. Find loop gain $A$.
3. Set feedback resistor $R_F$ for 50-Ω input matching.
4. Size transistor size (gate width) for low-noise, using (3.40).
5. Add feedback inductor to increase bandwidth and filter high-frequency noise.

Figure 3.29 shows the simulated $NF_{50}$, when varying the device size in a CMOS TIA. The optimum size is the same at all frequencies and does not depend on the channel length. The simulation was performed in three different design kits from two foundries. In the 65-nm node, the optimum size is around 30 µm, but $NF_{50}$ does not significantly degrade from its minimum value when $W = 20\mu m$. The latter size was selected for the CMOS TIA to further reduce the power dissipation without significantly increasing $NF$. 
3.3. Blocks implemented in CMOS

Figure 3.29: Simulated NF50 of CMOS TIA vs device size in three technology nodes. The total finger width corresponds to the size on the nMOSFET device.
Chapter 4

Measured Building Block Performance

This chapter presents the measured performance of the ADC building blocks analyzed previously. The test structures that were fabricated are the loop filter in 0.13-µm SiGe BiCMOS, the quantizer in 90-nm CMOS and the broadband amplifiers in 90-nm and 65-nm CMOS. First, small signal, large signal and noise measurements of the loop filter breakout are analyzed. Next, the 40-Gb/s operation of the CMOS single-bit quantizer is presented. A comparison is made with the SiGe BiCMOS version to investigate the benefits of porting the design to CMOS. The last part of this chapter focuses on the measured results from the broadband TIAs and the benefits of each topology compared to a SiGe TIA implementation.

4.1 Bandpass Filter in SiGe BiCMOS

The fourth order loop filter of Fig. 3.5 was fabricated in the 0.13-µm SiGe BiCMOS technology with HBTs having 150-GHz $f_T$. The chip shown in Fig. 4.1 measures 0.5×1.1 mm$^2$ and consumes 115 mW from a 2.5 V power supply. Single-ended S-parameter, $NF$ and differential $P_{1dB}$ and $IP3$ measurements were performed on wafer on the separate filter test structure, identical to the one used in the ADC. S-parameters were measured in a single-ended setup with a Wiltron 360B VNA, as in Fig. 4.2. Figure 4.3 illustrates the tunability of the filter for two varactor control voltages $V_{TUNE} = 0$ and 2.5 V. The measured low gain is due to the 50-Ω loading of the test setup. When employed inside the ADC, the filter will be loaded by a larger impedance. Compared to the simulation
Figure 4.1: Die photo of two-stage loop filter in 0.13µm SiGe BiCMOS.

Figure 4.2: Test setup for S-parameter measurements of ADC loop filter.
4.1. Bandpass Filter in SiGe BiCMOS

(a) $S_{21}$ and $S_{22}$ from 1-3 GHz.  
(b) $S_{21}$ around the passband.

Figure 4.3: Measured $S_{21}$ and $S_{22}$ of the ADC loop filter test structure.

Figure 4.4: Simulated and measured $S_{21}$ of the ADC loop filter test structure.
Figure 4.5: Test setup for noise measurements of ADC loop filter.

Figure 4.6: Measured $NF_{50}$ and $NF_{MIN}$ of the filter test structure.
of Fig. 3.8, the measured gain in the passband of the filter is about 2 dB lower, as can be seen in Fig. 4.4. The difference in gain between simulation and measurement at 1 GHz is 6 dB. Noise measurements were performed with a Focus Microwaves source-pull setup, illustrated in Fig. 4.5. The minimum value of the measured $NF_{MIN}$ is 2.29 dB at 2 GHz (Fig. 4.6).

To measure the linearity of the filter, the differential setup of Fig. 4.7 was used. A power combiner adds the two single-tone signal centered around 2 GHz. A 180° hybrid performs the single-ended to differential conversion. Special care must be taken so that the differential signals arrive at the inputs INP and INN with exactly 180° offset. The delay from the cables and connectors must be the same for both paths. Although the delay of each path can be made equal at 2 GHz, it is impossible to perform off-chip single-ended to differential conversion at mm-wave frequencies. As can be seen in Fig. 4.8, the maximum value of the differential $P_{1dB, out}$ is 0.5 dBm and occurs at 0.4 mA/$\mu$m current density, which coincides with the flat region of the transistor $g_m$-$I_{DS}$ transfer characteristic. Figure 4.9 reproduces the $P_{1dB}$ measurement at the peak-$g_m$ bias. The differential IIP3 and OIP3 of the filter are -0.5 dBm and 9 dBm, respectively, as can be found in Fig. 4.10. The ADC linearity is expected to be better than that of the loop filter test structure because of the feedback network.
Chapter 4. Measured Building Block Performance

Figure 4.8: Measured filter linearity and $g_m$ of nMOSFET vs current density.

Figure 4.9: Measured $P_{1dB}$ of the filter test structure.
4.2 40-GHz Quantizer in CMOS

The decision circuit was fabricated in two different 90-nm CMOS processes to investigate the portability of the design across foundries. All transistor sizes are identical and the passive components have the same value (R and L) in both technologies. Both dies (Fig. 4.11) occupy 800×600 \mu m^2 including the pads.

The circuits were tested on wafer with 67-GHz single-ended and differential probes using the test setup of Fig. 4.12. In the absence of a full-fledged 40-Gb/s bit error rate tester (BERT), the 40-Gb/s pseudorandom binary sequence (PRBS) data were generated by multiplexing four appropriately shifted pseudorandom streams at 10 Gb/s each. The external clock was provided by a low phase noise Agilent E8257D PSG signal source and data were captured by an Agilent Infiniium DCA-86100C oscilloscope with 70-GHz remote heads, as shown in Fig. 4.13.

It should be noted that contributions from the test setup and oscilloscope have not been de-embedded from the measured jitter, amplitude and rise/fall times shown in Figs. 4.14(a)-4.16 and 4.19. Figure 4.14(a) reproduces the input and output eye diagrams at 30 Gb/s and 1.2-V supply, showing a significant reduction in jitter from 1.7 to 0.5 ps rms. The rise/fall times are improved from 14 ps to less than 7 ps (Fig. 4.14(b)). Compared to the decision circuit of [70], where 40-Gb/s operation required \( V_{DD} = 1.5 \) V, an improved clock distribution tree in this design allowed for 40 Gb/s full-rate retiming from 1.2 V (Figs. 4.15 and 4.16). Figure 4.16 illustrates the output eye diagram at 40 Gb/s for
Figure 4.11: Die photo of decision circuit in 90 nm CMOS.

Figure 4.12: Test setup for 40-Gb/s measurements with on wafer probing of retiming flip-flop.
a $4 \times (2^{31} - 1)$ input pattern. The measured phase margin of the latch is $163^\circ$. The resulting bathtub curve at 40 Gb/s can be found in Fig. 4.17. Error-free operation was verified for an input pattern of $4 \times (2^7 - 1) = 508$ bits, by capturing the input and output bitstreams on the sampling scope. Part of the captured bitstream at 40 Gb/s is shown in Fig. 4.18. Power dissipation of the latch and the entire decision circuit at 1.2 V are 10.8 mW and 130 mW, respectively.

The decision circuit was tested across temperature for different supply voltages to verify the robustness of the latch biasing scheme in the absence of current sources. Measurements were conducted for supply voltages between 1 V and 1.5 V and at temperatures up to 100°C. At 1-V supply and 100°C, the maximum rate with retiming and jitter reduction is 32 Gb/s. Figure 4.19 shows the 40-Gb/s eye diagram at 1.2 V and 100°C. Even though no errors were observed in this case, the output jitter is not improved over that at the input, indicating that the clock path does not have enough bandwidth and that the latches do not retime the data.

Table 4.1 compares this circuit to state-of-the-art latches in SiGe BiCMOS and InP technologies. The proposed MOS-CML latch has the lowest power dissipation. At 40 Gb/s the CMOS latch consumes half the power of the 43-Gb/s SiGe BiCMOS latch.
Chapter 4. Measured Building Block Performance

(a) Input (top, channel 4) and output (bottom, channel 3) eye diagrams.

Figure 4.14: Eye diagrams at 30 Gb/s ($V_{DD}$=1.2V, 508-bit pattern).

(b) Output eye diagram

Figure 4.15: Input (top, channel 4) and output (bottom, channel 3) eye diagrams at 40 Gb/s ($V_{DD}$=1.2V, 508-bit pattern).

Figure 4.16: Output eye diagram at 40 Gb/s and 25°C ($V_{DD}$=1.2V) with $2 \times 255mV_{pp}$ output swing for a $4 \times (2^{31} - 1)$ input pattern.
4.2. 40-GHz Quantizer in CMOS

Figure 4.17: Bathtub curve of output at 40 Gb/s and 25°C (V_{DD}=1.2V, 508-bit pattern).

![Bathtub curve](image1)

Figure 4.18: Input (top) and output (bottom) signals for a 508-bit pattern at 40 Gb/s and 25°C (V_{DD}=1.2V, 508-bit pattern).

![Input and output signals](image2)

Figure 4.19: Input (top, channel 4) and output (bottom, channel 3) eye diagrams at 40 Gb/s and 100°C (V_{DD}=1.2V, 508-bit pattern).

![Eye diagrams](image3)
Table 4.1: Comparison of high-speed latches in decision circuits

<table>
<thead>
<tr>
<th>Ref</th>
<th>Technology</th>
<th>Rate (Gb/s)</th>
<th>Supply (V)</th>
<th>$P_{\text{latch}}$ (mW)</th>
<th>Area ($\mu m^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[57]</td>
<td>245-GHz InP HEMT</td>
<td>80</td>
<td>5.7</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>[58]</td>
<td>150-GHz InP HBT</td>
<td>50</td>
<td>1.5</td>
<td>20</td>
<td>N/A</td>
</tr>
<tr>
<td>[56]</td>
<td>150-GHz SiGe BiCMOS</td>
<td>43</td>
<td>2.5</td>
<td>20</td>
<td>55$\times$63</td>
</tr>
<tr>
<td>[59]</td>
<td>120-GHz SiGe HBT</td>
<td>43</td>
<td>3.3</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>This work</td>
<td>120-GHz CMOS</td>
<td>40</td>
<td>1.2</td>
<td>10.8</td>
<td>100$\times$80</td>
</tr>
</tbody>
</table>

4.3 Broadband Transimpedance Amplifiers in CMOS

The NMOS TIA with PMOS active load (Fig. 3.23b) was fabricated in 90-nm GP and 65-nm LP CMOS technologies. The CMOS inverter TIA (Fig. 3.23c) was fabricated in the 65-nm LP technology. The values of the transistor total gate width $W$, feedback resistor $R_F$, and inductor $L_F$ can be found in Table 3.1 of chapter 3. In all cases, the core TIA stage is followed by a buffer, which drives the signal to the external 50-$\Omega$ load. The differential TIA in 90-nm CMOS, shown in Fig. 4.20, measures $600\times470\mu m^2$. Both single-ended TIA versions in 90-nm and 65-nm of Fig. 4.21 occupy $420\times350\mu m^2$. The die photo of the 65-nm CMOS TIA is reproduced in Fig. 4.22. The circuit occupies an area of $300\times370\mu m^2$ including the pads. The core area of the TIA is $85\times65\mu m^2$ and the 600-$\mu$H inductor has a diameter of 10 $\mu$m with 0.5 $\mu$m metal width and is realized in the top three metal layers of the process. S-parameter, eye diagram and noise measurements were performed on wafer.

The measured S-parameters of the differential TIA in 90-nm CMOS are illustrated in Fig. 4.23. The DC gain ($S_{21}$) and 3-dB bandwidth of the circuit are 7 dB and 26 GHz, respectively, when the circuit is biased from 1 V. Compared to 8 dB of gain and 29 GHz of bandwidth in simulation after parasitic extraction, these results are in good agreement. Due to the higher threshold voltage of the 65-nm LP MOSFETs compared to the GP technology (Fig. 3.24), and therefore the larger $V_{GS}$ required for maximum gain and lowest noise [45], the supply voltage $V_{DD} = V_{GSn} + V_{SGp}$ of the TIA exceeds
Figure 4.20: Die photo of differential NMOS TIA in 90 nm CMOS.

(a) Die photo of NMOS TIA in 90 nm CMOS.  
(b) Die photo of NMOS TIA in 65 nm LP CMOS.

Figure 4.21: Fabricated NMOS TIA in 90 nm GP and 65 nm LP CMOS.
Figure 4.22: Die photo of CMOS TIA in 65 nm LP CMOS.

Figure 4.23: Measured S-parameters of differential NMOS TIA in 90 nm CMOS.

Figure 4.24: Measured S-parameters of CMOS TIA in 65 nm LP CMOS.
4.3. Broadband Transimpedance Amplifiers in CMOS

Figure 4.25: Measured $S_{21}$ of NMOS and CMOS TIAs in 65 nm LP CMOS.

Figure 4.26: Measured $NF_{MIN}$ vs drain current density for a single-ended 90-nm NMOS TIA at 10, 18, and 26 GHz.

Figure 4.27: $NF_{MIN}$ and $NF50$ at 10 GHz of CMOS TIA in 65 nm LP CMOS for different bias voltages.
Figure 4.28: $NF_{50}$ and $NF_{MIN}$ vs frequency of NMOS TIAs in 90 nm and 65 nm and CMOS TIA in 65 nm. Measurements taken at minimum noise bias. The 65 nm TIAs were fabricated in the LP CMOS process.

1.3 V. The measured S-parameters of the 65-nm CMOS TIA are provided in Fig. 4.24. The 3-dB bandwidth of the 65-nm CMOS and NMOS TIAs is 23 GHz and 21 GHz (Fig. 4.25), respectively, from 1.5-V power supplies. We also note that the 65-nm NMOS TIA has lower bandwidth while operating from higher supply voltages than its counterpart implemented in 90-nm GP CMOS.

Noise parameter measurements were performed up to 26 GHz with a Focus Microwaves system. To verify the low-noise bias scheme of 0.15 mA/µm, the noise parameters of single-ended NMOS TIA in 90-nm were measured as a function of current density. Figure 4.26 clearly demonstrates that the lowest value of $NF_{MIN}$ occurs between 0.15-0.20 mA/µm, irrespective of frequency. The $NF_{MIN}$ and $NF_{50}$ of the CMOS TIA is presented in Fig. 4.27 for various $V_{GS} = V_{DD}/2$ voltages. Figure 4.28 illustrates the $NF_{MIN}$ vs frequency of all 90-nm and 65-nm TIAs. Despite its lower current, the CMOS TIA has lower $NF_{50}$ due to its lower noise resistance $R_n$ and because the real part of its optimum noise impedance $R_{S_{opt}}$ is closer to 50Ω. All the implementations in 90-nm and 65-nm CMOS have lower $NF$ (Fig. 4.29) compared to the SiGe BiCMOS TIA in [46], because the $NF_{MIN}$ of the MOSFET is lower than that of the HBT.

Eye diagrams were measured for all TIA circuits with $4 \times (2^7 - 1) = 508$ bits and $4 \times (2^{31} - 1)$ bits pseudo random sequences having $100mV_{pp}$ amplitude. The output eye diagrams of the 90-nm differential NMOS TIA at 25 Gb/s and 38.8 Gb/s are shown in Fig. 4.30. The output eye diagrams of the 65-nm amplifiers at 37-Gb/s are illustrated in Figs. 4.31(a) and 4.31(b). The bandwidth improvement is apparent in the eye diagrams,
4.3. Broadband Transimpedance Amplifiers in CMOS

Figure 4.29: $NF_{50}$ vs frequency of different broadband amplifier topologies in 0.13 $\mu$m SiGe BiCMOS, 90 nm GP and 65 nm LP CMOS. The 65 nm TIAs were fabricated in the LP CMOS process.

Figure 4.30: Output eye diagram at (a) 25 Gb/s and (b) 38.8 Gb/s of differential NMOS TIA in 90 nm CMOS with 100 mV$_{pp}$ input and 508-bit pattern.
Figure 4.31: Output eye diagram at 37 Gb/s of (a) NMOS TIA and (b) CMOS TIA in 65 nm LP CMOS with 100 mV$_{pp}$ input and 508-bit pattern.

Figure 4.32: Output eye diagram at 40 Gb/s of CMOS TIA in 65 nm CMOS with 100 mV$_{pp}$ input and $4 \times (2^{31} - 1)$ pattern.
with the CMOS TIA having a larger eye opening. The better frequency response of the CMOS inverter TIA allowed for 40-Gb/s operation as shown in Fig. 4.32. For a power consumption of 6 mW in its gain stage, the circuit achieves 0.15 mW/Gb/s, while having a noise figure lower than 9 dB with 6 dB gain.

The 65-nm TIA experiments prove that, in a given technology node, the CMOS inverter TIA has lower noise figure, higher gain and larger bandwidth, while consuming less than half the power of a NMOS TIA. The 40-Gb/s CMOS TIA also consumes less power than common-gate TIAs [71], [72]. However, when comparing the performance of the same NMOS TIA topologies in 90-nm GP and 65-nm LP technologies we find that, despite the lower metal pitch and area, the 65-nm LP circuits suffer from higher noise, lower bandwidth and dissipate more power than the 90-nm GP ones. Table 4.2 provides a comparison between the TIA topologies developed in this work and a SiGe BiCMOS TIA from [46], which is also biased for low noise. The CMOS inverter TIA has the lowest power dissipation and $NF$, despite being fabricated in a slower technology than the SiGe TIA with EF. Overall, the TIAs in nanoscale CMOS have lower noise than the SiGe TIA, proving that CMOS performs better in terms of noise, so long as the devices are biased in their low-noise current density region of 0.15 mA/µm.
Table 4.2: Comparison of TIA measured performance in SiGe BiCMOS and CMOS

<table>
<thead>
<tr>
<th>Topology</th>
<th>90-nm NMOS (Fig. 3.23b)</th>
<th>65-nm NMOS (Fig. 3.23b)</th>
<th>65-nm CMOS (Fig. 3.23c)</th>
<th>0.13-µm SiGe BiCMOS TIA with EF ( [46])</th>
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<td>50</td>
<td>20</td>
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<td>600</td>
<td>600</td>
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<td>10</td>
<td>4</td>
<td>4</td>
</tr>
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<td>29</td>
<td>40</td>
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<td>8</td>
<td>7.8</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
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<td>1.3</td>
<td>1.5</td>
<td>2.5</td>
</tr>
<tr>
<td>$P$ (mW)</td>
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<td>13</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td>$NF_{50@26GHz}$ (dB)</td>
<td>7.7</td>
<td>9.75</td>
<td>6.96</td>
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</tr>
</tbody>
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Chapter 5

Implementation of 2-5 GHz Digital Receivers

This chapter discusses the performance of two tunable bandpass digital $\Delta\Sigma$ receivers centered at 2 GHz and 5 GHz in SiGe BiCMOS. Each receiver consists of a continuous-time bandpass $\Delta\Sigma$ ADC integrated with a 40-GHz VCO/PLL. First, the measured behavior of a standalone ADC centered at 2 GHz is analyzed. Next, characterization results of the digital receivers are presented. The impact of clock jitter and center frequency scaling on the ADC resolution is studied through the analysis of measured SNR data at the two center frequencies. The last section of this chapter provides a performance summary and comparison to state-of-the-art GHz-sampling ADCs.

5.1 ADC Performance at 2 GHz

As mentioned in chapter 2, the continuous-time $\Delta\Sigma$ ADC performance is a function of the loop filter $Q$ and the jitter of the sampling source. To investigate the feasibility of mm-wave $\Delta\Sigma$ ADCs and study the non-idealities that limit their performance, an ADC clocked with an external source was fabricated and tested in SiGe BiCMOS.

The top level diagram of Fig. 5.1 shows the placement of the SiGe building blocks inside the ADC and the allocation of power. The $\Delta\Sigma$M comprises a 2-GHz loop filter (Fig. 3.5), two RZ DACs (Fig. 3.13) and a master-slave-master D-type flip-flop (Fig. 3.15). The closed loop simulation at the transistor level of the entire circuit, after parasitic extraction is illustrated in Fig. 5.2. The circuit must be simulated over a large number of clock cycles to accurately predict the quantization noise levels [20], but the required time
and amount of generated data makes such a simulation prohibitive at 40-GHz sampling rates. The simulation period for 32768 samples is 0.82 $\mu$s. The spectrum at the output of the driver is plotted for an input power of -10 dBm and 32768 FFT points. The simulated SNR of 51 dB is calculated over a bandwidth of 60 MHz.

The circuit was implemented in a 0.13-µm SiGe BiCMOS process and occupies $1.52 \times 1.58$ mm$^2$. The ADC dissipates 1.6 W from a 2.5-V power supply. The chip microphotograph is shown in Fig. 5.3. S-parameter, eye diagram and power spectrum measurements of the ADC were performed on wafer using 65-GHz GGB probes. The test setups for the ADC S-parameter and large signal measurements are described in Figs. 5.4 and 5.5. The measured single-ended $S_{21}$ and $S_{22}$ of the ADC from DC-65 GHz are shown in Fig. 5.6(a). Figure 5.6(b) illustrates the measured $S_{21}$ and $S_{22}$ in the passband of the ADC without applying a clock signal to the circuit. Instead, a DC signal was applied at the clock input of the circuit to switch the latches to one side and put them in transparent mode. This way the main path of the ADC (loop filter and latches) can be measured. The filter $Q$ is 17.5 and the 3-dB bandwidth is 120 MHz. Although this measurement is a characterization of the loop filter rather than the full ADC, it is useful to determine the $Q$ that sets the quantization noise floor of the closed loop system.

Large signal measurements were conducted by directly connecting one differential output of the circuit to a 50-GHz Agilent E4448A spectrum analyzer (PSA) and the other output to an Agilent Infiniium DCA-86100C oscilloscope with 70-GHz remote heads. The
5.1. ADC Performance at 2 GHz

Simulated ADC spectrum ($N_{FFT} = 32768$).

The clock signal was provided from a low phase noise Agilent E8257D PSG signal source and the RF input signals were obtained from Agilent E4422B and 83650B signal sources.

The 40-Gb/s output eye diagram is reproduced in Fig. 5.7 for a 2-GHz input, when the feedback loop is turned off and the analog input is sampled by the quantizer at 40 GS/s. This mode of operation does not fully capture the real effect of clock jitter on the SNR, but provides an upper limit in the modulator performance. The eye jitter is less than 0.375 ps rms. For the measured jitter value $\sigma_t = 0.375\,\text{ps}$ and $OSR = 333$, the SNR limit due to jitter from (2.13) is 71.76 dB. A similar result can be found if the SNR expression accounts for the jitter generated by the feedback DAC in a $\Delta\Sigma$ modulator [73], whose input peak voltage is $V_{IN}$ and its DAC switches at an average rate of $F_{DAC}$ (assumed equal to $F_S/2$). Assuming that the jitter in closed loop remains the same, the SNR is

$$SNR = 10 \log_{10} \frac{V_{IN}^2 \text{OSR}}{\Delta^2 F_{DAC}^2 \sigma_t^2} = 70.22\,\text{dB};$$

indicating that the dominant source of in-band noise is quantization noise and that the ADC is not close to the theoretical jitter limit [14].

Figure 5.8 shows the measured $\Delta\Sigma$ ADC output spectrum with and without an input sinusoidal signal at 2 GHz. Losses in the test setup have not been de-embedded. The loop remains stable in the absence of the input signal and maintains its noise shaping, despite the finite $Q$ of the resonators [15]. The noise shaping in the lower part of the spectrum is $>35$ dB/decade, as displayed in the inset. The theoretical noise shaping of a fourth order bandpass loop is 40 dB/decade. The inset is obtained by shifting the
spectrum to 0 GHz, flipping it along the vertical axis and plotting on a log scale.

The SNR was found from the measured power spectrum by integrating the noise around the input signal over the bandwidth of interest using the built-in integration function of the PSA. To accurately measure the SNR, the resolution bandwidth of the PSA was lowered until the noise floor remained constant. The noise floor obtained in this manner represents the quantization noise from the ADC. The noise at the ADC output integrated over 10 MHz band centered at 2 GHz is -73 dBm, as depicted in Fig. 5.9 (top trace). When the feedback is turned off, the circuit and thermal noise contributions are below the -83 dBm (-153 dBm/Hz) sensitivity of the spectrum analyzer (Fig. 5.9, bottom trace), indicating that quantization noise is the main limitation in the circuit. The output vs input power transfer characteristic at 2-GHz is reproduced in Fig. 5.10. The single-ended SNR is plotted as a function of input power for 10-MHz, 60-MHz and 120-MHz bandwidths in Fig. 5.11(a). The ADC achieves SNR values of 63 dB, 55 dB and 52 dB over 10 MHz, 60 MHz and 120 MHz, respectively, for a single tone at 2 GHz. The measured peak SNR as a function of bandwidth can be found in Fig. 5.11(b). The simulated SNR (Fig. 5.2) has 32768 samples, corresponding to an FFT bin of 1.22 MHz, 100 times larger than the PSA resolution bandwidth. As can be seen in Fig. 5.9, the ADC passband has an approximately flat noise distribution. The SNR can be further improved by adding cross-coupled negative resistance cells across the filter tanks to increase their $Q$ [16]. However, this option should be carefully analyzed as high-$Q$ circuits suffer from
Figure 5.4: Test setup for ADC S-parameter measurement of the main path.
Figure 5.5: Test setup for ADC time domain dynamic range measurements.
5.1. ADC Performance at 2 GHz

Figure 5.6: Measured ADC single-ended S-parameters.

(a) $S_{21}$ and $S_{22}$ from DC-65 GHz.

(b) $S_{21}$ and $S_{22}$ around the ADC passband.

Figure 5.7: Measured output eye diagram at 40 Gb/s.
Figure 5.8: Measured ADC output spectrum with (top) and without (bottom) a 2-GHz input sinusoid.
5.1. ADC Performance at 2 GHz

Figure 5.9: Measured noise floor at the ADC output (top trace). The noise floor of the ADC drops from -73 dBm to -83.45 dBm (bottom trace) when the feedback is off, indicating that quantization noise is limiting the ADC.

Figure 5.10: Measured output vs input power of the ADC for 2-GHz input.

low linearity, high noise and instability.

The single-ended IIP3 = +4 dBm, $P_{1dB} = -4$ dBm, and SFDR = 61 dB of the entire ADC were obtained from two-tone measurements with 10-MHz spacing, as shown in Figs. 5.12 and 5.13. The ADC linearity is better than that of the filter test structure discussed in chapter 4 due to the application of feedback. From the measured $P_{1dB}$ value and noise floor of Fig. 5.10, the dynamic range (DR) of the receiver over 60 MHz, is 53 dB.
Figure 5.11: Measured (a) dynamic range, and (b) peak SNR vs bandwidth for a 2-GHz single tone input.

Figure 5.12: Measured ADC two-tone spectra at 2 GHz with $P_{IN} = -35 \text{ dBm}$. 
5.2 Digital Receivers at 2 GHz and 5 GHz

To fully investigate the possibility of a mm-wave direct sampling receiver without the need for an external sampling clock source, the continuous-time bandpass ∆Σ ADC was integrated with a 40-GHz PLL. In addition to the increased functionality compared to the standalone ADC in Fig. 5.1, the 40 GS/s ADC with on-chip PLL features the bandpass filter topology of Fig. 3.10 leading to lower noise and higher linearity. As a result, the receiver resolution is improved by approximately 6 dB over the ADC of the previous section, approaching 60 dB over a 60 MHz band centered at 2 GHz. More importantly, by testing the chip with clock signals generated both on-chip and externally, it is demonstrated that the jitter of the on-chip VCO and PLL does not limit performance.

In the system level analysis of continuous-time bandpass ∆Σ ADCs presented in chapter 2, it was found that a tunable receiver suffers significant loss of resolution when the center frequency is scaled. To analyze this interesting phenomenon, a receiver was also designed at 5 GHz. Compared to the 2-GHz receiver, the 5-GHz version employs the loop filter of Fig. 3.11 and two latches in the flip-flop to maintain stability in the presence of loop delay, as discussed in section 2.5.

The system level block diagram of the 2-5 GHz receivers is shown in Fig. 5.14. The digital part and clock generation unit are identical in both cases, with the exception of having a master-slave instead of a master-slave-master D-type flip-flop in the 5-GHz version. The center frequency can be tuned from an external power control voltage. The 40-GHz sampling clock is generated by an integer-N PLL [46], with $N = 16$, and employ-
Chapter 5. Implementation of 2-5 GHz Digital Receivers

Figure 5.14: System level block diagram of the digital receiver with ΔΣ ADC and PLL.

ing a Colpitts VCO [56] and a 2.5-GHz external reference. Figure 5.15 reproduces the schematics of the phase frequency detector (PFD), charge pump (CP) and asynchronous resettable latch. The AND gate inside the PFD is shown in Fig. 5.16. A selector allows the chip to be operated either with the internal or with an external clock in order to study the impact of PLL jitter on receiver resolution.

The digital receivers were implemented in a production 0.13-µm SiGe BiCMOS technology described before. The chips shown in Figs. 5.17 and 5.18 occupy an area of 1.58×2.39 mm² including the pads. All measurements were performed on wafer.

When operating in the receiver chips, the PLL phase noise is -80 dBc/Hz at 100 kHz offset from the 39.7-GHz clock (Fig. 5.19). The corresponding histogram measurement in the time domain (Fig. 5.20) shows that the 40-GHz PLL signal has 848 fs of rms jitter. For this measured jitter value \( \sigma_t = 0.848 \) ps and \( OSR = 333 \), the SNR limit due to jitter (5.1) is

\[
SNR = 10 \log_{10} \frac{V_{IN}^2 \cdot OSR}{\Delta^2 \cdot F_{DAC}^2 \cdot \sigma_t^2} = 64dB.
\]  

The measured spectrum around 2 GHz at the receiver output is reproduced in Figs. 5.21 and 5.22 when the ADC is clocked by the PLL and the external source, respectively. The 2.5-GHz feedthrough signal poses no problems because it falls outside the receiver bandwidth and is an artifact of the wafer probing setup where the external PLL reference is applied through a pad adjacent to the receiver output pads.

To measure the forward path of the 5-GHz ADC and find the \( Q \) of its filter in the
5.2. Digital Receivers at 2 GHz and 5 GHz

Figure 5.15: Circuit schematic of the PFD, CP and asynchronous resettable latch in the PLL.

Figure 5.16: Circuit schematic of the AND gate in the PLL.
Figure 5.17: Die photo of $\Delta\Sigma$ digital receiver centered at 2 GHz.
Figure 5.18: Die photo of $\Delta\Sigma$ digital receiver centered at 5 GHz.
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Figure 5.19: Measured phase noise of PLL at 39.7 GHz.

Figure 5.20: Histogram measurement of PLL signal at 40 GHz.
5.2. Digital Receivers at 2 GHz and 5 GHz

Figure 5.21: Measured spectrum of digital receiver for a -10 dBm input tone at 2 GHz and on-chip 40-GHz clock. The tone at 2.5 GHz is the feedthrough from the external reference signal for the PLL.

absence of a separate breakout, the S-parameter test setup of Fig. 5.4 was employed. The \( NF \) of the main path (filter and flip-flop) was measured with an Agilent 8975A NFA and 6-dB ENR noise source by setting the latches to transparent mode and disabling the feedback. This mode allows to measure the small signal response of the filter followed by a wideband buffer consisting of the latches and driver. The bandpass filter response is plotted in Fig. 5.24 for three values of the varactor tuning voltage \( V_{TUNE} \). The maximum gain is 23.25 dB at 5.5 GHz, while the \( NF_{50} \) has its minimum of 9.7 dB at 5.4 GHz. The 3-dB bandwidth of the filter at 4.2 GHz is 320 MHz, resulting in a \( Q \) value of 13. When the filter is tuned to 5.5 GHz, the 3-dB bandwidth and \( Q \) become 400 MHz and 13.8, respectively. The same filter \( Q \) was measured in the NTF response. In comparison, the 2-GHz loop filter has a \( Q \) of 17.5.

The SNR and DR of the receiver were found by integrating the noise around the carrier. A comparison of the integrated noise power over 60 MHz when the 2-GHz receiver is clocked from the on-chip PLL, and when the PLL is turned off and an external clock is applied from a low-noise Agilent E8257D signal source, shows that the noise floor is the same in both cases (-65 dBm/60MHz), proving that clock jitter does not have an measurable impact on performance at this resolution. Quantization noise due to low filter \( Q \) is the dominant noise contributor in the band suggesting that further performance improvement is possible with \( Q \)-enhancement techniques. The 2-GHz receiver has a peak-
Figure 5.22: Measured spectrum of digital receiver for a -5 dBm input tone at 2 GHz and external 40-GHz clock.

SNR of 59.84 dB, a DR of 58.5 dB (Fig. 5.29) and a SFDR of 59 dB (Fig. 5.23) for a bandwidth of 60 MHz. Although the SNR is set by quantization noise, the receiver noise floor approaches the jitter limit, since (5.2) predicts an SNR 4 dB higher than the measured value. This is also captured in the integration of the in-band noise for different PLL bandwidths. As shown in Fig. 5.30, the total noise integrated over 10 MHz increases when the PLL bandwidth becomes larger. Noise from clock jitter becomes significant when the charge pump control voltage $V_{CP}$ exceeds 1.5 V, corresponding to a PLL bandwidth of 20 MHz.

The noise floor in the center of the passband was also the same when the 5-GHz receiver was tested with an external and on-chip clock, as seen in Figs. 5.25 and 5.26. Due to the wider tuning range of the ADC loop filter, it was possible to tune the center frequency from 4.5 GHz to 5.8 GHz, as illustrated in Fig. 5.27. Quantization noise was integrated over a wider bandwidth for the 5-GHz receiver. The measured peak SNR, DR and SFDR are 37.9 dB, 37.2 dB and 48 dB, respectively, over 500 MHz. The captured spectrum at the output of the circuit for a two-tone test is illustrated in Fig. 5.28. The measured dynamic range is plotted in Fig. 5.31. The output vs input power plots of both receivers are reproduced in Fig. 5.32.

Except for clock jitter and quantization noise, the SNR in high-speed converters can be limited by quantizer metastability [15, 74]. If the quantizer is not fast enough to resolve small inputs, the noise floor is raised and the SNR degrades. It has been
stated in [15, 74] that the SNR (in bits) due to metastability can be approximated by
\[ \text{SNR} = 11.5 + 0.5 \log_2 \text{OSR} \]
when \( F_S/f_T < 5\% \) and the input is -8 dBFS. In a \( \Delta \Sigma \) modulator that achieves the maximum SNR closer to the FS level (e.g. -2 dBFS), this expression becomes \( \text{SNR} = 12.5 + 0.5 \log_2 \text{OSR} \) or 16.7 bits for \( \text{OSR} = 333 \). When the clock rate exceeds 6\% of \( f_T \), the SNR is 3 bits lower and drops by another 1 bit for every octave of increase in the ratio \( F_S/f_T \) above the 6\% point. For \( F_S/f_T = 40/150 = 0.26 \), the resolution limit by metastability can be found to be \( \text{SNR} = 13.7 - \log_2 0.26/0.06 = 11.6 \) bits. Compared to the SNR resolution of 9.65 bits in the 2-GHz receiver presented in this work, the simple analysis based on the expressions of [15, 74] shows that the metastability noise contribution is 1.5 bits below the current performance.

Table 5.1 summarizes the performance of the ADC. In comparison to recently-published ADCs (Fig. 5.33), both digital receivers achieve the best FoM using \( (1.11) \)
\[ \text{FoM} = \frac{2^B \times 2BW}{P_{DC}} \]
among the bandpass \( \Delta \Sigma \) designs [17–21] and comparable performance to the lowpass ADCs of [23] and [22], which were implemented in 200-GHz \( f_T \) InP and SiGe HBT technologies, respectively. The 2-GHz receiver performs better than two flash ADCs with sampling rates around 20 GS/s [75, 76] (FoM for the flash ADCs calculated from SNDR in lack of SNR data). The FoMs of the 2-GHz and 5-GHz receiver are 65.5 GHz/W and 30.6 GHz/W, respectively, including the power of the ADC and PLL. It should be
Figure 5.24: Measured gain ($S_{21}$) and $NF$ vs center frequency $f_o$ of the forward path in the 5-GHz receiver.

Figure 5.25: Measured spectrum of digital receiver for an input tone at 5 GHz and on-chip 40-GHz clock. The second harmonic of the 2.5 GHz reference is below the receiver noise floor.
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Figure 5.26: Measured spectrum of digital receiver for an input tone at 5 GHz and external 40-GHz clock.

Figure 5.27: Tunability of digital receiver between 4.5 and 5.8 GHz for a -20 dBm input tone.
Figure 5.28: Measured receiver two-tone spectra at 5 GHz.

Figure 5.29: Measured dynamic range and SNR of 2-GHz receiver.

(a) Dynamic range with on-chip clock. (b) Peak SNR vs bandwidth with on-chip and external clock.
Figure 5.30: Measured noise floor of the digital receiver at 2 GHz vs charge pump control voltage. When $V_{CP} > 1.5\,\text{V}$, the PLL bandwidth exceeds 20 MHz.

Figure 5.31: Measured dynamic range with on-chip clock of 5-GHz receiver.
noted that the FoM is calculated from SNR rather than SNDR data provided in each published ADC. Although the effective number of bits \((\text{ENOB})\) is the standard method of calculating FoM because it takes into consideration the distortion generated by the ADC, all authors of bandpass \(\Delta \Sigma\) ADCs report the measured SNR and the third order intermodulation products (IM3) for signals near the FS level of the modulator. If the SNDR is calculated from the IM3 data of Fig. 5.32, the 2-GHz and 5-GHz receivers achieve 35.2 dB and 22.1 dB when the IM3 products equal the integrated noise power over 60 MHz and 500 MHz, respectively. A comparison of FoM based on SNDR between the 2-GHz receiver of this work and two flash ADCs [75, 76] can be found in Table 5.2.

If the \(f_T\) of each technology used for the fabrication of ADCs is considered, then the FoM changes to

\[
\text{FoM}_{f_T} = \frac{2^B \times 2BW}{f_T P_{DC}}. \tag{5.4}
\]

The comparison based on (5.4) and shown in Fig. 5.34 reveals that the 2-GHz receiver of this work has almost the same performance as the ADCs in [21, 75]. The FoM of the receivers at 2 GHz and 5 GHz is 0.44 1/W and 0.2 1/W, respectively.

The FoM definition of (1.11), however, contains no information about the center frequency, where the bandpass \(\Delta \Sigma M\) is centered at. It is important to capture the effect of center frequency scaling, since it degrades the performance, as has been proven in this thesis. Therefore, a modified FoM is proposed, which is equal to (5.3) multiplied by the center frequency \(f_o\).
Table 5.1: Performance summary of ∆Σ digital receivers in SiGe BiCMOS

<table>
<thead>
<tr>
<th>Center Frequency</th>
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<th>5 GHz</th>
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<tr>
<td>Clock Rate</td>
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<td>40 GHz</td>
</tr>
<tr>
<td>OSR</td>
<td>333</td>
<td>40</td>
</tr>
<tr>
<td>SNR</td>
<td>59.8 dB / 60 MHz</td>
<td>37.9 dB / 500 MHz</td>
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<tr>
<td>SNDR</td>
<td>35.2 dB / 60 MHz</td>
<td>22.1 dB / 500 MHz</td>
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<tr>
<td>SFDR</td>
<td>59 dB</td>
<td>48 dB</td>
</tr>
<tr>
<td>$P_{1dB}$</td>
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<td>-13.5 dBm</td>
</tr>
<tr>
<td>DR</td>
<td>58.5 dB</td>
<td>37.2 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2.19 W</td>
<td>2.09 W</td>
</tr>
<tr>
<td>Power Supply</td>
<td>2.5 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Chip Area</td>
<td>1.59 × 2.39 mm$^2$</td>
<td>1.59 × 2.39 mm$^2$</td>
</tr>
<tr>
<td>FoM</td>
<td>65.5 GHz/W</td>
<td>30.6 GHz/W</td>
</tr>
<tr>
<td>$1/FoM$</td>
<td>15.3 pJ/bit</td>
<td>32.7 pJ/bit</td>
</tr>
<tr>
<td>FoM2</td>
<td>131 GHz$^2$/W</td>
<td>153 GHz$^2$/W</td>
</tr>
</tbody>
</table>

1 Measured at $P_{IN}$ = -45.80 dBm
2 Measured at $P_{IN}$ = -43.25 dBm

Table 5.2: Comparison of ADC performance based on SNDR

<table>
<thead>
<tr>
<th>Reference</th>
<th>$f_O$ (GHz)</th>
<th>$F_S$ (GHz)</th>
<th>FoM (GHz/W)</th>
</tr>
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<tr>
<td>[Schvan, ISSCC2006] (Flash)</td>
<td>-</td>
<td>22</td>
<td>53.0</td>
</tr>
<tr>
<td>[Poulton, ISSCC2003] (Flash)</td>
<td>-</td>
<td>20</td>
<td>29.1</td>
</tr>
<tr>
<td>This work (ΔΣ ADC and PLL)</td>
<td>2</td>
<td>40</td>
<td>5.2</td>
</tr>
<tr>
<td>This work (ΔΣ ADC and PLL)</td>
<td>5</td>
<td>40</td>
<td>5.0</td>
</tr>
</tbody>
</table>

$$FoM2 = \frac{2^B \times 2BW \times f_o}{P_{DC}}.$$  \hspace{1cm} (5.5)

Figure 5.35 compares the FoM2 of the continuous-time bandpass ∆Σ ADCs from Fig. 5.33. The 5-GHz receiver now outperforms the other designs with 153 GHz$^2$/W, as opposed to 131 GHz$^2$/W for the 2-GHz version.
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Figure 5.33: FoM comparison of state-of-the-art ADCs with GHz-sampling clocks.

Figure 5.34: FoM/$f_T$ comparison of state-of-the-art ADCs with GHz-sampling clocks.
5.2. Digital Receivers at 2 GHz and 5 GHz

Figure 5.35: Modified FoM comparison of continuous-time bandpass ΔΣ ADCs with GHz-sampling clocks.
Chapter 6

Conclusion

This thesis presented the design and implementation of bandpass tunable $\Delta \Sigma$ digital receivers in SiGe BiCMOS for wireless radio applications. The continuous-time bandpass $\Delta \Sigma$ ADC of the receiver is able to digitize RF signals at 2 GHz and 5 GHz without requiring any analog downconversion stage. A new design methodology of the $\Delta \Sigma$ loop in continuous-time has been proposed to analyze stability and accurately estimate the SNR as a function of the filter $Q$ and the center frequency of the bandpass loop. This theoretical analysis, which is supported by measured results set the link between center frequency scaling and resolution. Two receivers at 2-GHz and 5-GHz consisting of a $\Delta \Sigma$ ADC and PLL achieved an SNR of 59.8 dB over 60 MHz and 37.2 dB over 500 MHz, respectively. Experimental data proved that the dominant limitation is quantization noise, rather than the jitter of the clock source. An investigation of porting the high-speed blocks of the ADC into nanoscale CMOS technologies demonstrated that significant power savings can be attained. Specifically, it was shown that a CMOS latch can operate at 40-Gb/s with only half the power compared to SiGe BiCMOS. Broadband amplifiers were realized in CMOS achieving 40-Gb/s operation with record low $NF$ performance and power consumption.

6.1 Contributions

The original contributions of this thesis can be summarized as follows

- A new theoretical analysis of the continuous-time $\Delta \Sigma$ loop was developed in $s$-domain. By providing a rational approximation of the quantizer, the loop stability
can be predicted. It has been demonstrated that the SNR of a continuous-time $\Delta\Sigma$ modulator can be found analytically by an expression that accounts for the effect of the loop filter $Q$. The study of loop stability in $s$-domain helps to simplify the design procedure of $\Delta\Sigma$ loops. The ADC design methodology was presented at the 2006 RFIC Symposium [77] and in the May 2007 issue of the Journal of Solid-State Circuits [78].

- The ADC in this thesis represents the world’s fastest $\Delta\Sigma$ modulator in any semiconductor technology. The sampling rate of 40 GHz is two and ten times higher than any published lowpass [22] and bandpass [19] continuous-time topology, respectively. The 4.5 to 5.8-GHz center frequency of the ADC presented in this work is also larger than the highest reported sampling clock of 4.3-GHz [19] in bandpass modulators. More importantly, this work demonstrated that the use of a mm-wave clock in ADCs leads to true direct RF sampling without compromising performance. Not only does the 40-GHz clock allow for directly sampling an RF signal, it helps achieve the best FoM when compared to similar attempts, too. This was made possible by employing the MOS-HBT cascode topology, biased at the peak-$g_m$ current density, which provides the best linearity, and the best frequency response in both the analog and digital parts of the chip. The measurements of both receivers show clearly that a $\Delta\Sigma$ ADC can be clocked higher than 20% of the $f_{tr}$ [15], without compromising stability. The ADC centered at 2 GHz was presented at the 2006 RFIC Symposium [77] and subsequently in the Journal of Solid-State Circuits special issue on the 2006 RFIC Symposium [78]. The digital receiver (ADC and on-chip PLL) was presented at the 2007 Symposium on VLSI circuits [79].

- The quantizer developed in this thesis, as a low-power alternative to the SiGe latch, is the first full-rate 40-Gb/s retiming flip-flop in CMOS. The latch operates at this speed with record low power consumption of 10 mW (half than best reported 40-Gb/s latch in SiGe BiCMOS [56]). Operation at 40 Gb/s is achieved by a combination of low and high-$V_T$ MOSFETs in the latch. Full-rate retiming with jitter reduction is demonstrated up to 40 Gb/s. Low-power broadband amplifiers based on resistor-inductor transimpedance feedback were realized in 90-nm and 65-nm CMOS to investigate the portability of high-speed building blocks across technology nodes. Experiments showed that the transimpedance amplifier based on
the CMOS inverter can reach 40-Gb/s operation with a record power consumption of 0.15 mW/Gb/s. The latch and broadband amplifiers were published at the 2006 ESSCIRC Conference [70], 2005 CICC Conference [64] and subsequently in the respective special issues of the Journal of Solid-State Circuits (July 2007 [80] and August 2006 [45]).

6.2 Future Work

Although the output stream of the ADC must be decimated to lower rates, a low-power 40-Gb/s decimation filter consisting of a de-multiplexer (DEMUX) and digital filters can be realized in SiGe BiCMOS with only 20 mW per latch [56] at 2.5 V. The power dissipation of a 1:2 DEMUX consisting of three latches would be 60 mW. Once the bitstream is decimated below 10 Gb/s, pure CMOS blocks can be employed to perform digital downconversion and filtering, as in [81]. The FoM would not be significantly degraded by the decimation stage.

As nanoscale CMOS evolves to speeds surpassing those of HBTs, it would be advantageous to implement a mm-wave ∆Σ ADC in such a technology. Operation from 1.2 V would provide significant power reduction in the digital part of the ADC, making it realistic to integrate in a handheld cellular device. The main challenge in CMOS, however, would be the linearity of the ADC loop filter. Further research is needed to investigate filter topologies that have large swings from sub-1.2-V power supplies.

To be able to reach the 12-bit resolution in the 2-GHz receiver, as required by the wireless standard presented in chapter 2, the sensitivity must be improved. One way is to include a low-noise broadband amplifier in front of the first $G_m$ stage. To handle the interference, the amplifier must also have automatic gain control (AGC). The bandwidth of the amplifier must extend from 2-6 GHz, therefore a transimpedance feedback amplifier, realized with a similar topology to the ones proposed in chapter 3, is more suitable. With a gain of 20 dB, $NF$ between 2-3 dB across the 3-dB bandwidth and AGC, the sensitivity of the receiver will increase. The combination of an input low-noise AGC amplifier with a tunable resonator from 2-6 GHz at the tank of the receiver will set the path for the versatile software-defined radio receiver, as envisioned by Mitola [1].
6.3 List of Publications

The research that was conducted in this thesis has resulted in the following publications in IEEE journals and conference proceedings.

6.3.1 Journal Articles


6.3.2 Papers at International Refereed Conferences


Bibliography


