A Sub-mW Integrating Mixer SAR Spectrum Sensor for Portable Cognitive Radio Applications

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***Abstract*— A low power mixed-signal integrating mixer successive approximation register (SAR) architecture is proposed for direct spectrum estimation in portable transceivers targeting IEEE 802.22 wireless regional area network cognitive radio applications. The integrating mixer SAR implements the short-time Fourier transform in the analog domain and digitizes its amplitude at the end of the integration period. The architecture consists of an array of folded double balanced mixers connected to a common subset of binary-weighted capacitive loads. Current domain windowing is applied in the first stage followed by mixing, integration and analog-to-digital conversion (ADC) in the second stage. Windowing sets the detection bandwidth and provides flexible low pass filtering while a load capacitor array enables integration with programmable time constant and acts as the sampling capacitors of a SAR ADC. A prototype chip is fabricated in IBM's 0.13μm CMOS process. The measured results indicate an average dynamic range of 27.9–25.7 dB over a frequency range of 0.05–1.25 GHz, while consuming 0.88 mW from 1.1/1.2 V supplies.**

***Index Terms*— Cognitive radio, spectrum sensing, short-time Fourier transform, energy detection, successive approximation register analog-to-digital converter.**

I. Introduction

COGNITIVE radios are reactive devices that identify unused spectrum segments known as spectral holes and dynamically adjust their transmission characteristics into these holes while avoiding interference with licensed/primary users. They are an extension of software-defined radios envisioned by Joseph Mitola [1] and must be cognizant of spectral, temporal and spatial components of the environment in which they are operating. Spectrum sharing is essential for efficient spectrum utilization and standards such as IEEE 802.22 WRAN [2] have been developed for dynamic spectrum allocation by license-exempt devices on a non-interfering basis in the 54-862MHz spectrum allocated to digital television (DTV) broadcast.

Spectrum sensing deals with signal detection and is the enabling technology behind cognitive radio, which detects the presence of a primary user (PU) signal within a given frequency band. Spectrum sensing seeks to distinguish between a band containing a PU signal, $s(t)$, or additive white Gaussian noise, $n(t)$, and is given by the hypotheses:

$$\mathcal{H}_0: \; x(t) = n(t)$$
$$\mathcal{H}_1: \; x(t) = s(t) + n(t)$$

where $\mathcal{H}_0$ is the hypothesis the band is a spectral hole and $\mathcal{H}_1$ is the hypothesis the band contains a PU signal.

Non-coherent signal detection, such as energy detection, requires little to no prior knowledge of the PU signal and does not require synchronization. Energy detectors compute the energy contained in a frequency band and compare the magnitude of the power spectrum to a threshold based on the estimated noise power to determine if a signal is present. The energy detection component of recent mixed-signal implementations that target the DTV frequency bands consume 17.5% to 24% of the total receiver power dissipation [3]–[5]. Low power implementation of spectrum sensing can result in a substantial overall power savings for a cognitive radio receiver.

The IEEE 802.22 WRAN standard [2] specifies the air interface and cognitive medium access control of point-to-multipoint wireless regional area networks for fixed and portable devices operating in the DTV bands. Portable devices require spectrum sensing every 2s with an accuracy of −114dBm for license-exempt transmission in DTV band. One of the potential applications for portable devices is public safety networks [6], [7], which require power efficient operation for mobile devices in order for emergency personnel to broadcast voice, data and location based services.

This paper presents an expanded discussion on the integrating mixer SAR architecture for energy-based detection [8], which targets incorporation within portable cognitive radio transceivers for IEEE 802.22 WRAN applications. The architecture implements the STFT in the analog domain and digitizes its amplitude at the end of the integration period. Here we also include analysis of the transconductance window function, discuss the digital implementation, present the equivalent circuits for calculating the time constants for each operating mode, and include additional measurement results. The integrating mixer SAR builds upon the integrating mixer [9] by the same authors. However, in this work, an array of mixer cells are utilized to remove current-domain restrictions on the window function thereby reducing its side-lobe oscillations while binary-weighted load capacitors enable charge redistribution to be incorporated for a SAR ADC. The architecture results in power consumption an order-of-magnitude lower

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TABLE I
WINDOW FUNCTION PROPERTIES

Window[a]	Side lobe (dBc)	Fall off (dB/octave)	DC Gain	3-dB BW (f_w)[b]
Rectangle	−13	−6	1.0	0.89
Triangle	−27	−12	0.5	1.28
Hann[c]	−32	−18	0.5	1.44
Hamming	−43	−6	0.54	1.3
$\cos^4(x)$	−47	−30	0.38	1.86

[a] Refer to [12] for additional window functions/properties.
[b] FFT bins for a digital implementation.
[c] Equivalent to $\alpha = 0.5$ in equation (2).

than previously reported methods based on energy detection [3]–[5], [10], [11] while obtaining fast spectral estimates over the full frequency range in the order of a few milliseconds.

II. Short-Time Fourier Transform

The STFT augments the Fourier transform with a window function that shapes the frequency response and restricts its integral to a finite time segment. The continuous-time STFT is defined as

$$X_\tau(f) = \int_{-\tau/2}^{\tau/2} x(t) w(t,\tau) e^{-j2\pi f t} dt \tag{1}$$

where $w(t,\tau)$ is the window function and τ is the period of the window function. The detection bandwidth (DBW) is set by the 3-dB bandwidth (BW) of the window function. The magnitude of the power spectrum can be calculated directly as the magnitude-squared of the STFT such that $|S_{xx}(f)|^2 = |X_\tau(f)|^2$.

A number of functions can be selected to implement the time-domain windowing operation, including the functions listed in Table I. The Hann and Hamming functions belong to a family of window functions that are commonly utilized to minimize spectral leakage in the fast Fourier transform (FFT) and are applied here to time-limit the STFT as well as provide low pass filtering (LPF). The Hann-Hamming window function is characterized by the parameter α and the continuous-time version is defined as

$$w(t,\tau) = \begin{cases} \alpha + (1-\alpha)\cdot\cos(2\pi f_w t) & \text{if } |t| \le \tau/2 \\ 0 & \text{otherwise} \end{cases} \tag{2}$$

where $\alpha = 0.5$ and $\alpha = 0.54$ for the Hann and Hamming functions, respectively. In Figure 1, the frequency domain response of equation (2) with $\alpha = 0.5$ and $\alpha = 0.85$ is illustrated. The initial side-lobe is −32dBc with a −18dB/octave fall off for $\alpha = 0.5$ while the initial side-lobe is −16.8dBc with a −6.3dB/octave fall off for $\alpha = 0.85$.

As illustrated in Figure 2, the STFT can be implemented directly with two mixing/multiplication stages followed by an integration stage. The input RF signal is mixed with the LO signal to obtain an IF signal that is multiplied by a window function, $w(t)$, prior to integration. An ADC synchronized to the end of the integration period samples the STFT with signal T_W and the magnitude-squared is computed in the digital

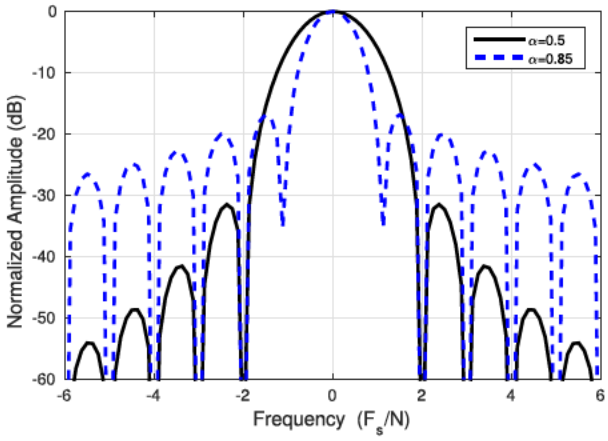

Fig. 1. Frequency domain response of the Hann-Hamming window function for $\alpha = 0.5$ and $\alpha = 0.85$.

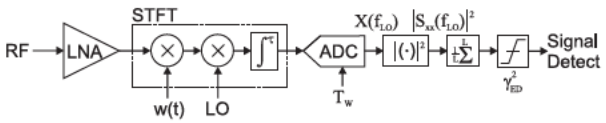

Fig. 2. Analog realization of STFT-based energy detector.

domain to obtain a spectral estimate at the LO frequency. A threshold detector compares the spectrum estimate with a threshold based on the noise floor estimate, γ_{ED}^2, to determine if a signal is present, where γ_{ED}^2 is chosen to meet a specified probability of detection, P_D, and false alarm, P_{FA}, pair.

There are a number of factors to consider when choosing between digital and analog architectures for spectrum sensing. These include DBW, acquisition/processing time and power dissipation. In the case of a fixed DBW, Δf, both detectors have the same acquisition time, $1/\Delta f$, while the FFT-based energy detector will require a sampling frequency scaled by the FFT size, $f_s = \mathrm{N_{FFT}} \cdot \Delta f$. Conversely, the STFT-based detector requires half the number of samples ($\mathrm{N_{FFT}}/2$) to cover the same frequency range. The main advantage of the STFT-based detector over digital implementations is the power dissipation, which is dominated by the ADC component in both implementations. As ADC power dissipation scales with sampling frequency, a significant reduction in power dissipation can be achieved with STFT-based energy detection.

III. State of the Art

A number of mixed-signal spectrum sensing implementations based on energy detection have been proposed for cognitive radio [3]–[5], [10], [11]. The first implementation to target IEEE 802.22 WRAN applications incorporated multi-resolution spectrum sensing (MRSS) in a dual-mode direct-conversion receiver [3]. In the spectrum sensing mode, the STFT is implemented directly using an analog correlator and a digital window generator (DWG). The correlator consists of a multiplier and an integrator while the DWG consists of a lookup table (LUT), 11-bit digital-to-analog converter (DAC), and LPF to implement a $\cos^4(x)$ window. The sensitivity is −74dBm with a 32dB dynamic range and 35dB of interference

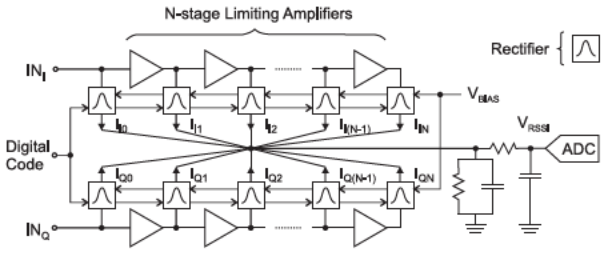

Fig. 3. Received signal strength indicator energy detector [5].

rejection. The energy detection component consists of the analog correlator with the DWG and consumes 43.2mW, which represents 24% of the total power dissipation. A second MRSS receiver implementation focused on power optimization [4]. The sensitivity is -72.5dBm with a power consumption of 23.8mW for 19.4% of the total power dissipation. However, the dynamic range is reduced to 24dB.

In addition to the STFT-based implementations, rectifier [5], [10] and envelope-based implementations [11] have been proposed for energy detection. A harmonic rejection mixer that incorporates a received signal strength indicator (RSSI) circuit is implemented in [5], which targets cognitive radio up to 2.4GHz. As illustrated in Figure 3, the architecture is comprised of limiting amplifiers, rectifiers and a passive RC filter. The sensitivity and dynamic range can be adjusted by turning on/off rectifier stages and changing the current mirror ratios. In the high sensitivity mode, only the last few rectifier stages are activated with large current. In the wide dynamic range mode, all the rectifier stages are activated with low current. The sensitivity is -83dBm with $29-48$dB dynamic range. The high dynamic range is achieved for input powers between -30dBm to $+18$dBm and the overall gain is dependent on the mode of the RSSI detector. The energy detection component consists of the limiting amplifiers and rectifiers and consumes 7.7mW, which represents 17.5% of the total power dissipation.

The STFT-based implementations relax the ADC sampling requirements while the incorporation of windowing adds a LPF effect, thereby reducing the specifications for the channel select filter [3]. The consequence of fine DBWs are long integration times, which can significantly increase the sensing time (e.g. sensing time of 4.8ms per DTV channel with 50kHz DBW). In contrast, the rectifier and envelope-based implementations offer fast detection since sensing time is dependent on settling time (e.g. settling time of 54μs per DTV channel for [11]). Low minimum receiver sensitivity can be achieved with all the reviewed architectures with the RSSI-based implementation [5] achieving -83dBm. Despite the potential for low power realization, the STFT-based implementations [3], [4] report the highest power dissipation while the RSSI-based implementation reports the lowest (13.9mW). An alternative to energy detection is the use of crosscorrelation. In [13], two identical RF frontends in combination with attenuators and crosscorrelation are utilized to achieve high linearity while reducing the noise contribution. The design achieves a spurious-free dynamic range (SFDR) of 88dB with a NF of 5dB.

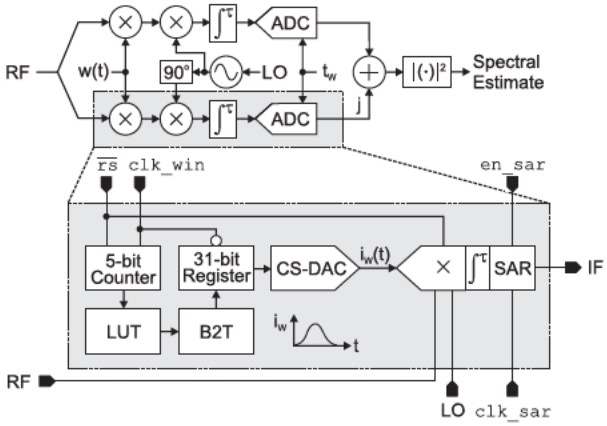

Fig. 4. Block diagram of the integrating mixer SAR ADC illustrated for a single path of an STFT-based spectral estimate (chip implements both paths).

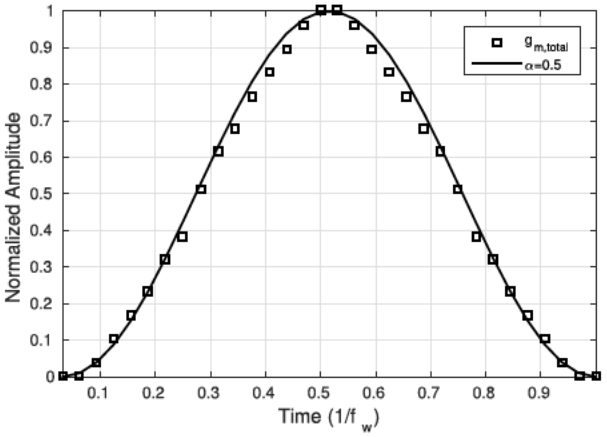

Fig. 5. Normalized total transconductance window function and corresponding α-value.

This work targets incorporation within low power cognitive radio transceivers for portable IEEE 802.22 applications. Low power operation is crucial to extend the battery life of portable transceivers and a sub-mW spectrum sensor that utilizes the relaxed ADC sampling requirements of the STFT-based energy detector is proposed.

IV. Integrating Mixer SAR Circuit Design

The integrating mixer SAR implements the STFT in the analog domain and digitizes its amplitude at the end of the integration period. In order to reduce the number of stages, windowing is applied in the current-domain while integration is incorporated within the mixer by using capacitive loads, which double as the sampling capacitors of a SAR ADC. The integrating mixer SAR operates in three modes: a *reset mode* where both terminals of the load capacitors are connected to V_{DD}, resetting the accumulated signal and discharging the capacitors; an *integration/sample mode* where the capacitive loads provide bias current while integrating and sampling the IF signal; and a *conversion mode* where charge redistribution is applied to the sampled STFT signal across the binary-weighted load capacitors of the SAR ADC.

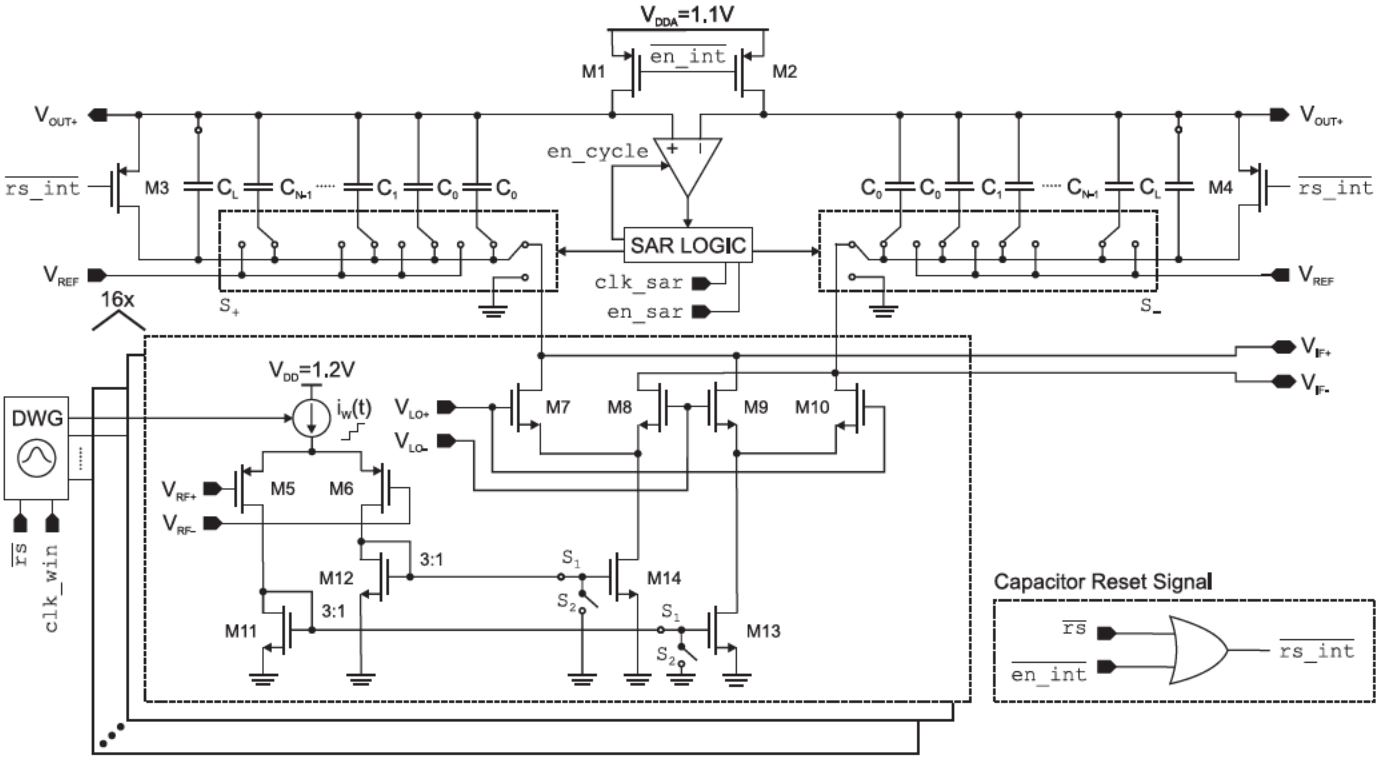

Fig. 6. Integrating mixer SAR schematic with control signals $\overline{\texttt{rs\_int}}$ and $\overline{\texttt{en\_int}}$.

A system block diagram of the integrating mixer SAR is illustrated in Figure 4, where the digital input signals $\overline{\texttt{rs}}$, clk_win, clk_sar and en_sar control system operation. The input $\overline{\texttt{rs}}$ selects the mode of operation where $\overline{\texttt{rs}}$ ='0' and $\overline{\texttt{rs}}$ ='1' correspond to reset and integration modes, respectively. The window function is generated by a 5-bit parallel binary counter that cycles through the binary coefficients stored in a LUT each integration period at a frequency set by clk_win. A binary to thermometer encoder with registered output drives a distributed 5-bit thermometer coded current switching DAC (CS-DAC) that implements the window function in the current-domain and is mirrored to the integrating mixer SAR. The en_sar signal triggers a SAR conversion at a frequency set by clk_sar and cannot switch modes until the conversion process is complete. The LO signal is supplied off chip.

A. Window Function

The Hann function is selected for the window function and is implemented in the current-domain. Here, 5-bit quantization is selected since it minimizes the complexity while only incurring a 0.9dB penalty on the initial side-lobe with a -11.1dB/octave roll off. In addition, the window function is sampled 32 times to reduce the hardware complexity such that $f_{clk\_win} = 32 \cdot f_w$.

The integrating mixer SAR utilizes an array of 16 folded mixer cells with a 3-level CS-DAC, which realize a distributed 5-bit thermometer coded CS-DAC. The current window function is generated by switching individual cells on/off in a thermometer sequence, where the sum of the currents is the value of the window function. This removes the minimum current restriction on the selection of the window function, which improves the achievable side-lobe reduction and fall off. The transconductance of the input pair implements the windowing operation. In Figure 5, the simulated value of the normalized total transconductance is compared to the Hann window function ($\alpha = 0.5$). The total transconductance, $g_{m,total}$, closely follows the Hann window function using IBM's 0.13μm CMRF8SF CMOS process. In other deep submicron processes, the normalized total transconductance might be less likely to follow the window function closely and pre-distortion must be used to achieve correlation.

B. Integrating Mixer SAR

As illustrated in Figure 6, the proposed integrating mixer SAR consists of a folded mixer array that is connected to binary-weighted load capacitors that form the sampling capacitors of an 11-bit differential SAR ADC. The first stage of the mixer implements current domain windowing while the second stage implements downconversion mixing, integration and charge redistribution. The binary-weighted capacitors are implemented with a unit capacitance of $C_U = 62.5$fF such that $C_N = 2^N \cdot C_U$. In addition, a programmable load capacitor, C_L, sets the integration time and realizes the four integration modes listed in Table II. The array consists of 16 folded mixers with 3-level CS-DACs that are driven by a DWG, which turn on/off individual cells to implement the window function. The supply voltage, V_{DDA}, is connected to the V_{OUT+} and V_{OUT-} buses through the PMOS transistors M1 and M2 using control signal $\overline{\texttt{en\_int}}$, which is enabled during the integration/sample and reset modes. These common buses are the inputs to a comparator that is clocked during charge redistribution in the conversion mode. A double-tail voltage sense amplifier [14] is used to implement the com-

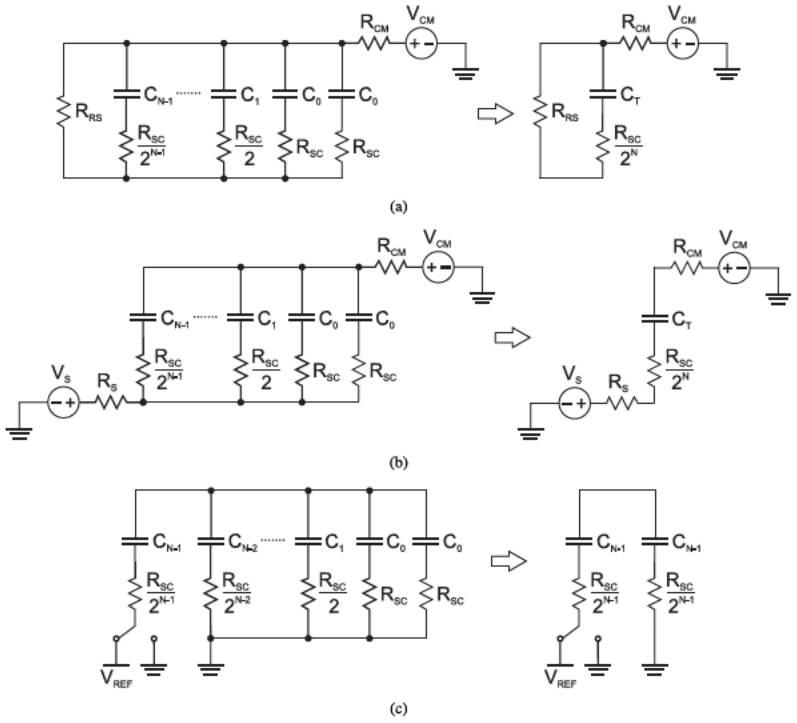

Fig. 7. Integrating mixer SAR equivalent circuits for time constant calculations in each operating mode. (a) Equivalent circuit for capacitor discharge (τ_{reset} calculation). (b) Equivalent circuit for sample mode pre-charge (τ_{samp} calculation). (c) Equivalent circuit for charge redistribution (τ_{conv} calculation).

TABLE II
INTEGRATING MIXER SAR MODES

f_w	Int. Period	C_L	C_{TOTAL}	DBW
250kHz	4.0μs	384pF	512pF	360kHz
333kHz	3.0μs	256pF	384pF	480kHz
500kHz	2.0μs	128pF	256pF	720kHz
1MHz	1.0μs	–	128pF	1.44MHz

parator. PMOS transistors M3 and M4 are utilized to reset the capacitive loads and are controlled by the signal $\overline{\texttt{rs\_int}}$, which is enabled only when $\overline{\texttt{rs}}$ ='0' and conv ='0' to prevent accidental resetting of the capacitors during a conversion.

The mixer array cells utilize a folded architecture to maximize the transconductance of the input differential pair in the first stage while minimizing the current provided by the capacitive loads in the second stage. In the first stage, the current from the 3-level CS-DAC is mirrored to the PMOS differential pair (M5:M6). The transconductance values g_{m5} and g_{m6} implement the window multiplication. The input differential pair operates linearly over a differential swing of 600mV with a common-mode voltage of 475mV. The output currents are mirrored to the second stage with a gain of approximately 1/3. The second stage consists of a mixing quad (M7:M10) that connects to the load capacitors through switch arrays that toggle between $V_{IF+/-}$, V_{REF} and 0V based on the operating mode. The mixing quad has a common-mode voltage of 1V and the LO has a voltage swing of 400mV.

In the reset mode, the signals $\overline{\texttt{en\_int}}$ ='0' and $\overline{\texttt{rs\_int}}$ ='0' while the capacitor arrays are switched to the $V_{IF+/-}$ signals. The PMOS transistors M1:M4 are in deep triode such that V_{DDA} is applied to both the $V_{OUT+/-}$ buses and the $V_{IF+/-}$ outputs. This causes the load capacitors to discharge and resets the accumulated IF signal. NMOS switches, S_1 and S_2, disable the current mirrors between the first and second mixer stages by pulling the gates of NMOS transistors M13 and M14 to ground, which disables the LO downconversion operation in the second stage. This reduces the reset time of the load capacitors. The reset time constant, τ_{reset}, can be obtained from the equivalent circuit illustrated in Figure 7(a) and is given by

$$\tau_{reset} = \left(R_{RS} + \frac{R_{SC}}{2^N} + R_{CM}\right) C_T \tag{3}$$

where R_{RS} is the on resistance of the PMOS transistors M3 and M4, R_{SC} is the on resistance of the PMOS transistors that set the load capacitance, R_{CM} is the common mode resistance, and $C_T = 2^N C_U$ is the total capacitance. As in [15], the switch resistance is assumed to be binary scaled for circuit simplification of the binary-weighted capacitor array, which is presented in Appendix.

In the integration/sample mode, $\overline{\texttt{rs\_int}}$ ='1' and $\overline{\texttt{en\_int}}$ ='0' while the capacitor arrays are switched to the $V_{IF+/-}$ signals. The PMOS transistors M1:M2 are in deep triode such that V_{DDA} is applied to $V_{OUT+/-}$ while M3:M4 are in cutoff. The capacitors supply bias current while simultaneously integrating the IF signal after LO downconversion. NMOS switches, S_1 and S_2, enable the current mirrors between the first and second mixer stages. The differential IF signal at the end of the integration period is the magnitude of the spectrum at the LO frequency while the DBW is set by the 3-dB BW of the window function. The sample mode time constant, τ_{samp}, can be obtained from the equivalent circuit

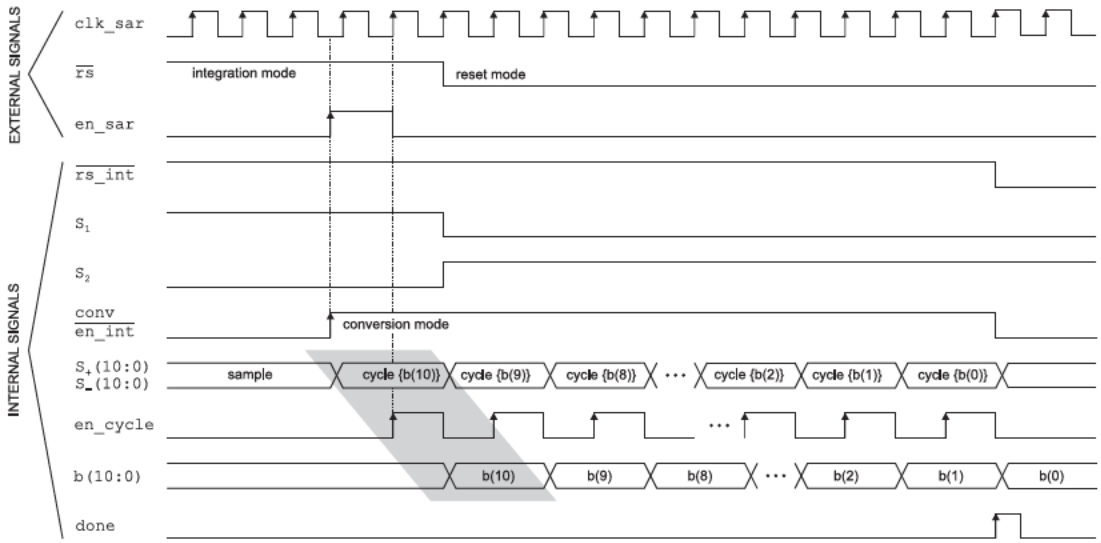

Fig. 8. Integrating mixer SAR control and output waveforms.

illustrated in Figure 7(b) and is given by

$$\tau_{samp} = \left(R_S + \frac{R_{SC}}{2^N} + R_{CM}\right) C_T \tag{4}$$

where R_S is the source resistance.

In the conversion mode, the internal signal conv ='1' after a SAR conversion is triggered, which causes the signals $\overline{\texttt{en\_int}}$ ='1' and $\overline{\texttt{rs\_int}}$ ='1'. Consequently, the PMOS transistors M1:M4 are in cutoff disconnecting V_{DDA} from $V_{OUT+/-}$. In addition, PMOS switches are used to disconnect C_L from $V_{OUT+/-}$ to isolate the binary-weighted capacitors. A combined sequencer and code register [16] switches the binary-weighted capacitors during charge redistribution and incrementally store the bit comparison in the code register. As illustrated in Figure 8, a bit comparison is a three step process: (1) the sequencer sets the switch arrays S+ and S− for charge redistribution to toggle between 0V and V_{REF}; (2) the comparator is triggered by en_cycle during the next clock cycle; (3) and finally, the next bit comparison samples the current bit value and sets b(n) during the third clock cycle. The conversion mode time constant, τ_{conv}, can be obtained from the equivalent circuit illustrated in Figure 7(c) and is given by

$$\tau_{conv} = \frac{R_{SC}}{2^N} C_T. \tag{5}$$

The comparator input voltage fluctuates due to charge redistribution during the SAR process. The maximum voltage that occurs on $V_{OUT+/-}$ occurs during comparison with $3/4V_{REF}$ such that $V_{OUT+/-}(\text{max}) = V_{DDA} - V_{IF+/-} + 3/4V_{REF}$. This causes a potential voltage limitation in the absence of thick oxide devices. In the target IBM CMRF8SF process, standard devices are limited to a maximum of 1.6V while the standard supply is 1.2V. The integrating mixer is designed to operate with a maximum voltage drop of 0.6V across the output $V_{IF+/-}$ voltage, which results in a maximum voltage of $V_{OUT+/-} = 1.425$V. In order to reduce the maximum voltage, a supply of $V_{DDA} = 1.1$V is utilized and a saturation circuit disables integration once a drop of 0.6V is detected, which limits the maximum voltage to $V_{OUT+/-} = 1.325$V.

The total sensing time, t_{sense}, for a specified frequency range, $f_{end} - f_{start}$, and frequency step, f_{step}, is given by

$$t_{sense} = \left(\frac{f_{end} - f_{start}}{f_{step}} + 1\right) \times \left(N_{ave}\left(T_w + t_{reset} + t_{conv}\right) + t_{sw}\right) \tag{6}$$

where N_{ave} is the number of spectrum averages at a single LO frequency, T_w is the window period, t_{reset} is the time to discharge the load capacitors during the reset period, t_{conv} is the conversion time, and t_{sw} is the settling time of the LO signal. The maximum frequency step is f_{step} = DBW while the minimum value of t_{reset} can be estimated from the RC time constant in equation (3) for the reset mode and t_{conv} can be estimated from the RC time constant in equation (5). The value of t_{sw} depends on the settling time of the applied LO signal. In contrast to direct implementation of the STFT, the t_{reset} and t_{conv} terms in equation (6) increase the sensing time and should be minimized. In general, the overall sensing time should be minimized to reduce the overhead associated with spectrum sensing and maximize the spectrum utilization.

V. Implementation Results

A full quadrature integrating mixer SAR prototype was implemented in IBM's 0.13μm CMRF8SF CMOS process with 1.2V and 1.1V supplies and low-V_t devices for analog components. The capacitive loads were implemented with metal-insulator-metal capacitors (MIMCAP) while the DWG and SAR logic is isolated from the analog circuitry in guard rings and located directly under the MIMCAPs. A unit capacitor size of 62.5fF was applied for the SAR ADC. A die microphotograph is shown in Figure 9. The binary-weighted SAR capacitor arrays are surrounded by 64pF capacitors that combine to form C_L, which sets the integration time. The silicon area of the prototype is 1.33mm^2. The prototype die is packaged in a 52 pin QFN package and mounted on a custom designed printed circuit board.

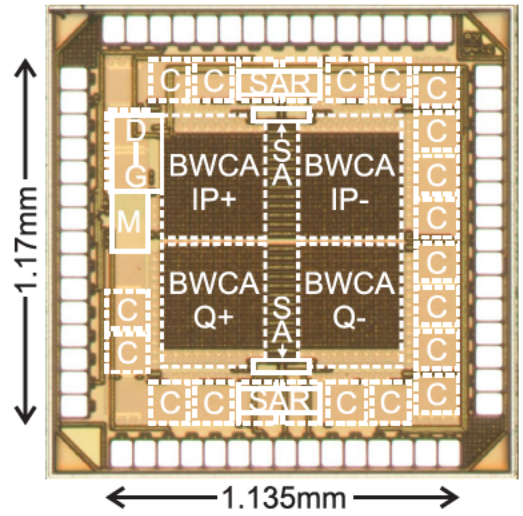

Fig. 9. Die microphotograph of integrating mixer SAR prototype (BWCA: binary-weighted capacitor array; C: load capacitor, C_L; DIG: digital window; IP: in-phase; M: mixer/CS-DAC; Q: quadrature; SA: switch array; SAR logic).

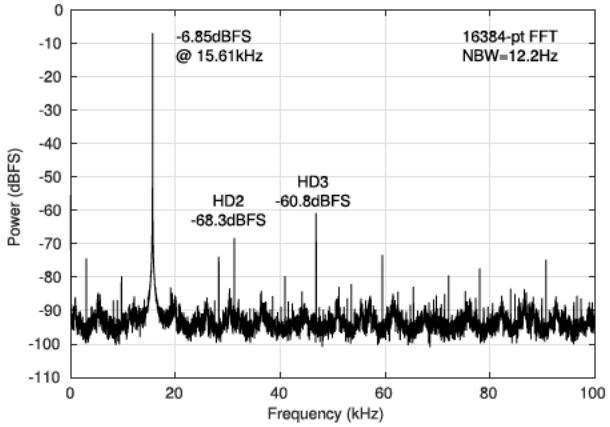

Fig. 10. Measured SAR ADC power spectrum for $f_s = 200$kHz.

A. SAR ADC

In order to characterize the integrated 11-bit SAR ADC, the converter is isolated from the integrating mixer by applying the input signal directly to $V_{IF+/-}$ and setting $V_{CM} = 0$V for the mixer LO, thereby cutting off the LO switching pairs and tail currents in the mixer. The SAR ADC is designed to operate for a single-ended input voltage between $0.6\text{V} \leq V_{IF+/-} \leq 1.1\text{V}$ for a 1V differential voltage, which restricts the maximum input to -6.85dBFS and the converter resolution to 9.86-bit.

The peak signal-to-noise-and-distortion ratio (SNDR) of 45.4dB at -6.85dBFS 15.6128kHz input is observed with $f_s = 200$kHz, which results in 7.25-ENOB while consuming a total of 134μW from 1.1/1.2V supplies. Figure 10 illustrates the measured spectrum at peak SNDR. The third order harmonic is -54dBc.

The SNDR, signal-to-noise ratio (SNR), and SFDR performance is measured versus input amplitude and sampling frequency. In Figure 11, the input signal amplitude is increased from -30.42dBFS to -6.80dBFS. The SNDR increases linearly with input signal amplitude and the extrapolated SNDR value at 0dBFS is 52.14dB. As the input amplitude increases, the spurious tones become dominant and the converter is limited by linearity. In Figure 12, the sampling frequency is increased from 50kHz to 250kHz while maintaining the same $f_{in} : f_s$ ratio. The SNDR increases with sampling frequency at a rate of $+1.33$dB/100kHz with peak SNDR at 200kHz. The power dissipation scales linearly with sampling frequency to a maximum of 164μW at $f_s = 250$kHz. The performance results are summarized in Table III, where the figure of merit is defined as

$$\text{FOM (dB)} \equiv \text{SNDR(dB)} + 10 \cdot \log_{10}(\text{BW/Power}). \quad (7)$$

The differential non-linearity (DNL) and integral non-linearity (INL) are measured by applying a 15.6128kHz sinusoid at the maximum input amplitude of -6.85dBFS, which results in only a subset of 935 codes used from the possible 2048 codes. As illustrated in Figure 13, the DNL is $+1.7/-1$ LSB while the INL is $+2.3/-3.4$ LSB. As the DNL > 1, the ADC transfer function is not guaranteed to be monotonic. The converter is missing 9 codes (DNL $= -1$), however, the maximum INL error is 0.36%. The INL limits the

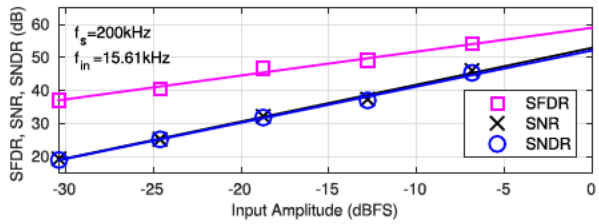

Fig. 11. Measured SFDR, SNR, and SNDR versus input amplitude.

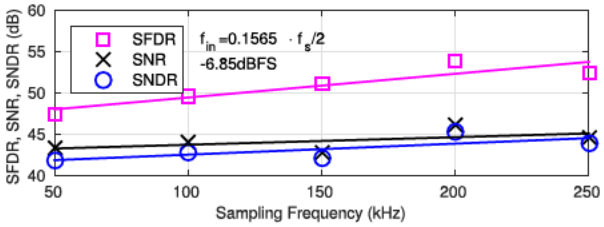

Fig. 12. Measured SFDR, SNR, and SNDR versus sampling frequency.

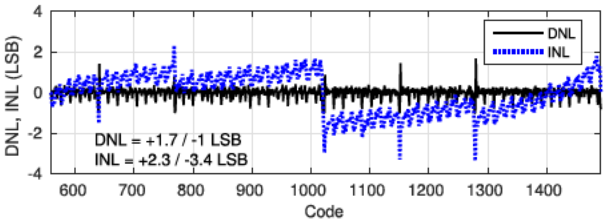

Fig. 13. Measured DNL and INL.

TABLE III
SAR ADC MEASUREMENT SUMMARY

	Measured
Technology	0.13μm
Supply	1.1/1.2V
Max Input/Full Scale	1V/2.2V
BW	250kHz
SNDR (Peak, $0.5 \cdot f_s$)	45.4dB, 43.8dB
SNR (Peak, $0.5 \cdot f_s$)	46.2dB, 44.5dB
SFDR (Peak, $0.5 \cdot f_s$)	54.0dB, 52.7dB
DNL, INL	$+1.7/-1$ LSB, $+2.3/-3.4$ LSB
Power	164.0μW
FOM (Shreier)	136.3dB

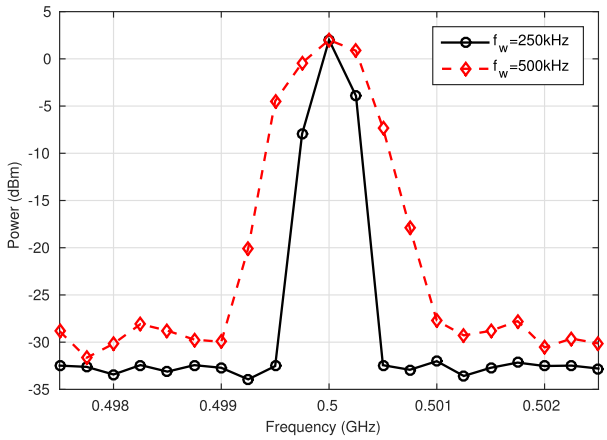

Fig. 14. Spectrum estimates for a tone at 0.5GHz with +2dBm of power and $f_w = 250$kHz and $f_w = 500$kHz.

TABLE IV
INTEGRATING MIXER SAR MEASUREMENT SUMMARY

	Measured
Technology	0.13μm
Supply	1.1/1.2V
Frequency Range	1.25GHz
DR_{ave} (f_w: 250kHz, 500kHz)	27.9dB, 25.7dB
Int. Gain (f_w: 250kHz, 500kHz)	-13.9dB, -13.5dB
1dB Compression	+0.2dBm

TABLE V
INTEGRATING MIXER SAR POWER SUMMARY

Circuit	Measured	Simulated[a]
Input pair/Latch/CS-DAC	737μW	$760-1183\mu$W
Downconversion/Integrator	48μW	$46-95\mu$W
SAR logic/DWG	93μW	$135-155\mu$W
	878μW	$941-1433\mu$W

[a] Over corners slow-slow 27°C to typical-typical 27°C.

maximum converter resolution. A maximum INL of 3.4 LSB reduces the converter resolution by 2.06 bits, resulting in a maximum resolution of 7.8 bits with −6.85dBFS input.

B. Spectrum Estimation and Linearity

The measured power spectrum of a tone at 0.5GHz with an input power of +2dBm is illustrated in Figure 14 for $f_w = 250$kHz and $f_w = 500$kHz. The LO frequency is swept over 250kHz intervals, which shows spreading of the input signal. The side-lobe oscillations are nearly completely suppressed, which is expected as the Hann window function achieves > 30dB side-lobe rejection. As shown in Table IV and illustrated in Figure 15 for $f_w = 250$kHz, the measured frequency range is 1.25GHz while the average DR is 27.9dB for $f_w = 250$kHz and 25.7dB for $f_w = 500$kHz. The maximum DR is limited by the noise floor, which depends on the DBW set by f_w and the window function. The 2.2dB reduction in DR from a DBW of 360kHz to 720kHz is slightly less than the 3dB drop expected. The interference rejection for a tone at 0.5GHz is measured for $f_w = 250$kHz, which results in 33.2dB rejection without using any filter in the RF signal path. There is a constant integration gain associated with each

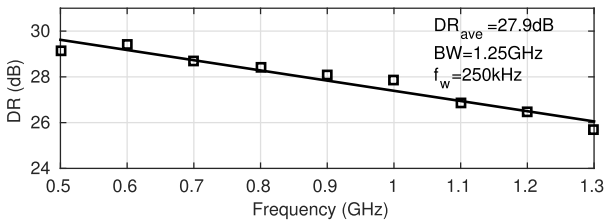

Fig. 15. DR over 0.5GHz to 1.3GHz for $f_w = 250$kHz.

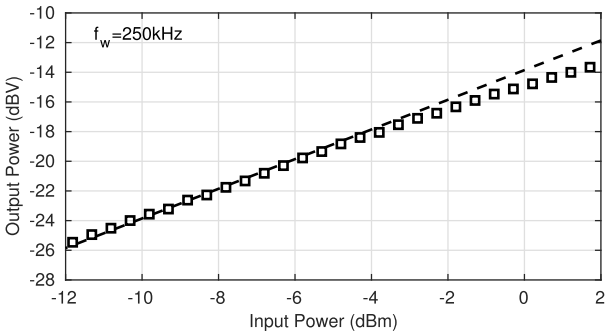

Fig. 16. 1dB compression for $f_w = 250$kHz.

window frequency, which is proportional to the voltage drop across capacitive loads.

The input 1dB compression point is +0.2dBm according to Figure 16 while the total harmonic distortion (THD) for a tone at 0.5GHz with a power of −0.5dBm is 0.79%. The overall performance is summarized in Table IV while a breakdown of the power dissipation is listed in Table V. The total power dissipation is 878μW, which is 6.7% less than that simulated for the slow-slow 27°C corner.

C. Comparisons

In Table VI, the proposed integrating mixer SAR is compared to recent spectrum sensing implementations based on energy detection [3]–[5], [10], [11] and the original integrating mixer prototype [9]. In comparison to recent spectrum sensing implementations, the integrating mixer SAR prototype achieves greater than 15× reduction in power dissipation and an average DR of 26.8dB, which is slightly higher than the average DR of [4]. This leads to the highest DR/P value of $31.7 - 29.3$dB/mW, where DR/P is used to measure the implementation efficiency. The higher the value of DR/P, the less power required per 1-dB of DR. The RSSI design in [5] obtains the second largest frequency range and the largest DR at 48dB, however, the high DR is only achieved in the wide-DR mode which covers input powers between −30dBm to +18dBm where the overall gain is dependent on the mode of the RSSI detector. The envelope-based implementation of [11] achieves the widest frequency range and the second largest DR but has a DBW of 40MHz, which is much wider than the 6MHz channels in the DTV bands. The higher power consumption of the STFT implementations in [3] and [4] are in part due to direct realization of the STFT (with two double balanced mixers and an integrator) and the high resolution DAC utilized for the DWG. In order to match the best receiver sensitivity of −83dBm, the proposed design would require an analog front end with a LNA and

TABLE VI
COMPARISON OF SPECTRUM SENSING IMPLEMENTATIONS BASED ON ENERGY DETECTION COVERING THE DTV BAND

	[3]	[4]	[5]	[10]	[11]	[9]	This work
Technology	0.18μm	0.18μm	90nm	0.18μm	0.13μm	0.13μm	0.13μm
Active Area (mm^2)	11.52	9.2	2.34	3.33	0.17	0.21	1.33
Supply (V)	1.8	1.8	1.2	1.8	1.5/1.3	1.2	1.2/1.1
P (mW)	43.2[a]	23.8[a]	13.9[b]	17.8[c]	19.5 – 28.5	2.5	**0.878**
DR (dB)	32	24	29 – 48	34	n/a	24 – 21	27.9 – 25.7
Frequency Range (GHz)	0.4-0.9	0.4 – 0.9	0.03 – 2.4	0.4 – 0.8	0.25 – 3.25	0.05 – 3	0.05 – 1.25
Window	$\cos^4 x$	$\cos^4 x$	n/a	n/a	n/a	Hann-Hamming[d]	Hann
f_w (MHz)	0.025 – 1	0.025 – 1	n/a	n/a	n/a	1 – 4	0.25 – 0.5
DBW (MHz)	0.05 – 2	0.05 – 2	0.2 – 30	0.4	40	1 – 4	0.36 – 0.72
Sensing Time (μs)[e]	4800 – 3	4800 – 3	n/a	< 7.5	54[f]	12-0.75[g]	133.33–33.33[g]
DR/P (dB/mW)	0.7	1.0	2.1 – 3.4	n/a	n/a	9.6 – 8.4	**31.7 – 29.3**

[a] Power for analog correlator and digital window generation.
[b] Power for mixer, BB filter and RSSI circuitry.
[c] Power for LNA, QPLL, analog correlator, and wavelet generator over LO frequency range.
[d] Hann-Hamming function with $\alpha = 0.85$.
[e] Sensing time for a single DTV channel with a BW of 6MHz.
[f] Average settling time of 54μs per DTV channel (360μs for a 40MHz DBW).
[g] Utilizing a 50% duty ratio for the reset signal.

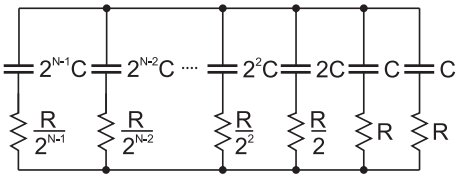

Fig. 17. Binary weighted capacitor array.

gain stages that provide a gain of 58dB, which is 9dB less than [5]. The DBW of the proposed design is limited by the integrating capacitor size but maintains a respectable minimum of 360kHz. The proposed design is well suited as the first in a dual-stage sensing process to quickly identify potential vacant spectrum for detailed sensing with a method such as feature detection.

In comparison to the original integrating mixer [9], the integrating mixer SAR prototype decreases the power dissipation by over 60% while slightly increasing the average DR to 26.8dB. As a consequence, the second prototype achieves a higher DR/P value of 31.7−29.3dB/mW. The minimum DBW is improved from 1MHz to 360kHz, however, the frequency range is reduced to 1.25GHz. The power reduction is due in part to the reduced maximum tail current of the input differential pair (1.1mA to 0.356mA) as well as the reduced average value of the current window function over the integration period ($0.75 \cdot i_{w,\max}$ to $0.5 \cdot i_{w,\max}$).

VI. CONCLUSION

A full quadrature prototype chip for spectrum sensing was fabricated in IBMs CMRF8SF 0.13μm CMOS process that consists of an array of folded mixers combining mixing, current-domain windowing, integration and SAR A/D conversion to obtain a digital estimate of the STFT. The design operates over a frequency range of 0.05 to 1.25GHz, consumes 0.88mW and obtains an average DR of 25.7 to 27.9dB. The architecture results in the lowest reported power consumption for mixed-signal spectrum sensing based on energy detection and includes mixing, baseband filtering and A/D conversion, which further reduces the overall receiver power dissipation. Spectral estimates can be obtained in as little as 4.5ms over the DTV bands. The architecture is well suited for incorporation within cognitive radio transceivers that target portable IEEE 802.22 applications. The integrating mixer prototype can be utilized with cooperative spectrum sensing or as the first in a dual-stage sensing process to quickly identify potential vacant spectrum for detailed sensing with cyclostationary feature detection and exceeds the frequency range requirements of IEEE 802.22 WRAN.

APPENDIX
BINARY WEIGHTED CAPACITOR ARRAY SIMPLIFICATION

In Figure 17, a binary-weighted capacitor array with binary-scaled resistors is illustrated for an N-bit SAR ADC. The series impedance of the k-th branch is given by

$$Z_k = \frac{R}{2^k} + \frac{1}{2^k Cs} \rightarrow \frac{RCs+1}{2^k Cs}.$$

The total impedance, Z_T, is computed from the branch impedances in parallel and is given by

$$\begin{aligned} Z_T &= Z_{N-1} \| Z_{N-2} \| \cdots \| Z_2 \| Z_1 \| Z_0 \| Z_0 \\ &= \left(\frac{1}{Z_{N-1}} + \frac{1}{Z_{N-2}} + \cdots + \frac{1}{Z_2} + \frac{1}{Z_1} + \frac{1}{Z_0} + \frac{1}{Z_0} \right)^{-1} \\ &= \left(\frac{2^{N-1}Cs}{RCs+1} + \frac{2^{N-2}Cs}{RCs+1} + \cdots + \frac{2^2 Cs}{RCs+1} + \frac{2^1 Cs}{RCs+1} \right. \\ &\quad \left. + \frac{2^0 Cs}{RCs+1} + \frac{2^0 Cs}{RCs+1} \right)^{-1} \\ &= \left(\frac{Cs}{RCs+1} \left(2^{N-1} + 2^{N-2} + \cdots + 2^2 + 2^1 + 2^0 + 2^0 \right) \right)^{-1} \\ &= \frac{RCs+1}{2^N Cs} \rightarrow \frac{R}{2^N} + \frac{1}{2^N Cs}. \end{aligned}$$

Therefore, the equivalent impedance of a binary-weighted capacitor array with binary-scaled resistors for an N-bit SAR ADC is the total array capacitance, $C_T = \sum C_k = 2^N C$, in series with $R/2^N$, where C is the unit capacitance.

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