A 1.55mW Mixed-Signal Integrating Mixer for Direct Spectrum Estimation in 0.13μm CMOS

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***Abstract*— A low power integrating mixer prototype chip for direct spectrum estimation is fabricated for opportunistic spectrum access, interference detection and built-in test applications. The integrating mixer consists of a folded architecture that combines mixing, current-domain windowing, and integration to implement the short-time Fourier transform (STFT). The design operates over a frequency range of 0.05-3GHz, consumes 1.55mW from a 1.2V supply and obtains a dynamic range (DR) of 24dB.**

I. Introduction

Opportunistic spectrum access is a method to increase spectrum utilization and alleviate the need for new bandwidth (BW) allocation. Spectrum sensing is the enabling technology, which detects unused segments of the frequency spectrum for data transmission. Additional applications include interference detection and RF built-in self-test, which benefit from low-power and direct spectrum estimation. Instead of sampling the downconverted signal and utilizing the fast Fourier transform (FFT) to estimate the spectrum in the digital domain, we estimate the spectrum directly utilizing the STFT in the analog domain. This relaxes the analog-to-digital converter (ADC) requirements as the integration window is longer than the symbol period, thereby reducing the sampling frequency and the overall power consumption. We propose an integrated architecture that combines mixing, windowing and integration in a single folded integrating mixer. The architecture results in power consumption an order-of-magnitude lower than previously reported methods based on energy detection [1]-[3] while obtaining fast spectral estimates over the full BW in the order of a few milliseconds.

II. Short-Time Fourier Transform

The continuous-time STFT is defined as

$$X(\omega,\tau)=\int_{-\tau/2}^{\tau/2}x(t)w(t,\tau)e^{-j\omega t}dt \qquad (1)$$

where $w(t,\tau)$ is a window function that time-limits the Fourier transform and τ is the window period. The spectrum can be calculated directly from the STFT as $|X(\omega,\tau)|$.

The von Hann function is a common window applied to minimize spectral leakage in the FFT and is applied to time-limit the STFT. The continuous-time version is defined as

$$w(t,\tau)=\begin{cases}\alpha+(1-\alpha)\cdot\cos(2\pi f_w t) & \text{if } |t|\le\tau/2\\ 0 & \text{otherwise}\end{cases} \qquad (2)$$

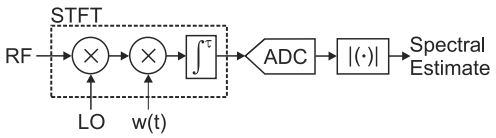


Fig. 1. Direct realization of the STFT for spectrum estimation.

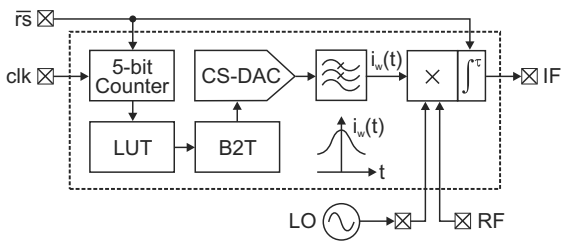


Fig. 2. Integrating mixer block diagram implementing the STFT in the analog domain (B2T: Binary to Thermometer encoder).

where $\alpha=0.5$ for the von Hann window.

The window provides a low pass filtering effect with a corner frequency of $f_w=1/\tau$.

III. Concept

As illustrated in Fig. 1, the STFT can be implemented directly with two mixing/multiplication stages followed by an integration stage. The input RF signal is mixed with the LO signal to obtain an IF signal that is multiplied by a window function prior to integration. An ADC synchronized to the end of the integration period samples the STFT and the magnitude is computed in the digital domain to obtain a spectral estimate at the LO frequency. To reduce the number of stages, an integrated architecture is proposed that implements the window function in the current-domain and incorporates integration within the mixer by utilizing capacitive loads. The integrating mixer operates in two modes: a *reset mode* where both terminals of the capacitor are connected to $\mathrm{V_{DD}}$, resetting the accumulated signal and discharging the capacitor, and an *integration mode* where the capacitive loads provide DC bias current while integrating the AC signal.

IV. Circuit Design

A system block diagram of the proposed integrating mixer is illustrated in Fig. 2, where the digital input signals $\overline{\mathrm{rs}}$ and clk control system operation. The input clk is set to $32\cdot f_w$ while $\overline{\mathrm{rs}}=0\mathrm{V}$ and $\overline{\mathrm{rs}}=\mathrm{V_{DD}}$ correspond to reset and integration

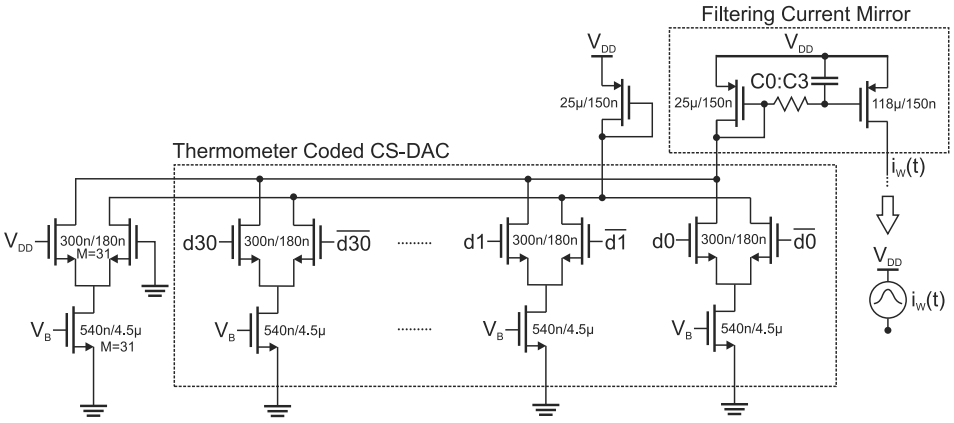


Fig. 3. CS-DAC and filtering current mirror schematic (M: multiplication factor).

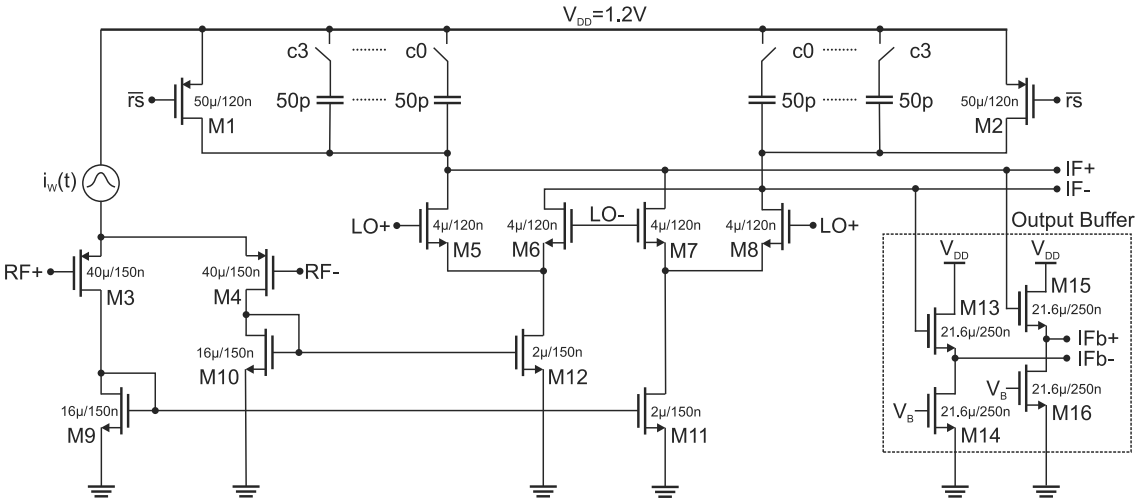


Fig. 4. Simplified integrating mixer schematic.

modes, respectively. The window function is generated by a 5-bit counter that cycles through the binary coefficients stored in a lookup table (LUT) each integration period. A binary to thermometer encoder drives a 5-bit current switching digital-to-analog converter (CS-DAC) that implements the window function in the current-domain and is mirrored to the integrating mixer. The LO signal and ADC are supplied off chip.

A. Window Function

Implementing the window function in the current-domain restricts the selection of α in equation (2) since a minimum current is required for correct mixer operation. The LUT entries are chosen so that the tail mixer bias current follows equation (2) with a value of $\alpha = 0.75$ in order to ensure a minimum current of $\mathrm{I_{max}}/2$, where $\mathrm{I_{max}}$ is the current with no windowing applied. Simulation results indicate the mixer gain is proportional to the square-root of the differential pair tail current so the window function's effective coefficient is $\alpha_{\mathrm{eff}} = 0.85$. As a consequence, side-lobe oscillations of the window in the frequency domain are expected to be reduced by 17dB with a 19.9dB/decade roll-off.

B. Current-Steering Digital-to-Analog Converter

The 5-bit CS-DAC is designed to implement the current window function on chip. Thermometer coding is utilized to prevent glitches during switching and the bias voltage ($\mathrm{V_B}$) applied to the NMOS current sources is chosen to maintain a high effective over-drive voltage of approximately $V_{\mathrm{eff}} = 700m\mathrm{V}$. As illustrated in Fig. 3, there are 31 constant current sources in parallel with the switched current sources in the CS-DAC since the minimum current is always $\mathrm{I_{max}}/2$. A LPF is built into the current mirror to prevent aliasing and smooth the coarse transitions of the CS-DAC [4], where the cut-off frequency is set based on the integration period with four parallel capacitors (C0:C3) with PMOS enabling switches.

C. Integrating Mixer

A simplified schematic of the proposed integrating mixer is illustrated in Fig. 4. A folded architecture is utilized to increase the operating headroom of MOS transistors. In the first stage, the current from the CS-DAC is mirrored to the PMOS differential pair (M3:M4) with a gain of 4. The differential pair operates linearly over a differential swing of 400mV for

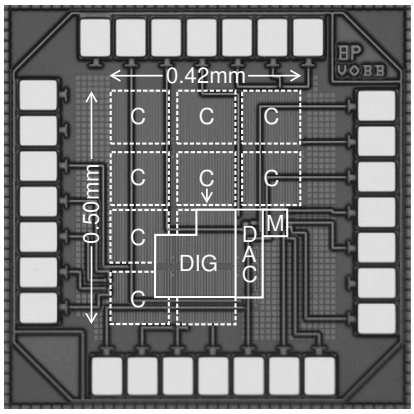


Fig. 5. Die microphotograph (C: Capacitor, M: Mixer, DIG: Digital).

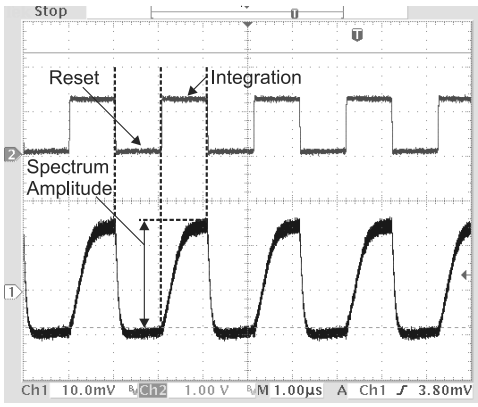
the RF signal. The output currents are then mirrored to the second stage with a gain of 0.125.

The second stage of the integrating mixer consists of a mixing quad (M5:M8) with capacitive loads. In reset mode, $\overline{\mathrm{rs}} = 0\mathrm{V}$ is applied to the PMOS transistors M1 and M2 in parallel with the capacitive loads such that both terminals of the capacitors are at $\mathrm{V_{DD}}$ and the capacitors discharge while the accumulated AC signal resets. In the integration mode, $\overline{\mathrm{rs}} = \mathrm{V_{DD}}$ is applied to the PMOS transistors, the capacitors supply DC bias current while simultaneously integrating the AC signal after LO downconversion. The differential IF signal at the end of the integration period is the magnitude of the power spectrum at the LO frequency while the BW of the window function (i.e. f_w) is the detection BW (DBW). A buffered version of the IF signal is available off-chip through common-drain buffers (M13:M16), which allows debugging of the analog integrator waveforms.

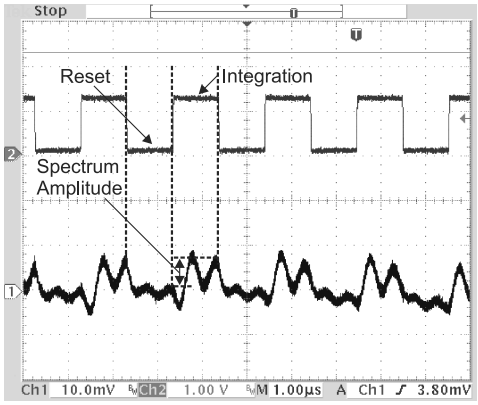
The current in the second stage is minimized to reduce the capacitor size and load. A first order approximation of the voltage drop across the capacitors is $\Delta V_C = I_C \Delta t / C$. In order to achieve an integration time of 1μs and estimating a maximum current of $I_C = 62.5\mu$A for each branch of the mixer, 200pF loads are required for a voltage drop of 300mV. The capacitive loads are broken down into four 50pF parallel capacitors. PMOS switches are utilized to obtain four integration times corresponding to four DBWs: 4MHz (0.25μs), 2MHz (0.5μs), 1.333MHz (0.75μs) and 1MHz (1μs).

V. Implementation Results

The prototype integrating mixer was implemented in a silicon area of $0.18\mathrm{mm}^2$ in IBM's CMRF8SF 0.13μm CMOS process with a 1.2V supply and low-V_t devices for analog components. A die microphotograph is shown in Fig. 5. The capacitive loads were implemented with metal-insulator-metal capacitors (MIMCAPs) and lie above the digital window and control logic. The silicon area not including the MIMCAPs is $0.06\mathrm{mm}^2$. When applying the $\overline{\mathrm{rs}}$ signal with a 50% duty cycle and $f_{\mathrm{LO}} = 3$GHz, the mixer and CS-DAC dissipate 1.31mW, while the digital window and control logic dissipate a further 0.24mW for a total of 1.55mW.



(a) No frequency offset.



(b) 2MHz frequency offset.

Fig. 6. Integrator waveforms.

A. Integrator Waveforms

Integrator waveforms are illustrated in Fig. 6, which demonstrate the operation of the integrating mixer. In each screen capture, the top signal (channel 2) is the $\overline{\mathrm{rs}}$ signal while the bottom signal (channel 1) is the differential IF signal from the on-chip output buffers. The input RF signal in each case is a sinusoid at $f_{\mathrm{RF}} = 3$GHz.

In Fig. 6(a), there is no frequency offset and the DC value is clearly integrated over a 1μs period when $\overline{\mathrm{rs}} = \mathrm{V_{DD}}$, reaching a maximum value at the end of the period. The spectrum magnitude at the LO frequency is the difference between the final and initial amplitude of the integration period (polarity is phase dependent). There is a sharp drop in the differential IF signal when $\overline{\mathrm{rs}} = 0\mathrm{V}$ as the IF signal resets and the capacitors discharge. In Fig. 6(b), there is a 2MHz offset ($f_{\mathrm{LO}} = 2.998$GHz) and the signal across the integrator is sinusoidal, approximately spanning two periods. The final integrator value is no longer the maximum amplitude during the integration period. The non-linear shaping of the sinusoidal IF signal is in part due to the window function and a slight DC offset present. In addition, a small amount of the LO signal is integrated when $\overline{\mathrm{rs}} = 0\mathrm{V}$ due to some leakage between the LO and IF ports during the reset mode. However, this does not affect the amplitude calculation.

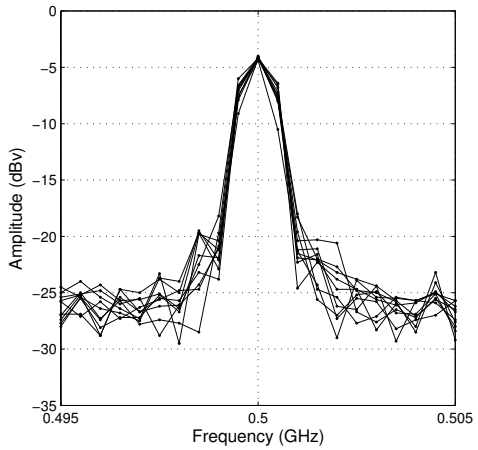


Fig. 7. Spectrum estimate for a single tone at 0.5GHz with -4dBm of power and a DBW of 1MHz (swept over 0.5MHz intervals).

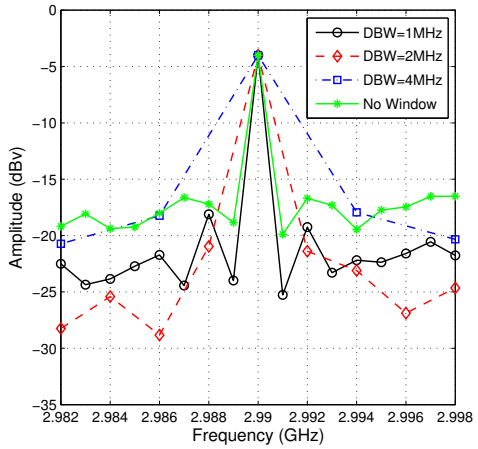


Fig. 8. Spectrum estimates for a single tone at 2.99GHz with -4dBm of power and DBW of 1MHz, 2MHz, 4MHz and with no window applied.

B. Spectrum Estimation and Comparison

The measured power spectrum of a single tone at 0.5GHz with an input power of -4dBm is shown in Fig. 7. The spectrum overlays 10 spectrum estimates at a DBW of 1MHz with the LO frequency swept over 0.5MHz intervals, which shows spreading of the signal. The average DR is 24dB and the side-lobe oscillations are suppressed by 19dB. The DR is calculated as the difference between the noise floor and the integrated signal for the maximum input power. The average DR across the full BW is 24dB for all DBW's except 4MHz, which has an average DR of 21dB. The total harmonic distortion for a sinusoidal tone at 0.5GHz is 3.9%. In Fig. 8, measured spectrum estimates are shown for different DBWs and with no window applied ($\alpha = 1$) for a single tone at 2.99GHz with an input power of -4dBm. The LO frequency is swept over the respective DBW. As expected, side-lobe oscillations are largest for no windowing. One full sweep over the entire 2.95GHz frequency band with dual integrating mixers takes 5.9ms with a 1MHz DBW and a $\overline{\text{rs}}$ signal with 50% duty ratio. That time drops to 1.5ms with a 4MHz DBW.

TABLE I

COMPARISON OF ENERGY-BASED SPECTRUM SENSING IMPLEMENTATIONS.

	[1]	[2]	[3]	Proposed
Technology	0.18μm	0.18μm	90nm	0.13μm
Supply (V)	1.8	1.8	1.2	1.2
Power (mW)	59.9[a]	42.8[a]	30-44[b]	**2.5**[c]
DR (dB)	32	24	29-48	21,24[d]
Range (GHz)	0.4-0.9	0.4-0.9	0.03-2.4	**0.05-3**
DBW (MHz)	0.025-1	0.025-1	0.2-30	1-4

[a] Power for analog correlator and digital window generation.
[b] Power for entire receiver.
[c] Estimated power for a dual mixer based on single mixer.
[d] 24dB for DBW's 1MHz to 2MHz, 21dB for DBW of 4MHz.

In Table I, the proposed integrating mixer is compared with recent energy-based spectrum sensing implementations [1]-[3]. The proposed design operates over the largest frequency range and consumes an-order-of-magnitude less power while obtaining a DR of 24dB, equal to [2]. The DR can further be improved by incorporating DC offset cancellation. The noise floor is -28dBm (DBW=1MHz) without gain prior to the integrating mixer. To reach a sensitivity of -83dBm (equal to that of [3]), the proposed design would require an analog front end with a low-noise amplifier and gain stages that provide a gain of 55dB. The DBW of the proposed design is limited by the integrating capacitor size but maintains a respectable minimum of 1MHz. If larger capacitors were utilized the DBW would improve while maintaining the same power dissipation at the cost of area. With the trend of increasing BW and the need for fast and low-power solutions, a DBW of 1MHz may be an acceptable design trade-off. The proposed design is also well suited as the first in a dual-stage sensing process to quickly identify potential vacant spectrum for detailed sensing with a method such as feature detection.

VI. CONCLUSION

A prototype chip for direct spectrum estimation was fabricated in 0.13μm CMOS that consists of a folded architecture that combines mixing, current-domain windowing and integration to implement the STFT. The design operates over a frequency range of 0.05-3GHz, consumes 1.55mW from a 1.2V supply and obtains a DR of 24dB. The architecture results in power consumption an order-of-magnitude lower than previously reported while obtaining fast spectral estimates over the full BW in as little as 1.5ms.

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