A Passive Resonant Clocking Network for Distribution of a 2.5-GHz Clock in a Flash ADC

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***Abstract*—This paper analyzes the impact of clock skew between comparators in a flash ADC, showing that the SNDR penalty introduced by this effect can become significant at high frequencies. To address this issue, a passive resonant clock network is proposed to distribute the clock to the comparators in a flash ADC. The inductive termination of this network serves to resonate out the parasitic and input capacitances of the ADC, allowing for a 2.5-GHz clock signal to be conveyed to a load of 256 comparators while consuming less power than traditional clock networks due to the reduced number of active clock buffers required. This clock network produces little timing skew at the resonant frequency, thereby obviating the need for a track-and-hold amplifier, which further reduces the power requirements of the ADC. This clock network was implemented in a 5-bit flash ADC designed in 65 nm CMOS, with a measured SNDR of 26 dB.**

I. Introduction

Analog equalization, decision-feedback equalization, and pulse amplitude modulation, have become common in high-performance wireline transceivers. But the complexity involved in such techniques is resulting in a trend towards fully ADC-based transceivers that would move complex equalization and clock recovery blocks into the digital domain. Results have shown that feed-forward digital clock and data recovery is possible up to 10 Gb/s [1].

However, as clock speeds continue to increase, skew arising from the clock distribution to individual comparators within the ADC can begin to degrade the performance. This problem is illustrated for a flash ADC in Fig. 1 where the difference between clock phases, ϕ, increases with both the length of the physical wire connecting the clock to each comparator and the frequency of the clock itself. In this paper skew refers to the deterministic differences in timings caused by differences in the physical layout of the clock distribution path, and is analyzed independently from random timing noise (i.e. jitter), whose effects on ADCs have been characterized [2]. The effects of skew in a flash ADC are mitigated using a track and hold amplifier (THA), however it is becoming increasingly difficult since THAs become power-hungry and difficult to design at high frequencies, presenting a strong motivation for alternative approaches [3].

This paper first presents an analysis of the increasingly important problem of clock skew between flash ADC comparators (lacking a full-rate front-end THA), quantifying its impact on ADC resolution. Then, in an effort to address this issue in a power-efficient way, this paper proposes the use of a passive, resonant clock path. This path uses an inductor to resonate out the interconnect parasitic capacitance as well as the input capacitance of the subsequent clock buffer stages as shown in Fig. 2. In addition to the power savings achieved through the use of passive clock distribution, this technique reduces significantly the skew experienced on the clock line when operating at frequencies close to the resonant frequency of the clock path. By eliminating the skew in this way, the THA that is commonly found at the input of a high-speed ADC can be omitted, simplifying the design and affording further power savings.

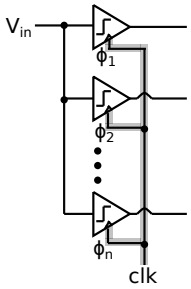


Fig. 1. Increasing the length of the wire connecting the clock to each comparator and the frequency of the clock itself can increase skew in a flash ADC.

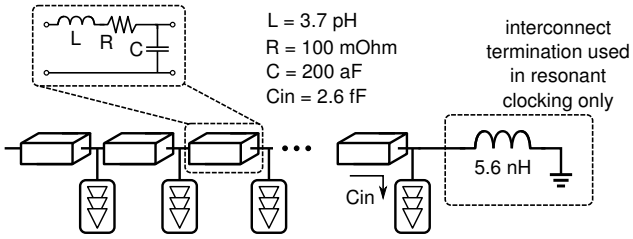


Fig. 2. Interconnect modeled as a transmission line periodically loaded by clock buffers.

II. Relating Skew to SNDR in a Flash ADC

In order to evaluate the effect that this resonant clock network has on circuit performance, it is useful to relate skew to SNDR. Skew in clock arrival time between different points in the comparator array degrades the performance of a flash ADC by effectively introducing a threshold offset as shown in Fig. 3.

If the input signal to the ADC is a sinusoid, it can be represented as:

$$v = \sin\left(2\pi f_{in} t\right), \tag{1}$$

and we can calculate the effective threshold offset, Δv, result-

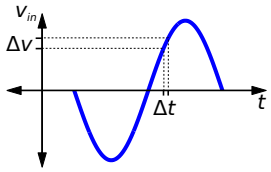


Fig. 3. Clock skew Δt introduces an effective threshold shift given by ΔV.

ing from skew Δt as:

$$v + \Delta v = \sin\left[2\pi f_{in}(t + \Delta t)\right] \quad (2)$$

$$\Delta v = \sin\left[2\pi f_{in}(t + \Delta t)\right] - v \quad (3)$$

$$\Delta v = \sin\left[2\pi f_{in}\left(\frac{\sin^{-1}(v)}{2\pi f_{in}} + \Delta t\right)\right] - v \quad (4)$$

$$\Delta v = \sin\left[\sin^{-1}(v) + 2\pi T_{skew}\right] - v, \quad (5)$$

Where $T_{skew} = f_{in}\Delta t$. The change in threshold voltage introduced by skew can in turn be thought of as the addition of some quantization noise, V_Q to the ADC. If we define a N-bit quantizer as a set of threshold levels m_i and output levels n_i located at:

$$m_i = \frac{1}{2}\,\text{LSB}, \frac{3}{2}\,\text{LSB}, ..., \left(2^N - \frac{3}{2}\right)\,\text{LSB} \quad (6)$$

$$n_i = 0,\ \text{LSB}, \ldots \left(2^N - 1\right)\ \text{LSB} \quad (7)$$

then P_{nai}, the added noise power due to threshold offset on comparator i, can be calculated for an N-bit flash ADC as

$$P_{nai} = \frac{1}{V_{FSR}} \int_{m_i}^{m_i + \Delta v_i} \Delta V_Q^2 \, dv_{in} \quad (8)$$

$$= \left(\frac{1}{(2^N - 1)\text{LSB}}\right) \int_{m_i}^{m_i + \Delta v_i} \left[(v_{in} - n_i)^2 - (v_{in} - n_{i+1})^2\right] dv_{in} \quad (9)$$

$$= \left(\frac{1}{(2^N - 1)\text{LSB}}\right) (1\ \text{LSB})\, \Delta v_i^2 \quad (10)$$

$$= \left(\frac{\Delta v_i^2}{2^N - 1}\right) \quad (11)$$

Since there are $2^N - 1$ thresholds, the total noise added due to threshold offsets on all comparators is:

$$P_{\text{na}} = \sum_{i=1}^{2^N - 1} \left(\frac{1}{2^N - 1}\right) \Delta v_i^2 \quad (12)$$

where the Δv_i are the skew-induced threshold shifts for each comparator as given by equation (5) for a sinusoidal input. Note that although this equation introduces some inaccuracy since the constant weighting factor of $2^N - 1$ assumes uniform distribution of the input, this inaccuracy will be small for large N.

Having translated skew to some added noise power, we can then use this to describe its impact on the SNDR of the ADC as:

$$SNDR = \frac{P_{signal}}{P_{ni} + P_{na}} \quad (13)$$

where P_{ni} is the ideal quantization noise power obtained when the decision thresholds are at their optimal locations.

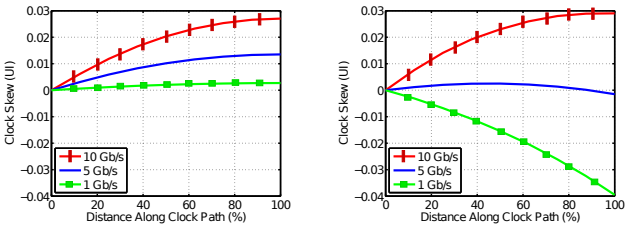


Fig. 4. Clock skew vs. position for (a) the interconnect shown in Fig. 2, (b) the same interconnect terminated with a 5.6 nH inductor.

The above analysis provides the tools required to evaluate the impact of skew on SNDR by:

1) Given a set of clock skews, calculate a set of threshold shifts using equation (5).
2) Use these threshold shifts to calculate the noise added using equation (12).
3) Calculate SNDR using equation (13).

As an example, in order for a 5-bit Flash ADC to achieve an ENOB of 4.5 for a 10-GHz input signal, the standard deviation of the clock skew must remain below 0.4% of one period of the input signal, or 400 fs. This level of skew can be introduced by as little as an 80-μm mismatch in clock path length or a small mismatch in capacitive loading along the clock paths, which highlights the importance of this problem as clock frequencies continue to increase. The following section proposes the use of passive resonant clocking as a power-efficient solution to this problem.

III. Resonant Clock Path

Resonant clock paths have previously been used to distribute a clock throughout a wireline transceiver system [4]. Such clock paths offer lower power than buffer-based clock distribution and, since there are fewer buffers in the clock path, better immunity to power supply-induced jitter. Here the same technique is used to distribute the clock to a comparator array in a flash ADC. The main difference is that in a multi-channel wireline transceiver clock skew between lanes is removed by per-channel clock recovery. In a flash ADC with no THA, clock skew between comparators directly degrades SNDR and must therefore be considered.

Using the transmission line model shown in Fig. 2, simulations of clock skew along the length of an RLC delay line were performed for three different clock rates. The results are shown in Fig. 4. This simulation assumes that the comparators in the ADC are arranged in order of threshold voltage along the clock-distribution line from which they receive their sampling clock. In a traditional clocking scheme skew measured in UI increases as the sampling frequency increases. In contrast, resonant clocking can produce approximately zero skew at any single desired frequency, ω_{clk} = 5 GHz in the case of Fig. 4(b). The value of the 5.6-nH inductor, L_{term}, used to terminate the clock path, was chosen to resonate with the simulated total capacitive load C_{in}, of the resonant clock line, according to

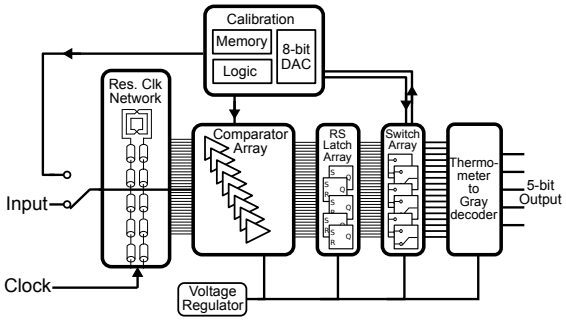


Fig. 5. Block diagram of the prototype 5-bit flash ADC including resonant clock network and redundant comparators.

the equation

$$\omega_{clk} = \frac{1}{\sqrt{L_{term}C_{in}}}. \tag{14}$$

This equation makes it clear that any variation in L_{term} may cause the network to resonate at an undesired frequency. To compensate for this, it may be necessary to add some variable capacitance that can be used to calibrate the line.

IV. Measured Results

The ADC resolution required of course depends upon the application. For serial chip-to-chip communication, generally at least 4.5 bits are necessary [5]. In this work, a 5-bit flash ADC was chosen as the architecture used to demonstrate the proposed resonant clocking scheme in 65 nm CMOS. The ADC makes use of redundant comparators in an effort to reduce mismatch and power, as described in [6], [7]. A block diagram of this prototype ADC, including the resonant clock network and redundant comparator banks is shown in Fig. 5.

In this implementation, the redundant comparators are arranged in 32 groups of 8, resulting in a total of 256 comparators, each with a width of 2 μm for the input transistors. Each group of 8 comparators is followed by an 8-to-1 switch and the 31 thermometer-coded outputs are then decoded into a 5-bit gray code, with the 32nd comparator included for balance. The prototype also contains an on-chip calibration block that includes a differential 8-bit DAC as well as memory to store the locations of the chosen comparators [8]. All blocks are powered by an on-chip regulator. A switch at the ADC input allows either normal operation or calibration mode, but does not act as a THA. A die photo of the ADC is shown in Fig. 6.

A. Clock Path Bandwidth

Although direct examination of the bandwidth of the clock path was not possible, it was possible to obtain an estimate by measuring the hysteresis in the comparators. Hysteresis exists when the threshold depends on the previous decision; it is equal to the difference between the two observed thresholds. Ideally the comparator should have little hysteresis, but it can occur when there is insufficient swing, or significant duty-cycle distortion on the clock. Since the resonant clock path is narrow-band by nature, both of these effects may be expected when the resonant clock distribution is driven far from its

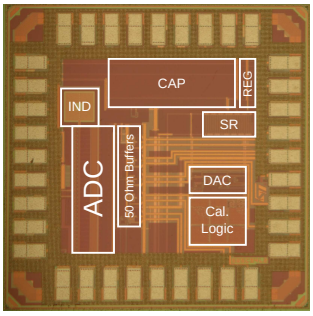
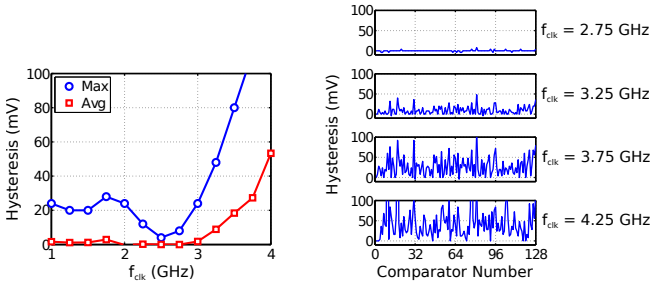


Fig. 6. Die photo of the test chip with ADC and inductor. Die area is $1\,\mathrm{mm}^2$. ADC and inductor combined area is $0.07\,\mathrm{mm}^2 + 0.01\,\mathrm{mm}^2 = 0.08\,\mathrm{mm}^2$.



(a) (b)

Fig. 7. Measurement of comparator hysteresis vs. f_{clk} indicating a centre frequency for the resonant clock path of approximately 2.5 GHz.

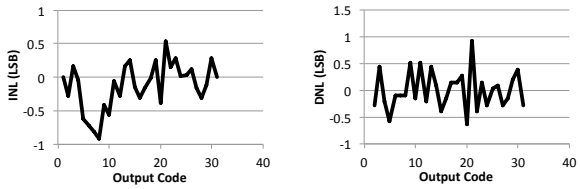
resonant frequency, allowing the amount of hysteresis to be used to indicate the location of this frequency.

Fig. 7 shows measured hysteresis for 128 comparators as clock frequency is changed and indicates that the centre frequency of the resonant clock path is approximately 2.5 GHz with acceptably low hysteresis between 2 and 3 GHz. Note that this frequency is lower than the 5 GHz frequency reported earlier due to the increased parasitic capacitance of the clock path and comparator inputs obtained from extraction of the physical layout, which was not included in earlier simulations.

B. Linearity

After calibration and selection of the comparators that minimize nonlinearity, measurement of the ADC was performed at the clock centre frequency of 2.5 GHz. INL and DNL measurements are shown in Fig. 8. The results of a 4096-point measurement for a sinusoidal input are shown in Fig. 9, giving an SNDR of 26.0 dB or 4.0 effective bits.

The SNDR is then plotted versus sampling frequency, and input frequency in Fig. 10(a). These results indicate that the



(a) INL (b) DNL

Fig. 8. Measured INL and DNL of the calibrated ADC.

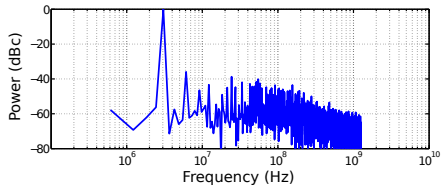
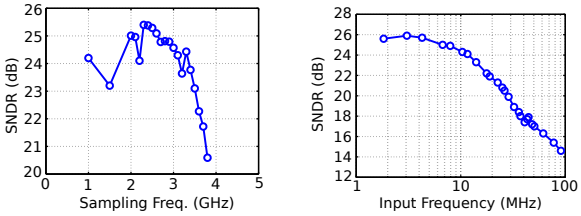


Fig. 9. Measurement of the 4096-point ADC output spectrum. Computed SNDR is 26.0 dB.



(a) $F_{in} \approx 10\,MHz$ (b) $F_{clk} = 2.5\,GHz$

Fig. 10. Measurement of (a) SNDR vs. sampling frequency and (b) SNDR vs. input frequency.

resonant frequency of the clock network is approximately 2.5 GHz. Unfortunately, some unmodeled and unbalanced capacitance in the decoding logic of the prototype limited the input bandwidth to approximately 20 MHz, as shown in Fig. 10(b). This problem was identified and duplicated in simulations and is independent of the resonant clock path, whose effectiveness is demonstrated by the correct operation of the ADC using low-frequency input signals.

C. Power Consumption

After calibration the power consumption of the entire chip was measured. Besides the constant approximately 7 mW static power consumed by the clock input matching circuit and the voltage regulator, ADC power increases linearly with the clock frequency used, as shown in Fig. 11.

The power efficiency is 5mW/GS/s, which is better than previously-reported ADCs operating at similar speeds with a traditional clock distribution network as can be seen by the comparison to other recently published 5-bit flash ADC architectures [9], [10], [11] in Fig. 12. This low power is a direct result of the absence of a THA and the low-power clock path, both of which are enabled by the resonant clock network.

V. Conclusions

Removing the THA from the input of a flash ADC can reduce design complexity and save power but can lead to performance degradation caused by timing skew in the clock distribution network. The resolution penalty arising from this skew has been analyzed and quantified and shows that in order to achieve an ENOB of 4.5 for a 10-GHz input signal, the standard deviation of the clock skew must remain below 400 fs.

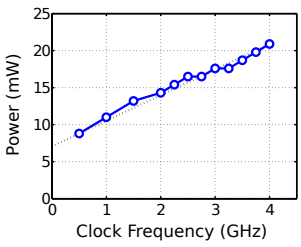


Fig. 11. Measurement: ADC power versus clock frequency.

Fig. 12. Comparison of the measured power consumption to other single-channel 5-bit flash ADC architectures.

Replacing the traditional clock network with a passive resonant clock structure is shown to be a power-efficient technique for alleviating this penalty. The resonant clock architecture presented in this paper is able to distribute a 2.5 GHz clock in a 5-bit flash ADC with 8x comparator redundancy without the extensive network of clock buffers that would normally be required. The relationship between timing skew and SNDR has been defined and measurements of a 5-bit flash ADC fabricated using this clock network in 65 nm CMOS show an SNDR of 26 dB and lower power than other comparable architectures.

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