All-Digital Calibration of Timing Mismatch Error in Time-Interleaved Analog-to-Digital Converters

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***Abstract*— This paper presents an all-digital background calibration for timing mismatch in time-interleaved analog-to-digital converters (TI-ADCs). It combines digital adaptive timing mismatch estimation and digital derivative-based correction, achieving lower hardware cost and better suppression of timing mismatch tones than previous work. In addition, for the first time closed-form exact expressions for the signal-to-noise and distortion ratio (SNDR) of a four-channel TI-ADC with timing mismatch after derivative-based digital correction are obtained, which can be used to guide the design. Simulation results of a four-channel TI-ADC behavioral model and measurement results from a commercial 12-bit 3.6-GS/s two-channel TI-ADC show that the proposed all-digital calibration can accurately estimate the timing skew and effectively correct the timing mismatch errors, while also confirming the analytic SNDR expressions.**

***Index Terms*— All-digital calibration, analog-to-digital converter (ADC), derivative, finite-impulse response (FIR) filter, time interleaving (TI), timing mismatch.**

I. Introduction

DATA communication systems such as full-band capture cable tuners and baseband backplane/optical receivers require the use of high-speed analog-to-digital converters (ADCs) [1]. By exploiting multiple sub-ADCs operating in parallel, a time-interleaved (TI) ADC can achieve a high aggregate sampling rate. The input signal is sequentially sampled and digitized by the sub-ADCs in turn in a round-robin fashion. However, gain, offset, and timing mismatches between the sub-ADCs can significantly degrade the signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of the TI-ADC. Although large transistor size and careful layout can alleviate these mismatches, these solutions are area-hungry and impractical for high-resolution applications [2]. Therefore, much work has focused on the calibration of these mismatch errors in TI-ADCs. Whereas gain and offset calibration are relatively simple, the calibration of timing mismatch error remains a significant challenge [3]–[20], and is the focus of this paper.

Techniques for timing mismatch calibration can be divided into two categories: mixed-signal and all-digital. Mixed-signal correction employs an analog variable delay line (VDL) in each sub-ADC's clock path to compensate the timing skew [4]–[12], whereas a digital approach directly corrects the TI-ADC outputs using digital signal processing (DSP) [13]–[20]. Although an analog correction obviates the need for complex DSP, it is subject to process, voltage, and temperature (PVT) variations and the additional jitter introduced by the VDL. Digital calibration is immune to PVT variations and well-suited to scaled CMOS technologies, therefore attracting recent interest.

Conventional all-digital calibration uses a bank of adaptive finite-impulse response (FIR) filters, but accommodating the dynamic filter coefficients consumes relatively high power and area [13]–[15]. A more power/area-efficient approach is to leverage a first-order Taylor approximation to eliminate the timing mismatch error, which requires only a derivative FIR filter with fixed coefficients. This derivative-based method requires the estimation of timing mismatch in each sub-ADC after the first-order derivative of the TI-ADC output is obtained by the filter. In [17], an open-loop method for timing mismatch estimation is demonstrated; however, the estimation accuracy is insufficient for large timing mismatches and the hardware cost is considerable. In [18] and [19], an extra FIR derivative filter is employed to estimate timing mismatch in closed loop for better accuracy'Cbut at the expense of significant added hardware cost. In this paper, we combine the derivative-based digital correction with our proposed timing mismatch detection algorithm in [10], achieving more accurate timing mismatch estimation than [17] and lower hardware cost than [17]–[19]. In addition, the analysis on a four-channel TI-ADC with timing mismatch before and after the derivative-based digital correction is presented. For the first time closed-form expressions are obtained to calculate SNDR and the bound on the maximum tolerable timing mismatch, providing important guidance for designers.

The remainder of this paper is organized as follows. Section II provides an analysis of TI-ADC timing mismatch errors before and after derivative-based digital correction. Section III describes the proposed all-digital timing mismatch calibration technique. Simulation results of the proposed all-digital calibration for a four-channel TI-ADC and measurement results for a two-channel TI-ADC are given in Section IV. Finally, Section V describes the conclusions.

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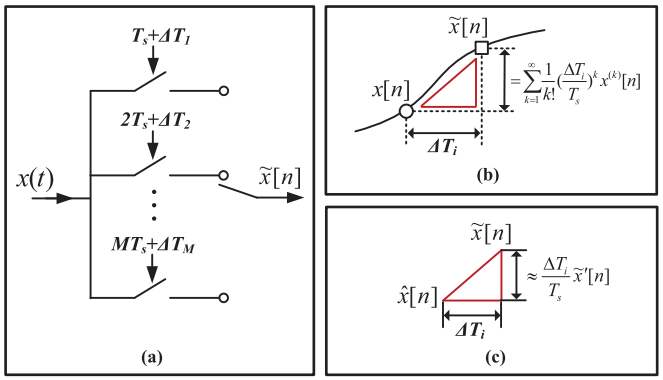

Fig. 1. Sampling diagram of a TI-ADC with timing mismatch. The number of sub-ADC channels is M and $i = 1, 2, \ldots M$. The sampling period of the TI-ADC is T_s, and the timing skew of the ith sub-ADC is ΔT_i. $\tilde{x'}[n]$ and $x^{(k)}[n]$ represent the first-order derivative of $\tilde{x}[n]$ and the k-order derivative of $x[n]$. (a) M-channel TI-ADC with timing mismatch. (b) Sampling in the ith sub-ADC. (c) Derivative-based correction.

II. Analysis of Derivative-Based Digital Correction

As shown in Fig. 1(a), timing mismatch in a TI-ADC causes nonuniform sampling of the input due to the clock skew ΔT_i. In the ith sub-ADC, the error between the obtained samples $\tilde{x}[n]$ and the ideal samples $x[n]$ without timing mismatch can be approximated by the Taylor expansion in terms of $x[n]$ and ΔT_i, as described in Fig. 1(b). Hence, if the first-order derivative of $x[n]$ and the value of the timing mismatch ΔT_i are known, the first-order Taylor approximation can be used to estimate the error and subtract it from $\tilde{x}[n]$, resulting in the digitally corrected output $\hat{x}[n]$ in Fig. 1(c).

For a four-channel TI-ADC ($M = 4$), the samples $\tilde{x}[n]$ are expressed as

$$\tilde{x}[n] = \begin{cases} x[n], & n = 1,\ 5,\ 9\ \ldots \\ x[n] + \sum_{k=1}^{\infty} \frac{1}{k!} r_2^k x^{(k)}[n], & n = 2,\ 6,\ 10\ \ldots \\ x[n] + \sum_{k=1}^{\infty} \frac{1}{k!} r_3^k x^{(k)}[n], & n = 3,\ 7,\ 11\ \ldots \\ x[n] + \sum_{k=1}^{\infty} \frac{1}{k!} r_4^k x^{(k)}[n], & n = 4,\ 8,\ 12\ \ldots \end{cases} \tag{1}$$

where the sub-ADC1 is taken as the reference channel and the normalized timing mismatches $r_{2\sim4} = (\Delta T_{2\sim4} - \Delta T_1)/T_s$. Using the terms $e^{j\pi/2n}$, $e^{j\pi/2(n-1)}$, and $e^{j\pi n}$, the equations in (1) can be merged into one equation

$$\begin{aligned} \tilde{x}[n] = x[n] &+ \frac{(1+e^{j\pi n})(1-e^{j\frac{\pi}{2}n})}{4} \sum_{k=1}^{\infty} \frac{1}{k!} r_2^k x^{(k)}[n] \\ &+ \frac{(1-e^{j\pi n})(1-e^{j\frac{\pi}{2}(n-1)})}{4} \sum_{k=1}^{\infty} \frac{1}{k!} r_3^k x^{(k)}[n] \\ &+ \frac{(1+e^{j\pi n})(1+e^{j\frac{\pi}{2}n})}{4} \sum_{k=1}^{\infty} \frac{1}{k!} r_4^k x^{(k)}[n]. \end{aligned} \tag{2}$$

Reordering (2) into

$$\begin{aligned} \tilde{x}[n] = x[n] &+ \frac{1}{4} \sum_{k=1}^{\infty} \frac{1}{k!} \left(r_2^k + r_3^k + r_4^k\right) x^{(k)}[n] \\ &+ \frac{e^{j\pi n}}{4} \sum_{k=1}^{\infty} \frac{1}{k!} (r_2^k - r_3^k + r_4^k) x^{(k)}[n] \\ &+ \frac{e^{j\frac{\pi}{2}n}}{4} \sum_{k=1}^{\infty} \frac{1}{k!} \left(-r_2^k + j r_3^k + r_4^k\right) x^{(k)}[n] \\ &+ \frac{e^{j\frac{3\pi}{2}n}}{4} \sum_{k=1}^{\infty} \frac{1}{k!} \left(-r_2^k - j r_3^k + r_4^k\right) x^{(k)}[n]. \end{aligned} \tag{3}$$

Note that the terms $e^{j\pi n}$, $e^{j\pi/2n}$, and $e^{j3\pi/2n}$ represent frequency shifts, and the frequency response of a derivative filter is $H_d(e^{j\omega}) = j\omega$, $-\pi < \omega < \pi$; the discrete-time Fourier transform (DTFT) of (3) is

$$\begin{aligned} &\tilde{X}(e^{j\omega}) \\ &= \left[1 + \frac{1}{4} \sum_{k=1}^{\infty} \frac{1}{k!} (r_2^k + r_3^k + r_4^k) H_d^k(e^{j\omega})\right] X(e^{j\omega}) \\ &\quad + \frac{1}{4} \sum_{k=1}^{\infty} \frac{1}{k!} (r_2^k - r_3^k + r_4^k) H_d^k(e^{j(\omega-\pi)}) X(e^{j(\omega-\pi)}) \\ &\quad + \frac{1}{4} \sum_{k=1}^{\infty} \frac{1}{k!} (-r_2^k + j r_3^k + r_4^k) H_d^k\left(e^{j(\omega-\frac{\pi}{2})}\right) X\left(e^{j(\omega-\frac{\pi}{2})}\right) \\ &\quad + \frac{1}{4} \sum_{k=1}^{\infty} \frac{1}{k!} (-r_2^k - j r_3^k + r_4^k) H_d^k\left(e^{j(\omega-\frac{3\pi}{2})}\right) X\left(e^{j(\omega-\frac{3\pi}{2})}\right). \end{aligned} \tag{4}$$

Using the following equation:

$$\sum_{k=1}^{\infty} \frac{1}{k!} r^k H_d^k(e^{j\omega}) = e^{r H_d(e^{j\omega})} - 1 \tag{5}$$

(4) can be rewritten as

$$\begin{aligned} \tilde{X}(e^{j\omega}) = C_1 X(e^{j\omega}) + C_2 X(e^{j(\omega-\pi)}) + C_3 X\left(e^{j(\omega-\frac{\pi}{2})}\right) \\ + C_4 X\left(e^{j(\omega-\frac{3\pi}{2})}\right) \end{aligned} \tag{6}$$

where

$$\begin{cases} C_1 = \frac{1}{4}(e^{r_2 H_d(e^{j\omega})} + e^{r_3 H_d(e^{j\omega})} + e^{r_4 H_d(e^{j\omega})} + 1) \\ C_2 = \frac{1}{4}(e^{r_2 H_d(e^{j(\omega-\pi)})} - e^{r_3 H_d(e^{j(\omega-\pi)})} + e^{r_4 H_d(e^{j(\omega-\pi)})} - 1) \\ C_3 = \frac{1}{4}\Big(-e^{r_2 H_d\left(e^{j(\omega-\frac{\pi}{2})}\right)} + j e^{r_3 H_d\left(e^{j(\omega-\frac{\pi}{2})}\right)} \\ \qquad\qquad + e^{r_4 H_d\left(e^{j(\omega-\frac{\pi}{2})}\right)} - j\Big) \\ C_4 = \frac{1}{4}\Big(-e^{r_2 H_d\left(e^{j(\omega-\frac{3\pi}{2})}\right)} - j e^{r_3 H_d\left(e^{j(\omega-\frac{3\pi}{2})}\right)} \\ \qquad\qquad + e^{r_4 H_d\left(e^{j(\omega-\frac{3\pi}{2})}\right)} + j\Big). \end{cases} \tag{7}$$

For a sinusoidal input $x[n]=\cos(\omega_{\text{in}}n)$ with $\omega_{\text{in}}=2\pi f_{\text{in}}/f_s$ and small r_{2-4}, (7) can be simplified into

$$\begin{cases}|C_1|^2\approx 1, |C_2|^2\approx \dfrac{1}{16}\omega_{\text{in}}^2(r_2-r_3+r_4)^2\\ |C_3|^2=|C_4|^2\approx \dfrac{1}{16}\omega_{\text{in}}^2\left[(r_2-r_4)^2+r_3^2\right].\end{cases}\tag{8}$$

According to (6) and (8), for a B-bit four-channel TI-ADC with normalized timing mismatches $r_{2\sim4}$ and a sinusoidal input at f_{in}, the output spectrum contains three timing mismatch distortion tones located at $f_s/2-f_{\text{in}}$, $f_s/4-f_{\text{in}}$, and $f_s/4+f_{\text{in}}$ when $f_{\text{in}}<f_s/4$ or $f_s/2-f_{\text{in}}$, $f_{\text{in}}-f_s/4$, and $3f_s/4-f_{\text{in}}$ when $f_{\text{in}}>f_s/4$. The SNDR including the quantization noise and timing mismatch distortion tones without calibration is

$$\text{SNDR}=\frac{1}{\frac{1}{6}\left(\frac{2}{2^B}\right)^2+\frac{1}{4}\pi^2[(r_2-r_3+r_4)^2+2(r_2-r_4)^2+2r_3^2]\left(\frac{f_{\text{in}}}{f_s}\right)^2}.\tag{9}$$

Assuming the bound of the timing skew is $\Delta T_{1-4}\in[\Delta T_{\min},\Delta T_{\max}]$, the worst SNDR in (9) arises when $r_2=r_4=\pm r_{\max}$ and $r_3=0$, and $r_{\max}=(\Delta T_{\max}-\Delta T_{\min})/T_s$

$$\text{SNDR}_{\text{worst}}=\frac{1}{\frac{1}{6}\left(\frac{2}{2^B}\right)^2+\pi^2 r_{\max}^2\left(\frac{f_{\text{in}}}{f_s}\right)^2}.\tag{10}$$

Using the same approach, one can also obtain the SNDR after the derivative-based digital timing mismatch correction. In accordance with Fig. 1(c), the digitally corrected output $\hat{x}[n]$ can be expressed as

$$\hat{x}[n]=\begin{cases}\tilde{x}[n], & n=1,\ 5,\ 9\ \ldots\\ \tilde{x}[n]-r_2\tilde{x}'[n], & n=2,\ 6,\ 10\ \ldots\\ \tilde{x}[n]-r_3\tilde{x}'[n], & n=3,\ 7,\ 11\ \ldots\\ \tilde{x}[n]-r_4\tilde{x}'[n], & n=4,\ 8,\ 12\ \ldots..\end{cases}\tag{11}$$

The equations in (11) can be merged into

$$\begin{aligned}\hat{x}[n]=\tilde{x}[n]&-\frac{(1+e^{j\pi n})(1-e^{j\frac{\pi}{2}n})}{4}r_2\tilde{x}'[n]\\&-\frac{(1-e^{j\pi n})(1-e^{j\frac{\pi}{2}(n-1)})}{4}r_3\tilde{x}'[n]\\&-\frac{(1+e^{j\pi n})(1+e^{j\frac{\pi}{2}n})}{4}r_4\tilde{x}'[n].\end{aligned}\tag{12}$$

Substituting (2) into (12) and ignoring third-order $O(r_{2\sim4}^3)$ and higher-order terms provides an expression for $\hat{x}[n]$ in terms of $x[n]$, $x'[n]$, and $x''[n]$. Then taking the DTFT of $\hat{x}[n]$ and assuming the input is a sinusoid $x[n]=\cos(\omega_{\text{in}}n)$ with $\omega_{\text{in}}=2\pi f_{\text{in}}/f_s$, the SNDR after timing mismatch correction is shown to be

$$\text{SNDR}_{\text{cal}}=\begin{cases}\dfrac{1}{\frac{1}{6}\left(\frac{2}{2^B}\right)^2+|A_1|^2+|A_2|^2+|A_3|^2}, & f_{\text{in}}<\dfrac{f_s}{4}\\ \dfrac{1}{\frac{1}{6}\left(\frac{2}{2^B}\right)^2+|B_1|^2+|B_2|^2+|B_3|^2}, & f_{\text{in}}>\dfrac{f_s}{4}\end{cases}\tag{13}$$

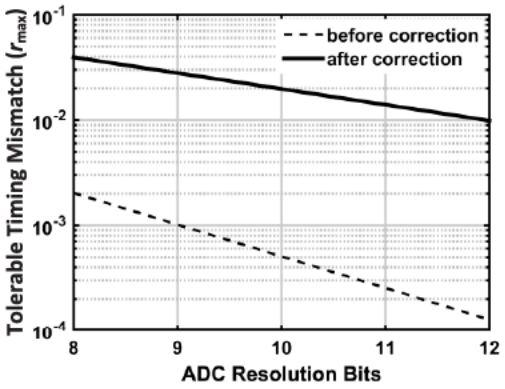

Fig. 2. Maximum tolerable timing mismatch versus resolution for 3-dB SNDR penalty in a four-channel TI-ADC before and after derivative-based digital correction ($f_{\text{in}}=f_s/2$).

where

$$\begin{cases}A_1=\dfrac{\pi^2 f_{\text{in}}}{4f_s}\left[\left(\dfrac{f_{\text{in}}}{f_s}-\dfrac{1}{2}\right)(r_2^2+r_4^2-r_3^2)-r_2r_4+jr_3(r_2-r_4)\right]\\ A_2=\dfrac{\pi^2 f_{\text{in}}}{4f_s}\left(\dfrac{f_{\text{in}}}{f_s}-\dfrac{1}{2}\right)(r_4^2-r_2^2+jr_3^2)\\ A_3=\dfrac{\pi^2 f_{\text{in}}}{4f_s}\left[\left(\dfrac{f_{\text{in}}}{f_s}-\dfrac{1}{2}\right)(r_4^2-r_2^2+jr_3^2)+(1+j)(jr_2r_3+r_3r_4)\right]\end{cases}\tag{14}$$

and

$$\begin{cases}B_1=\dfrac{\pi^2 f_{\text{in}}}{4f_s}\left[\left(\dfrac{f_{\text{in}}}{f_s}-\dfrac{3}{2}\right)(r_2^2+r_4^2-r_3^2)+r_2r_4-jr_3(r_2-r_4)\right]\\ B_2=\dfrac{\pi^2 f_{\text{in}}}{4f_s}\left(\dfrac{f_{\text{in}}}{f_s}-\dfrac{3}{2}\right)(r_4^2-r_2^2-jr_3^2)\\ B_3=\dfrac{\pi^2 f_{\text{in}}}{4f_s}\left[\left(\dfrac{f_{\text{in}}}{f_s}-\dfrac{3}{2}\right)(r_4^2-r_2^2-jr_3^2)-(1+j)(r_2r_3+jr_3r_4)\right].\end{cases}\tag{15}$$

The worst SNDR in (13) arises when $r_{2-4}=r_{\max}$ or $r_{2-4}=-r_{\max}$

$$\text{SNDR}_{\text{cal,worst}}=\frac{1}{\frac{1}{6}\left(\frac{2}{2^B}\right)^2+\frac{11}{16}\pi^4 r_{\max}^4\left(\frac{f_{\text{in}}}{f_s}\right)^4}.\tag{16}$$

According to (10) and (16), Fig. 2 shows the timing mismatch which results in 3-dB SNDR penalty versus ADC resolution for four-channel TI-ADCs. Derivative-based digital correction can improve the timing mismatch tolerance by approximately 76× for a 12-bit TI-ADC.

III. Proposed All-Digital Timing Calibration

The proposed timing mismatch calibration for the ith sub-ADC channel in a TI-ADC is described in Fig. 3(a), which is comprised of two parts: the derivative-based digital corrector and the timing mismatch estimator. The first-order derivative of each sub-ADC's output is obtained from the derivative

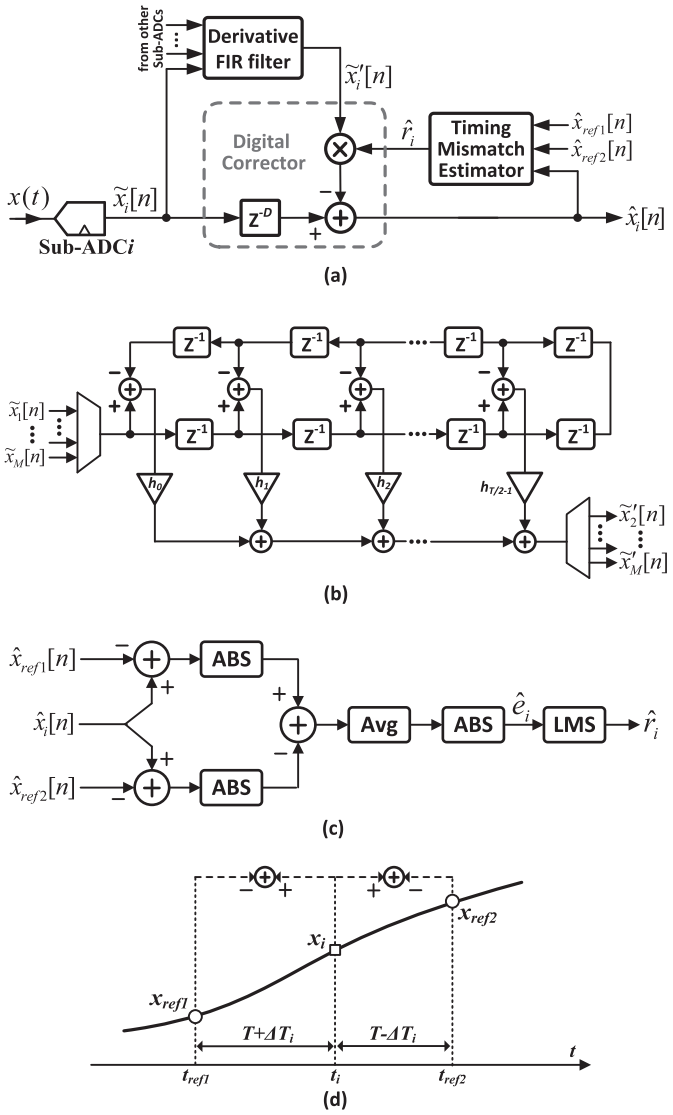

Fig. 3. (a) Proposed all-digital timing mismatch calibration for the ith sub-ADC channel in an M-channel TI-ADC. (b) Derivative FIR filter. (c) Timing mismatch estimator. (d) Sampling waveform.

FIR filter and then multiplied by the estimated timing mismatch $\hat{r}_i$ to generate the timing mismatch error which is finally subtracted from the sub-ADC's output. The delay unit z^{-D} is used to match the delay of the derivative FIR filter. The derivative FIR filter can be designed as a full-rate type-III linear-phase FIR filter as in Fig. 3(b), and is shared by all sub-ADC channels.

As depicted in Fig. 3(c), the timing mismatch estimator for each sub-ADC consists of three adders, three absolute value operators, a moving average calculator, and a least-mean-square (LMS) engine, which requires less hardware than the approaches in [17]–[20]. By collecting and processing the digitally-corrected outputs, the estimator can converge to the real timing mismatch in each sub-ADC and also track the mismatch drift due to PVT variations in background. Timing mismatch estimation for the ith sub-ADC channel requires the outputs from two reference sub-ADC channels (ref1 and ref2) which are equally-spaced before and after the ith sub-ADC channel. Initially, sub-ADC1 channel serves the reference channel and the other channels become the reference channels once after being calibrated. The estimation is iteratively updated to ensure the mean of the difference between the ith sub-ADC corrected output, and the ref1 sub-ADC corrected output is equal to the difference between the ith sub-ADC corrected output and the ref2 sub-ADC corrected output. Hence, the error signals $\hat{e}_i$ for the LMS block in the timing mismatch estimator are

$$\hat{e}_i = \left| \frac{1}{N} \sum_{k=1}^{N} \left(|\hat{x}_i[k] - \hat{x}_{\text{ref1}}[k]| - |\hat{x}_i[k] - \hat{x}_{\text{ref2}}[k]| \right) \right| \tag{17}$$

where N is the number of the sample points collected in every LMS iteration. Fig. 3(d) shows a sampling waveform for $\hat{x}_{\text{ref1}}$, $\hat{x}_i$, and $\hat{x}_{\text{ref2}}$. According to a first-order Taylor approximation, the difference between adjacent samples can be expressed as

$$\begin{aligned} \hat{x}_i[k] - \hat{x}_{\text{ref1}}[k] &= \hat{x}(t_{\text{ref1}} + (T + \Delta T_i)) - \hat{x}(t_{\text{ref1}}) \\ &= (T + \Delta T_i) \cdot \hat{x}'(t_{\text{ref1}}) \end{aligned} \tag{18}$$

$$\begin{aligned} \hat{x}_{\text{ref2}}[k] - \hat{x}_i[k] &= \hat{x}(t_i + (T - \Delta T_i)) - \hat{x}(t_i) \\ &= (T - \Delta T_i) \cdot \hat{x}'(t_i). \end{aligned} \tag{19}$$

Then, the expected values of the squares of (18) and (19) are

$$E[(\hat{x}_i[k] - \hat{x}_{\text{ref1}}[k])^2] = (T + \Delta T_i)^2 \cdot E(\hat{x'}^2_{\text{ref1}}) \tag{20}$$

$$E[(\hat{x}_i[k] - \hat{x}_{\text{ref2}}[k])^2] = (T - \Delta T_i)^2 \cdot E(\hat{x'}^2_i). \tag{21}$$

Since the expected value of the derivative of the signal is constant $E(\hat{x'}^2_i) = E(\hat{x'}^2_{\text{ref1}}) = C$, the difference between (20) and (21) can be written as

$$E](\hat{x}_i - \hat{x}_{\text{ref1}})^2] - E[(\hat{x}_i - \hat{x}_{\text{ref2}})^2] = 4T \cdot C \cdot \Delta T_i \tag{22}$$

which indicates the error signal $\hat{e}_i$ is proportional to the timing mismatch ΔT_i. Therefore, the average value of the difference between $|\hat{x}_i - \hat{x}_{\text{ref1}}|$ and $|\hat{x}_i - \hat{x}_{\text{ref2}}|$ can be used to measure the remaining timing mismatch error after calibration. The estimated timing mismatch $\hat{r}_i$ is updated iteratively by the following sign–sign LMS equation:

$$\hat{r}_i(n+1) = \hat{r}_i(n) - \mu \cdot \hat{e}_i[n] \cdot \frac{\text{sign}(\hat{e}_i[n] - \hat{e}_i[n-1])}{\text{sign}(\hat{r}_i[n] - \hat{r}_i[n-1])} \tag{23}$$

where μ is the LMS adaptation step size.

Fig. 4 shows a four-channel example of the proposed all-digital timing calibration and its estimation sequence. Sub-ADC1 channel is taken as the initial reference channel, so there is no need to calibrate its timing mismatch. First, two consecutive outputs of sub-ADC1 are used to estimate the timing mismatch r_3 in sub-ADC3 channel. After convergence of the sub-ADC3's estimation, its output is considered to be free from timing mismatch and it becomes a reference channel against which the timing mismatches of sub-ADC2 and sub-ADC4 are estimated.

IV. Verification

A. Simulation Result

The proposed all-digital timing mismatch calibration and the derived formulas are verified with a 12-bit 2 GS/s four-channel TI-ADC behavioral model in MATLAB. The derivative FIR filter is designed using the MATLAB function firpm to have 33 taps and a cutoff frequency of $0.42 f_s$.

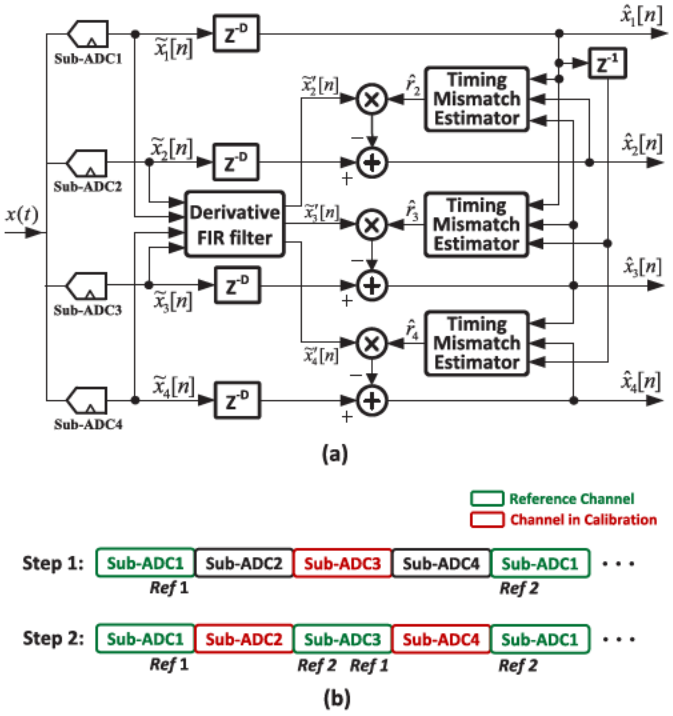

Fig. 4. (a) Four-channel example of the proposed all-digital calibration. (b) Estimation procedure.

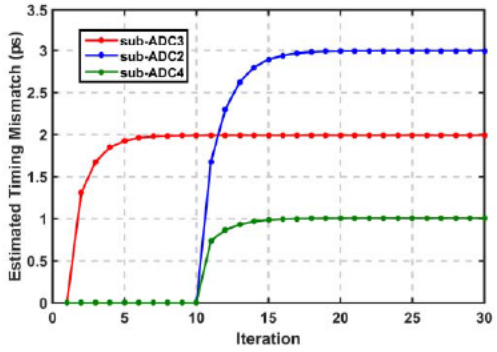

Fig. 5. Convergence of the estimated timing mismatch for a single-tone input at $0.41 f_s$ when ΔT_{1-4} are set at [1, 4, 3, and 2 ps]. SNDR after calibration versus different N for 12-bit resolution.

For a single-tone input at $0.41 f_s (3358/2^{13} \cdot f_s)$, Fig. 5 shows the simulated convergence of the estimated timing mismatches when the real timing mismatches ΔT_{1-4} are set at 1, 4, 3, and 2 ps. The estimator can accurately converge to $\Delta T_{2-4} - \Delta T_1$ with <0.1% error. Fig. 6 shows the output spectra before and after the all-digital timing calibration. All timing mismatch distortion tones are well suppressed and the SNDR increases from 44.78 to 73.81 dB.

Fig. 7 shows the SNDR versus different input sinusoidal frequencies for two different sets of ΔT_{1-4}. The proposed all-digital timing calibration can effectively improve the SNDR within the bandwidth of the derivative FIR filter, and the simulated SNDR matches with the theoretical results obtained from (9) and (13). Often, the input signal is bandlimited somewhat below $0.5 f_s$, so the drop of SNDR at $f_{\text{in}} > 0.42 f_s$ is tolerable. If not, more FIR taps can increase the filter bandwidth.

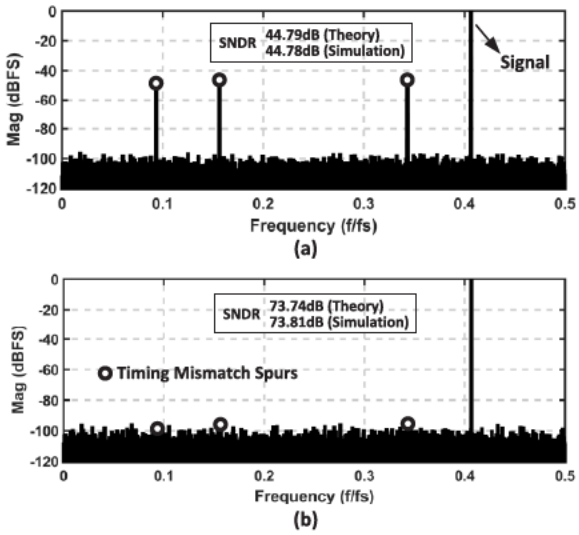

Fig. 6. Spectra of TI-ADC output for a single-tone input at $0.41 f_s$. (a) Without and (b) with the proposed all-digital timing mismatch calibration. Theoretical results are computed from (9) and (13).

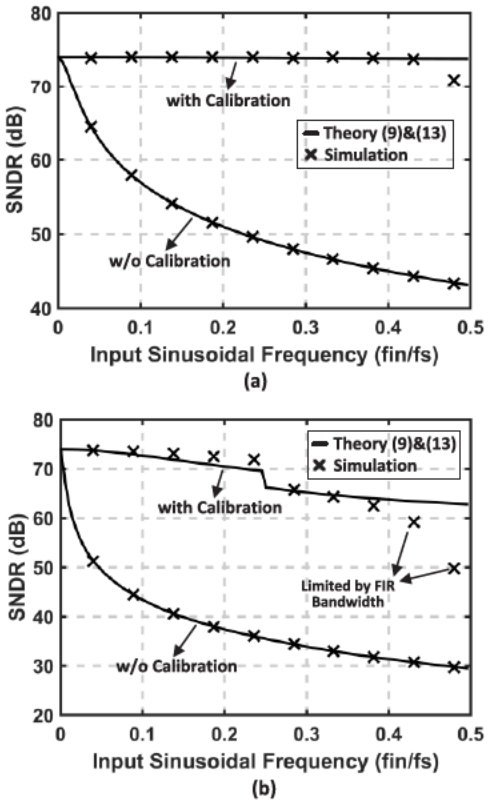

Fig. 7. SNDR versus different input sinusoidal frequencies. (a) $\Delta T_{1-4} =$ [1, 4, 3, and 2 ps]. (b) $\Delta T_{1-4} =$ [1, −7, 7, and 5 ps].

Fig. 8 shows the SNDR results of 1000 Monte-Carlo simulations, wherein the timing mismatches ΔT_{1-4} are independent Gaussian-distributed random variables with zero mean and standard deviation $\sigma = 1$ ps. The simulated worst SNDR increases from 40.28 to 71.36 dB after the all-digital timing calibration, which is consistent with the theoretical results obtained from (10) and (16) (36.29 and 70.57 dB) taking ΔT_{max} and ΔT_{min} to be $+3\sigma$ and -3σ ($r_{\text{max}} = 6\sigma/T_s$).

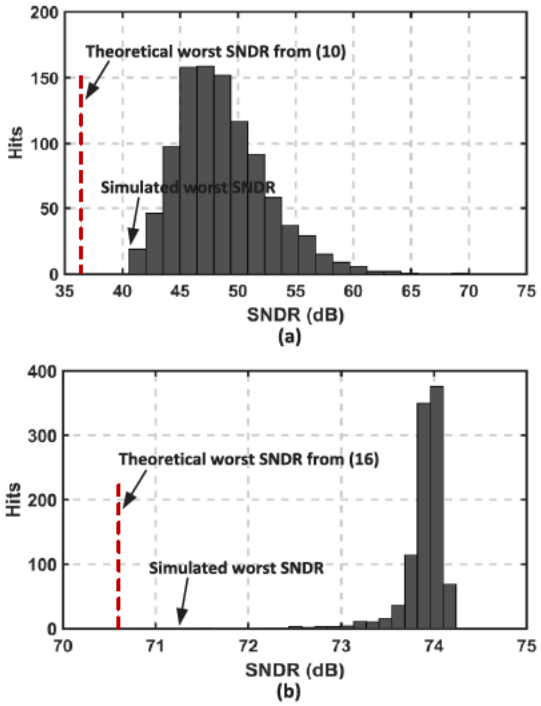

Fig. 8. Thousand times Monte-Carlo simulation of four-channel TI-ADC for Gaussian-distributed timing mismatch ΔT_{1-4} ($\sigma = 1$ ps). (a) Without and (b) with the proposed all-digital timing mismatch calibration. Theoretical worst SNDRs are calculated assuming $r_{\max} = 6\sigma/T_s$.

The performance of the proposed all-digital timing calibration is also verified for a quadrature phase-shift keying (QPSK) modulated input signal at a carrier frequency of $0.29f_s$ ($2375/2^{13} \cdot f_s$) and a symbol rate of 10 MHz, and a multitone input signal. Figs. 9 and 10 show the output spectra of the TI-ADC for the QPSK and multitone input signal, respectively, and all timing mismatch distortion tones are suppressed after the all-digital timing calibration. As expected, the calibration and correction perform well as long as the input signal is restricted within the bandwidth of the FIR filter, in this case up to approximately $0.41f_s$.

B. Measurement Result

A commercial 12-bit 3.6-GS/s two-channel TI-ADC [21] is also used to verify the proposed all-digital timing mismatch calibration. The test setup is shown in Fig. 11. Two 1.8 GS/s sub-ADCs on the chip operate as a TI-ADC. Manual analog timing skew adjustment can be performed on chip via a 7-bit control register. After on-chip gain and offset mismatch calibration are completed, the TI-ADC output data with timing mismatch error are sent to a computer via a USB port and processed with the proposed all-digital calibration off-chip.

For a single-tone input at 1065 MHz, Fig. 12 shows the convergence of the estimated timing mismatches with the on-chip manual timing skew adjustment code set (arbitrarily) at 7b′ 0. Fig. 13 shows the output spectra before and after the proposed all-digital timing calibration. After calibration, the SFDR is no longer limited by the timing mismatch distortion tone and the SNDR increases from 36.53 to 46.12 dB. Fig. 14 shows the SNDR at different input sinusoidal frequencies. The effective number of bits after the proposed calibration is about 7.3 bit,

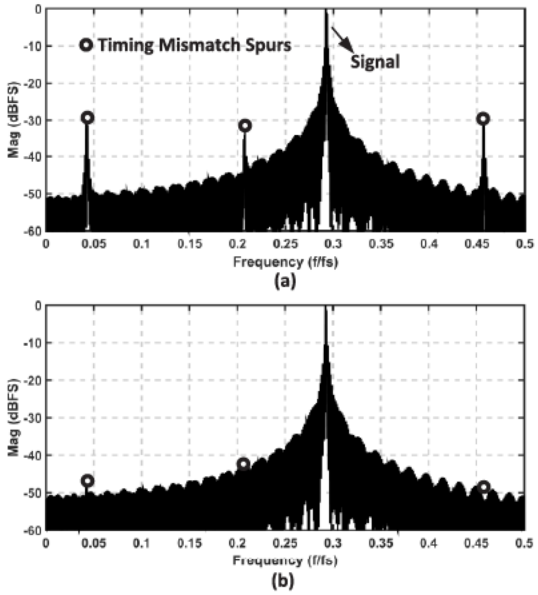

Fig. 9. Spectra of four-channel TI-ADC output for QPSK signal with a carrier frequency of $0.29f_s$ and a symbol rate of 10 MHz. (a) Without and (b) with the proposed all-digital timing mismatch calibration.

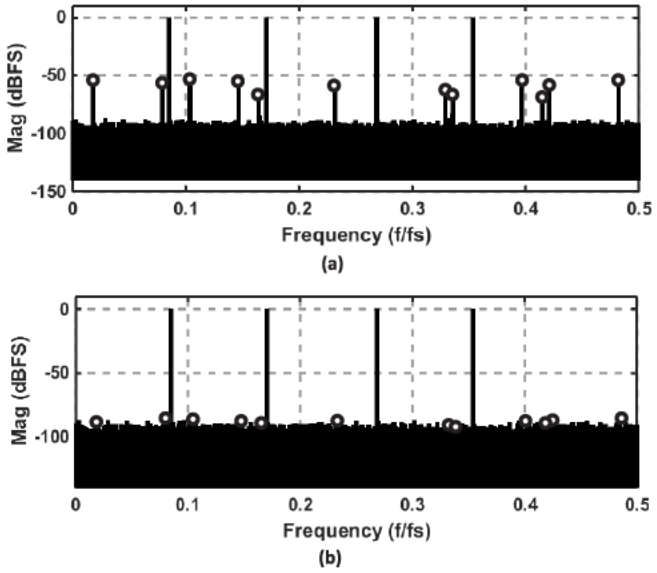

Fig. 10. Spectra of TI-ADC output for a multitone input. (a) Without and (b) with the proposed all-digital timing mismatch calibration.

slightly lower than 8 bit from the data sheet [21] due to the performance limitations of the signal generator and the bandpass filters in Fig. 11.

Fig. 15(a) shows the timing skew estimated by the proposed all-digital timing calibration versus different on-chip manual analog timing skew adjustment codes. The curve is monotonic and approximately linear as expected. When the code is around 7b′ 1000001, timing skew is completely compensated by the delay line, so the dynamic performance (SNDR and SFDR) can reach the optimum. Fig. 15(b) shows the SNDR and SFDR versus with different on-chip timing skew adjustment codes. For all timing skews, the proposed all-digital timing calibration can improve the SNDR and SFDR to the best that can be achieved with the analog timing skew adjustment.

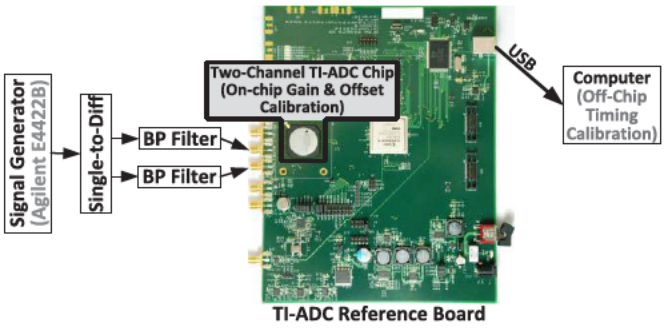

Fig. 11. Experimental setup for two-channel 3.6-GS/s TI-ADC timing mismatch calibration.

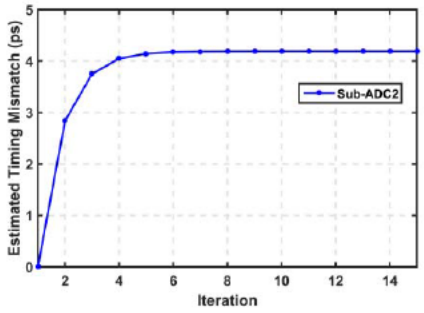

Fig. 12. Measured convergence of the estimated timing mismatch for a single-tone input at 1065 MHz. On-chip manual timing skew adjustment code is 7b′ 0.

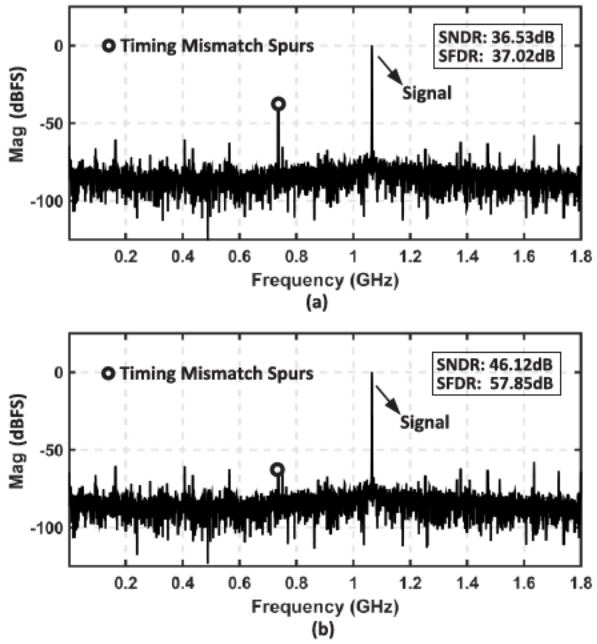

Fig. 13. Measured spectra of two-channel TI-ADC output for a single-tone input at 1065 MHz. On-chip manual timing skew adjustment code is 7b′ 0. (a) Without and (b) with the proposed all-digital timing mismatch calibration.

Fig. 16 compares the output spectra after the proposed calibration and the calibration technique in [17] for a single-tone input at 1065 MHz when the timing skew is set at the maximum value. (Code is 7b′ 0.) The suppression of the timing mismatch distortion tone with the calibration in [17] is about 9 dB worse than the proposed method, because its estimated timing mismatch is not as accurate.

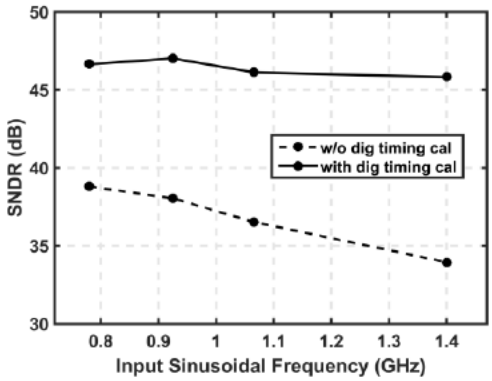

Fig. 14. Measured SNDR versus different input sinusoidal frequencies without and with the proposed all-digital timing calibration. On-chip analog timing skew adjustment code is 7b′ 0.

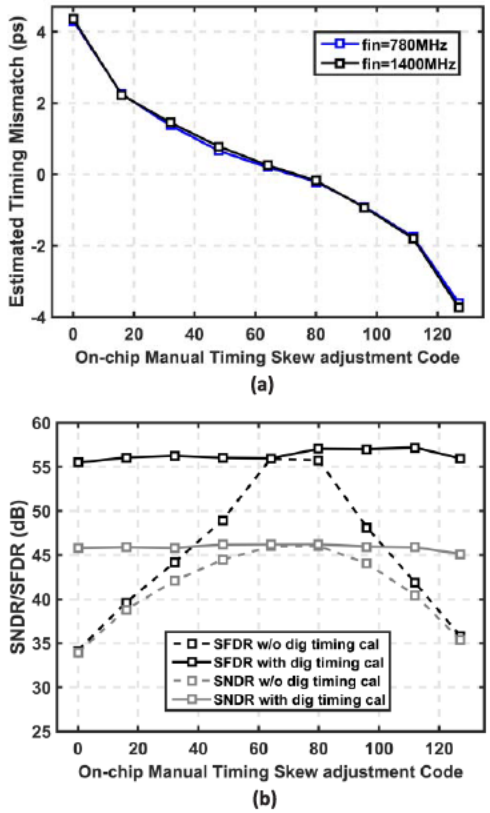

Fig. 15. (a) Estimated timing mismatch using the proposed all-digital timing calibration for a single-tone input at 1400 and 780 MHz. (b) SNDR and SFDR without and with the proposed all-digital timing calibration for a single-tone input at 1400 MHz.

Table I gives a summary of this work and comparison with other related works. The proposed all-digital timing mismatch calibration has lower hardware cost than [17]–[19] and better mismatch tone suppression than [17]. The hardware cost in [18] and [19] is high due to the use of two derivative FIR filters, and additional analog auxiliary ADC channels are required in [20].

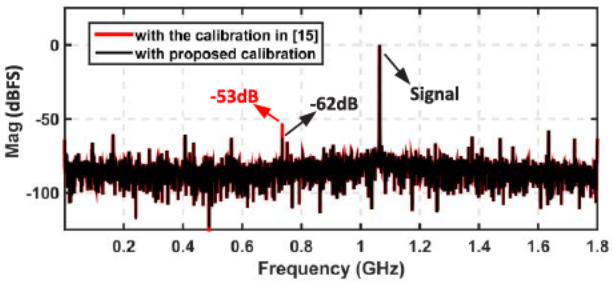

Fig. 16. Measured spectra of two-channel TI-ADC output for a single-tone input at 1065 MHz with the all-digital timing mismatch calibration in [17] and the proposed calibration. On-chip analog timing skew adjustment code is 7b′ 0.

TABLE I

COMPARISON WITH OTHER ALL-DIGITAL TIMING CALIBRATION

	This Work	[17] ISSCC 2014	[18] TCAS-I 2013	[19] TCAS-II 2016	[20] ISSCC 2016
Derivative Generator	FIR filter	FIR filter	Polyphase FIR filter	Polyphase FIR filter	Auxiliary ADCs
Timing Mismatch Estimation	subtraction detection	open-loop calculation	FIR filter + correlator	FIR filter + correlator	auto-correlation detection
# of FIR filter	1	1	2	2	0
# of Multiplier[1,2]	2	6	3	3	4
# of Adder[1,2]	7	3	2	2	9
Timing Mismatch Tone[3]	-62dB	-53dB	-62dB	-62dB	-
Convergence Time (Samples)	80K	1M	60K	10K	32K

[1] for per sub-ADC channel
[2] for the correction and estimation of timing mismatch
[3] for the 12bit 3.6GS/s two-channel TI-ADC with a single-tone input at 1065MHz

V. CONCLUSION

This paper presents an all-digital background timing mismatch correction technique for TI-ADCs with lower hardware cost than previous work. Derivative-based digital correction and digital adaptive timing mismatch estimation are combined to achieve accurate closed-loop timing mismatch estimation and effective distortion tone suppression. Explicit formulas (9), (10), (13), and (16) are also obtained accurately predicting SNDR and providing the bounds on the tolerable timing mismatch for four-channel TI-ADCs both before and after derivative-based digital correction, serving as useful guidelines for designers. The proposed timing mismatch calibration can also be applied in the interleaved ADC with other 2^N channels (e.g., 2 and 8 channels)

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REFERENCES

[1] A. Buchwald, "Practical considerations for application specific time interleaved ADCs," in *Proc. Custom Integr. Circuits Conf. (CICC)*, San Francisco, CA, USA, Sep. 2015, pp. 1–8.
[2] M. El-Chammas, "The world of time-interleaved ADCs," in *Proc. Tutorial IEEE Int. NEW Circuits Syst. Conf.*, Jun. 2012.
[3] P. Benabes *et al.*, "Mismatch calibration methods for high-speed time-interleaved ADCs," in *Proc. IEEE Int. NEW Circuits Syst. Conf.*, Jun. 2014, pp. 49–52.
[4] H. Wei *et al.*, "An 8-Bit 4-GS/s 120-mW CMOS ADC," in *Proc. Custom Integr. Circuits Conf. (CICC)*, San Francisco, CA, USA, Sep. 2014, pp. 1–4.
[5] J. Li *et al.*, "A digital timing mismatch calibration technique in time-interleaved ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 7, pp. 486–490, Jul. 2014.
[6] H. Lee, Aurangozeb, S. Park, J. Kim, and C. Kim, "A 6-bit 2.5-GS/s time-interleaved analog-to-digital converter using resistor-array sharing digital-to-analog converter," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2371–2383, Nov. 2015.
[7] H.-J. Kim *et al.*, "Time-interleaved and circuit-shared dual-channel 10 b 200 MS/s 0.18 μm CMOS analog-to-digital convertor," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 12, pp. 2209–2213 Dec. 2013.
[8] B. Razavi, "Design considerations for interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.
[9] C. Y. Wang and J. T. Wu, "A multiphase timing-skew calibration technique using zero-crossing detection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 6, pp. 1102–1114, Jun. 2009.
[10] L. Wang, Q. Wang, and A. C. Carusone, "Time interleaved C-2C SAR ADC with background timing skew calibration in 65 nm CMOS," in *Proc. Eur. Solid-State Circuits Conf.*, Venice, Italy, Jun. 2014, pp. 207–210.
[11] L. Wang, "Timing skew calibration for time interleaved analog to digital converters," M.S. thesis, Dept. Electr. Comput. Eng., Jun. 2014. [Online]. Available: https://tspace.library.utoronto.ca/handle/1807/67846
[12] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, "An 8 Bit 4 GS/s 120 mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1751–1761, Aug. 2014.
[13] S. M. Jamal, D. Fu, M. P. Singh, P. J. Hurst, and S. H. Lewis, "Calibration of sample-time error in a two-channel time-interleaved analog-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 130–139, Jan. 2004.
[14] R. S. Prendergast, B. C. Levy, and P. J. Hurst, "Reconstruction of band-limited periodic nonuniformly sampled signals through multirate filter banks," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 8, pp. 1612–1622, Aug. 2004.
[15] T. H. Tsai, P. J. Hurst, and S. H. Lewis, "Correction of mismatches in a time-interleaved analog-to-digital converter in an adaptively equalized digital communication receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 307–319, Feb. 2009.
[16] S. Tertinek and C. Vogel, "Reconstruction of two-periodic nonuniformly sampled bandlimited signals using a discrete time differentiator and a time-varying multiplier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 7, pp. 616–620, Jul. 2007.
[17] N. L. Dortz *et al.*, "A 1.62gs/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70 dBFS," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2014, pp. 386–388.
[18] J. Matsuno, T. Yamaji, M. Furuta, and T. Itakura, "All-digital background calibration technique for time-interleaved ADC using pseudo aliasing signal," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1113–1121, May 2013.
[19] H. Le Duc *et al.*, "All-digital calibration of timing skews for TIADCs using the polyphase decomposition," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, pp. 99–103, Jan. 2016.
[20] C.-Y. Lin, Y.-H. Wei, and T.-C. Lee, "A 10b 2.6GS/s time-interleaved SAR ADC with background timing-skew calibration," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2016, pp. 468–469.
[21] *12-Bit, Dual 1.6/1.8 GSPS or Single 3.2/3.6 GSPS ADC12D1800 Reference Board*, accessed on Oct. 10, 2016. [Online]. Available: http://www.ti.com/tool/adc12d1800rb

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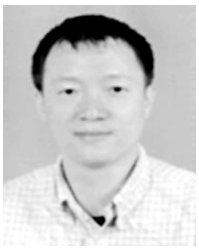

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