A 4PAM/2PAM Coaxial Cable Driver targeting 40Gb/s in $0.13\mu m$ CMOS

by

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Graduate Department of Electrical and Computer Engineering
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Abstract

The main contribution of this thesis work is the design of a coaxial cable driver with Pulse-Width Modulation Pre-Emphasis (PWM-PE) and 4PAM/2PAM signaling. The high-speed Current Mode Logic (CML) design approach discussed in this thesis enabled the circuit to operate up to 32.5Gb/s and 16.25Gb/s in 4PAM and 2PAM modes in a $0.13\mu m$ CMOS technology. Features such as adjustable duty-cycle (50-75%) and output amplitude controls (0.4-1.2Vpp per side) are successfully designed and tested. The transmitter compensated a maximum of 30.3dB of cable loss at 16.25Gb/s in 2PAM and 8.9dB at 32.5Gb/s in 4PAM. The design occupies an area of 1.71mm $\times$ 1.83mm, and consumes a total of 1.578W.

Acknowledgments

I would like to acknowledge my advisor Professor A. Chan-Carusone for his continuing guidance and support throughout this work. Without his knowledge and inspiration, this work would not have been possible.

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I would like to thank Gennum Corp. and NSERC for their generous support for the 40Gb/s transceiver link project, of which this thesis work is a part of.

Last but certainly not least, I would like to thank my family and friends for their constant, unfailing support and understanding throughout the highs and lows of this thesis work.

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List of Acronyms

4PAM 4-level Pulse Amplitude Modulation

ADS Advanced Design System

BER Bit-Error Rate

BJT Bipolar Junction Transistor

CDR Clock Data Recovery

CML Current Mode Logic

CMOS Complimentary MOS

CMRR Common-Mode Rejection Ratio

DAC Digital-Analog Converter

DCC Duty Cycle Control

DFE Decision Feedback Equalizer

DLL Delay-Locked Loop

ECL Emitter Coupled Logic

FIR Finite Impulse Response

FIR-PE Finite Impulse Response Pre-Emphasis

ISI Inter-Symbol Interference

LMS Least Mean Square

LSB Least Significant Bit

LVDS Low Voltage Differential Signalling

MCML MOS Current Mode Logic

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MSB Most Significant Bit

NMOS Negative-Channel Metal Oxide Semiconductor

NRZ Non-Return-to-Zero

OCTC Open-Circuit Time Constant

PAM Pulse Amplitude Modulation

PMOS Positive-Channel Metal Oxide Semiconductor

PRBS Pseudo-Random Binary Sequence

PWM Pulse-Width Modulation

PWM-PE Pulse-Width Modulation Pre-Emphasis

SNR Signal-to-Noise Ratio

VTC Voltage Transfer Characteristic

1 Introduction

1.1 Motivation

Multi-Gb/s transceivers including equalization is an area of ongoing research for channels such as backplane traces or coaxial cables. Due to frequency-dependent channel impairments such as skin-effect and dielectric loss, transmitter and/or receiver equalization becomes necessary. Pulse Amplitude Modulation (PAM) techniques beyond that of base-band binary signaling are also employed to combat channel loss at severe cases. This thesis is part of a larger project targeting the design of a 40-Gb/s transceiver for a 40-m Belden 1694A coaxial cable having 50-dB of loss at 20 GHz (one-half of the bit rate). System simulations indicated that a combination of linear transmitter and receiver equalization with 4-level Pulse Amplitude Modulation (4PAM) signaling offered a possible solution to overcoming the large channel loss. The goal of this thesis project was to build the 4PAM/2PAM transmitter in $0.13\mu m$ CMOS technology, with adjustable pre-emphasis and amplitude controls. The use of Pulse-Width Modulation Pre-Emphasis (PWM-PE) in a 4PAM transmitter is another major contribution of this work. As part of the larger transceiver project, the Masters thesis work of another student involved the design and fabrication of a 40-Gb/s 4PAM receiver in 90-nm Complimentary MOS (CMOS) with equalization [1].

The basic block diagram for the transceiver link is shown in fig. 1.1. Estimation of channel response of the the time-invariant or slowly time-varying channel, which is important for pre-emphasis (or transmit equalization), can be obtained from the receiver using a seperate backchannel [2] [3]. Backchannel link and adaptation of pre-emphasis and amplitude controls were beyond the scope of this work, but are to be included in the full transceiver system. In this work, "transmitter" is used to refer to the implemented transmitter circuit without the adaptation module throughout this thesis.

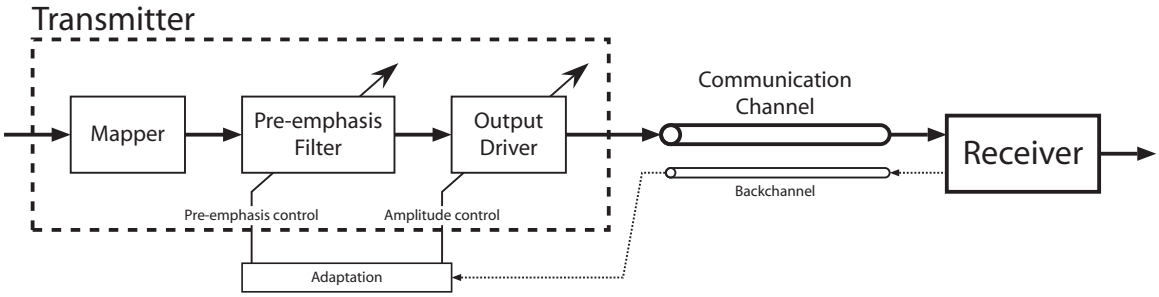


Figure 1.1: Transceiver Link

1.2 State of the Art

The following provides a survey of the current state of the art for transmitters in CMOS. To provide some context for the larger transceiver project goal in terms of speed and loss-compensation, current state of the art 4PAM transceivers in acCMOS are also briefly described.

The 4PAM transmitter reported in [4] achieved 25Gb/s in 90-nm CMOS SOI with 4-tap Finite Impulse Response (FIR) pre-emphasis. Loss compensation of 3dB at 6.25GHz was achieved.

The 4PAM transmitter in [5], implemented in 90-nm CMOS technology, uses 4-channel Analog Multi-Tone (AMT) to achieve maximum data rate of 24Gb/s with channel loss of 14.5dB at 6GHz. Digital equalization with 64 coefficients is used for AMT mode and baseband mode of operation.

The transmitter in [6] achieved 10Gb/s in 0.25-μm CMOS using 2-tap symbol-space FIR pre-emphasis. The maximum simulated data rate of 20Gb/s [7] is accomplished through multiplexing of five parallel data streams.

The 4PAM transmitter in [8] achieved 10Gb/s in 0.4-umm CMOS technology with 3-tap FIR pre-emphasis. The same transmitter architecture is also used in [9].

The 4PAM transceiver in [9] achieved 8 Gb/s in 0.3-μm CMOS, and implemented 2-tap symbol-spaced FIR transmit pre-emphasis and 1-tap 1/2-symbol-spaced FIR receive equalization.

The 4PAM transceiver in [10] achieved 5Gb/s in 0.25-μm CMOS using a FIR (3-tap + 1 long-latency tap) transmit equalizer with a slicing receiver, and an 8B5Q coding scheme meant to facilitate adaptive equalization and timing recovery.

The 4PAM transceiver in [11] achieved 10Gb/s in 0.13-μm CMOS, and combined a 5-tap symbol-spaced FIR transmitter with a 5-tap Decision Feedback Equalizer

(DFE) at the receiver. Use of a DFE was motivated by the high-reflection backplane environment, and a loss of approximately 12-dB at 2.5GHz was compensated.

The transceiver in [12] achieved data rate up to 10Gb/s in 0.13-μm CMOS with dualmode (PAM2 one-tap DFE/PAM4) adaptive equalization. Common mode signaling is used in backchannel communication path for adaptation of transmit equalization.

1.3 Thesis Organization

This thesis describes the design of a 4PAM transmitter with PWM-PE in 0.13-μm CMOS. Chapter 2 outlines the motivation for this work; analysis of pre-emphasis techniques for the channel; and design of high-speed CML circuits in the traditional approach. Chapter 3 presents a design approach to Current Mode Logic (CML) circuits for high-speed applications. In chapter 4, circuit specifications, system architecture, circuit design for individual components, system integration along with layout and fabrication issues are presented. Measurement results of the transmitter in binary and 4PAM modes are presented in chapter 5. Finally, chapter 6 concludes and suggests directions for future research.

2 Background

2.1 Motivation

The communication channel targeted in this thesis work is the Belden 1694A coaxial cable. Its characteristic impedance is 75Ω and it is intended for use in the frequency range up to 4.5 GHz [13]. Hence, its losses are only characterized up to 4.5 GHz in the datasheet provided by manufacturer [13]. The targeted data rate of 40Gb/s is far beyond this frequency range. Hence, a general RLGC model of wireline channels was fitted to measured data [14]. A more detailed discussion of the de-embedding technique and channel modeling is provided in [1]. Samples of the cable of length 50m, 30m, and 10m were provided by Gennum Corporation for this purpose. After de-embedding of the measurement setup a scalable model was developed and 56dB of loss was predicted at 20GHz for a 40m cable as shown in fig. 2.1. In order to ensure reliable transmission over this cable, loss compensation techniques are required at both the transmitter and receiver. In addition, multilevel modulation was considered to reduce the amount of loss incurred in the channel.

This section provides background information on two alternative pre-emphasis techniques and 4-level Pulse Amplitude Modulation (4PAM).

2.2 Pre-emphasis

Pre-emphasis is a linear filter applied to the transmitted data to modulate the transmitted pulse shape in an attempt to flatten the combined response of the transmitter and channel.

The dominant loss mechanisms in coaxial cable are skin effect and dielectric losses, both of which increase at high frequency. These bandwidth limitations lengthen the channel's impulse response, causing adjacent symbols to overlap and introducing Inter-Symbol Interference (ISI). In order to reduce ISI at the receiver input, it is desirable that the overall frequency response of the transmitter and channel be as

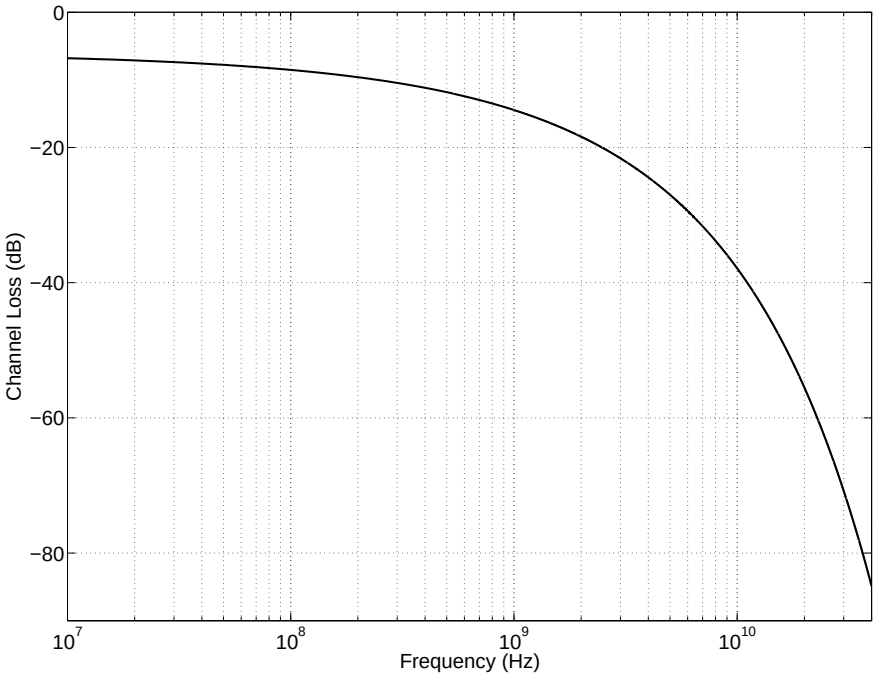


Figure 2.1: Channel loss characteristic of 1694A coaxial cable of length 40m

flat as possible, up to the bandwidth required to support the targeted data rate. Pre-emphasis at the transmitter generally increase the high-frequency content of the signal relative to its low-freqency content, in order to flatten the overall response. In the following sections, two methods to implement pre-emphasis in multi-Gb/s links are analyzed and compared.

2.2.1 Pre-emphasis Techniques

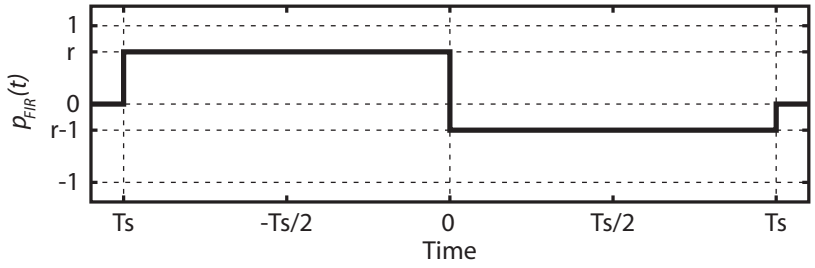
Two pre-emphasis techniques are considered in this section. The first is a 2-tap symbol-spaced Finite Impulse Response (FIR) pre-emphasis approach[1], it is widely used and well understood [16] [17] [18]. This pre-emphasis approach extends the transmitter's pulse response to two symbol periods. The following analysis uses the approach outlined in [15] but applied to the channel of interest for this work. Define

[1]FIR pre-emphasis with greater than two taps is also common at lower data rates, but the added complexity entailed was considered impractical for the targeted data rate and process technology. In addition, adaptation algorithm using Least Mean Square (LMS) has more complex implementation for Finite Impulse Response Pre-Emphasis (FIR-PE) with multiple filter tap coefficients compared to the single-coefficient cases considered here. [15]

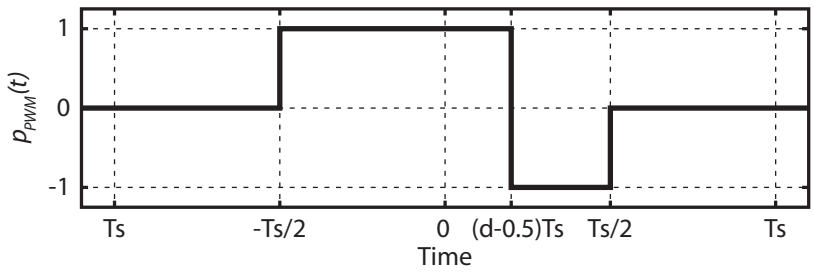
the amplitude of the pulse in the first symbol period to be r while the second symbol period has amplitude of $(r-1)$, where r is an adjustable parameter in the range $0 < r \leq 1$ as shown in fig. 2.2(a). Note that the peak transmitter output swing with two neighbouring pulse responses overlapping is $\pm[r-(r-1)] = \pm 1$.

The second approach to pre-emphasis uses pulse width modulation. Referred to as Pulse-Width Modulation Pre-Emphasis (PWM-PE), this is a relatively new approach that has produced promising results in recent literature [19] [20] [15]. It uses the timing resolution within one symbol period to shape the transmit-pulse response, while keeping the transmitted waveform at its full-swing values. The pulse response comprises a positive portion of duration $d \cdot T_S$, and a negative portion of duration $(1-d) \cdot T_S$, as shown in fig. 2.2(b) with normalized amplitude of ± 1. PWM-PE with $d = 50\%$ is equivalent to Manchester-encoded signal.

Both FIR and Pulse-Width Modulation (PWM) pre-emphasis have simple Non-Return-to-Zero (NRZ) pulse responses when $r = 1$ and $d = 100\%$, respectively.



(a) Pulse shape of 2-tap symbol-spaced FIR pre-emphasis



(b) Pulse shape of PWM pre-emphasis

Figure 2.2: Pulse shape of FIR and PWM pre-emphasis

2.2.2 Analysis

In order to have a fair comparison between the two pre-emphasis approaches, the maximum transmitter output swing is normalized to 1 in both cases.

In order to understand the relationship between pulse shape and its frequency content, it is informative to study the spectrum of the two pre-emphasis pulses. Taking the Fourier transform of the pulses shown in fig. 2.2(a) and fig. 2.2(b) gives the magnitude of the transmit spectrum in both case (assuming random uncorrelated data).

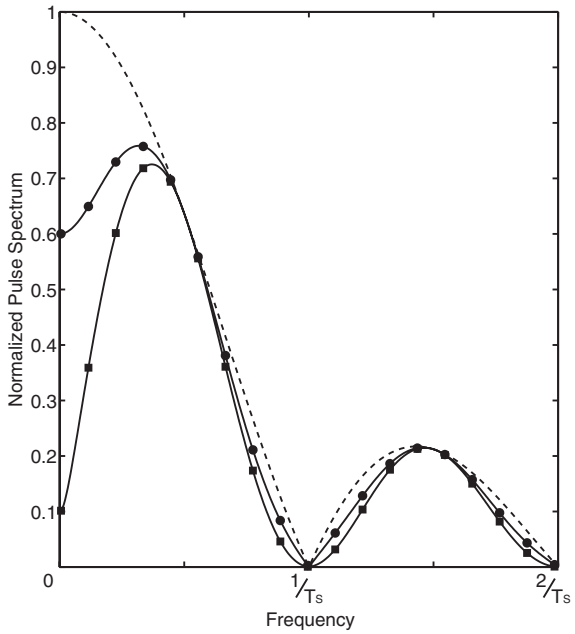
$$|P_{FIR}(f)| = \frac{1}{\sqrt{2}}\sqrt{(1-\cos(2\pi f T_S))(2r(r-1)\cos(2\pi f T_S)+r^2+(r-1)^2)} \quad (2.1)$$

$$|P_{PWM}(f)| = \sqrt{\cos^2(\pi f T_S) - 2\cos(\pi f T_S)\cos(2\pi f(d-0.5)T_S)+1} \quad (2.2)$$

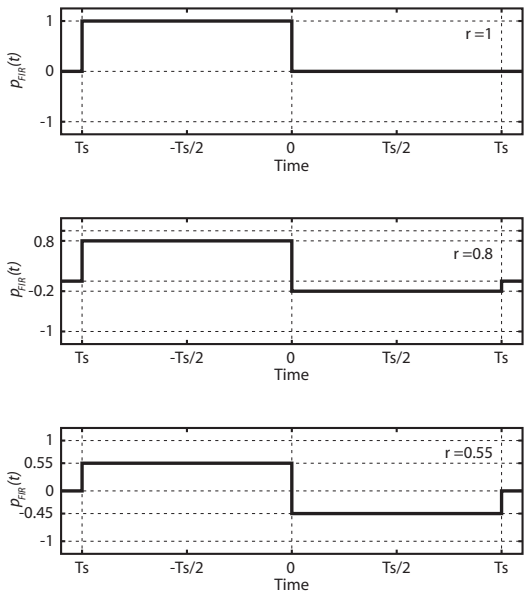
As expected, the pulse spectra of the two techniques are strongly dependent on the pre-emphasis settings, namely r and d respectively. Fig. 2.3(a) shows the effect of changing the pre-emphasis setting, r, has on the FIR pulse spectrum. Similarly, fig. 2.3(c) illustrates the effect of changing the pre-emphasis setting, d, on the PWM pulse spectrum.

In both cases, the amount of pre-emphasis is increased by reducing parameters r and d from 1 to 0.5, resulting in less low-frequency signal content. Hence, these approaches are often referred to as de-emphasis, although it will continue to be referred to as pre-emphasis here. A strong pre-emphasis suppresses the low-frequency content of the signal while enhancing the high-frequency component. In FIR-PE, the low-frequency content from DC to roughly $f = \frac{1}{2 \cdot T_S}$ is strongly affected by the change in r, while the nulls at integer multiples of $f = \frac{1}{T_S}$ remain; second and higher order lobes is not strongly affected by changes in pre-emphasis setting. Note that the frequency content at all frequencies is maximized by taking $r = 1$ (no pre-emphasis); decreasing r provides relative high-frequency boost by attenuating some portions of the spectrum (those near DC) more than others. However, the overall pulse spectrum of PWM-PE changes more significantly. As show in fig. 2.3(c), as the pre-emphasis setting d changes, the pulse spectrum no longer has nulls at integer multiples of $\frac{1}{T_S}$ as in the case of FIR-PE. Low-frequency components are suppressed, while the high frequency components receive a stronger boost as compared to the 2-tap symbol-spaced FIR pre-emphasis approach.

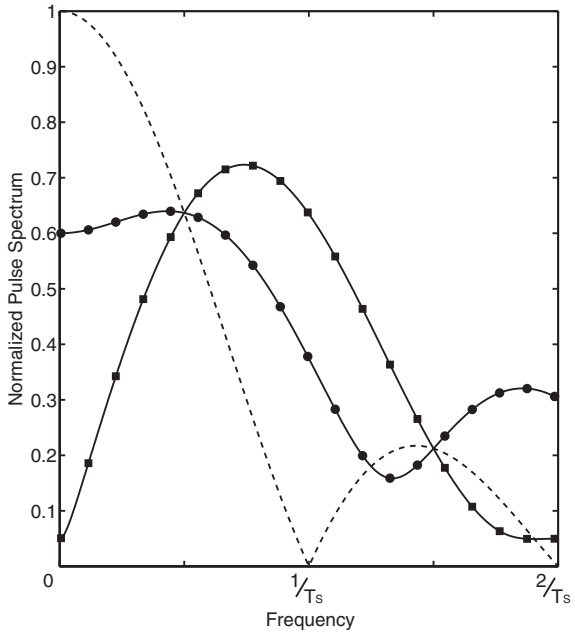
The implementation of PWM-PE, which is shown to have superior performance



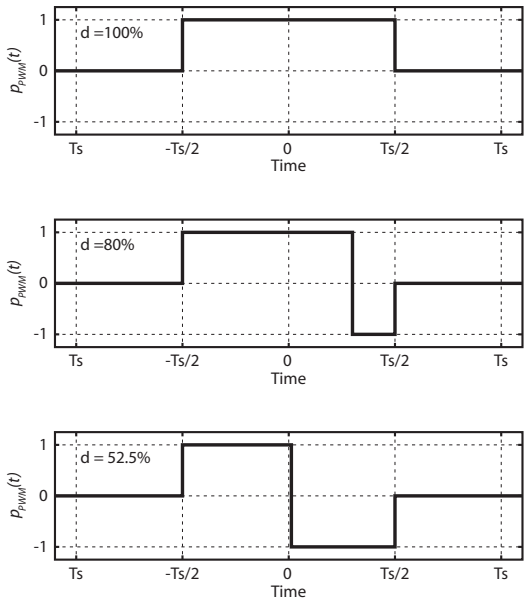
(a) Pulse spectrum of FIR pre-emphasis; dashed: r = 1 (NRZ); circle: r = 0.8; square: r = 0.55



(b) Time-domain pulse shape of FIR pre-emphasis; r = 1, 0.8, 0.55



(c) Pulse spectrum of PWM pre-emphasis; dashed: d = 100% (NRZ); circle: d = 80%; square: d = 52.5%



(d) Time-domain pulse shape of PWM pre-emphasis; d = 100%, 80%, 52.5%

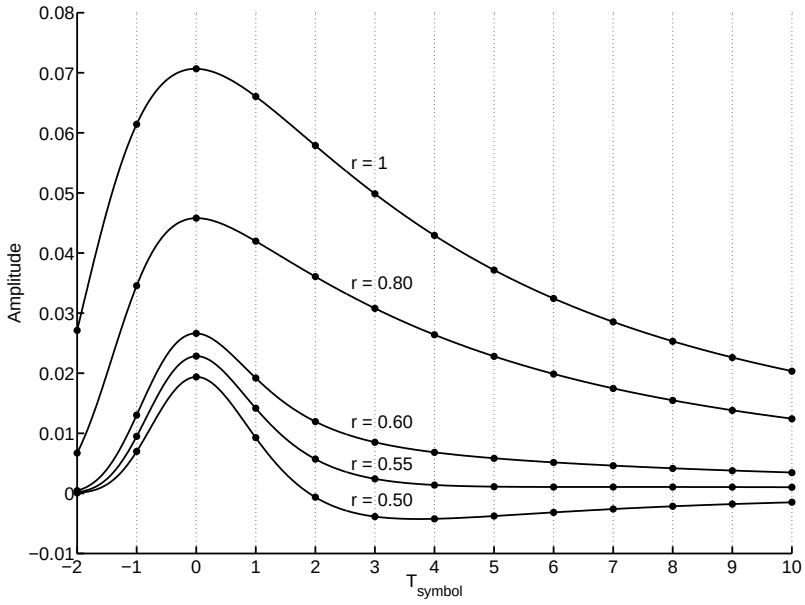
Figure 2.3: Pulse spectrum and shape for different pre-emphasis settings

in providing high-frequency boost to the transmit waveform, requires careful consideration. The maximum switching speed for a given technology limits the shortest pulse-width achievable. Hence, it is difficult to achieve narrow negative duty-cycle pulse ($d \sim 90$ – 100 %) at high data rates. For the same reason, PWM-PE requires a technology with higher maximum switching speed compared to an implementation with symbol-spaced FIR-PE at the same maximum data rate. The higher spectral contents of the pulse with PWM-PE require higher bandwidth for the circuit blocks. The higher bandwidth requirement necessitate more complex circuit design and/or higher power consumption.

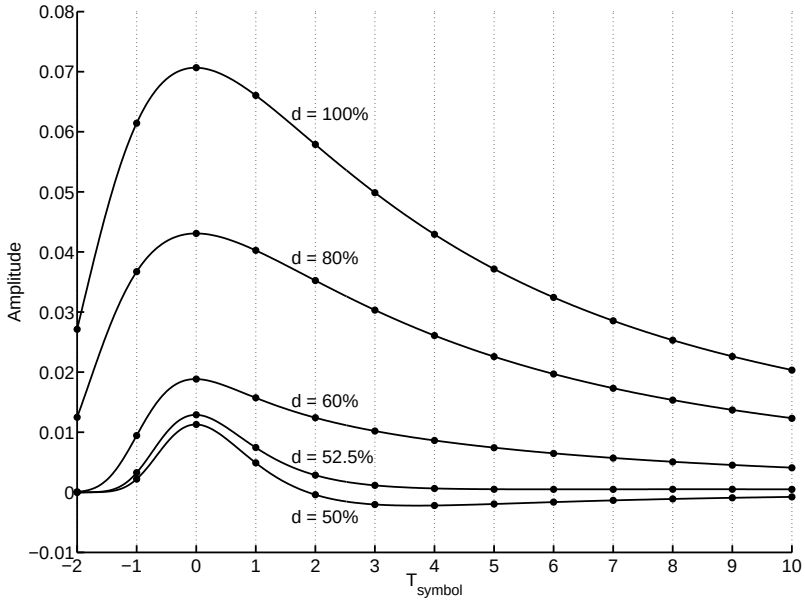
In order to gain a good understanding of the effectiveness of the two pre-emphasis techniques, further simulations were perfromed in MATLAB environment. Pulse shapes of various pre-emphasis settings are generated in MATLAB and convolved with the impulse reponse of the 40m coaxial cable channel. Using this approach, the pulse responses at the input of the receiver can be visualized and the effectiveness of the pre-emphasis approaches can be judged. Fig. 2.4 illustrates the pulse reponses of different pre-emphasis settings at the receiver input with $T_{symbol} = 25ps$ corresponding to a data-rate of 40Gb/s using binary signalling. At the Nyquist rate of 20GHz, channel loss is approximately 56dB as shown in fig. 2.1. Markers are shown at symbol intervals to help identify the amount of pre-cursor and post-cursor ISI in the recieved pulse. As seen in fig. 2.4, ISI of the recieved pulse is severe for all pre-emphasis settings using the two techniques outlined. The receiver input has completely closed eye diagrams for all settings (not shown).

2.2.3 Pulse Amplitude Modulation (PAM)

Neither of the two pre-emphasis approaches is sufficient to combat the 56dB loss at one-half the bit rate, 20GHz. A system that requires less bandwidth will benefit from a reduction in channel loss. A 4PAM system, by virtue of using different amplitudes to encode two bits of information within a single symbol, only requires half the bandwidth of a binary system. For a 4PAM system that utilizes the same channel, a loss of approximately 38dB is experienced at one-half the symbol rate (10GHz), 18dB less than using binary signaling. However, 4PAM signal level spacing is also reduced for the same peak transmitter swing due to multi-level encoding. The level spacing in a 4PAM system is one-third of that in a binary system, which corresponds to a 9.6dB reduction. So overall, transmission using 4PAM reduces channel losses at the



(a) Pulse response of FIR pre-emphasis at $T_{symbol} = 25ps$



(b) Pulse response of PWM pre-emphasis at $T_{symbol} = 25ps$

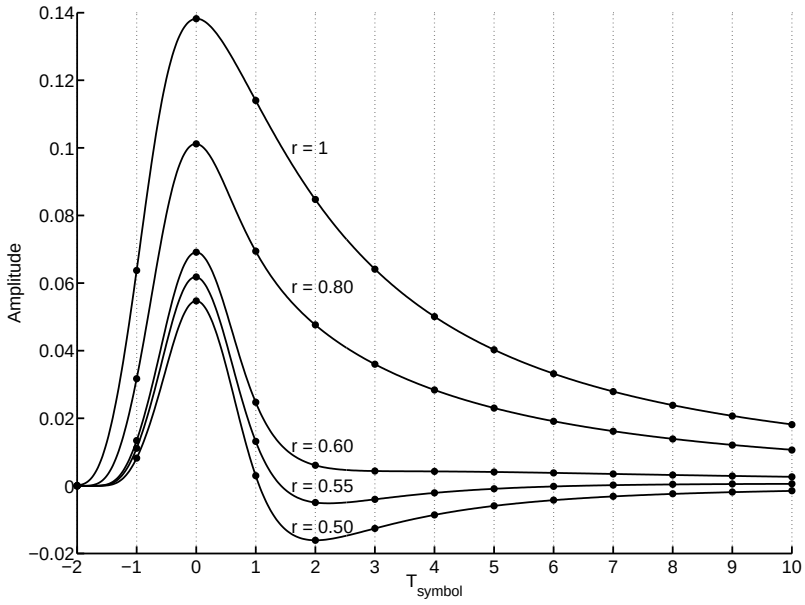
Figure 2.4: Pulse response after 40m of Belden 1694A coaxial cable at $T_{symbol} = 25ps$

expense of reduced level spacing. The trade off must be carefully investigated for systems with significant channel loss such as the 40m of Belden 1694A coaxial cable considered here. Pulse responses for $T_{symbol} = 50ps$, corresponding to 20GSymbol/s, are shown in fig. 2.5 with markedly improved the ISI at the input of the receiver. For transmitted pulses with FIR-PE, the best setting is near $r = 0.55$, but some amount of pre-cursor and post-cursor ISI are still present, as shown in fig. 2.5(a). The best configuration using PWM-PE is a duty-cycle of approximately 52.5%, as shown in fig. 2.5(b). In this configuration, pre-cursor ISI is removed but a small amount of post-cursor ISI still remains to be compensated by the receiver.

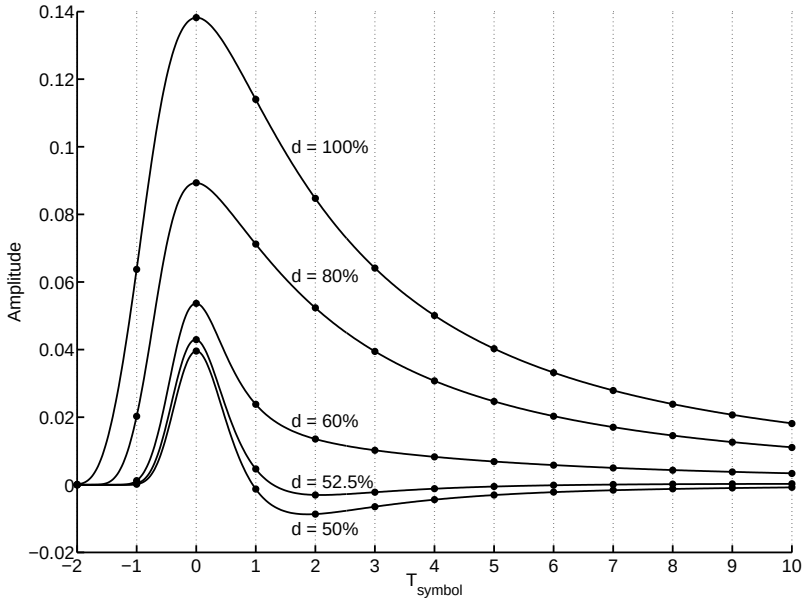
The two pre-emphasis techniques can also be compared in the frequency domain. Fig. 2.6 illustrates the combined response of the channel and the best-case setting for both pre-emphasis techniques. The symbol duration is chosen to be $50ps$ in accordance with the symbol-rate requirement for a 4PAM system. The amount of pre-emphasis produced by PWM-PE with $d = 52.5\%$ matches the inverse of the channel loss curve more closely, resulting in an overall flatter response and subsequently less ISI. However, since the channel response is equalized by attenuating low-frequency content, this benefit comes in expense of higher overall attenuation of the signal. The transmitter must attenuate the DC content by roughly the same amount as the channel attenuates the content near $\frac{1}{2T_S}$. The large amount of attenuation due to combined de-emphasis and channel response is a major challenge in the link design.

The decision was made to adopt the 4PAM system with PWM-PE due to the reduction in ISI. Note that PWM-PE is a linear operation. Hence, implementation of PWM-PE is possible in a 4PAM system, although this has not been done previously.

In a 4PAM system, the mapping from 2-bits of information to one of the four PAM levels is not unique. The two most commonly-used schemes are the binary code (00-01-10-11 arrangement) and Gray code (00-01-11-10 arrangement). Given the same symbol-error rate of in a communication link, Gray code yields lower Bit-Error Rate (BER) compared to binary encoding. This is due to the arrangement of bit patterns in the symbol constellation, in which only one bit is altered between adjacent symbols in Gray coding. The mapping from 2-bit input patterns and output pulses for the proposed 4PAM transmitter with PWM-PE and Gray coding as depicted in fig. 2.7.



(a) Pulse response of FIR pre-emphasis at $T_{symbol} = 50ps$



(b) Pulse response of PWM pre-emphasis at $T_{symbol} = 50ps$

Figure 2.5: Pulse response after 40m of Belden 1694A coaxial cable at $T_{symbol} = 50ps$

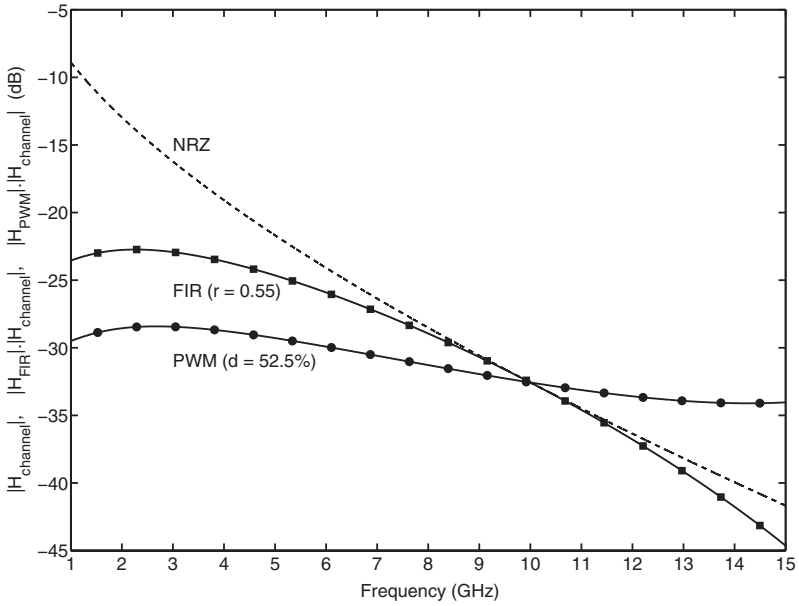


Figure 2.6: Combined pre-emphasis and channel response for FIR-PE and PWM-PE

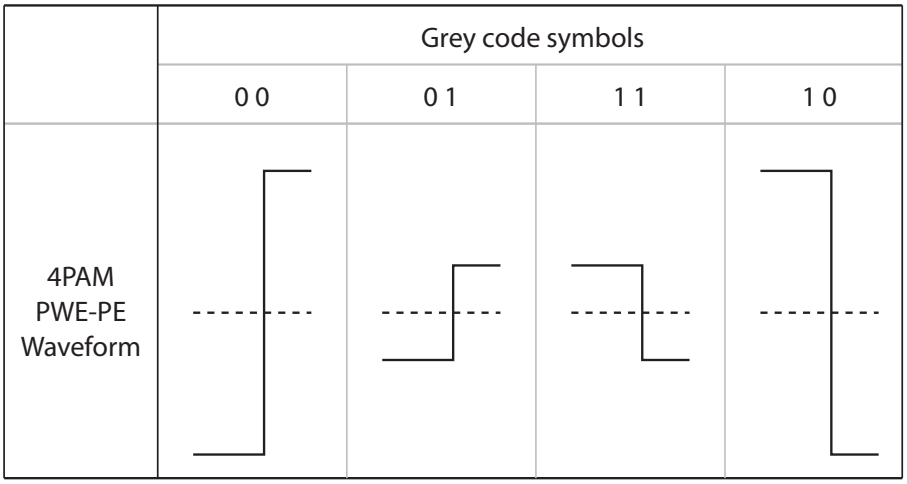
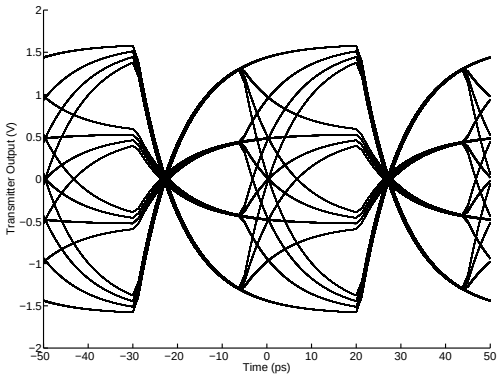


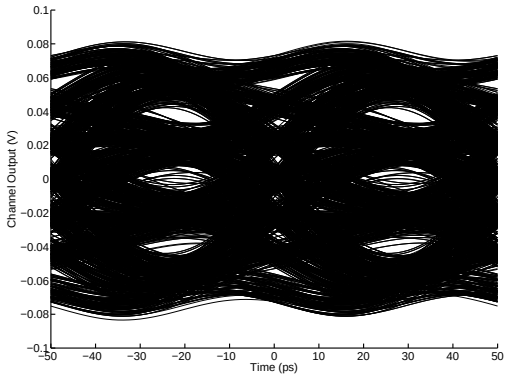
Figure 2.7: Output waveform of 4PAM transmitter with PWM-PE

2.2.4 System-Level Simulation

System-level simulation were performed in MATLAB with Simulink. Fig. 2.8(a) shows the eye-diagram of the transmitter output with duty-cycle of 52.5%, and fig. 2.8(b) shows the eye-diagram at the output of the targeted 40m coaxial cable channel. Although the signal integrity there is still poor, it is shown in [1] that the addition of a peaking equalizer at the front-end of the receiver can provide a modest eye-opening in this case.



(a) Eye diagram of transmitter output with PWM-PE, $d = 52.5\%, T_{symbol} = 50ps$



(b) Eye diagram of 40-meter channel output with PWM-PE, $d = 52.5\%, T_{symbol} = 50ps$

Figure 2.8: Matlab Simulink eye diagrams

2.2.5 Technology Choice

It has been shown that the severe channel loss at high data rate necessitates the use of strong pre-emphasis, which results in a significant decrease in received signal amplitude. This can be seen in fig. 2.6, where the combined pre-emphasis and channel response results in a loss of approximately 32dB. This is also confirmed by the system-level simulation results in fig. 2.8, where a transmit amplitude of $\pm 1.6V$ is assumed, but the received amplitude after the 40m cable is only $\pm 60mV$. In order to maintain sufficient input amplitude at the input of the receiver, large output amplitude is required at the transmitter. To accommodate a high output voltage at the last stage of the transmitter, transistors with large drain-source breakdown voltage are required.

The device drain-source breakdown voltage decreases with technology scaling. For this reason, 90nm or 65nm Complimentary MOS (CMOS) processes were ruled out despite their higher f_T. The $0.13\mu m$ CMOS technology has demonstrated adequate device speed for this application in the literature [21] [22] [23] and has a drain-source breakdown voltage of 1.6V, making it a suitable choice of technology.

2.2.6 Summary

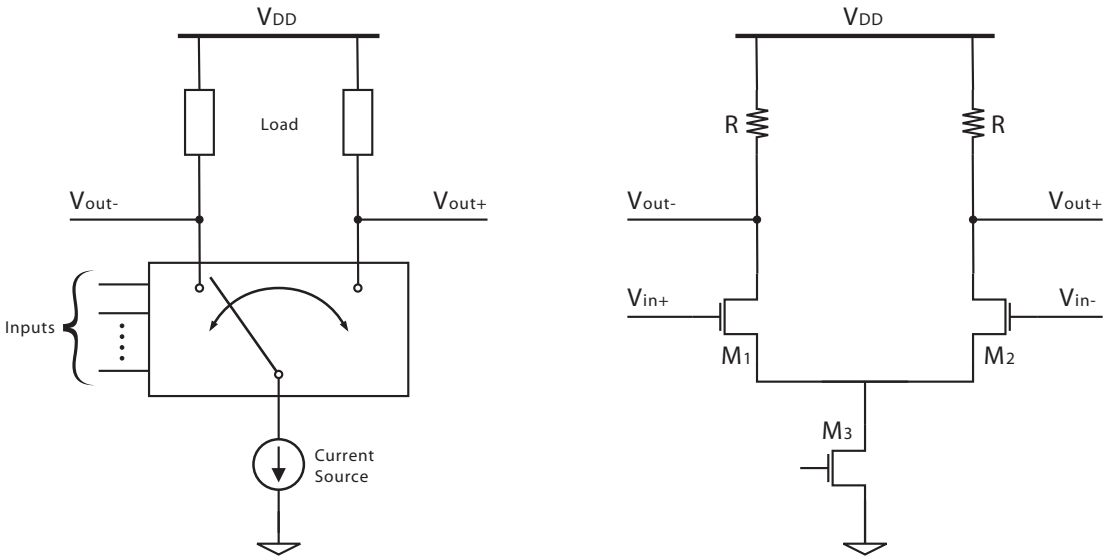
In this section, the concept of PWM-PE was introduced and compared with traditional FIR-PE as a means of combating the severe channel loss of the targeted coaxial cable at high frequency. In addition, the use of PAM to mitigate channel loss is also explored. Different combinations of pre-emphasis and amplitude-modulation techniques were explored by system-level simulations using MATLAB Simulink. The combination of PWM-PE and 4PAM was chosen because it provided the best channel output eye diagram. The large amount of attenuation due to the combined effect of channel loss and de-emphasis necessitates a large voltage swing at the transmitter output. This requirement combined with speed considerations make the $0.13\mu m$ CMOS technology an appropriate choice for implementation.

2.3 Current Mode Logic (CML) in CMOS

The speed of traditional CMOS logic, which utilizes a combination of Positive-Channel Metal Oxide Semiconductor (PMOS) and Negative-Channel Metal Oxide Semiconductor (NMOS), is limited. This is mainly attributed to the low f_T of PMOS transistors. High speed digital logic is often implemented with a logic family that utilizes current instead of voltage signals. Some of the key representatives of this logic family include CML and Emitter Coupled Logic (ECL). Historically, Bipolar Junction Transistors (BJTs) have dominated these logic families due to their low switching voltage and higher f_T compared to CMOS technologies. However, with the rapid scaling of CMOS technology, CML in CMOS has become popular for high-speed digital logic. CMOS has the benefits of higher yield, lower production cost, and lower power consumption compared to their bipolar counterparts; these advantages have generally come at the cost of slower operation.

True to its name, CML uses current as the primary mode of signal processing. Figure 2.9(a) illustrates a generalized block schematic of a CML gate. The fundamental

component of a CML gate is the pull-down network. Its primary function is to steer the tail current to one of the two load resistances. The different currents through the two loads generates an output differential voltage at the output nodes.



(a) Block Diagram of CML general architecture

(b) Schematic of CML buffer

Figure 2.9: CML architecture and schematic

The schematic of a simple CMOS CML inverter is shown in fig 2.9(b). NMOS transistors M_1 and M_2 form the common-source differential pair which functions as the pull-down network. Transistor M_3 is biased in saturation to provide a constant tail current. Output voltage is generated across the load (shown as R in fig. 2.9(b)), where resistors or PMOS transistors biased in deep triode operating regions are used.

2.3.1 Square-law CML Design

The operation of a CML circuit, in a traditional sense, relies on the routing of tail current through one of the loads. When the differential input voltages are sufficiently large, such that only one path through the pull-down network is conducting, the CML gate is said be under full-switching mode of operation. The CML output differential voltage under full-switching region of operation is $\Delta V_{MAX} = I_{TAIL} \cdot R$ with one of

the output nodes at the supply voltage, V_{DD}, while the other output node is at $V_{DD} - \Delta V_{MAX}$.

Voltage Transfer Characteristic (VTC) is useful in understanding the behavior of CML gates. The input to output voltage transfer relationship is illustrated graphically in a VTC plot; an example of a full-switching CML circuit is shown in fig. 2.10. The VTC crosses the origin, as a differential input voltage of zero results in a balanced state with zero differential output voltage. The tail current is steered increasingly to one side as the differential voltage increases. This results in an increase in voltages across the output nodes. Eventually, at sufficiently large input voltage, the tail current is fully-switched to one of the two sides and the targeted ΔV_{MAX} is achieved at the output. Due to the symmetrical nature of CML circuits, the VTC has odd symmetry about the origin. Therefore, it is sufficient to shown the VTC only in the first-quadrant in describing the entire transfer characteristic of a CML gate.

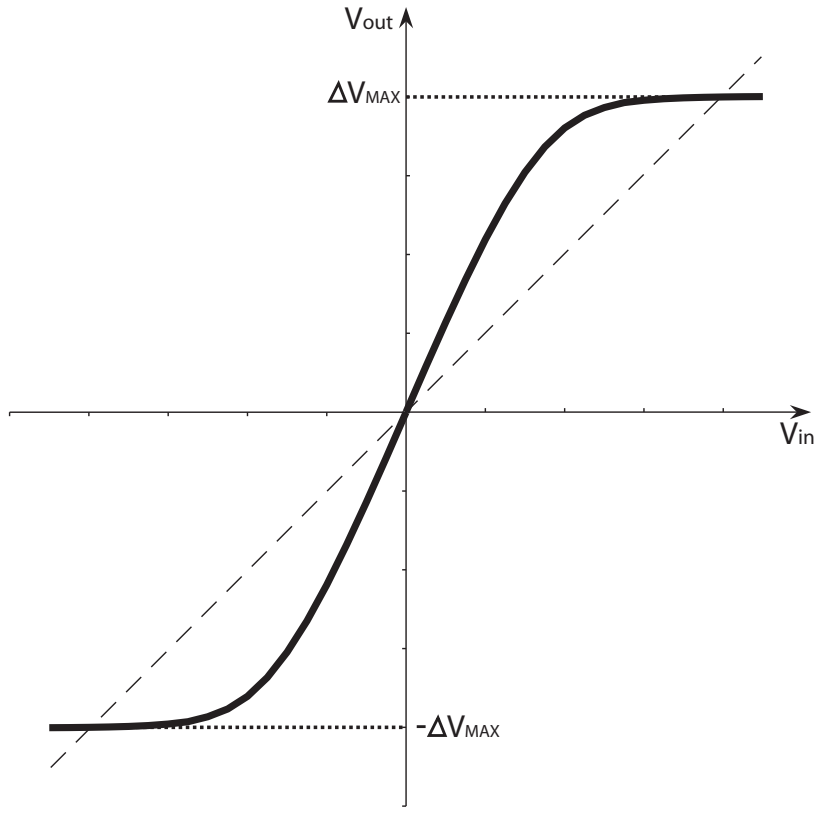


Figure 2.10: VTC of a CML circuit operating in full-switching region

In the attenuating region of operation for a CML circuit, the output voltage is less than its input for any input voltage. In this case, even with large input voltages

a significant portion of tail current flows through the "off" transistor such that the output voltage across the loads is below ΔV_{MAX}. This region of operation is generally avoided by circuit designers. An example of a VTC curve in the attenuating region is shown in fig. 2.11.

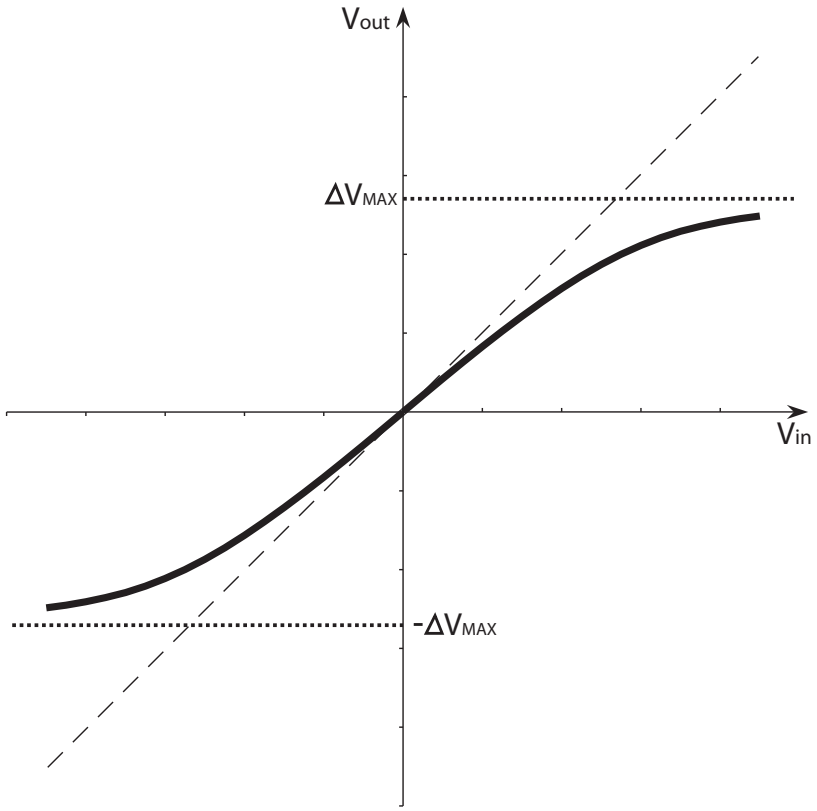
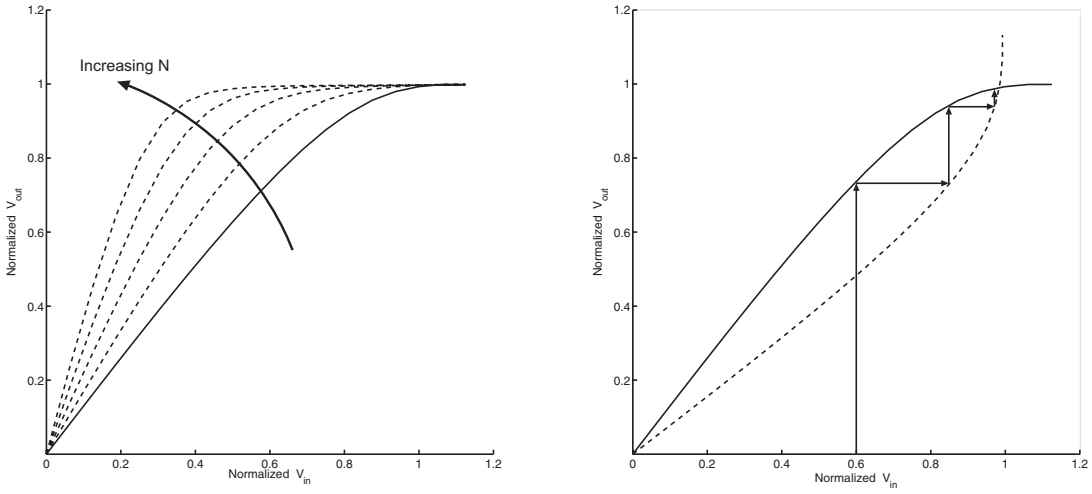


Figure 2.11: VTC of a CML circuit operating in attenuating region

CML circuits most commonly used in pre-driver, Delay-Locked Loop (DLL), and clock distribution network circuits. A cascade of roughly constant fanout buffers intended to provide sufficient logic drive or to route signals to different parts of the system. The VTC is useful for understanding the operation of CML circuits in such cascade arrangements. Consider a cascade of full-switching CML buffers with identical VTCs as shown in the solid line in fig. 2.12(a). The aggregate input-output transfer characteristic of CML buffers with constant fanout, where the number of stages is denoted by N, can be derived from the original VTC, as in the dotted lines in fig. 2.12(a). The minimum input voltage required for a full-switching output of ΔV_{MAX} decreases as N increases. The slope of the cascaded VTC is also steeper, which corresponds to the increase in overall large-signal gain of multiple CML buffers.

Fig. 2.12(b) illustrates the voltage transfer within the same CML buffers. An input that is below ΔV_{MAX} is amplified to its full-switching value after a few stages of buffering, as shown by the upward arrows.



(a) VTCs of a cascade of full-switching CML buffers; solid line - one stage VTC; dash line - cascaded stage 2 to 5

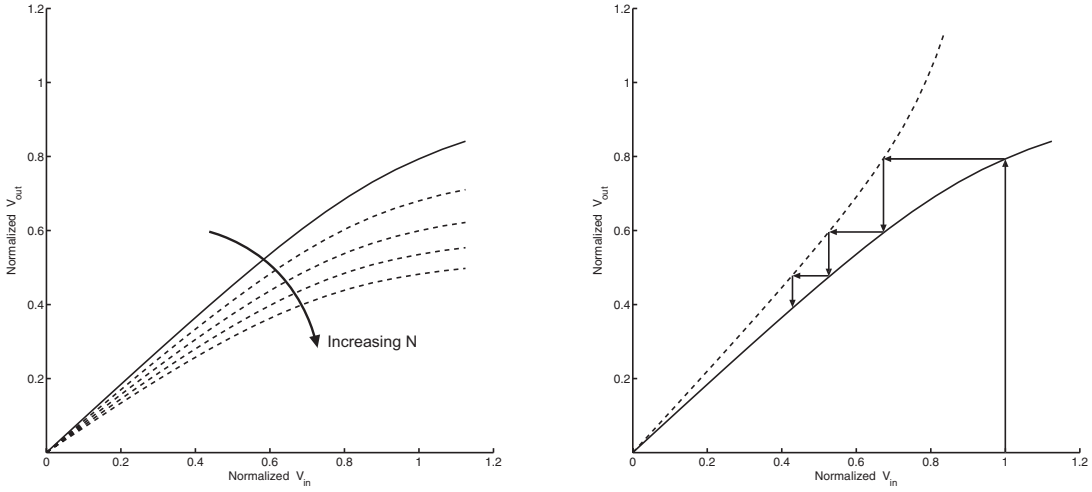
(b) Transfer of voltage for cascade of full-switching CML stages with identical VTC

Figure 2.12: VTC of a cascade of full-switching CML buffers

Alternatively, consider the a chain of CML buffers operating in the attenuating region with VTCs as the solid line shown in fig. 2.13(a). Due to the attenuating nature of each CML buffer, the aggregate VTC leads to severe reduction in output signal as the number of stages increases. The attenuation of signal can also be visualized in fig. 2.13(b). Even with an input of ΔV_{MAX}, the output at each subsequent stage is reduced as depicted in the figure.

Design Criteria for Square-law CML Design

CML circuits are commonly used in larger systems such as DLL and Clock Data Recovery (CDR). Circuit designers have analyzed its operation and put forth design methodologies for CML design for both high-speed (high-power) and low-power (low-speed) applications. Due to the scope of this work, design methodologies for low-power, low-speed operations are not analyzed. The majority of published literatures



(a) VTCs of a cascade of attenuating CML buffers; solid line - one stage VTC; dash line - cascaded stage 2 to 5

(b) Transfer of voltage for cascade of attenuating CML stages with identical VTC

Figure 2.13: VTC of a cascade of attenuating CML buffers

analyze CML circuits using a small-signal analysis for differential devices operating in saturation region [24] [25] [26]. A derivation of the conditions required for full-switching CML gates based on the sources cited is provided in appendix A. A concise summary of the most important findings are provided below.

Assuming that the differential pair devices operate within saturation region and obey the square-law voltage-current relationship, the minimum small-signal gain in the balanced state required to ensure full-switching at the output arrives at the expression presented in (2.3) [24] [26].

$$A_v = gm \cdot R \geq \sqrt{2} = 3dB \tag{2.3}$$

It states that for a CML gate to fully-switch, it must have a small-signal gain of 3dB or above when the inputs are balanced. For a cascade of CML buffers, an additional constraint is required on the fully-switched output voltage ΔV_{MAX} in order to ensure that the next-stage differential pair operates in saturation region as assumed above

[24].

$$V_t \geq I_{TAIL} \cdot R = \Delta V_{MAX} \tag{2.4}$$

The threshold voltage, V_t, in equation (2.4) is that of the differential pair devices. In standard CML topology, as shown in fig. 2.9(b), the source voltage of the differential pair devices are above zero in order for the tail current transistor to operate in saturation region. Therefore, the V_t of the two differential pair transistors are increased from their V_{t0} value due to body effect.

In summary, the two expressions presented above are derived from CML circuits with their differential pair devices operating in saturation region and obeying a square law. For a cascade of CML buffers to operate in full-switching region, they must have small-signal gain greater than 3dB and the product of I_{TAIL} and R less than the threshold voltage of the differential pair devices.

3 High-speed CML Design

3.1 Background

In the section 2.3 of the previous chapter, the square-law design approach for CML in CMOS was presented. The square-law design approach ensures that the differential pair devices operate at all times either in saturation or cut-off regions while avoiding the triode or linear region of operation. However, (2.3) and (2.4) place a limit on the value of V_{eff} of the differential transistors as the gain of a CML buffer (assuming square-law operation) is given by:

$$A_V = \frac{\Delta V_{MAX}}{V_{eff}} \tag{3.1}$$

Since the maximum value of ΔV_{MAX} is limited to the threshold voltage of the differential pair transistor, V_{eff} must be less than $\frac{V_t}{\sqrt{2}}$. Hence, the differential pair devices must operate at low current density to ensure their V_{eff} satisfies the square-law design criteria, as given by expression $V_{eff} = \sqrt{\frac{L}{\mu_n C_{ox}} J}$.

The square-law design methodology, which places emphasis on maintaining transistors in saturation region, neglects one important aspect of CML design for high-speed applications. The Open-Circuit Time Constant (OCTC) time constant for a CML circuit is an important design parameter in high-speed applications. Metrics that are critical to high-speed operation of CML circuits such as maximum frequency of operation and gate delay are all closely related to the OCTC of a CML design [27][28]. The dominant pole of the CML circuit frequency response is primarily related to the RC time constant at its output node. With the assumption that the transistor device parasitic capacitances are the dominant form of load capacitance at the output node of a CML buffer, the total load capacitance is proportional to the widths of the input and output transistors connected to that node. Hence, the OCTC at the output node

is roughly proportional to W and R:

$$\tau \propto R \cdot W \tag{3.2}$$

It is possible to rearrange (3.1) in terms of load resistance and device widths.

$$A_V = R\sqrt{\frac{\mu_n C_{ox} I_{TAIL}}{L} W} \tag{3.3}$$

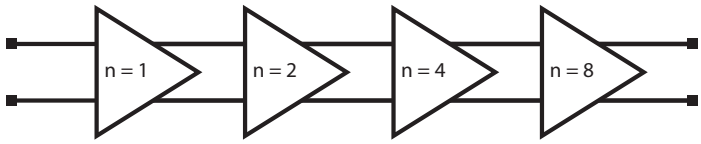
$$A_V \propto R\sqrt{W} \tag{3.4}$$

For a given CML circuit, (3.4) highlights the trade-off between load resistance and device width for a fixed amount of voltage gain and tail current [26]. Based on (3.2) and (3.4), it is possible to reduce the RC time constant of a CML stage without affecting the small-signal gain by increasing its load resistance by some factor x and decreasing its width by a factor x^2 (hence, increasing its current density) at the same time. In fact, this observation is consistent with several published high-speed CML designs [23][22][21]. The CML circuits in these published works all employ high current-densities to reduce load capacitances. The values of ΔV_{MAX} of these CML gates also exceed the device threshold voltage as prescribed in (2.4). The circuit simulation experiment detailed in the next section was devised with the aim of obtaining a better understanding of the operation of CML circuits for high-speed applications.

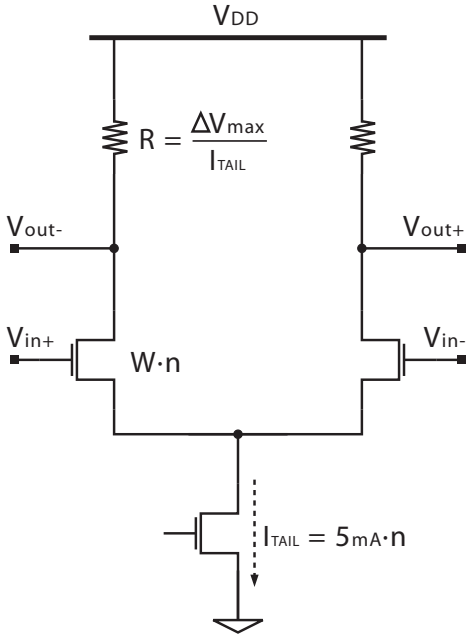
3.2 Circuit Simulation

The simulation setup shown in fig. 3.1 is designed to investigate the effect of different current-densities and resistive loads on CML circuits. A cascade of CML buffers with fanout of two is used, as shown in the block diagram in fig. 3.1(a). Each of the CML buffers has the same current density (J) and full-switching voltage (ΔV_{MAX}). The schematic of the generalized CML buffer is shown in fig. 3.1(b). The tail currents, device widths, and load resistors are scaled by the fanout factor (2 in this case) along the cascade of buffers. Throughout the experiment, the tail currents and the source voltages of the differential pairs are kept the same. It is important to maintain the source node voltage to approximately 400mV as it affects the threshold voltage of the differential pairs via body effect. The voltage of 400mV is chosen as it allows the tail

current device to operate in saturation. With the source-to-body voltage of 400mV, the threshold voltage of the differential pair devices is 480mV. All simulations in this section are performed in $0.13\mu m$ CMOS at the typical (tt) design corner and at a temperature of 75^oC.



(a) Cascade of CML buffers used for circuit simulation



(b) Schematic of CML buffer used for circuit simulation

Figure 3.1: Circuit simulation setup

3.2.1 Design I

The first design (referred to as design I) uses the square-law design methodology as the basis. As such, it has a full-switching voltage of $\Delta V_{MAX} = 400mV$, which is less than the V_t of the differential pair devices. Under a fixed tail current, the small-signal

transconductance of the transistors is proportional to $\sqrt{W}$. Its voltage gain reaches 3dB for a differential pair device width of $W = 54\mu m$. The current density, J, of this configuration is $0.092\frac{mA}{\mu m}$. The VTC of design I at DC is shown in fig. 3.2(a). The VTC confirms a fully-switched output of 400mV.

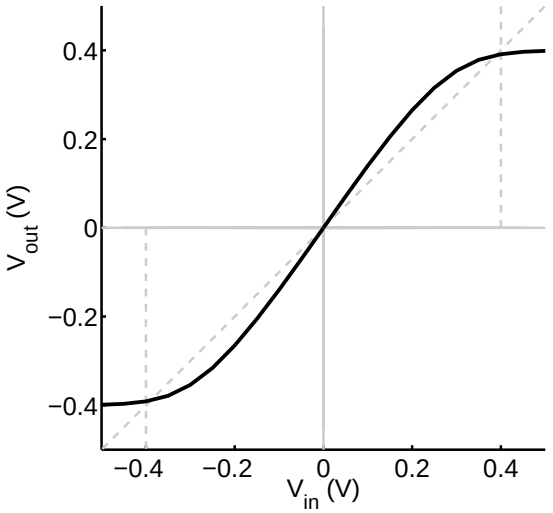
3.2.2 Design II

The second design (referred to as design II) is a modification of design I. The differential pair device widths are halved to $W = 27\mu m$, hence the current density is doubled to $0.19\frac{mA}{\mu m}$. The value of ΔV_{MAX} is kept at 400mV. Hence, the load resistors remains unchanged. However, the load capacitance due to transistor parasitics are reduced by approximately 50%. In this configuration, the small-signal voltage gain is reduced to -0.6dB, much lower than the 3dB requirement. The VTC of design II at DC is shown in fig. 3.2(b). The shape of the VTC indicates that the buffers operate in the attenuating region so this is not a workable solution.

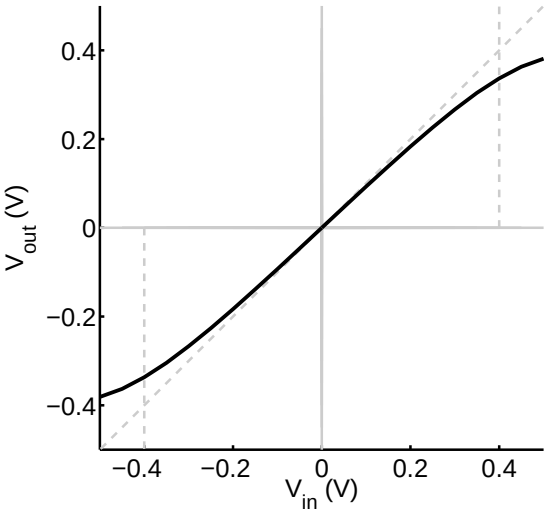
3.2.3 Design III

Based on the results from design I and II, it can be concluded that violation of the 3dB minimum gain requirement leads to designs that do not operate in the full-switching region. The third design (design III) maintains the same current density as design II, but increases its load resistance so that $A_v = 3$dB and $\Delta V_{MAX} = 635$mV. Its VTC is shown in fig. 3.2(c). The shape is similar to that of design I, indicating full-switching operation. Hence, this is a viable design alternative.

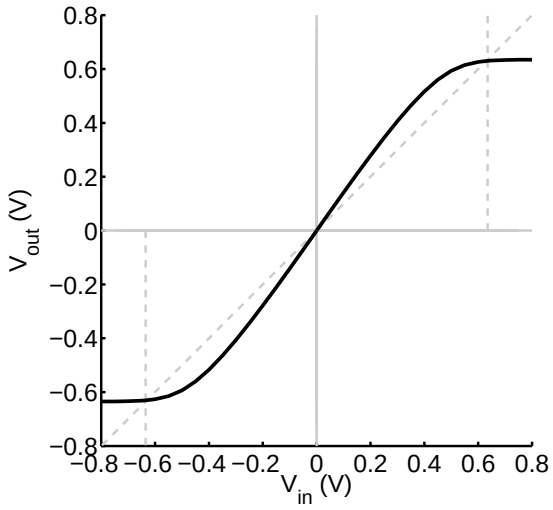
Based on these DC simulation results, one cannot distinguish whether design I or III has better high-speed performance. One can use the output RC time constant as an indication. By reducing the width by half and increasing the resistance by 58.75%, the RC time constant of design III is reduced by 19.6% from that of design I. However, the use of the RC time constant is not conclusive. The usual approach to investigate a circuit's high frequency behavior is through AC simulation. However, AC simulation linearizes the circuit with its small-signal parameters, which renders the analysis unsuitable for the large-signal operation of CML gates. Instead, a more generalized transient simulation can be used to characterize the circuit's performance at frequencies above DC. The approach taken is to excite the CML circuit with a single-tone sinusoid and observe its output. By varying the input amplitude and measuring the



(a) Design I: $W = 54\mu m$, $\Delta V_{MAX} = 400mV$



(b) Design II: $W = 27\mu m$, $\Delta V_{MAX} = 400mV$



(c) Design III: $W = 27\mu m$, $\Delta V_{MAX} = 635mV$

Figure 3.2: VTCs of CML buffers at DC

output amplitude it is possible to obtain the entire input-output transfer characteristics at any particular input frequency. This is equivalent to a VTC but at frequencies other than at DC. These frequency-dependent VTCs allows one to characterize the circuit's response across a broad frequency band.

Of course, the small-signal gain response of the CML circuit is embedded within its frequency-dependent VTC. The small-signal voltage gain at a particular frequency, $A_v(\omega)$, is simply the slope of the corresponding VTC around the origin. Hence, the small-signal gain response of a circuit can be obtained by making this observation across the desired frequency range. This has been verified with results from AC simulation.

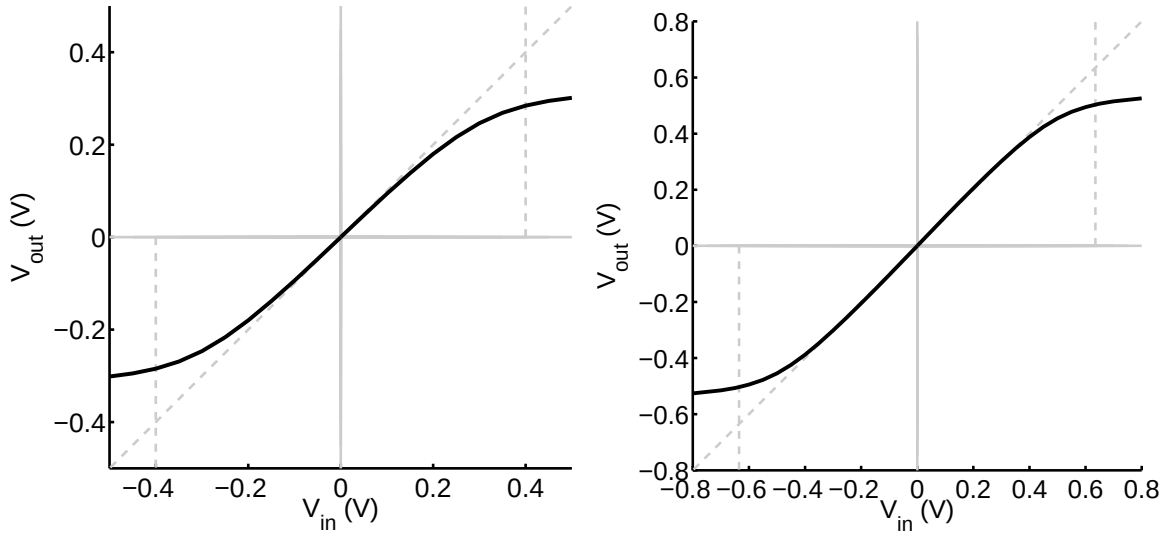
One can formalize the concept of a frequency-dependent VTC by defining the mathematical function in (3.5).

$$V_{out} = H_{CML}(V_{in}, \omega) \tag{3.5}$$

This representation is particularly useful in MATLAB environment as the frequency-dependent VTC is represented in matrix format. Fig. 3.3 illustrates the VTCs of designs I and III at 5GHz. At 5GHz, the VTC of design I starts to fall below the unity-gain line (dotted line in figure) at $V_{in} = 0.1V$. On the other hand, the VTC of design III starts to drop below the unity-gain line at $V_{in} = 0.35V$. With the inputs normalized to their full-swing ΔV_{MAX} the performance of design III is superior to that of design I. Therefore, it is possible to use a frequency-dependent VTC to evaluate the performance of CML circuits at high frequencies.

This concept of frequency-dependent VTC allows the analysis of the input-output voltage transfer for a CML circuit over a wide range of frequencies. However, numerous x-y plots like those in fig. 3.3 would be required to cover the frequency range of interest. Furthermore, insight into the overall VTC over different frequencies is easily lost by spreading the data across multiple plots. A 3-D mesh representations allows all the simulations results to be displayed concisely in one single diagram. By using frequency as the third axis, the 3-D mesh plot can be generated in MATLAB. The 3-D meshs for designs I and III are shown in fig. 3.4 with their VTCs normalized to their respective ΔV_{MAX}. The highlighted solid and dashed lines correspond to the VTCs shown in fig. 3.2 and 3.3 at DC and 5GHz respectively.

The 3-D meshes in fig. 3.4 allow quick visualization of the behavior of the CML gates over the entire frequency range of interest. The shape of the VTC mesh reflects



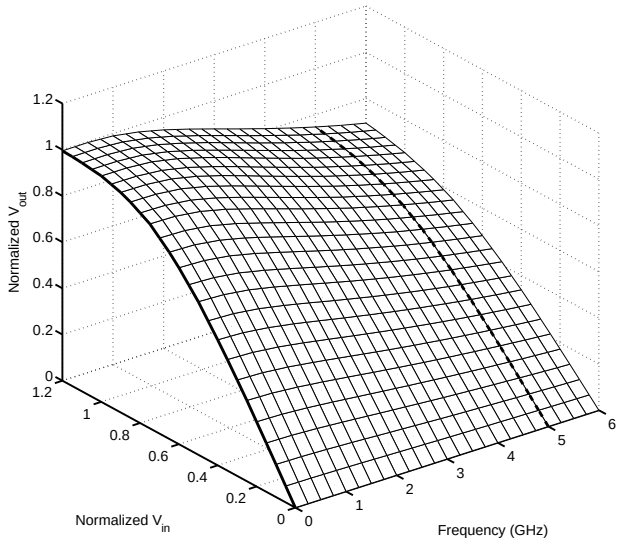
(a) Design I: $W = 54\mu m$, $\Delta V_{MAX} = 400mV$

(b) Design III: $W = 27\mu m$, $\Delta V_{MAX} = 635mV$

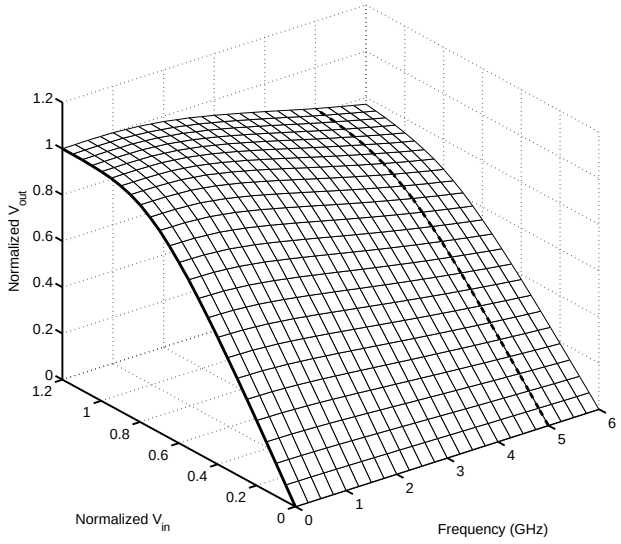
Figure 3.3: Frequency-dependent VTCs of CML buffers at 5GHz

the high-frequency performance of the CML design. Design I's VTC mesh drops down significantly at high frequencies compared to that of Design III. One can observe that design I slips into the attenuating region of operation at a lower frequency.

Based on the simulation results of the three designs, one can conclude that by simultaneously increasing the current density of the differential pair and load resistance, the RC time constant of a CML stage can be reduced and the CML stages can maintain full swing signals up to higher frequencies. The improvement in performance is verified by using frequency-dependent VTC. However, $\Delta V_{MAX} = 635mV$ of design III is above the differential pair transistors' V_t of 480mV, which is a clear violation of condition put forth by (2.4). The square-law design methodology, with its emphasis on maintaining the saturation region of operation, is too conservative in high-speed CML design. The load capacitance and resistance, which is neglected in the square-law design methodology, plays an important role in high-speed operation of CML circuits. Furthermore, $\Delta V_{MAX} > V_t$ implies triode region of operation for the differential pair transistors during part of CML switching. The expressions (2.3) and (2.4) are derived with assumption of saturation (square-law) region of operation. As such, they are no longer valid for high-speed CML design with high current den-



(a) Design I: $W = 54\mu m$, $\Delta V_{MAX} = 400mV$



(b) Design III: $W = 27\mu m$, $\Delta V_{MAX} = 635mV$

Figure 3.4: Frequency-dependent VTCs of CML buffers from DC to 6GHz; DC (solid), 5GHz (dashed)

sities and high full-switching output voltages since velocity saturation and/or critical vertical electrical fields in the MOSFETs may cause sub-quadratic voltage-current relationships in the MOSFETs. This points to the possible existence of CML designs with even higher speeds of operation. The next section explores one such design with the aid of frequency-dependent VTC as a means of comparison.

3.3 Soft-switching

In the square-law CML design approach, only two regions of operation are considered: full-switching and attenuating. "Soft-switching" is the name given to a type of operation that fits in between those two. In this region of operation, the output swing is less than that of fully-switched case but sufficient to preserve signal strength. A small amount of current still flows in the "off" device of the CML differential pair. As a result, the output voltages of the CML buffers are less than its fully-switched value of ΔV_{MAX}. In summary, the three regions of operation for CML circuits: full-switching, soft-switching, and attenuating are illustrated in the voltage waveforms shown in fig. 3.5.

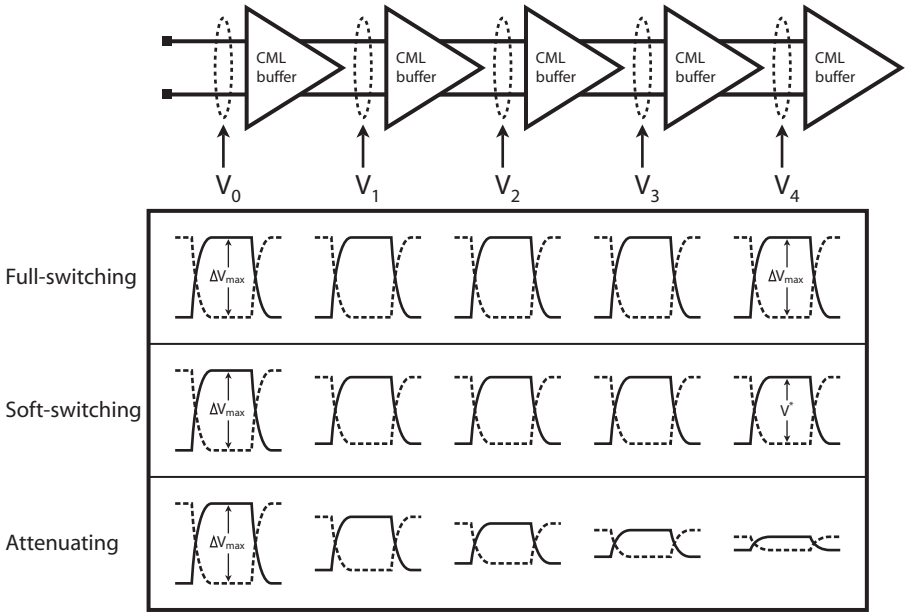


Figure 3.5: The three regions of operation for CML circuits

Using this relaxed definition of CML switching, it is possible to reduce the load resistance of CML gates compared to that required to maintain full-switching. The

lowered values of resistance is desirable for high-speed CML design as it translates to reduction in the *RC* time constant. The existence of CML design that operates in soft-switching region has been reported in [29]. Fig. 3.6 illustrates the VTC of a CML circuit operating in soft-switching region.

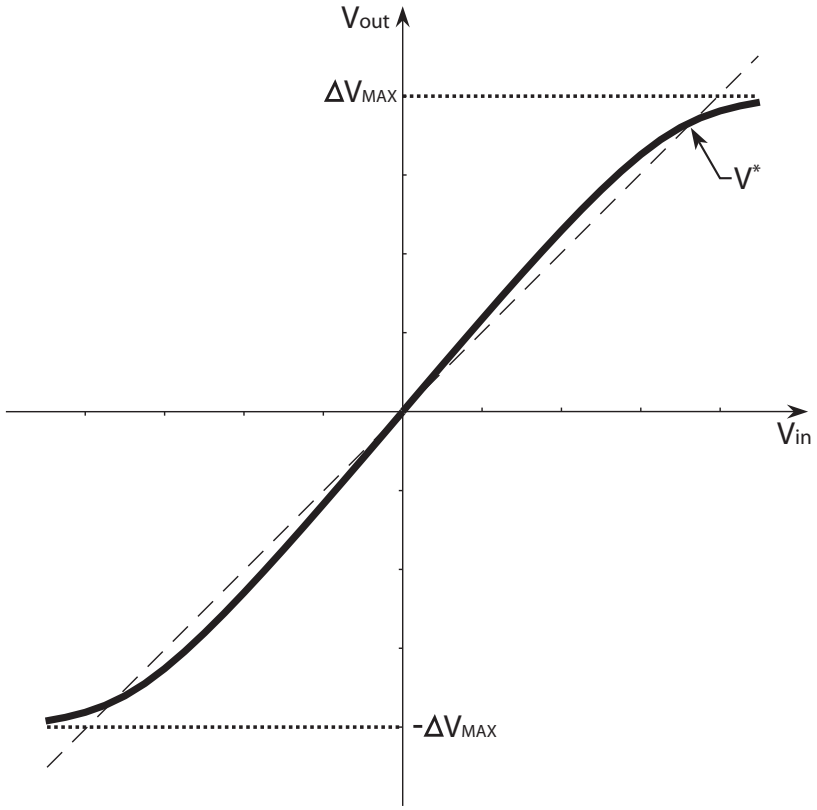


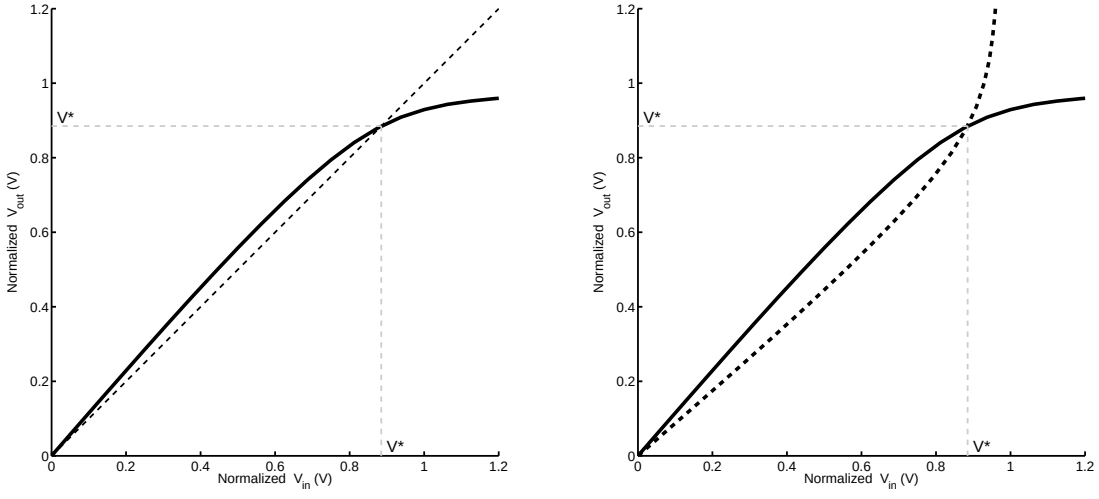
Figure 3.6: VTC of a CML circuit operating in soft-switching region

In the soft-switching region of operation, a small amount of current flows through the "off" device in the differential pair. As a result, the output voltage is less than the full-switching value of ΔV_{MAX}. In fact, the output voltage is given by $V_{out} = (I_{on} - I_{off}) \cdot R$. Under this relaxed definition of switching, a signal is preserved if the output swing is greater or equal to the input swing. The critical value that separate this region of operation from the attenuating region is the point where the input and output are identical. This voltage is defined as V^* such that $V^* = V_{in} = V_{out}$. A more vigorous definition of V^* is provided using the mathematical function.

$$V^*(\omega) = H_{CML}(V^*(\omega), \omega) \tag{3.6}$$

Another important note about V^* is that the CML circuit has a large-signal gain of

one at this point. In general, V^* is frequency-dependent and is there fore shown as $V^*(\omega)$ in (3.6). This definition can be extended to the full-switching region of CML operation, in which $V^* = \Delta V_{MAX}$. Graphically, V^* can be interpreted as the point at which the VTC intersects with line $V_{in} = V_{out}$. Fig. 3.7 illustrates two methods for obtaining V^* graphically from VTC.



(a) Using $V_{in} = V_{out}$

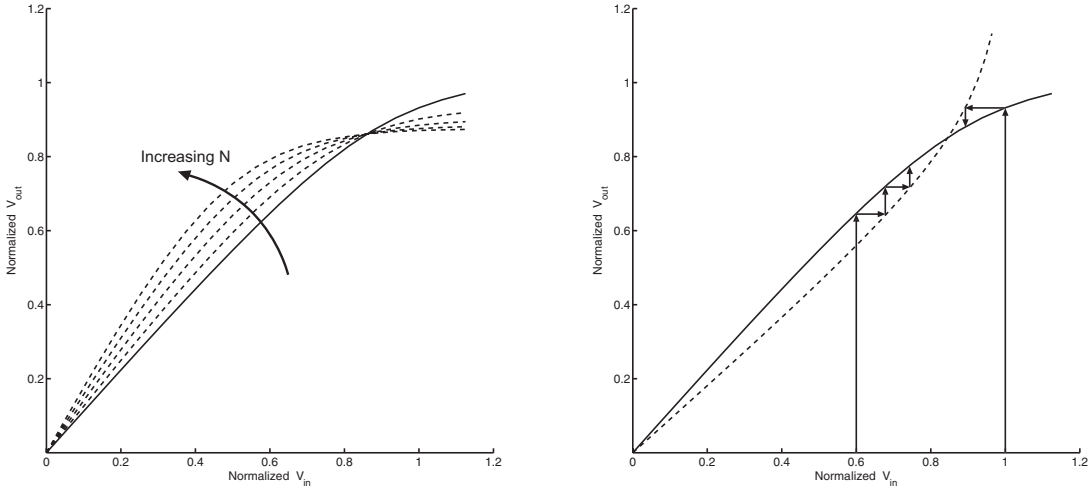
(b) Using mirrored VTC

Figure 3.7: Two methods of obtaining V^* from VTC

V^* is obtained from fig. 3.7(a) using the unity voltage gain definition, whereas fig. 3.7(b) obtains the same threshold voltage using the definition given in (3.6). By mirroring the VTC along the $y = x$ line, the input and output voltage transfer is reversed. The intercept of the original VTC and its inverse is the point where $V_{out} = V_{in} = V^*$. It is also possible to obtain the value of V^* using MATLAB given a VTC matrix obtained from SPICE simulation.

Consider a cascade of soft-switching CML buffers with identical VTCs as shown in the solid line in fig. 3.8(a). The aggregate input-output transfer characteristic of CML buffers, where the number of stages is denoted by N, can be derived using the original VTC. The dotted lines in fig. 3.8(a) are obtained in MATLAB from the original VTC vector which was obtained from a SPICE simulation of a single CML gate. Smaller input voltages result in an output of V^* as N increases. The importance

of V^* is clearly seen in this cascade configuration. As more stages are added to the cascade, the output voltage settles to V^* as inputs above V^* are compressed while inputs below are amplified. As a signal propagates down a cascade of CML buffers, the signal amplitude can be traced graphically by traversing the VTC and its inverse as shown in fig. 3.8(b). Again, this shows that input amplitudes both above and below V^* converge towards an amplitude of V^* after passing through a few gates.



(a) VTCs of a cascade of soft-switching CML buffers; solid line - one stage VTC; dashed line - cascaded stage 2 to 5

(b) Transfer of voltage for cascade of soft-switching CML stages with identical VTC

Figure 3.8: VTCs of a cascade of soft-switching CML buffers

3.3.1 Design IV

In the previous section, design III had the best performance of the three designs due to its lower RC product. Further RC improvements can be obtained by further increases in current density and load resistance. However, the V_{eff} of the transistor as well as the value of ΔV_{MAX} both increase in this design approach. Concerns about voltage headroom and/or power consumption of the design eventually limit the current density in practice. According to [27], biasing the transistors at the peak f_T yields minimum gate delay. This is used as a starting point for the new design

(design IV). Using a device width (W) of $17\mu m$ in the schematics in fig. 3.1(b), the current density when the device is fully-switched is $0.29\frac{mA}{\mu m}$. The load resistance in the simulation is increased until the soft-switching output voltage V^* approaches ΔV_{MAX}. For the design with full-switching voltage of 800mV, the corresponding V^* is 780mV at DC. The RC product of design IV is approximately 37% lower than design I. It has lower small-signal gain, 2.2dB at low frequency as shown in fig. 3.9. The lower voltage gain of $2.2dB < 3dB$ is a consequence of soft-switching. A larger value of load resistance would be required for gain of 3dB or higher, but that would lead to degradation in RC time constant. The AC gain response of design I (full-switching region) and design II (attenuating region) are also shown in fig. 3.9.

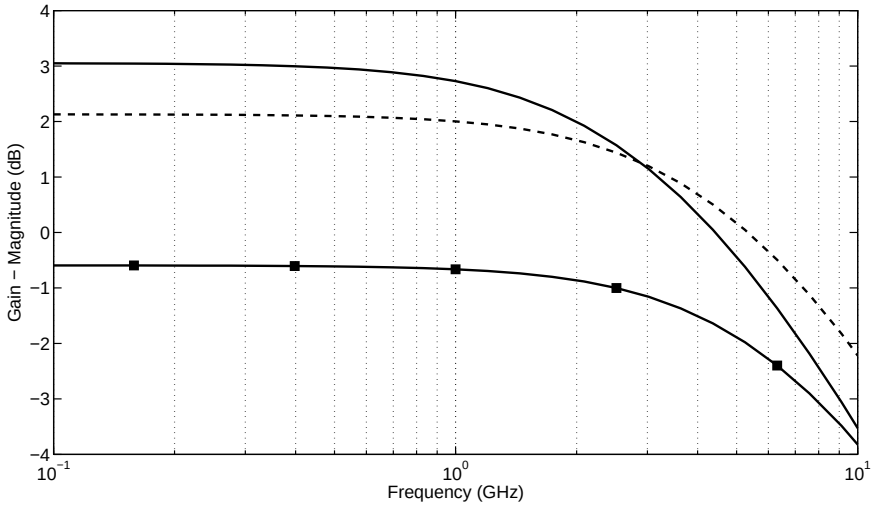
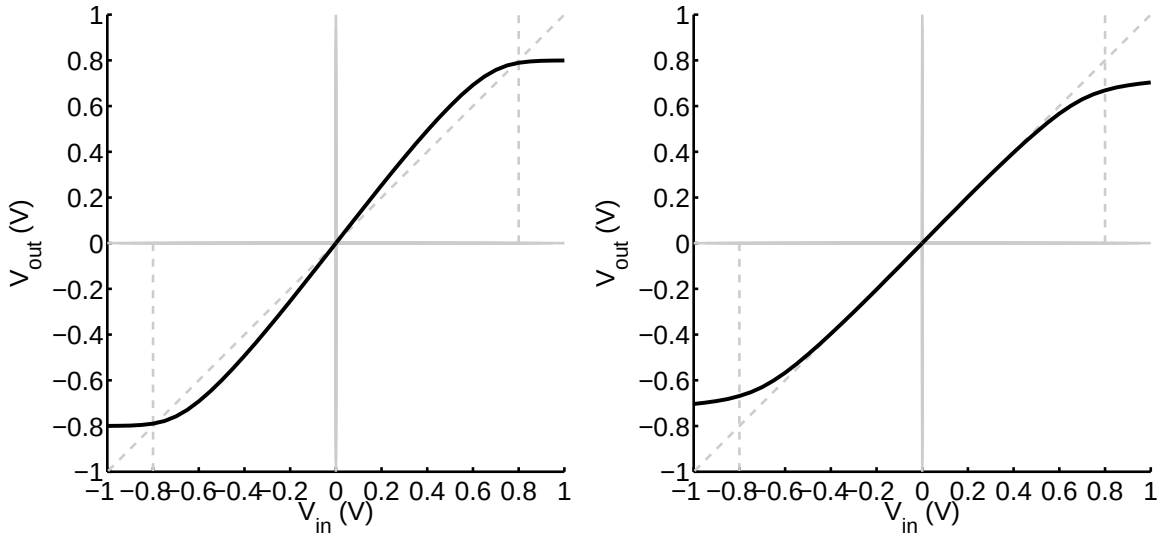


Figure 3.9: AC gain response for design I(solid), II(square marker), IV(dashed)

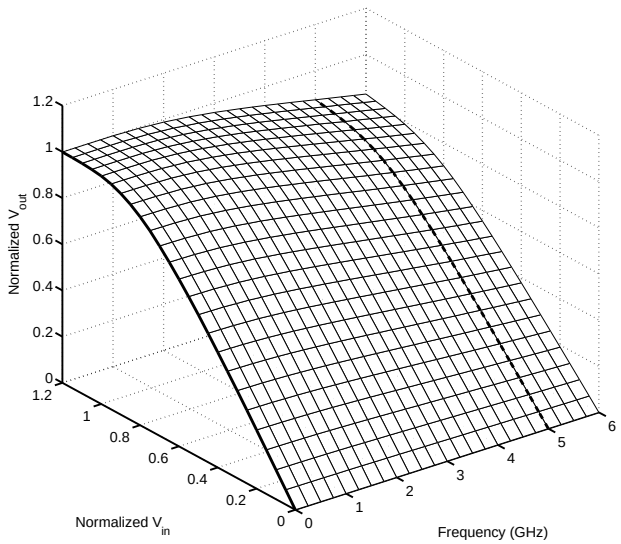
The VTCs of design IV at DC and 5GHz are shown in fig. 3.10(a) and 3.10(b). The VTC of design IV using a 3-D mesh representation is shown in fig. 3.10(c). The VTCs in the mesh representation are normalized to the ΔV_{MAX} of 800mV of design IV.

The soft-switching voltage, $V^*(\omega)$ as defined in (3.6), is a function of the input sinusoidal frequency ω. For a given CML circuit, there exists a value of V^* for every input frequency (provided that the circuit is not in the attenuating region of operation). In a 2-D plot of VTC, V^* is located at the point where the VTC intersects the line $y = x$, as shown in fig. 3.7(a). In the mesh representation, the values of $V^*(\omega)$ are located at the intersection of the VTC mesh and the $V_{out} = V_{in}$ plane. The VTC mesh of design I and IV are shown in fig. 3.11, along with the plane $V_{out} = V_{in}$ (in



(a) At DC

(b) At 5GHz



(c) 3-D mesh representation of VTC of design IV

Figure 3.10: VTCs of design IV: $W = 17\mu m$, $\Delta V_{MAX} = 800mV$

grey). The intersection of the two surfaces indicates the values of $V^*(\omega)$ from DC to 6GHz. Similar to other VTC meshes shown, the VTCs in fig. 3.11 have been normalized to their respective full-switching voltage (ΔV_{MAX}).

Fig. 3.11 illustrates clearly the importance of RC time constant in the design of high-speed CML circuits. V^* for design I, which strictly adheres to the square-law design methodology, drops below 80% of its full-switching value above 2.5GHz. On the other hand, design IV maintains a $V^*(\omega) > 0.8 \times \Delta V_{MAX}$ up to 3.7GHz. The intersection line between the VTC meshes and the unity-gain plane, representing $V^*(\omega)$ versus frequency, are plotted for designs I and IV in fig. 3.12.

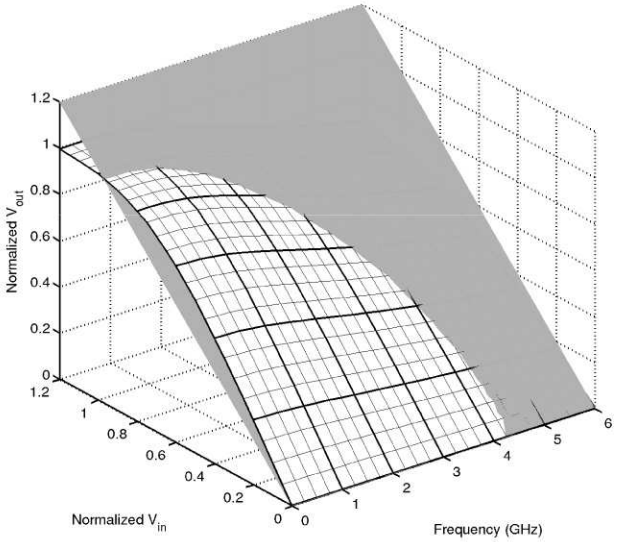
Fig. 3.12 allows the designer to quickly assess whether a CML design has the performance required to function at the desired frequency. Sufficient soft-switching voltage must be maintained across the target frequency range to ensure the circuits have sufficient swing to meet the output specification. For systems where CML circuits are most commonly employed, such as pre-drivers and clock distribution networks, the input-swing specification of the circuits being driven set the limit to the lowest permissible soft-switching voltage, $V^*(\omega)$.

Based on the simulation results obtained from design I through IV, it is concluded that the square-law CML design methodology leads to designs that are too conservative for high-speed operations. By relaxing the requirement for the switching transistors to operate in saturation region at all times and relaxing the requirement of full-switching, faster CML circuits can be designed. In particular, biasing the differential pair transistors at their peak f_T current density leads to higher speed CML designs. Design IV is chosen as the basis for the CML buffers in this work. Additional improvements in CML buffer design are detailed in the next section.

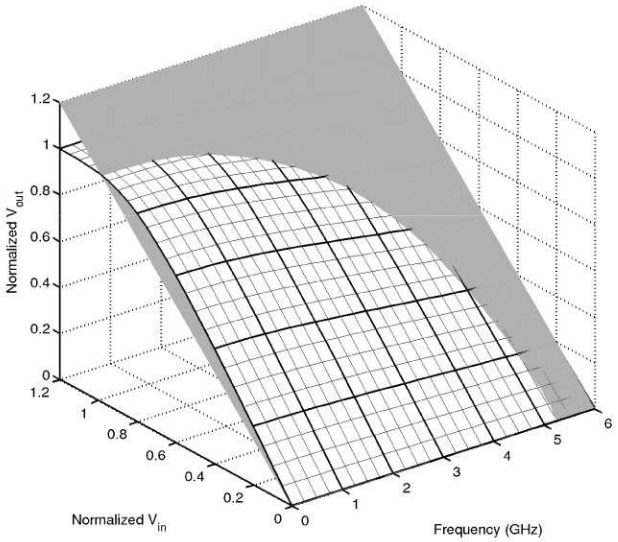
3.4 Design of CML buffers

To design a transmitter with a data-rate of 40Gb/s in 4PAM mode of transmission, the data path must have at least 10GHz of bandwidth while the clock signal required for PWM-PE has signal content at 20GHz. The designs proposed thus far in the simulation environment in the previous section are clearly insufficient for these speeds. Hence, further speed-improvement techniques are described in this section.

To increase the high-speed performance of the CML buffers, it is important to reduce the RC product at the output nodes. Inductive peaking [30] is commonly



(a) Design I: $W = 54\mu m$, $\Delta V_{MAX} = 400mV$



(b) Design IV: $W = 17\mu m$, $\Delta V_{MAX} = 800mV$

Figure 3.11: VTC meshs and the $V_{out} = V_{in}$ plane

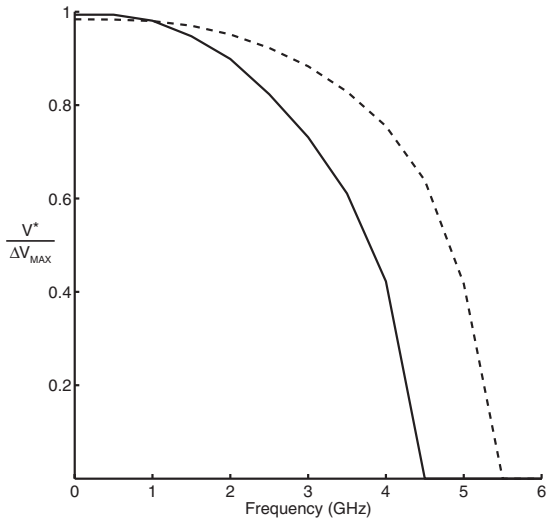


Figure 3.12: V^* versus frequency; design I(solid), design IV(dashed)

used to reduce the load capacitance and hence increase the bandwidth of the circuit. By introducing inductors with values of $L = \frac{CR^2}{3.1}$, it is possible to increase the 3-dB bandwidth of the CML stages by 60%. Although inductive peaking can extend the bandwidth of the CML stages, it comes with the cost of extra area for the spiral inductors as well as the added complexity in the modeling of such spiral inductors.

However, design IV still suffers from inadequate bandwidth even with inductive-peaking. In order to further increase its bandwidth for the clock and data distribution, the RC time constant at the output node must be further reduced. Since the resistive load at the output is already determined by the design parameters ΔV and J, the needed performance can only be gained by reducing the capacitive load. The OCTC of a CML circuit in CMOS technology is given by (3.7) [27].

$$\tau_{CML} = R_L(C_{gd} + C_{db} + (k + \frac{R_g}{R_L})(C_{gs} + (1 + gm \cdot R_L)C_{gd})) \tag{3.7}$$

$$\simeq R_L(C_{gd} + C_{db} + k(C_{gs} + (1 + gm \cdot R_L)C_{gd})) \tag{3.8}$$

Where k, represents the fanout ratio between CML gates. Assuming that $k \gg \frac{R_g}{R_L}$, expression in (3.7) can be approximated to (3.8). Since the parasitic capacitance due to device size is determined by the current density(J), the only variable which can be controlled is the fanout(k). The total load capacitance at the output of a CML gate driving another CML gate can be reduced by lowering the fanout ratio.

In a cascade of CML buffers, the output of one stage becomes the input of another

stage. This can be expressed in mathematical form:

$$V_{out} = H_{cascade}(V_{in}, \omega) \tag{3.9}$$

$$H_{cascade}(V_{in}, \omega) = H_{buf}(H_{buf}(H_{buf}(\ldots H_{buf}(V_{in}, \omega)\ldots, \omega), \omega), \omega) \tag{3.10}$$

The nested nature of the overall transfer function based on the individual CML buffer VTC is evident in the expression (3.10). Graphically this is shown in fig. 2.12, 2.13, and 3.8. Therefore, from knowledge of the VTC of a single CML buffer, the VTC of a cascade of buffers with constant fanout can be inferred. Fig. 3.13 shows the V^* versus

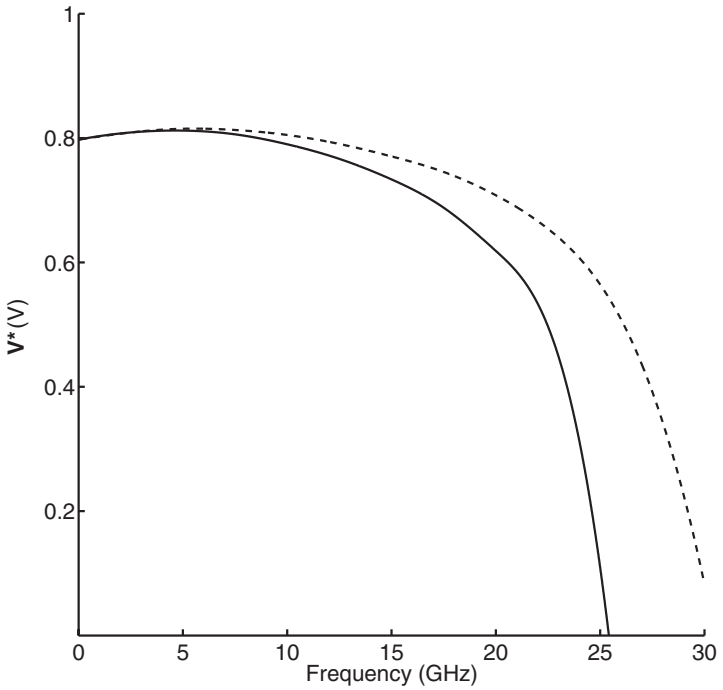


Figure 3.13: V^* as a function of frequency; $k = 1.5$(solid); $k = 1.2$(dashed)

frequency plot for a CML buffer based on design IV ($\Delta V_{MAX} = 800mV$, $J = 0.29\frac{mA}{\mu m}$) with fanout ratios of $k = 1.5$ and $k = 1.2$. Inductive peaking was used in the design of these CML circuits. Based on fig. 3.13, the cascade of buffers with $k = 1.5$ is sufficient for those parts of transmitter system that require a signal bandwidth up to 10GHz. However, for clock distribution requiring 20GHz signal bandwidth, only the cascade of buffers with $k = 1.2$ is suitable.

Of course, using low fanout ratio to achieve the desired bandwidth requires more

power and area. As the fanout ratio is reduced, more stages are required to provide sufficient drive strength at the output of a cascade.

Finally, since the design parameters of CML circuits are closely linked by simple design equations, a CML cascade can be designed quickly once the fanout ratio and the design of the first stage in the cascade are determined. The design equations for the parameters of a CML buffer (W_2, I_2, R_2, and L_2) in terms of the preceding buffer's parameters (W_1, I_1, R_1, and L_1) and the fanout, k, are given as follows.

$$W_2 = k \cdot W_1 \tag{3.11}$$

$$I_2 = k \cdot I_1 \tag{3.12}$$

$$R_2 = \frac{\Delta V}{I_2} = \frac{\Delta V}{k\dot{I}_1} = \frac{R_1}{k} \tag{3.13}$$

$$L_2 = \frac{L_1}{k} \tag{3.14}$$

3.5 Design of Complex CML gates

Complex CML gates, which include circuits such as latches, flip-flops, multiplexers, XORs, and combinational logic gates are often the bottlenecks for high-speed implementation. The complex topology of these circuits poses additional design challenges compared to the design of CML buffers. Some of these challenges and proposed solutions are presented in this section.

The primary challenge in the design of complex CML gates for high-speed applications is the high self-loading capacitance at the output of these circuits. For instance, the topologies for XOR and MUX require an additional differential pair due to the additional second input signal. The additional differential pair increases the output capacitance of the circuit, thereby adversely affecting its maximum operating frequency. An additional challenge for the design complex CML gates with multiple inputs is voltage headroom. For high-speed CML circuits biased at high current density (near peak f_T current density), the high effective gate voltage (V_{eff}) becomes an issue when more than one differential pair appears in a stack.

Due to the importance of these complex logic gates in larger systems, circuit designers have investigated solutions to these issues. Solutions for reducing self-loading

capacitance have been proposed in [22][31]. Similarly, a solution for the voltage headroom issue has also been proposed [32]. A different simpler solution is proposed in this work. The available design parameters in the standard CML topology are simply chosen to mitigate target these specific issues. Although the analysis performed in the previous section focused on CML buffers, the insights gained also allow for proper choice of design parameters for more complex CML gates in high-speed applications.

First, reduction of DC bias current density from $J = 0.30\frac{mA}{\mu m}$ to $J = 0.20\frac{mA}{\mu m}$ is proposed. The reduction in current density is accompanied by a reduction in V_{eff}. The full-switching output swing (ΔV_{MAX}) is also reduced from 800mV to 600mV. The combination of lowered V_{eff} of the differential pair devices and ΔV_{MAX} alleviates the voltage headroom issue. The gate delay increases by less than 10% with the reduction in J [27]. Furthermore, using this design approach the differential pairs are more strongly switched since the buffers preceding the complex gate will have a relatively larger ΔV_{MAX}. Inductive peaking is also used in the design of these complex CML gates.

As an example, consider the XOR circuit required in the transmitter design (block diagram shown in fig. 3.14). Fig. 3.15 shows the simulated VTC mesh of the XOR circuit with data as input and the clock signal differential pairs fully-switched. With an input voltage above 700mV, complete switching of the XOR gate is evident.

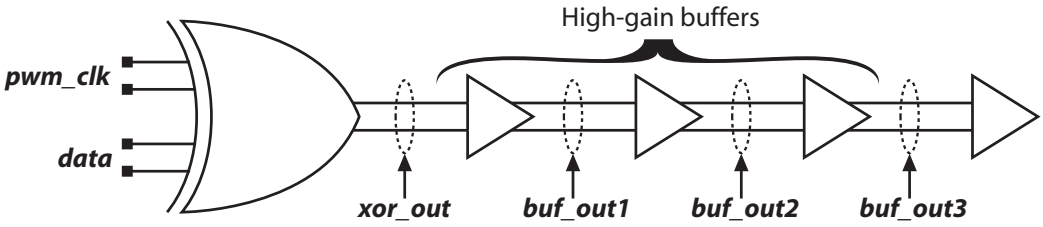


Figure 3.14: Block diagram of XOR CML circuit with high gain buffers

The design of the buffers following the complex CML circuit are also important. Firstly, the OCTC of the complex CML gate can be lowered by reducing the fanout ratio to the next stage buffer. For instance, the fanout ratio of the XOR gate to next-stage buffer in fig. 3.14 is $k = \frac{W_{BUF}}{W_{XOR}} = \frac{24\mu m}{40\mu m} = 0.6$. The use of inverse scaling ($k < 1$) as a means to extend the bandwidth of a CML circuit is reported in [33].

Secondly, due to reasons such as slight misalignment of the arrival of the two inputs or DC offset in the Duty Cycle Control (DCC) circuit, the output waveform of a complex CML gate may sometimes have insufficient amplitude to drive other CML

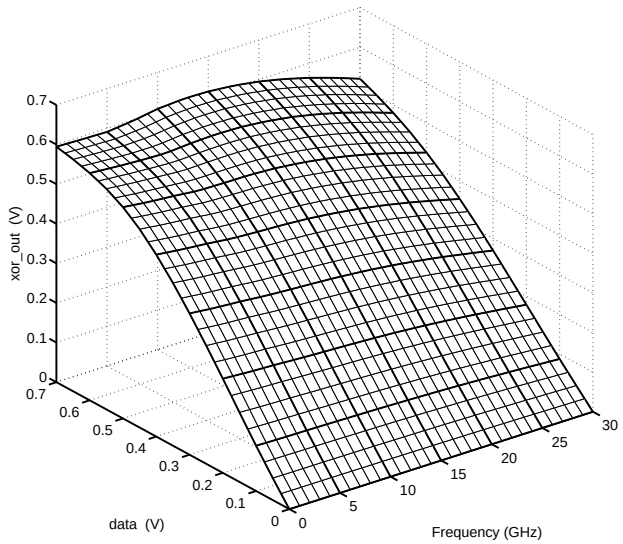


Figure 3.15: VTC of XOR circuit with data as input and clock signal fully-switched

gates. This issue can be solved by using one or more buffers with higher gain following the complex gate. This is illustrated in fig. 3.14 with the cascade of three high-gain buffers. The small-signal voltage gain is increased from 2.2dB of the standard buffers to 4.3dB for these high-gain buffers. In order to maintain the required bandwidth along with the increased voltage gain, the fanout ratio is necessarily reduced. Each of the high-gain buffers in fig. 3.14 has a fanout of one. The simulated VTC mesh of the high-gain buffer with a plane representing $V_{out} = V_{in}$ is shown in fig. 3.16.

Using MATLAB and the SPICE-simulated VTCs of the XOR circuit and high-gain buffers individually (H_{xor} and H_{hgb} respectively), it is possible to obtain the combined VTC from *data* to buf_out3 in fig. 3.14 as follows.

$$buf\_out3 = H_{hgb}(H_{hgb}(H_{hgb}(H_{xor}(data, \omega), \omega), \omega), \omega) \tag{3.15}$$

The VTCs of the cascade of the XOR gate and three high-gain buffers are shown in fig. 3.17. Note that at the output of the third high-gain buffer(buf_out3), the targeted soft-switching output swing is obtained for input swings as small as 600mV at 20GHz.

The VTC mesh of buf_out3 is shown in fig. 3.18(a) indicating that the combined XOR and high-gain buffer circuits can operate up to 20GHz. The drawback of this design approach is the additional power and area of the high-gain buffer stages.

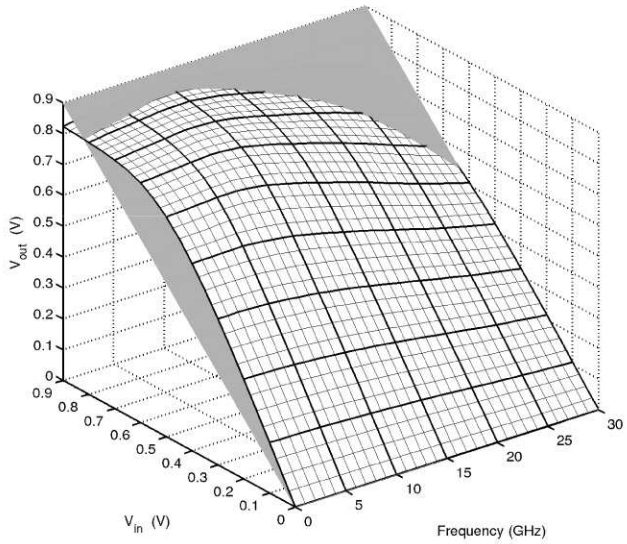
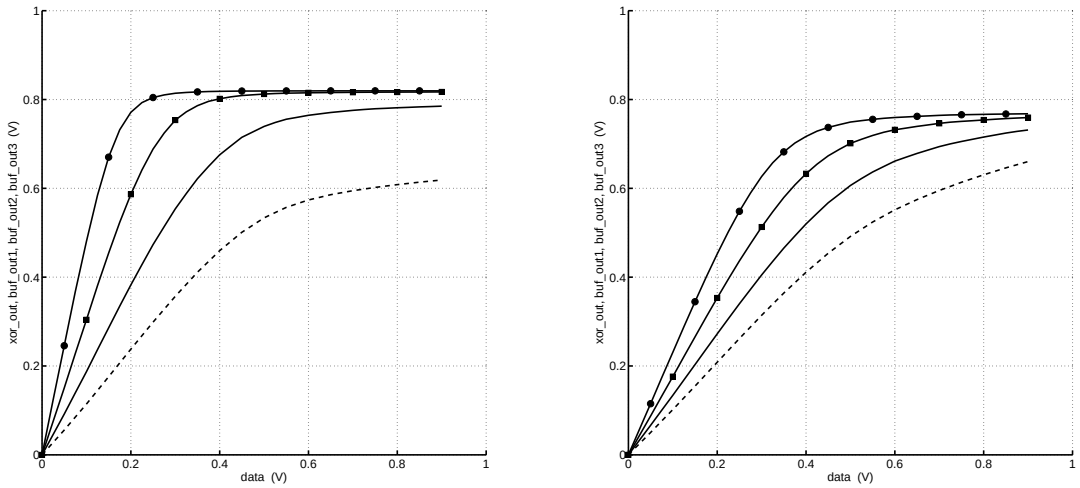


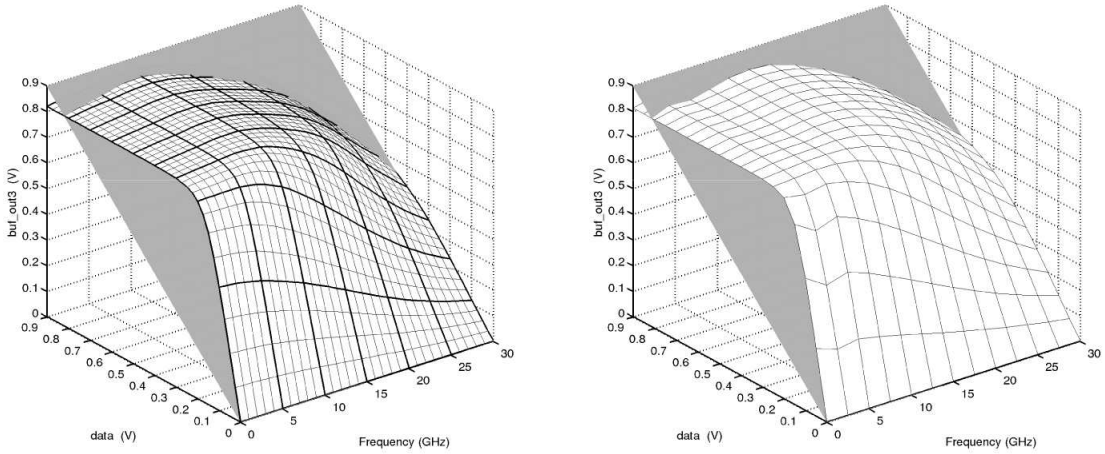
Figure 3.16: VTC of high-gain buffer with $V_{out} = V_{in}$ plane



(a) At DC

(b) At 20GHz

Figure 3.17: VTCs of XOR CML circuit with high gain buffers; xor_out(dashed), buf_out1(solid), buf_out2(square marker), buf_out3(circular marker)



(a) Generated in MATLAB (b) Simulated in Cadence

Figure 3.18: VTC of buf_out3 with $V_{out} = V_{in}$ plane

The mesh in fig. 3.18(a) is generated by simulating the frequency-dependent VTCs of an individual XOR gate and high-gain buffer in SPICE including the capacitive load of the next stage (H_{xor} and H_{hgb}), and then applying equation (3.15) in MATLAB. For verification purposes, the entire circuit shown in fig. 3.14 is re-simulated in SPICE sweeping the amplitude and frequency of the *data* input and capturing its output at buf_out3. The resulting VTC mesh is shown in fig. 3.18(b). The close correspondence of the two VTCs serves as a validation for the design methodology using input-output transfer characteristics of CML circuits. This approach is generalizable to other logic styles and saves considerable simulation time, especially for long cascades of logic and/or for performing verification over PVT variations.

3.6 Conclusion

A high-speed design approach for CML circuits in CMOS is presented in this section. Circuit simulation is used extensively to investigate the behavior of CML circuits in high-frequency domain. Concepts such as frequency-dependent VTC along with soft-switching of CML gates are introduced. It is found that superior performance can be gained by biasing the circuits at higher current densities than prescribed by

the square-law design approach. In addition, design of cascades of CML buffers as well as complex blocks are also presented. This high-speed CML design approach is used for circuits in this thesis work.

4 Design of a 40-Gb/s 4PAM PWM-PE Coaxial Cable Driver

4.1 Specifications

The transmitter is designed in $0.13\mu m$ CMOS technology for the reasons presented in section 2.2.5. Three single-ended, ac-coupled inputs are required: the Most Significant Bit (MSB) and Least Significant Bit (LSB) of data to be transmitted and the clock signal. The maximum input data rate for the MSB and LSB streams is 20Gb/s while the highest clock frequency is 20GHz. Differential output signals matched to 75Ω are available via output pads. They are designed to provide 1.6Vpp per side with a matched 75Ω load. Duty-cycles between 50 to 75 percents are required for the adjustable pre-emphasis control. To accommodate very short (hence, low loss) channels, the transmitter has the ability to turn off pre-emphasis, reduce the output swing, and for lower data rates, to transmit binary signals. Having such flexibility would ensure its usefulness in a wide range of scenarios with different channels and receivers.

4.2 System Architecture

Fig. 4.1 is the block diagram of the transmitter. Also shown are signals at various points within the transmitter. The two binary input streams are converted into a three-bit thermometer code with Gray coding. The input clock signal has its duty-cycle set by the DCC circuit. The data and clock signals then combine to create three data streams with PWM-PE. Finally, the three data streams converge at the output driver to create the 4PAM signal with PWM-PE. The major functional blocks of this circuit are the thermometer Gray code encoder, PWM-PE modulator, and the output driver. Each of these functional blocks are discussed in more detail in the following sections.

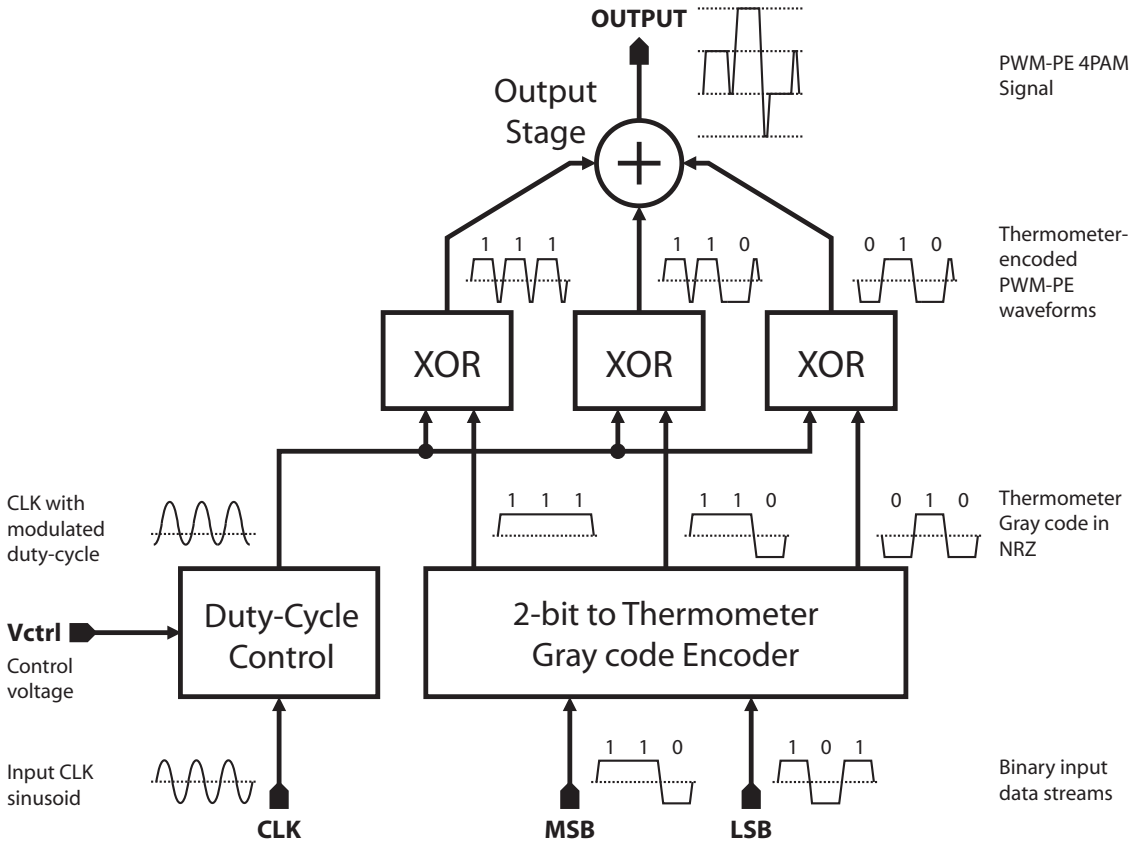


Figure 4.1: Functional block diagram of transmitter system architecture

4.2.1 Thermometer Gray-code Encoder

The role of the transmitter is similar to that of a 2-bit Digital-Analog Converter (DAC). The two digital input streams, MSB and LSB, are transformed into a 4-level (4PAM) output. One approach to generating the analog signal is to have the MSB drive twice the output current as the LSB. The main advantage of binary-weighted approach is that is does not require encoding logic, thus reducing circuit complexity and power. The drawbacks of this approach is that it necessitate the design of two distinct branches of circuits with different loadings for the MSB and LSB paths, but which must be designed to have identical delay. In addition, it cannot take advantage of Gray coding to reduce the BER of the transmitter.

In this work, the two binary input data-streams are encoded into three equally-weighted streams, A, B, and C as shown in fig. 4.1. Each of the three encoded streams drives the same load, making their delays well-matched. The circuits of the three branches can be duplicated. Furthermore, note that by using Gray coding, any

level mistaken for a neighbouring level results in only one bit error. This results in a lower BER than a binary-encoded link. The drawback is increased complexity in the encoder logic. Logic expressions implementing the truth table in table 4.1 are shown in (4.1), (4.2), and (4.3).

Table 4.1: Truth table for Gray-code encoder outputs

MSB	LSB	A	B	C
1	0	1	1	1
1	1	0	1	1
0	1	0	0	1
0	0	0	0	0

$$A = M \cdot \bar{L} \tag{4.1}$$

$$B = M \tag{4.2}$$

$$C = M + L \tag{4.3}$$

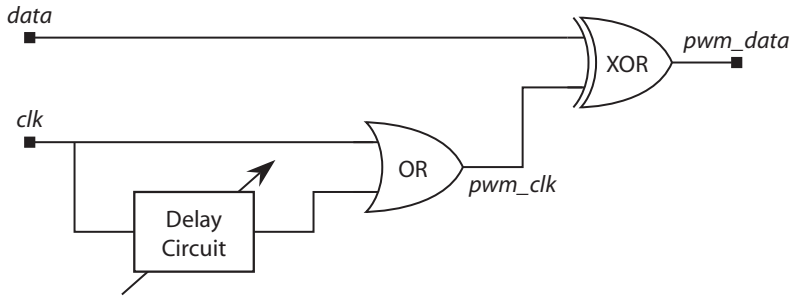
Furthermore, note that the Gray encoder facilitates operation in binary mode. If the LSB is set to logic 0, equations (4.1 – 4.3) reduces to $A = B = C = MSB$. Hence, the three outputs of the encoder switch in unison with the MSB input, thereby generating a full-swing binary output.

4.2.2 PWM-PE Topology

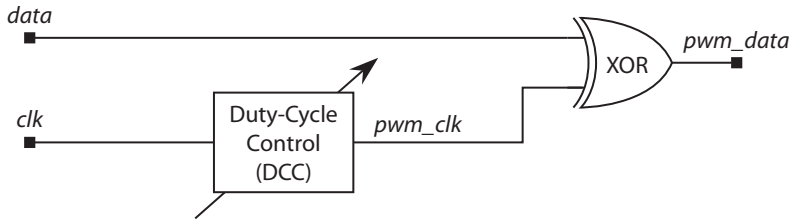
Implementation of PWM-PE requires a clock signal at the output symbol rate. Two architectures have been reported in literature [15] [20] to implement PWM-PE. Both architectures combine the data signal with a duty-cycle controlled clock using a XOR circuit. They differ only in the way the clock signal duty-cycle is controlled.

The first approach, shown in fig. 4.2(a) [15], uses a delay block and a logical-OR. The amount of delay determines the duty-cycle of the clock signal, and hence the amount of pre-emphasis in this implementation. The architecture reported in [15] requires two separate control voltages to adjust the duty-cycle. The second , shown in fig. 4.2(b), uses DC offset currents to control the clock's duty-cycle [20]. This approach is better suited to generating high pre-emphasis since zero offset current yields 50% duty-cycle at any clock frequency.

The ability to disable pre-emphasis for low-loss channels or testing purposes is also an important consideration. From the circuit block diagrams, since the clock input is ac-coupled, it is evident the first approach (fig. 4.2(a)) can only create a 100% duty-cycle (no pre-emphasis) if the delay is greater than half of the clock period. Using the second approach, however, pre-emphasis is disabled by disconnecting the clock input and applying a large offset current to the DCC. Based on the simpler circuit



(a) PWM-PE generation via clk delay



(b) PWM-PE generation via DCC

Figure 4.2: PWM-PE Topology

implementation and the ability to disable pre-emphasis reliably, the architecture with DCC is chosen. Its incorporation into the larger system architecture can be seen in fig. 4.1. The clock input undergoes duty-cycle modulation from DCC circuit, and its output is combined with the thermometer Gray-coded data streams at the XOR gates to create three PWM-PE data streams. These are inputs to the last stage of the transmitter, the output driver.

4.2.3 Output Driver

As shown in fig. 4.1, the binary thermometer Gray-coded data streams PWM-PE are combined at the output driver to create the PWM-PE 4PAM signal.

The conversion from three binary data streams to an output 4PAM signal is achieved by current summation. Three identical differential pairs, each taking one of the binary data streams as its input, are connected at their drain nodes. The result of this is a summation of the tail currents through their differential pair branches. Although the idea is simple, there are several implementation concerns which are addressed in more detail in section 4.3.5.

4.3 Circuit Blocks for 40Gb/s Transmitter

Fig. 4.3 illustrates the block diagram of the transmitter in more detail. Input buffers were inserted for broadband single-ended to differential conversion of data and clock inputs. The Thermometer Gray code encoder is implemented with logic gates as indicated in equations(4.1), (4.2), and (4.3). Three parallel CML differential pairs form the output driver as mentioned in section 4.2.3. Buffers are included between stages to provide sufficient drive strength; They have low fanout to provide sufficient bandwidth. In this section, implementation specifics of each of the components are presented. All simulations are performed on typical device models at 75^{o}C.

4.3.1 Cascades of Buffers

Cascades of CML buffers are required for two reasons in this design. Firstly, they are used to provide single-ended to differential conversion for the data and clock inputs. Secondly, they are used to buffer the outputs of complex logic blocks (DCC, Gray encoder, XOR) which have high self-loading and, hence, limited drive capability. The high-speed CML design process discussed in section 3.4 is used throughout the transmitter.

The buffers at various stages of the transmitter have different bandwidth requirements due to their different signal contents. All the following discussion assumes 40Gb/s transmission in 4PAM mode with PWM-PE. The data signal at the input to the XOR circuit has most of its signal content below the Nyquist rate, 10GHz. The clock signals, however, have signal content at 20GHz. The PWM-PE data streams

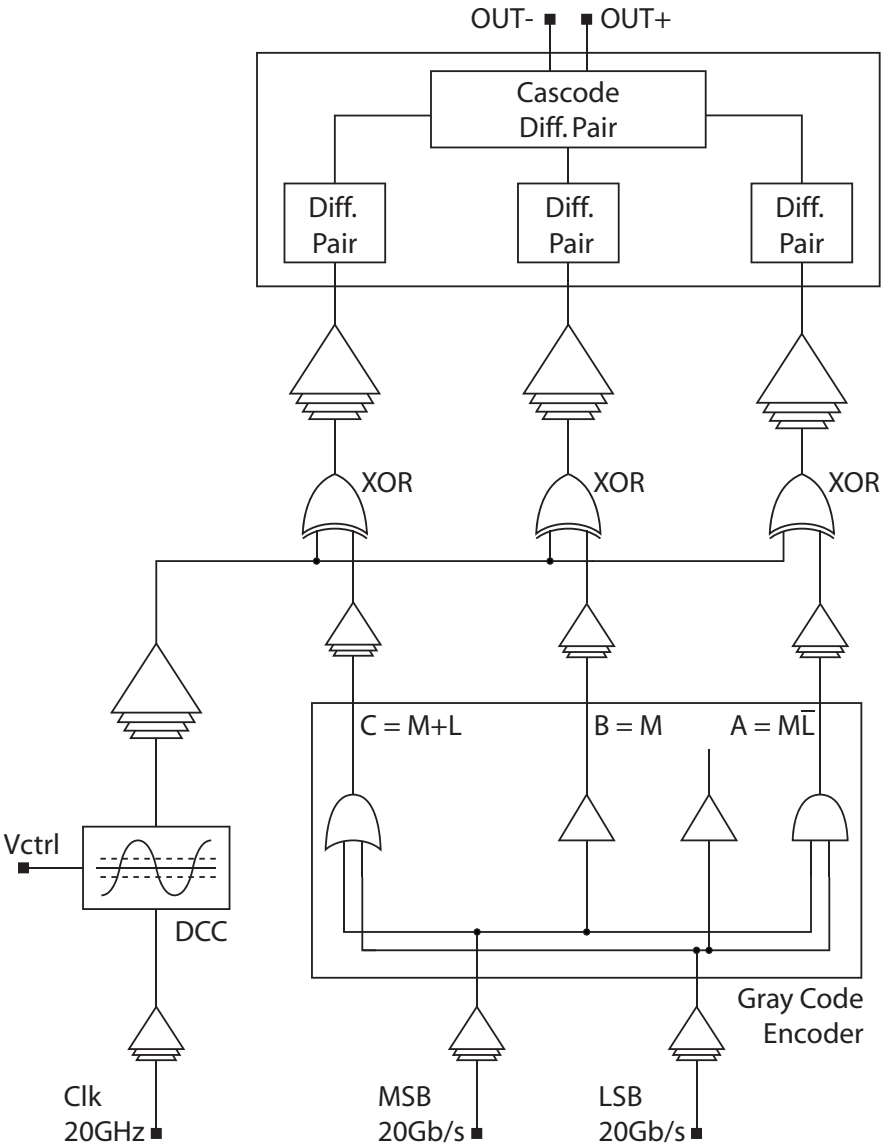


Figure 4.3: Block diagram of transmitter

after the XOR gates have frequency content inherited from the clock signal. Therefore the bandwidth requirement of such signals is also 20GHz.

The basic design parameters of CML buffers used in this transmitter are outlined in section 3.4. Shunt-peaking inductors are used to achieve bandwidth extension [30]. The design and modeling of inductors used in CML stages throughout the transmitter design is discussed with more detail in appendix B. Inductors with a value $L = \frac{CR^2}{3.1}$ can extend the 3-dB bandwidth of a circuit by 60% while maintaining a linear phase response up to its 3-dB bandwidth [30]. For broadband system this is the most commonly-used value. On the other hand, shunt-peaking inductors with a value $L = \frac{CR^2}{2.4}$ can extend the 3-dB bandwidth of a circuit by 72%. The additional bandwidth is gained at the cost of non-linear phase response. This value of inductive peaking is known as maximally flat response as it represent the maximum value of shunt-peaking where the gain response remains flat up to the 3-dB bandwidth.

Data signals M, L, A, B, and C have bandwidth requirements of 10GHz. Due to the broadband nature of the data signals, inductive peaking for linear phase response is used along the data signal paths. Fig. 4.4(a) illustrates the large-signal VTC mesh of the CML buffers with fanout of 1.5 from DC to 30GHz. A fanout of 1.5 is the maximum for which the value of $V*$ remains close to the target swing of 780mV up to 10GHz.

Clock signals require twice as much bandwidth, 20GHz. Maximally flat inductive peaking is used to in the clock path to provide extra bandwidth. Since it is a single-tone, the resulting non-linear phase response is not a problem. Furthermore, a lower fanout value of 1.2 is chosen. Fig. 4.4(b) illustrates its simulated large-signal VTC from DC to 30GHz.

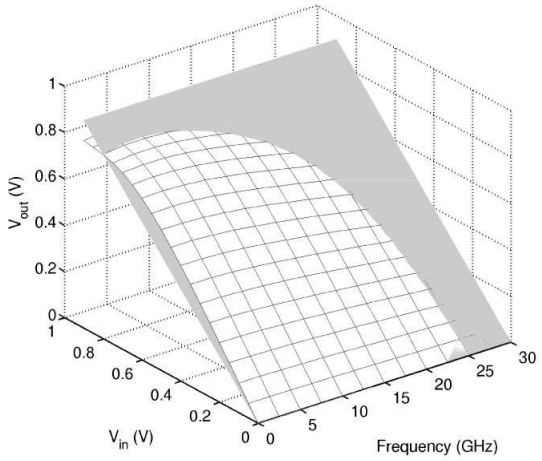
At the output of the XOR circuit, the data signals with pre-emphasis inherit the high frequency content of the clock signal. Therefore, a bandwidth of 20GHz is required to buffer these signals. However, with random data these signals are still broadband. These signals, therefore, present the most difficult challenge since they require both a high-bandwidth and broadband (linear phase) response. To achieve a 1.6Vpp swing through two parallel 75Ω loads requires a total tail current of 42.67mA in the output buffer, or 14.22mA in each of the three parallel differential pairs. For a current density of $0.3\frac{mA}{\mu m}$, it is determined that the output driver differential pair devices must have a width of $47.5\mu m$ each. The output of the high-gain stages immediately after the XOR circuit, which is discussed in more detail in section , only

has device width of $25\mu m$. This overall ratio of $\frac{47.5\mu m}{25\mu m} = 1.9$ has to be bridged by a cascade of CML buffers. If a fanout of 1.1 is used, it would require seven buffers to achieve sufficient logic drive strength. However, only 4 stages are required if the fanout value is increased to 1.2. Due to practical considerations such as power consumption and area, it is determined that a fanout value of approximately 1.2 with linear phase inductive peaking yields adequate performance for the cascade of CML buffers. Fig. 4.4(c) illustrates its large-signal VTC from DC to 30GHz. In the actual design, fanout values from 1.13 to 1.2 are used in this cascade. Simulation result confirms that sufficient swing is preserved for the differential pairs of the output drivers.

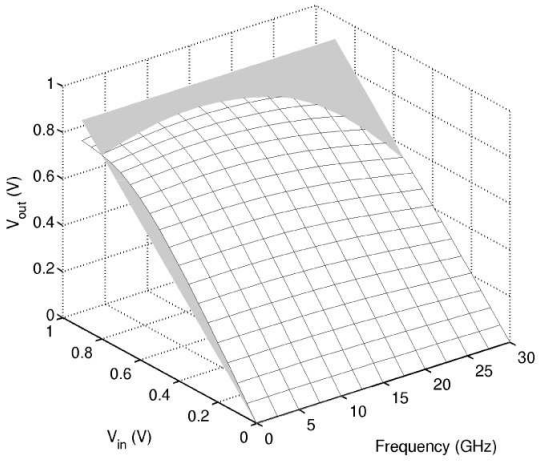
4.3.2 Duty Cycle Control (DCC)

Fig. 4.5 is the schematic of DCC CML gate. The differential inputs, $V_{offset+}$ and $V_{offset-}$, are derived from a single control voltage by a single-ended to differential conversion circuit (fig. 4.6(a)). These inputs introduce a DC offset current which adjusts the duty-cycle of the differential clock applied at $IN+$ and $IN-$. The switching differential pair has a tail current of 15mA while the offset differential pair has a tail current of 12mA. The target duty-cycle tuning range is between 50% and 75%. When the offset pair is balanced, the balanced DC offset current introduces no distortion to the switching signal. A positive differential input in the offset pair introduces offset current in the load resistance such that the zero-crossing in changed to increase the positive duty cycle of the clock waveform. Due to the presence of static current introduced by the offset differential pair, the extra voltage drop at the load resistors reduces the voltage headroom available to the transistors. This issue is addressed by reducing the bias current density to $0.20\frac{mA}{\mu m}$, and reducing the output voltage swing from 800mV to 600mV. The DC bias voltages of the DCC stage in its balanced state are shown in fig. 4.5.

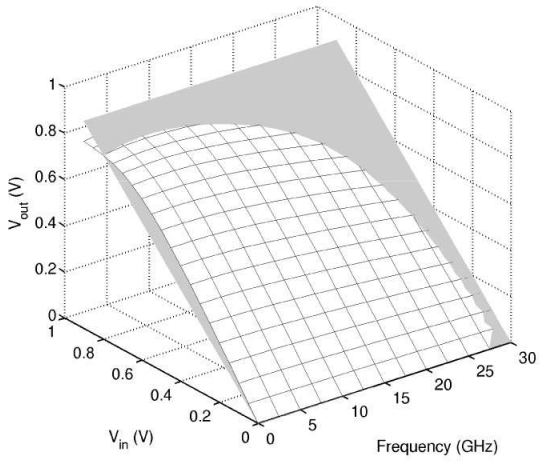
The generation of the inputs $V_{offset+}$ and $V_{offset-}$ from a single off-chip control signal, V_{ctrl} is performed by the circuit shown in fig. 4.6(a). The input common-mode voltage of $V_{offset+}$ and $V_{offset-}$ is of high importance as it affects the bias of the overall DCC circuit. A value of 1.4V was chosen to match the common-mode voltage of the input clock signal. In order to ensure this common-mode voltage, the last stage of the offset circuit consists of two differential pairs where one is in fully-switched state (M11 & M12) and the other in balanced state (M13 & M14). The tail current of each differential pair is mirrored from a PMOS differential pair (M5 & M6)



(a) Data path - fanout = 1.5, linear phase inductive peaking



(b) Clock path - fanout = 1.2, maximally flat inductive peaking



(c) Data with PWM-PE - fanout = 1.2, linear phase inductive peaking

Figure 4.4: VTC mesh of different fanout and peaking

with diode connected NMOS load acting as current mirrors (M7-M9 & M8-M10). The inputs to the PMOS differential pair (M5 & M6) is derived from off-chip control voltage and an internally-biased voltage via PMOS CML stage with transistors M2 and M3. Fig. 4.6(b) illustrates the tuning curve of $V_{offset+}$ and $V_{offset-}$ to V_{ctrl}. The output common-mode voltage is maintained around 1.4V for the entire tuning range. The differential control, $V_{offset} = V_{offset+} - V_{offset-}$, can be tuned from 0V to 880mV as shown in fig. 4.6(c). This range is selected to cover all from a balanced state to fully-switched state in pair M3 & M4 of the DCC circuit (fig. 4.5).

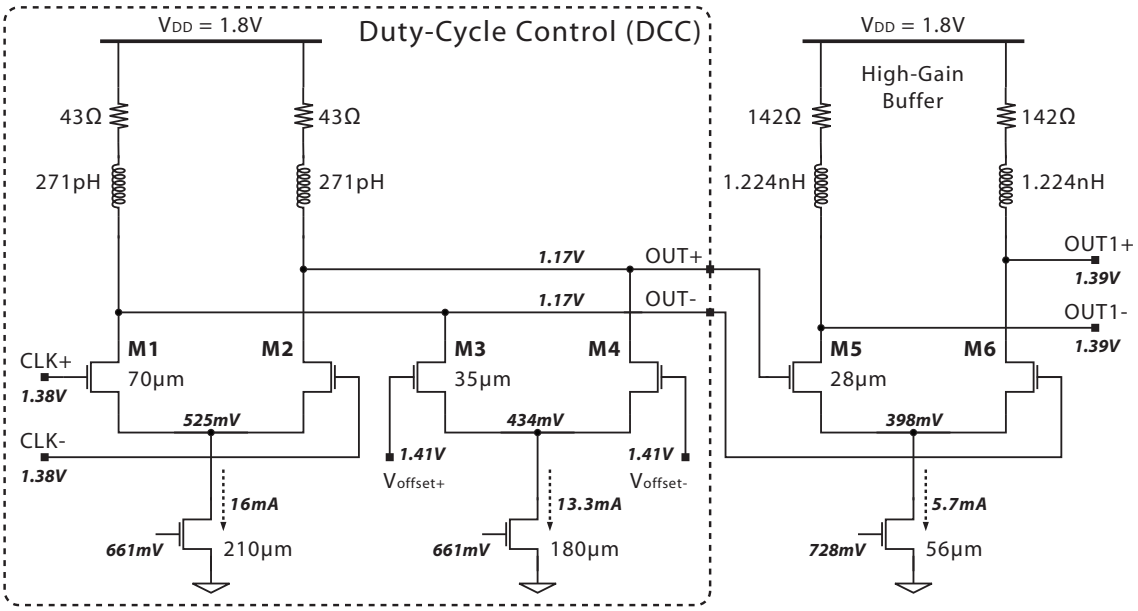
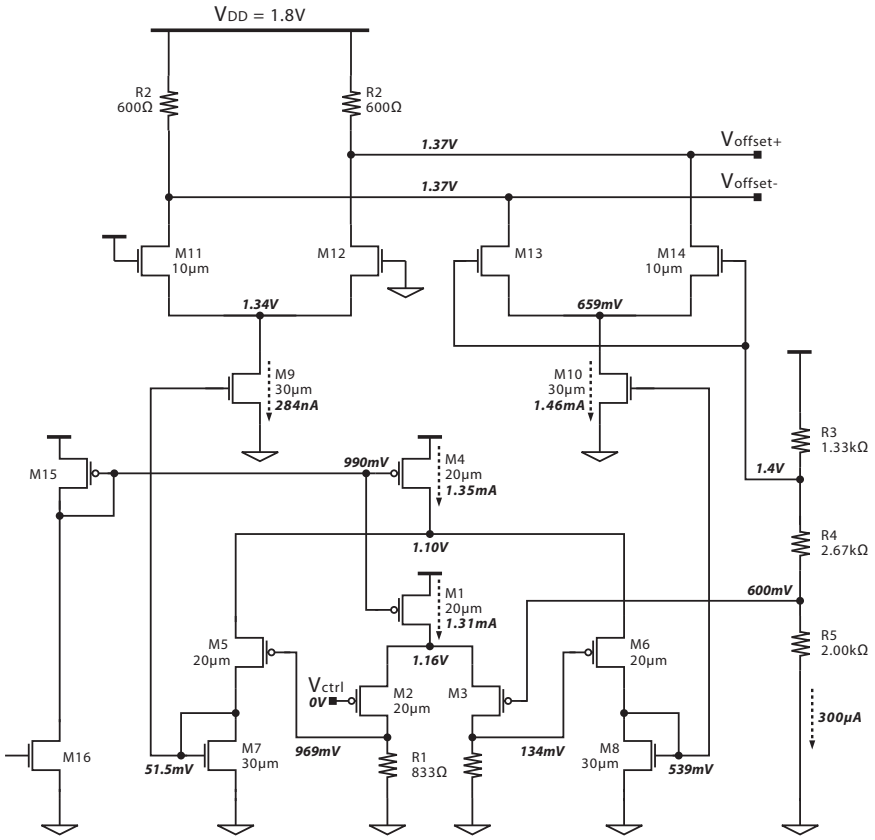
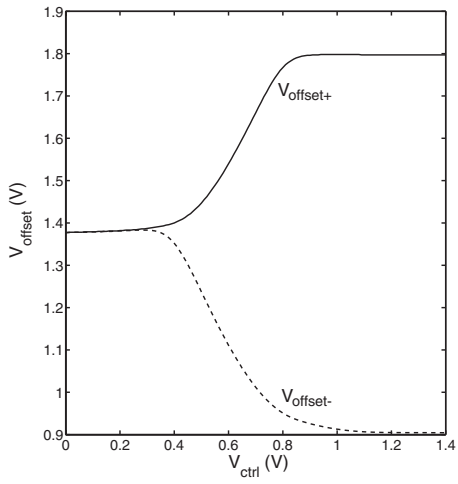


Figure 4.5: Schematic of DCC stage

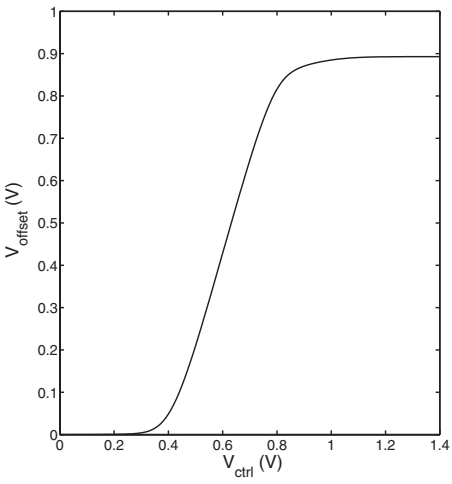
The output of the DCC stage also has a lower common-mode voltage than the other CML stages. In addition, for high duty-cycle settings the negative cycle of the clock is very narrow and hence has small amplitude. For example, the output swing during the negative cycle is approximately only 320mV at the highest duty-cycle setting. This small amplitude is insufficient to switch subsequent CML circuit. In order to increase the amplitude of the negative duty-cycle and to shift the common-mode voltage back to its desired value of 1.4V, a cascade of five CML stages with high gain is placed at the output of the DCC stage. A block diagram is shown in fig. 4.7. The five high-gain CML stages are identical. The schematic is shown in fig. 4.5. The high-gain stages are biased at $J = 0.20\frac{mA}{\mu m}$ to lower the switching voltage requirement from 780mV to 590mV, which helps to restore the amplitude in the negative duty-cycle



(a) DCC offset control circuit schematic



(b) Tuning curve: Single-ended outputs $V_{offset+}$ & $V_{offset-}$



(c) Tuning curve: Differential output $V_{offset} = V_{offset+} - V_{offset-}$

Figure 4.6: DCC offset control circuit

back to full-swing level. The reduced current density also increases their small-signal transconductance. In addition, the low fanout of one is used to provide high gain up to 20GHz. Fig. 4.8 illustrates the simulated waveforms within the DCC circuits in fig. 4.7.

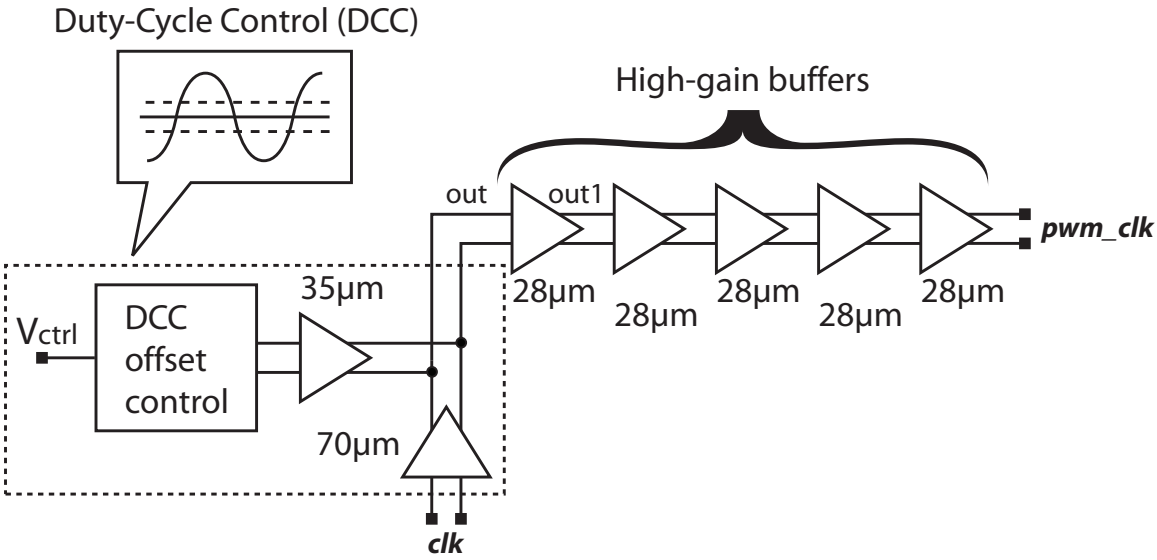
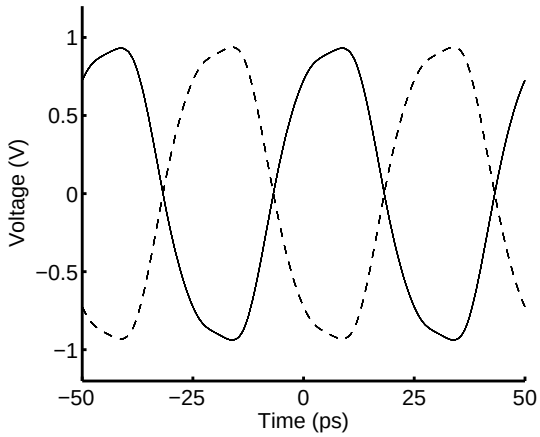
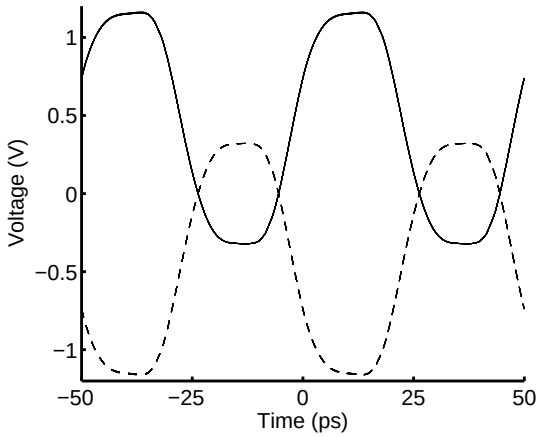


Figure 4.7: block diagram of DCC stage with high-gain buffers with the width of differential pair devices labeled for each stage

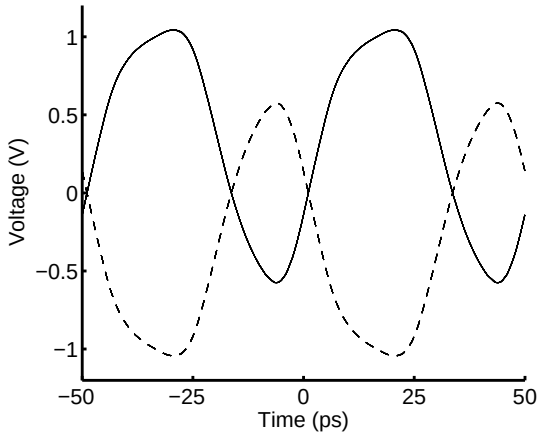
In addition to the ability to adjust the duty-cycle of the clock signal, the DCC circuit is also capable of turning off pre-emphasis in the transmitted data. Mild pre-emphasis requires duty-cycle of 80-99%. But this would require very narrow pulses that cannot be accomdated by the DCC circuit. Hence, in channels with low loss characteristics, even the minimum amount of pre-emphasis generated by the PWM-PE would be excessive and thus detrimental to the overall link. In such cases, transmission of NRZ signals format without pre-emphasis is advantageous. By disconnecting the clock input into the transmitter and applying a large DC voltage to the DCC offset control circuit, the offset differential pair in fig. 4.5 is capable generating a sufficient DC voltage to fully-switch the subsequent high-gain buffers. Hence, the *pwm_clk* signal at the inputs of the XOR gates would be at a constant logic level and would not alter the content of the input data signal, thereby providing NRZ signals to the output stage.



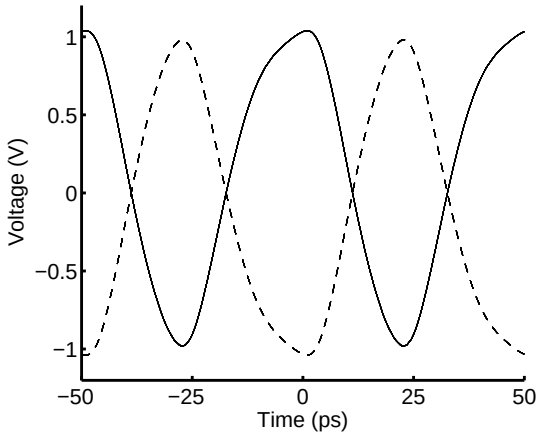
(a) Clk input to DCC



(b) Output of DCC



(c) Output of first gain stage

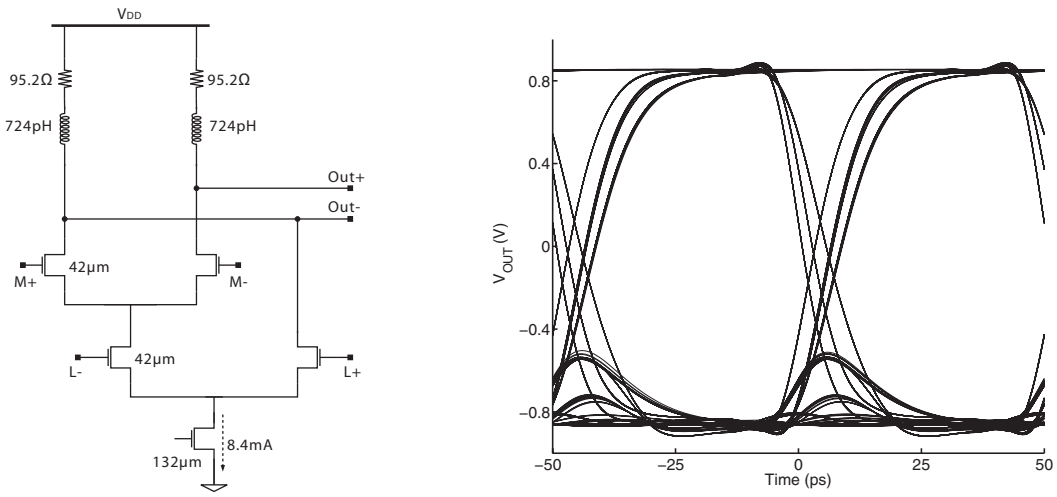


(d) Output of final gain stage

Figure 4.8: DCC and high-gain buffer waveforms; dotted line is inverted clock signal for eye diagram representation

4.3.3 Thermometer Gray Code Encoder

Current mode combinational logic gates were designed to implement the Gray encoding logic expressions shown in (4.1), (4.2), and (4.3). A simple CML topology that implements the logical AND in (4.1) is shown in fig. 4.9(a) [28]. Unlike standard CML XOR and MUX gates, circuit in fig. 4.9(a) is asymmetrical in that it presents different capacitive loads at the two differential outputs. The circuit shown in fig. 4.10(a) removes the problem by adding another differential pair on top of the $L+$ input. The simulated eye diagrams at the outputs of the two circuits are shown in fig. 4.9(b) and fig. 4.10(b) with perfectly synchronized random inputs. The input signals to the lower differential pair have a lower common mode voltage of 1V compared to 1.4V for the upper differential pair to improve the performance of the logic gate. Nevertheless, a large amount of systematic jitter, about 6-8ps, is present at the

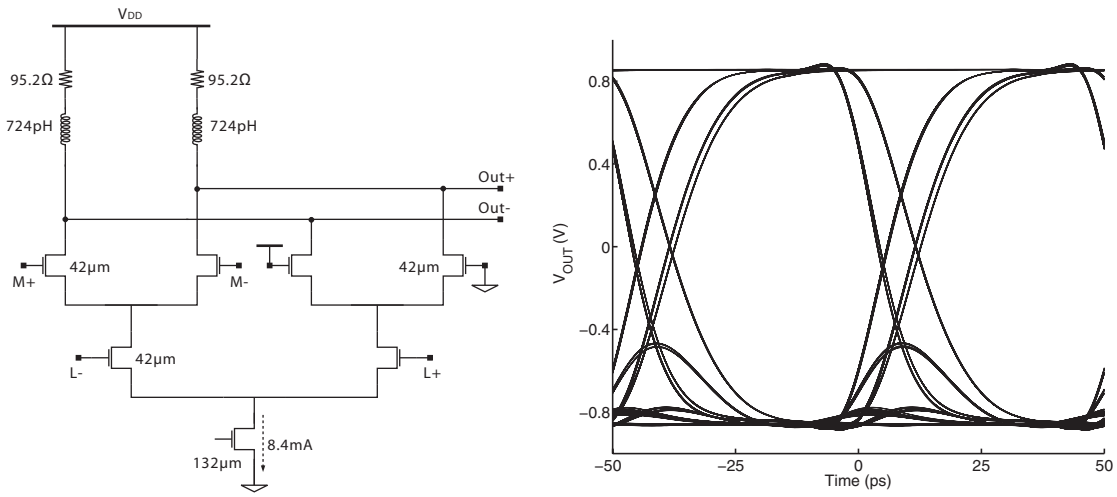


(a) Circuit schematic

(b) Simulated output eye diagram; 5.5ps jitter

Figure 4.9: Basic design for $A = M \cdot \bar{L}$

output waveform. The systematic jitter is mainly the result of a longer delay from the upper switching differential pair and the upper non-switching DC biased pair of the logic topology. Simulation has shown that the transition of the bottom differential pair is responsible for the later zero crossing in the eyediagrams such as one shown in fig. 4.10(b). The systematic delay can be reduced by delaying the inputs to the



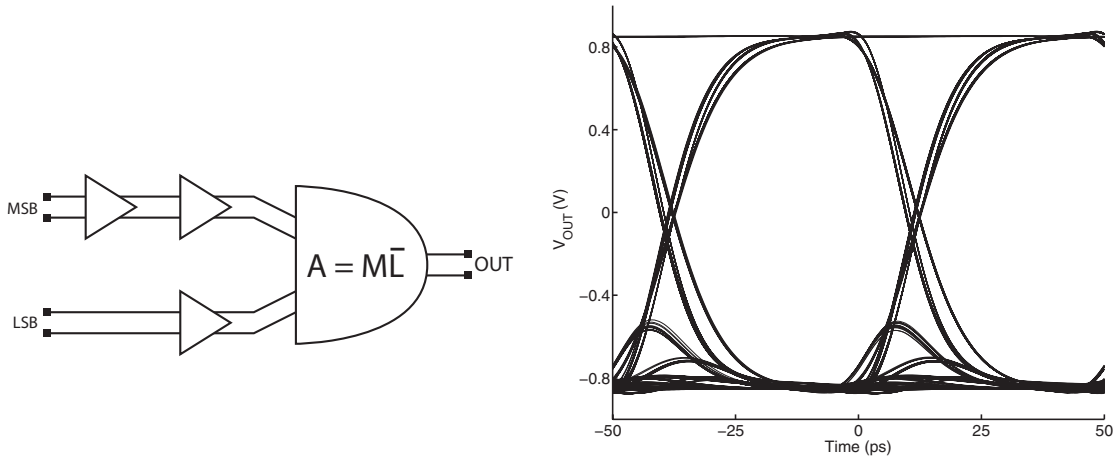
(a) Circuit schematic

(b) Simulated output eye diagram; 8ps jitter

Figure 4.10: Design with symmetrical capacitive load for $A = M \cdot \bar{L}$

top differential pair by 3 to 4 ps. Fortunately, the intrinsic gate delay of a CML buffer is in the range of 3 to 4 ps, and can therefore be used to provide the required delay, as shown in fig. 4.11(a). As shown in fig. 4.11(b), the systemic jitter from the encoder logic is significantly reduced compared to previous designsfrom 6-8 ps down to approximately 2 ps.

A drawback of the design in fig. 4.11(a) is that the reduced number of buffers in the LSB data path necessitate a higher fanout from the previous-stage buffer. To overcome this problem would require the design of a new series of buffers specifically for the LSB path, which significantly complicates circuit implementation. A new topology with identical MSB and LSB data path is achieved by dividing the circuit in fig. 4.10(a) into two identical parts and mirroring the top and bottom differential pairs inputs. The schematic of this design is shown in fig. 4.12(c). Note that the early version of LSB is used in the bottom differential pair with MSB on the top differential pair on the left half of the circuit, and the reverse for the right half of the circuit. The block diagram is shown in fig. 4.12(a). By taking the output of the CML buffers prior to the final buffers to the encoder logic gates and routing the early signals to the lower differential pairs, the necessary time difference can be achieved. The more symmetrical implementation of logical AND has an additional benefit that any small



(a) Block diagram

(b) Simulated output eye diagram; 2ps jitter

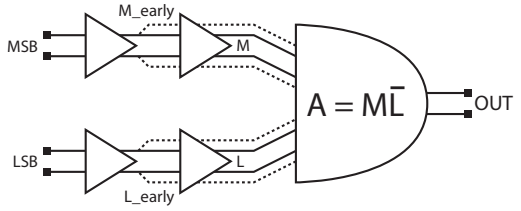
Figure 4.11: Design with early LSB input for $A = M \cdot \bar{L}$

relative delays between MSB and LSB streams would have less impact on the overall systematic jitter on the logic encoder output compared to design without the mirrored topology. Fig. 4.12(b) illustrates the simulated eye diagram of the output waveform using the mirrored logic topology.

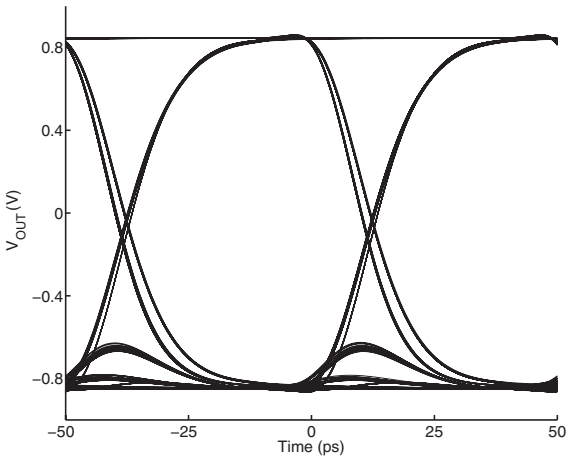
The logic expression shown in (4.1) is implemented by circuit shown in fig. 4.12(c), while expressions (4.2) and (4.3) are implemented by the circuits shown in fig. 4.13. All three logical expressions uses the same topology and device sizes to match their delays. The transistors in the encoder logic gates are biased at $J = 0.3\frac{mA}{\mu m}$ with the sum of the two tail currents totalling 8.4mA. The inputs to the top differential pairs have a swing of 800mV with a common-mode voltage of 1.4V while the inputs to bottom differential pairs have a reduced common-mode voltage of 1V. The output swing of the encoder logic is 800mV. Schematic with annotated bias voltages and currents of logic encoder for expression $B = M$ is shown in fig. 4.13(a).

4.3.4 XOR

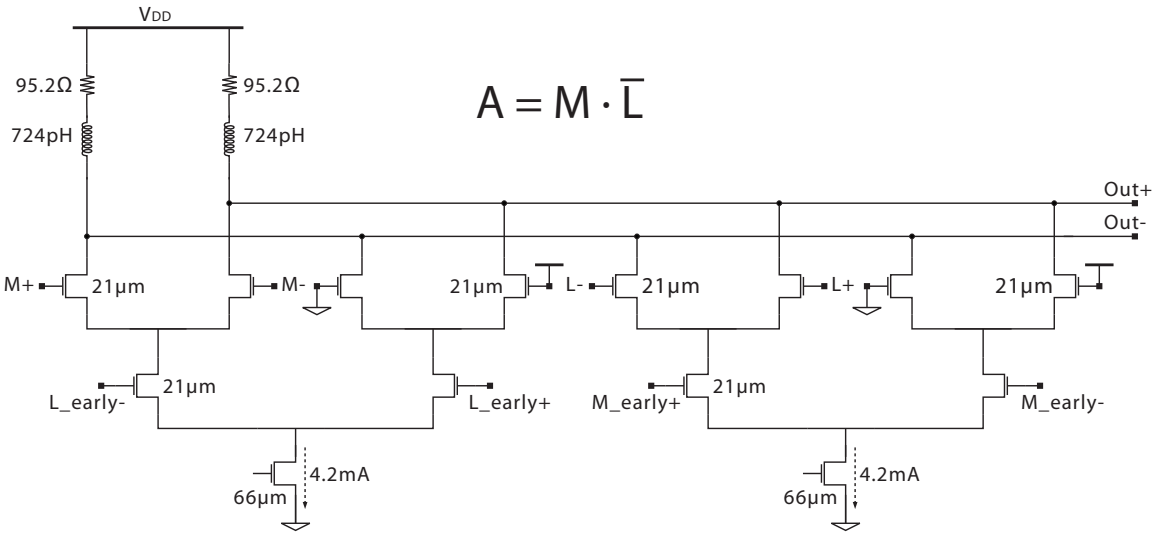
The design of the XOR gate is challenging since it generates a PWM-PE signal with increased high-frequency content. Fig. 4.14 is the schematic of XOR CML gate,



(a) Block diagram

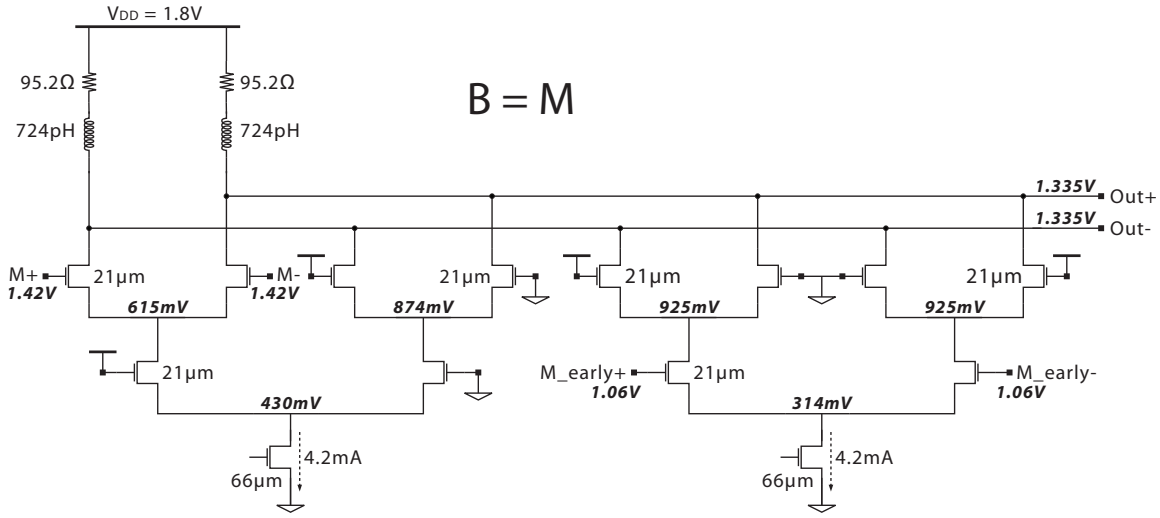


(b) Simulated output eye diagram

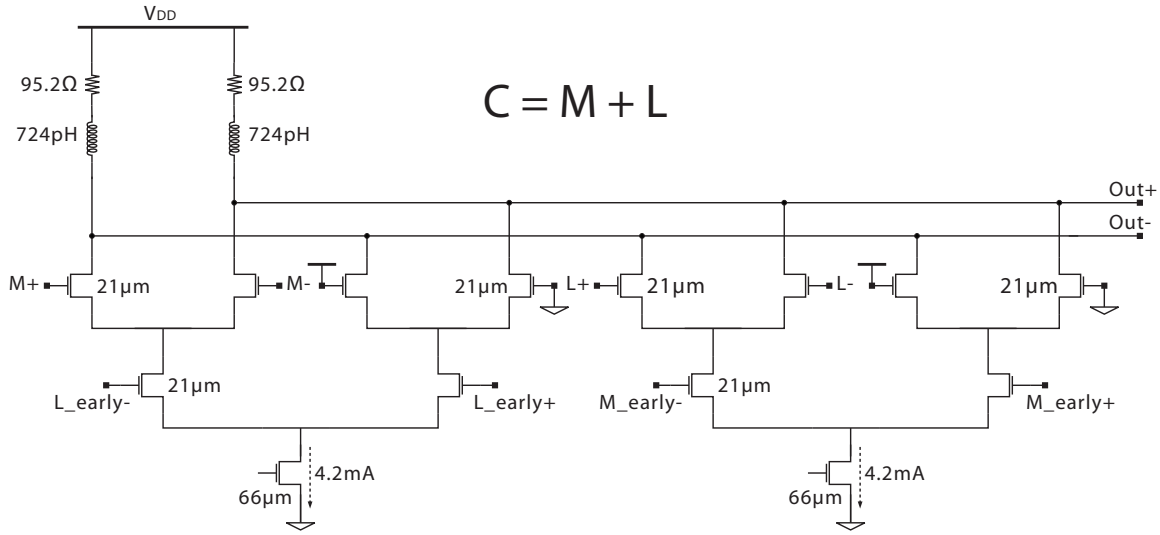


(c) Circuit schematic

Figure 4.12: Design with mirrored topology and early LSB input for $A = M \cdot \bar{L}$



(a) Gray Encoder - B; with bias current and voltages



(b) Gray Encoder - C

Figure 4.13: Schematic of Gray Encoder B & C

with annotated bias voltages and currents. To accomodate the extra differential pair within the same supply voltage of 1.8V, the current density of the differential pairs are reduced from $0.30\frac{mA}{\mu m}$ used in CML buffers to $0.20\frac{mA}{\mu m}$. The reduced current density lowers the gate over-drive voltage, V_{eff}, thus providing more voltage headroom for the stacked differential pairs. The reduced current density also reduces the voltage swing required to fully-switch the CML differential pairs. The inputs of differential pairs have a swing of 780mV, which is well above the 600mV required swing under the reduced current density. This has the added benefit of ensuring full-switching of the XOR gate differential pairs. The output swing is reduced from 800mV to 600mV to increase voltage headroom and reduce load resistance. The lower load resistance reduces the *RC* time constant at the critical output node of the XOR gate. Along with inductive peaking and a low fanout to the subsequent CML buffer stage, sufficient bandwidth for the PWM-PE signal is maintained.

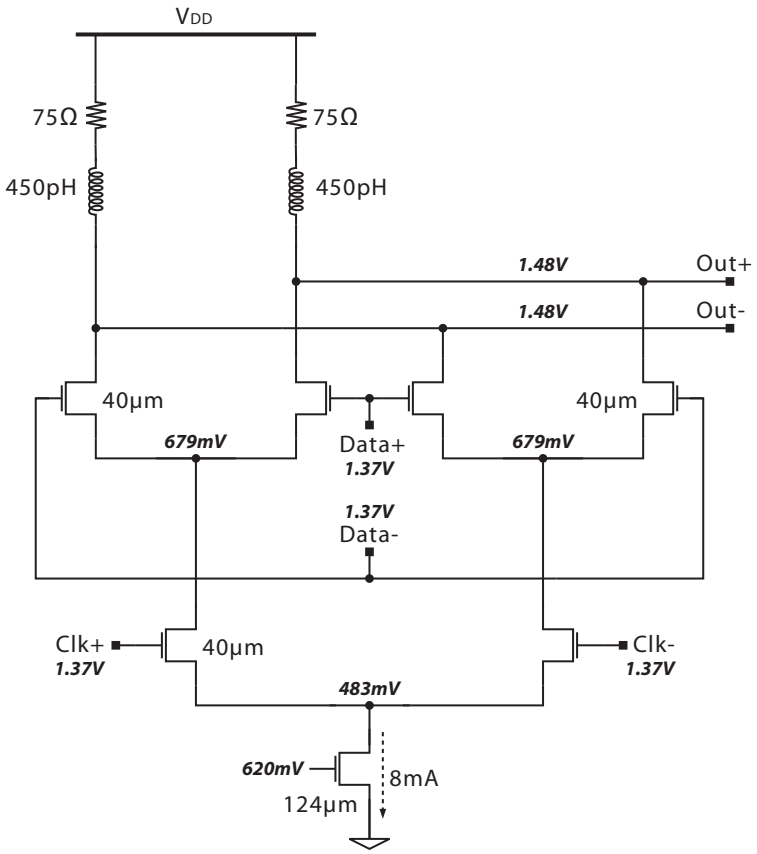


Figure 4.14: Schematic of XOR stage

Similar to the design of DCC stage, high-gain low-fanout buffers were used at the

output of XOR CML circuit as shown in fig. 4.15. They restore the output waveform to a full voltage swing of 800mV. Simulated transient waveforms of the XOR stage with high-gain buffers are shown in fig. 4.16. Note the undesirable deep notches in the *xor_out* waveform restored to their full-swing values at the output of the high-gain stages.

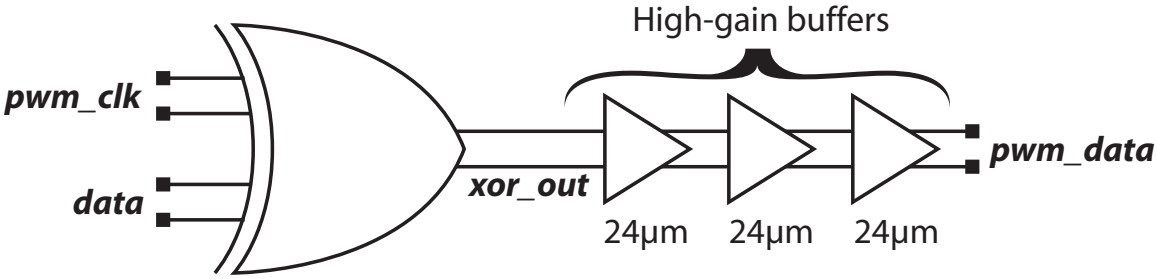


Figure 4.15: Block diagram of XOR stage with high-gain buffers

4.3.5 Output Driver

The last circuit component in the overall design is the output driver. The primary functions of the output driver are to provide a large output swing and to combine the three PWM-PE data streams to form the 4PAM output waveform with PWM-PE.

The 75Ω output matching requirement dictates the load resistance of the output driver. The high output swing of 1.6Vpp per side necessitates a separate power supply for the output stage and a total tail current of 42.67mA. Drawing all of the tail current through the load resistance would incur 1.6V of DC voltage drop across its load resistances when the circuit is in a balanced state. Such significant drop would necessitate an unreasonably high supply voltage. Hence, an additional path for DC currrent must be provided from the supply. This could be provided by the receiver in a DC-coupled link. In our measurement setup, the additional DC current is provided by bias-tees off-chip. A supply voltage of 3V is used. The schematic of the output driver, along with external bias-tees and associated DC resistance, is shown in fig. 4.17. A cascode topology is chosen for the output stage to provide wide swing [34] [35]. The cascode devices shield the input differential pair from excessive drain-source voltages and reduce the input Miller capacitance. The performance of the output driver is very sensitive to the value of the gate bias on the cascode devices, $V_{cascode}$. It is important to bias the cascode devices so that their drain-source voltage, V_{ds}, never exceeds the breakdown limit of 1.6V during operation. $V_{cascode}$ is an input

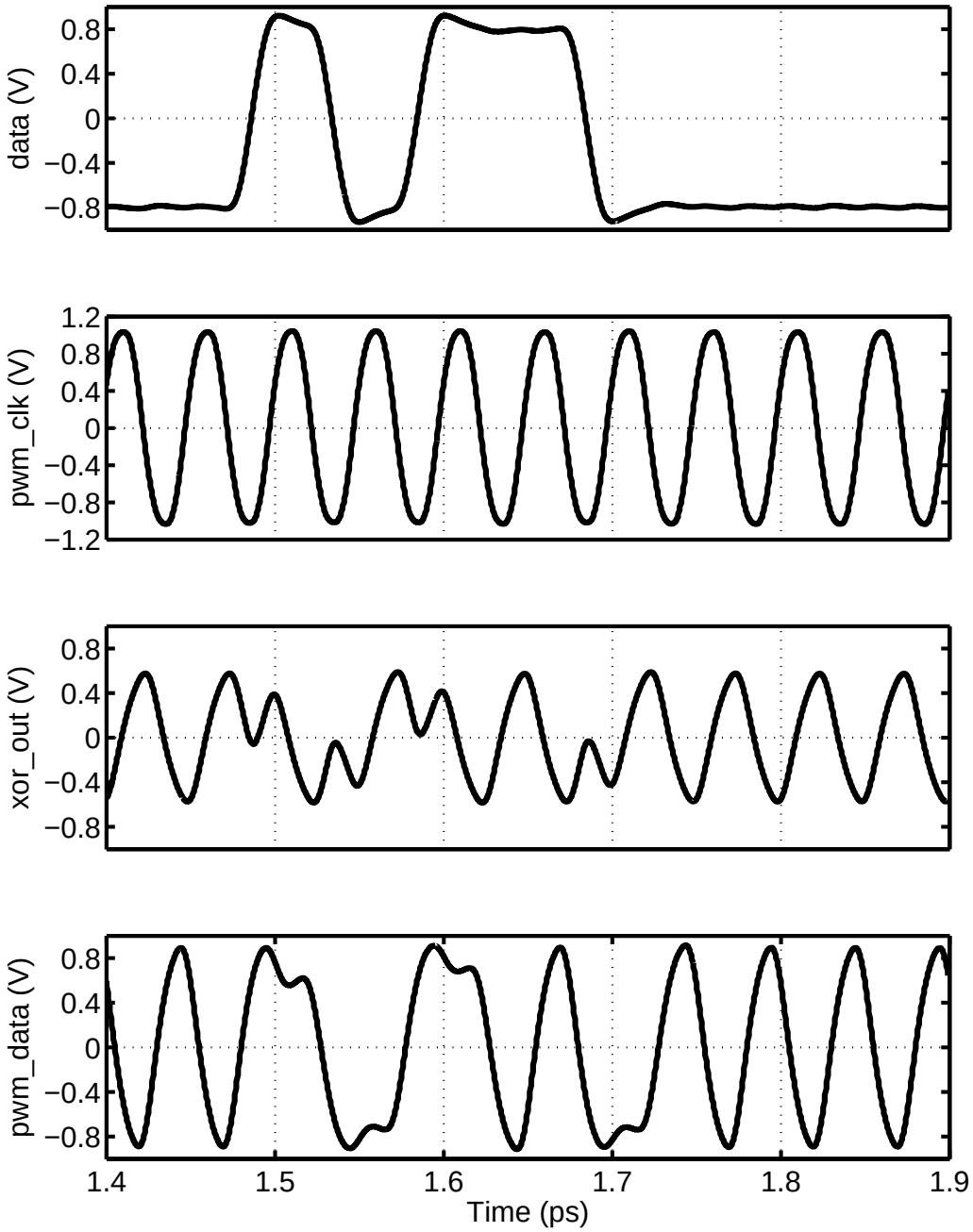


Figure 4.16: Simulated transient waveforms for XOR stage with high-gain buffers

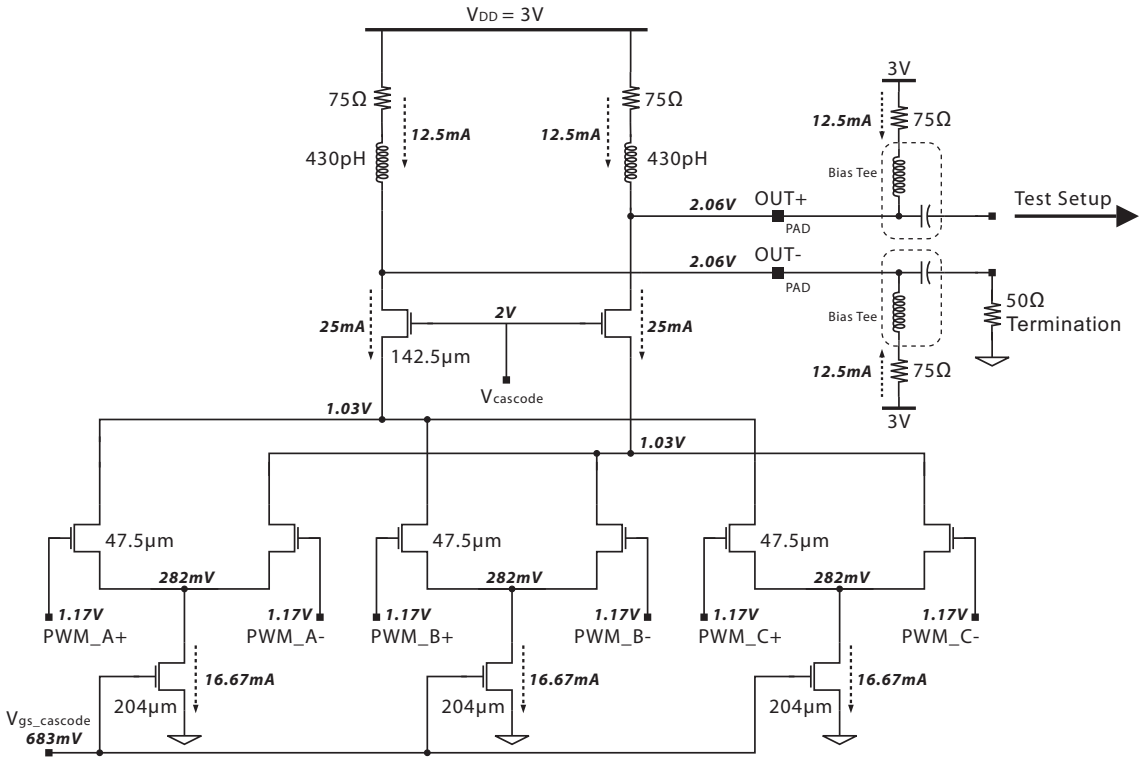
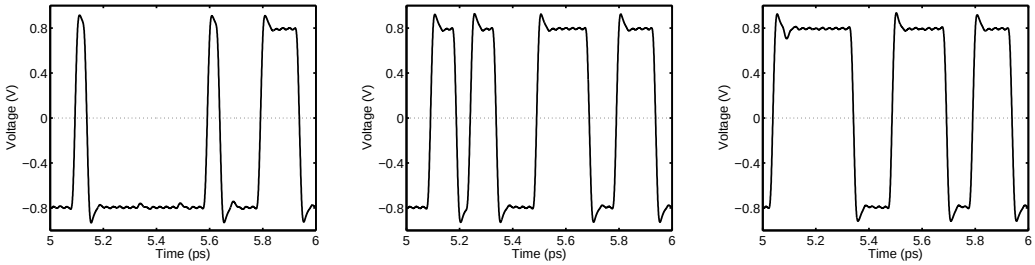


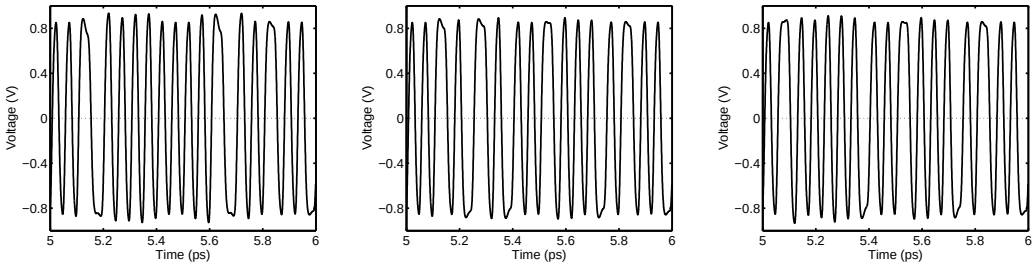
Figure 4.17: Schematic of Cascode stage

reference voltage taken from off-chip with a nominal value of 2V. The high output swing can be reduced for low-loss channels by reducing the the total tail current of the output driver by changing the gate bias voltage to the tail-current devices, provided as an external input to the chip.

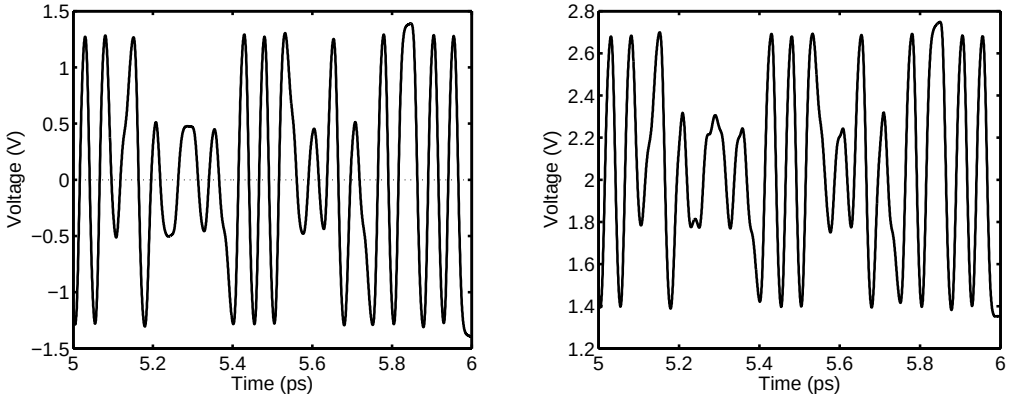
Simulated transient waveforms of the output driver are provided in fig. 4.18. The input data-streams in NRZ format are shown in fig. 4.18(a), 4.18(b), and 4.18(c). Their associated waveforms with PWM-PE are shown in fig. 4.18(d), 4.18(e), and 4.18(f) respectively. The differential and single-ended output waveforms are shown in fig. 4.18(g) and fig. 4.18(h) respectively. The simulation testbench used to generate the waveforms is as shown in fig. 4.17; a bias-tee is included and 50Ω loads are provided to mimic the 50Ω testing environment. The output driver is designed to provide 1.6Vpp per side in a 75Ω environment. Simulations in the 50Ω environment show the expected reduction in output swing to a maximum of 1.28Vpp per side.



(a) NRZ data - A (b) NRZ data - B (c) NRZ data - C



(d) PWM-PE data - A (e) PWM-PE data - B (f) PWM-PE data - C



(g) 4PAM output waveform, $OUT = OUT_+ - OUT_-$ (h) 4PAM output waveform, , OUT_+

Figure 4.18: Output driver waveforms

4.4 Integration

All the components mentioned in section 4.3 must be put together in the correct fashion for the transmitter to perform properly. The capacitive loading of CML stages throughout the circuit is an important consideration that has major impact on the overall integration. The transmitter can be divided into three major components: clock distribution, data distribution, and PWM-PE generation & output stage.

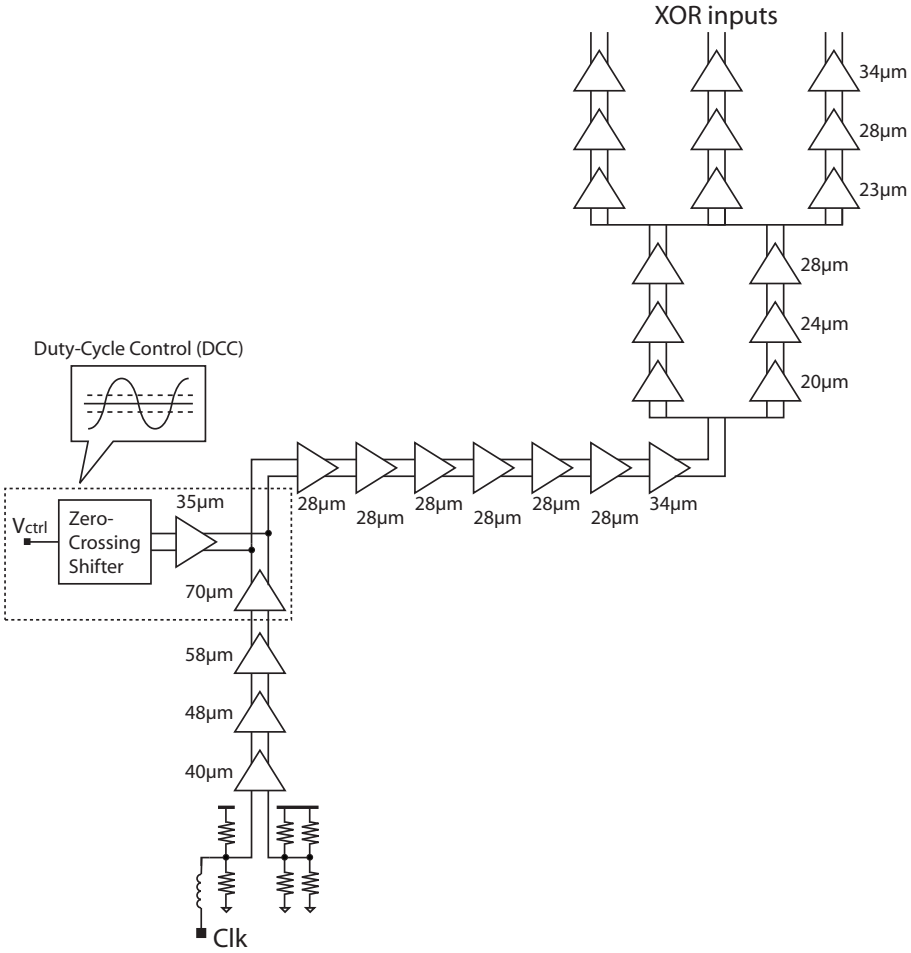
4.4.1 Clock Distribution

The clock distribution network consists of circuits from the clock input to the XOR gates. The major function of the clock distribution network is to ensure the clock signal with duty-cycle adjustment is properly routed to the input of the XOR gates, where they can be used to generate the data streams with PWM-PE. Fig. 4.19(a) illustrates the clock distribution network in block diagram format, with annotation for the differential pair device width of each CML circuit.

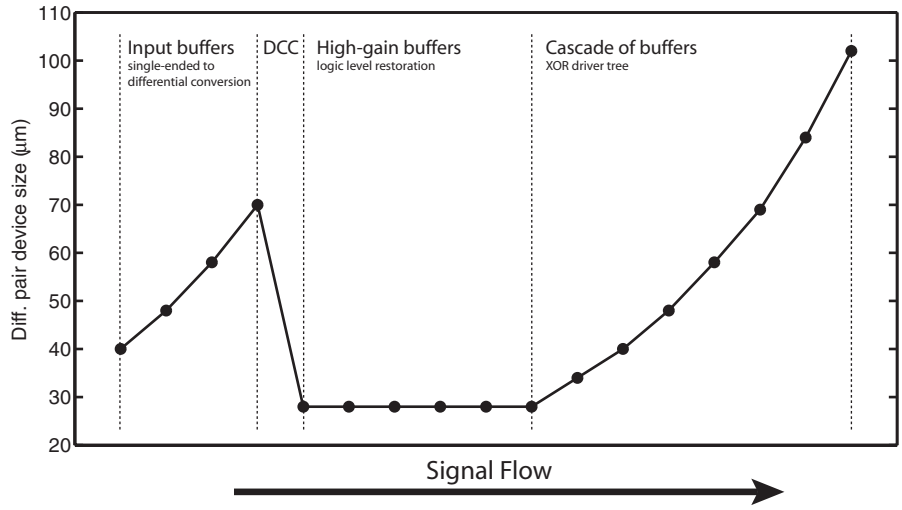
As the clock input is single-ended and has its DC component removed, three CML buffers are provided at the input to perform singled-ended to differential conversion. They also ensure the input swing requirement of 600mV of the DCC stage is met. The input buffer is biased by a passive network of resistors to provide input common-mode bias voltage of 1.4V. One side of the CML buffer input is connected to a pad while the other is internally terminated to a 50Ω resistance. The DCC stage along with the following high-gain buffers are discussed in section 4.3.2. The rest of the CML buffers are required to drive the three separate XOR gates. From simulations, it is determined that having separate CML buffers drive each of the three XOR circuits improves the overall signal quality over that of a single, common CML buffer. The increased isolation between the XOR inputs ensure transitions in the adjacent data paths do not couple through the XOR gate and affect the respective clock input. As discussed in section 4.3.1, the CML buffers used for clock distribution network have a fanout value of 1.2 along with peaking inductors of $L = \frac{CR^2}{2.4}$. The device widths of CML differential pairs along the clock signal path are plotted in fig. 4.19(b).

4.4.2 Data Distribution

The data distribution network consists of the circuits from the data inputs to the XOR gates. The chief function of the data distribution network is route the MSB



(a) Block diagram of clock distribution network



(b) Differential pair device widths along clock distribution network

Figure 4.19: Clock distribution network

and LSB inputs to the therometer Gray-code encoder, and subsequently to the input of the XOR CML circuits. Fig. 4.20 illustrates the data distribution network in block diagram format, with annotation for the differential pair device width of each of the CML circuits. Similar to the clock distribution network discussed in section 4.4.1,

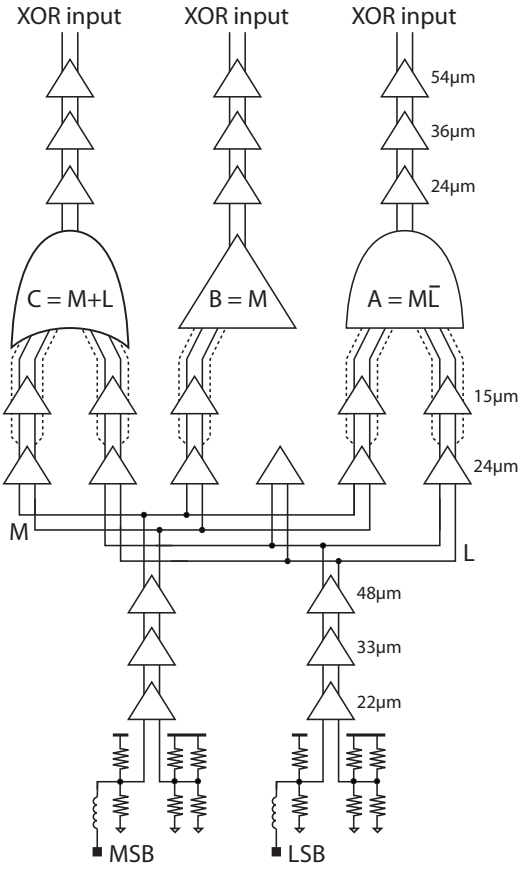


Figure 4.20: Data distribution circuits

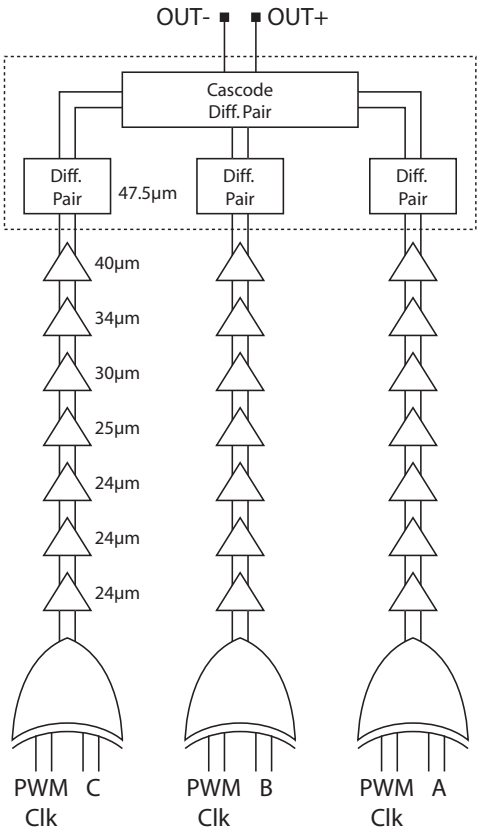
input buffers with passive biasing network are placed in the front section of the data distribution network to ensure the correct M and L signals are present at the input of the thermometer Gray-code encoder. The design of the thermometer Gray-code encoder is discussed in section 4.3.3. The generation and routing of the early version of M and L signals for the mirrored logic topology can be seen in fig. 4.20. Due to the mapping of the input signals to the thermometer Gray-code, signal L is not present in expression (4.2). In order to ensure the same loading on the M and L signal paths, an extra unused CML buffer is added. As discussed in section 4.3.1, the CML buffers used in the data distribution network have fanout of 1.5 and peaking inductors of $L = \frac{CR^2}{3.1}$.

4.4.3 PWM-PE generation & Output Driver

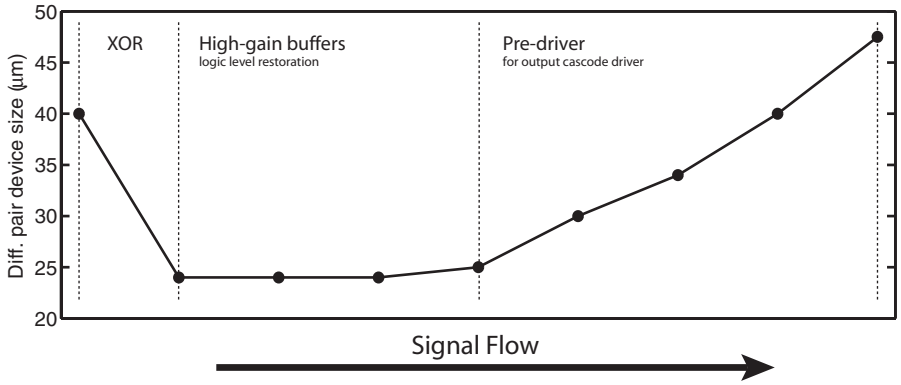
The final major component of the transmitter is the stage where the 4PAM output waveform with PWM-PE is generated. The outputs from the clock distribution and data distribution networks serve as inputs to this final section. The block diagram representation of circuits present in this section along with their differential pair device widths is shown in fig. 4.21(a). As discussed in section 4.3.4, XOR gates followed by high-gain buffers are used to combine the data signals and clock signal with variable duty-cycle to create three parallel, thermometer Gray-encoded data signals with PWM-PE. The final stage of this section is the output driver. The use of differential pairs as to perform the 4PAM signal summation from the three branches along with the various design considerations are discussed in detail in section 4.3.5. As discussed in section 4.3.1, the CML buffers used in the data distribution network have fanout of 1.2 along with peaking inductors of $L = \frac{CR^2}{3.1}$. The device widths of CML differential pairs from the XOR CML gates to the output driver are plotted in fig. 4.19(b).

4.4.4 Top-level Schematic

Fig. 4.22 illustrates the overall arrangement of circuit blocks in the clock distribution network, data distribution network, and the PWM-PE generation & output driver.



(a) Block diagram of PWM-PE and 4PAM generation circuits



(b) Differential pair device widths from XOR to output driver

Figure 4.21: PWM-PE generation & Output Driver

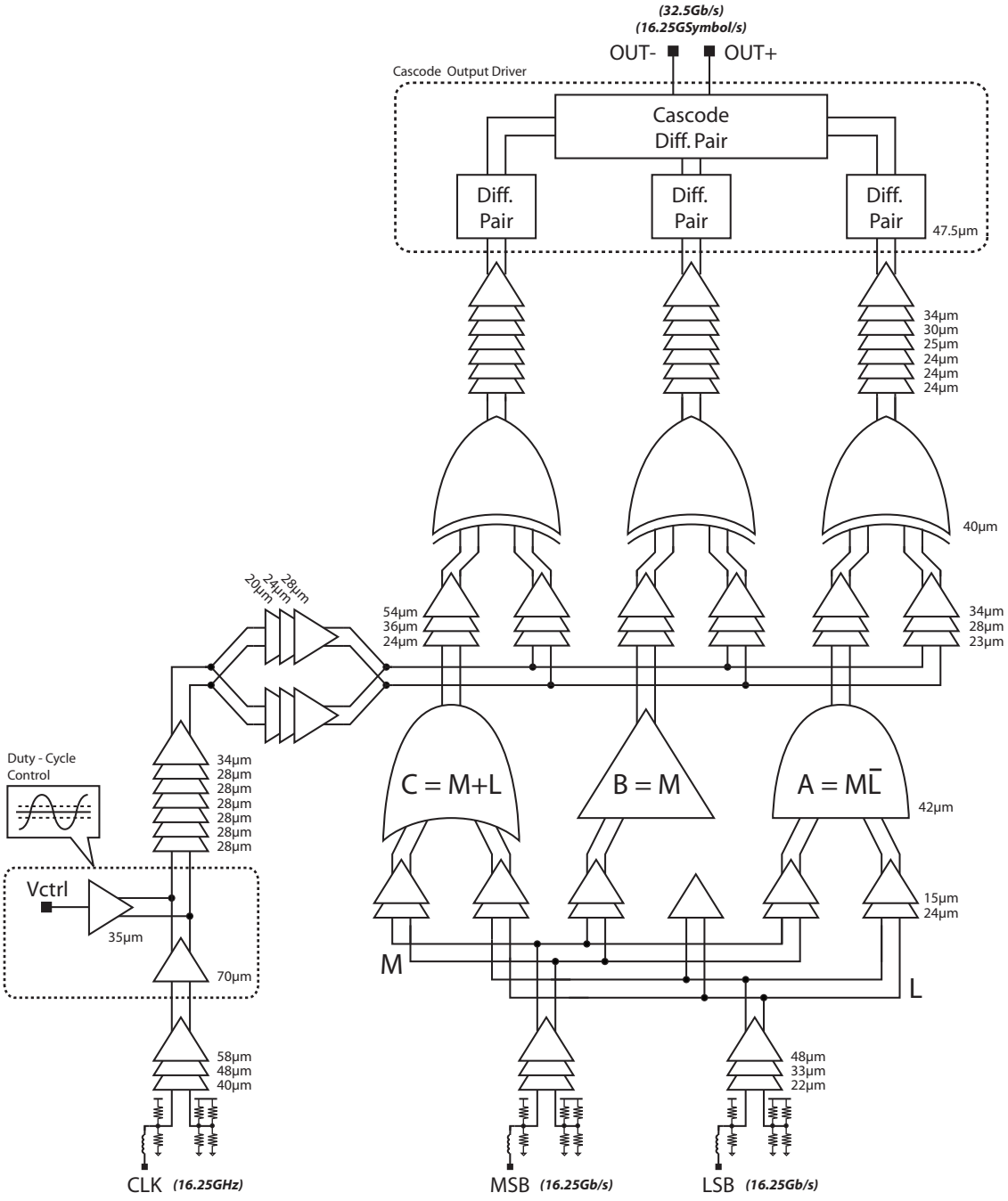


Figure 4.22: Complete transmitter circuit

4.5 Layout

The design was implemented in the IBM CMRF8SF 0.13μm technology. CMRF8SF technology provides 8 layers of metal with three thick copper and two thick aluminum layers. All devices in CML differential pairs have minimum drawn gate length of 0.12μm. Inductors are implemented using the 4^{th} and 5^{th} metal layers. For more details of inductor design and modeling please refer to appendix B. Load resistors in the CML circuits are implemented in a special metal resistance layer. Where possible, neighbouring metal layers are used to distribute V_{DD} and gnd to ensure low series resistance and increase decoupling capacitance for the supply voltage.

Fig. 4.23 is the complete layout of the transmitter. The three major components are integrated together in this layout. An extensive power grid is provided throughout the chip, with alternating layers of metals routing V_{DD} and gnd where possible. In addition, ESD and latchup design rules according to the design kit are met. The design occupies an area of 1.71mm x 1.83mm. A total of 165 spiral inductors and 80 CML gates are integrated into the design. The pad signals are labeled in fig. 4.23. The input pads are located along the bottom in $GSGSGSG$ configuration. The output pads are located along the top of the layout in $GSGSG$ configuration. The pads for the power supply voltages and control signals are located along the sides, each in $GPPGPPGPPGPPGPPG$ configuration. Two of the pads are allocated to the supply voltage for the output stage, with additional six pads allocated for various control and bias voltages. The remaining twelve pads are used for V_{DD} of the main circuit. The large number of pads helps to reduce contact resistance between the probes and the pads, in addition to ensuring a large safety margin for the current limits on the probes.

4.6 Fabrication

The layout was submitted to CMC on March 13th, 2007. Fabrication was done by IBM using in CMRF8SF 0.13μm technology. Forty finished dies were recieved on July 21st, 2007.

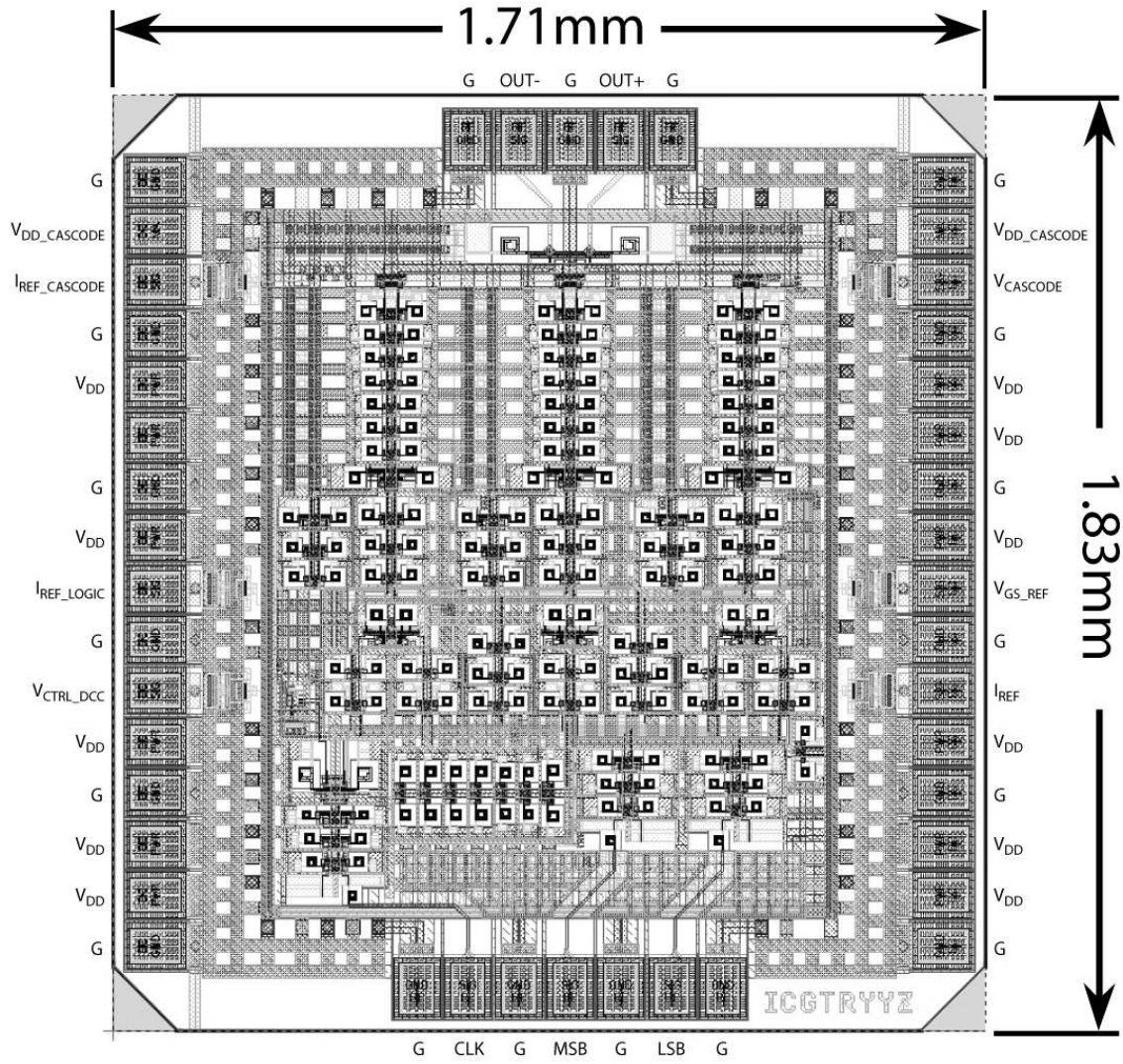


Figure 4.23: Layout of complete transmitter circuit

5 Measurements

The measurement setup and results of the fabricated design is detailed in this section. Due to bandwidth considerations the chip was not packaged and all measurements were performed on wafer. Fig. 5.1 is a die photo of the transmitter.

5.1 Measurement Setup

Fig. 5.2 illustrates the complete measurement setup. Two DC probes are used to route supply and control voltages to the transmitter. Input MSB, LSB, and clock signals are connected to the transmitter via a 67GHz bandwidth GSGSGSG probe. Each of the inputs is ac-coupled via a bias-tee. A phase-shifter is placed in the clock path

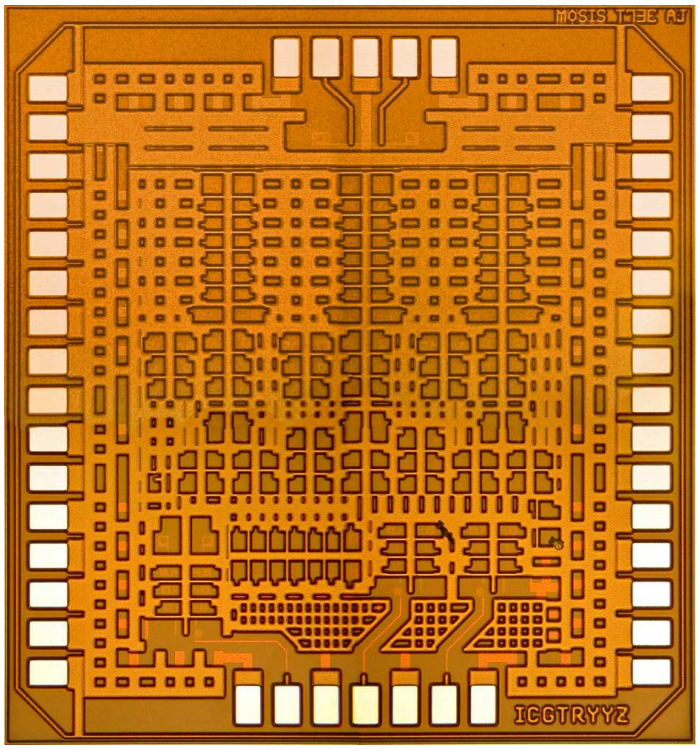


Figure 5.1: Die photo of transmitter

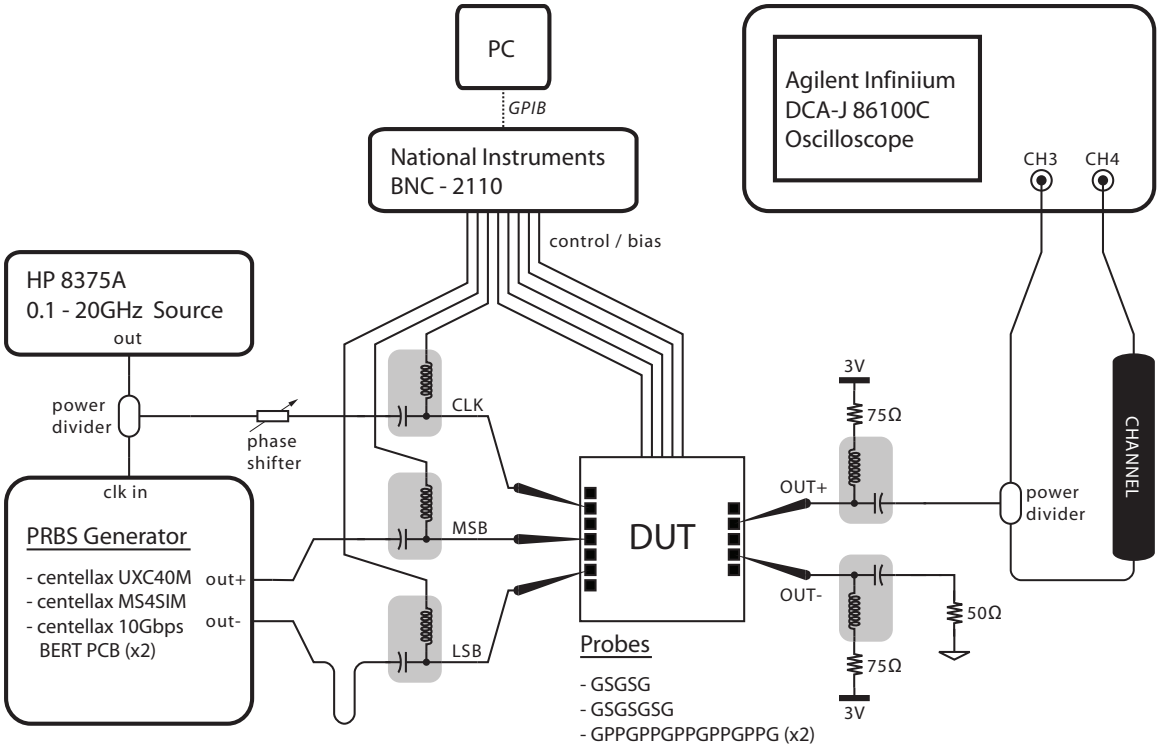


Figure 5.2: Measurement setup

to aid alignment of clock and data signals at the input of the XOR gates. The MSB and LSB inputs are taken from the differential outputs of the Pseudo-Random Binary Sequence (PRBS) setup. Different lengths of cables are used to shift their relative arrival times by several bit periods such that they appear as uncorrelated pseudo-random bit sequences. One of the outputs is terminated with a 50Ω termination while the other output is connected to a power divider. A power divider is used to allow the oscilloscope to measure the output signal of the transmitter. The 1.2Vpp output swing would overwhelm the oscilloscope without the 6dB attenuation provided by the power divider. This 6dB loss is accounted for by the oscilloscope so that the signal that appears on the screen has a 6dB gain applied by the oscilloscope's internal software. An additional benefit of the power divider is that it permits simlutaneous monitoring of both the input and output of the channel on the oscilloscope for the pre-emphasis experiments. Control voltages as well as input bias-tee DC voltages are controlled by Matlab using the NI BNC-2110 block via GPIB interface.

The transmitter draws a total power of 1.578W from the two power supplies. The simulated and measrured power consumption of the transmitter is summarized in table 5.1. The total power consumption from measurement matches closely with that

Table 5.1: Simulated and measured power consumption of transmitter

	Simulated	Measured
Clock distribution	496.7 mW	unknown
Data encoding	523.0 mW	unknown
PWM-PE generation	384.3 mW	unknown
Output driver	150.0 mW	147.0 mW
Total from 1.8V supply	1.404 W	1.431 W
Total from 3.0V supply	150.0 mW	147.0 mW
Total	1.554 W	1.578 W

of simulation. Based on simulation, clock distribution consumes approximately 32% of the total power, data encoding consumes approximately 33.7%, and the remaining 34.3% is used in the generation and propagation of PWM-PE data through the output driver.

5.1.1 List of Equipment

A comprehensive list of equipment and components is provided below.

- HP 8375A 0.1-20GHz synthesized sweeper
- Centellax UXC40M frequency divider
- Centellax MS4SIM 4:1 MUX
- Centellax OTB3P1A 10Gps BERT PCB (x2)
- NI BNC-2110 shielded connector block
- Agilent 86100C Infiniium DCA-J wideband oscilloscope
- HP 8510C Network Analyzer
- Agilent 6611C 40 Watt system power supply
- Agilent E3620A 50W dual output power supply (x2)
- Picosecond 5333 power divider (x2)
- Picosecond 5542 bias-tee (x3)
- Picosecond 5541A bias-tee (x2)

- GSGSG probe
- GSGSGSG probe
- GPPGPPGPPGPPGPPG probe (x2)

5.1.2 Channels

Three channels are used in the pre-emphasis experiments, each with different loss characteristics. Channel A is made up of six sections of 1-meter long SMA cables and the corresponding connectors. Channel B consists of 10 meters of Belden 1694A coaxial cable, six sections of 1-meter long SMA cables, and the corresponding connectors. Channel C is similar to channel B but with 30 meters of coaxial cable replacing the 10-meter cable. The loss characteristics of the three channels, measured using the HP 8510C network analyzer, are shown in fig. 5.3.

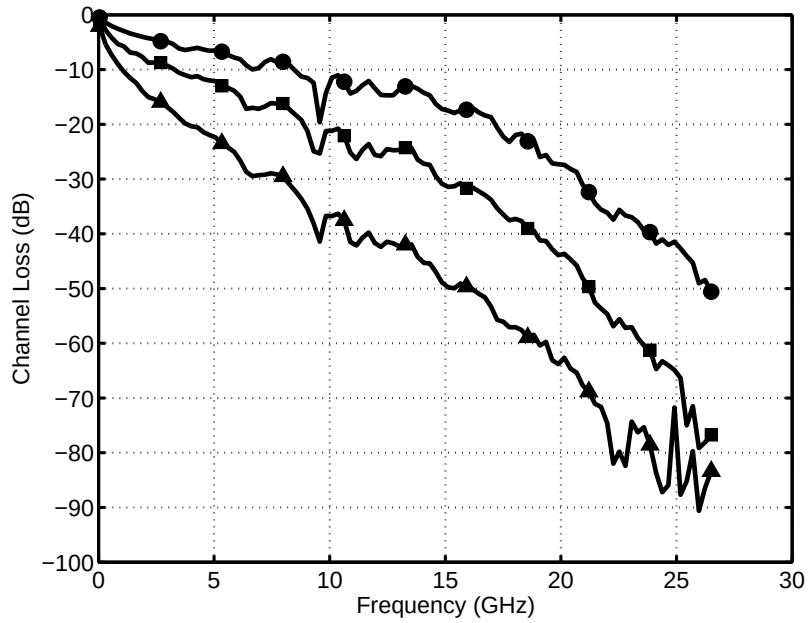


Figure 5.3: Cable channel responses: A (circular marker), B (square marker), C (triangular marker)

5.2 Binary Mode Measurements

For binary mode operation, the measurement setup is slightly modified. To remove the LSB input, the AC connection of the bias-tee is connected to a 50Ω load while

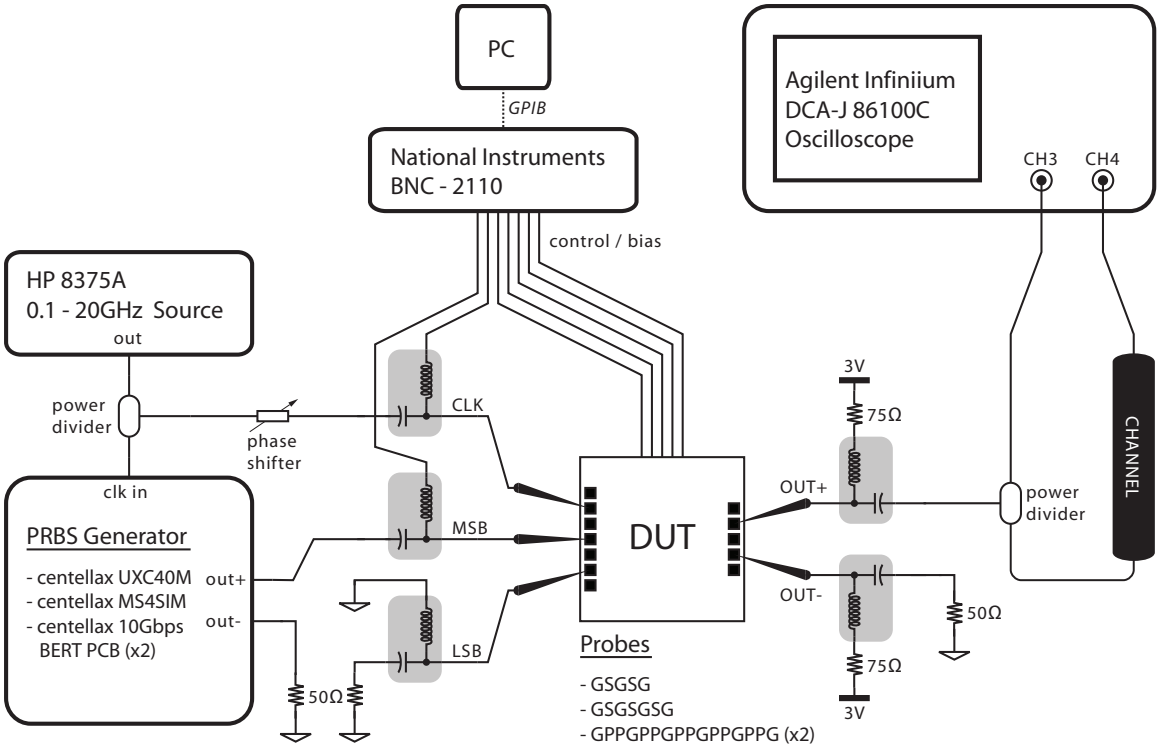


Figure 5.4: Binary mode measurement setup

the DC connection is shunted to ground. This provides a constant logical zero to the LSB signal path. The modified test setup is shown in fig. 5.4. The full-swing binary output follows the MSB input, as detailed in section 4.2.1. Alignment of the clock and MSB bit at the input of the XOR gates is critical to the operation of the transmitter. Due to the limited control provided by the external phase-shifter, only certain frequencies are useable for testing. Furthermore, proper alignment of signals within the PRBS setup was not possible at data rates between 16.5Gb/s to 20Gb/s. Hence, only data-rates of 11Gb/s, 14Gb/s, 16.25Gb/s, and 20.4Gb/s were used for testing.

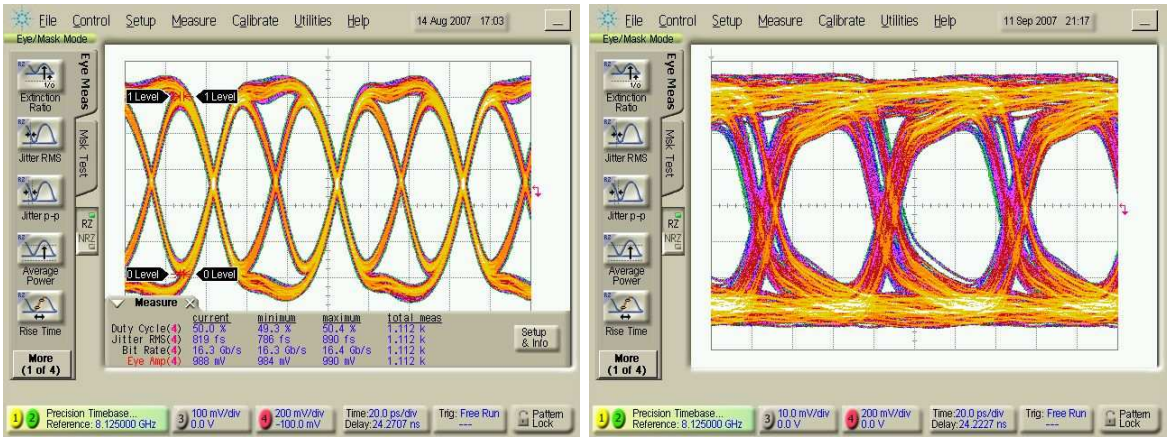
In this section, three sets of measurement results are presented. The first set of measurement results characterizes the output of the transmitter at 16.25Gb/s. The second set of measurement results comes from pre-emphasis experiments, also at a data-rate of 16.25Gb/s. The third set of measurements are results of the transmitter output at 20.4Gb/s.

5.2.1 Transmitter Output Transient Measurements

In this section, key features such as NRZ transmission, PWM-PE control, and amplitude control are tested in binary mode. All results are obtained with a binary input at 16.25Gb/s, and a clock signal of 16.25GHz.

PWM-PE & NRZ Modes

Fig. 5.5 illustrates the transmitter output with PWM-PE (50% duty-cycle) and in NRZ mode. Systematic jitter is clearly visible in NRZ mode transmission. This is due to the asymmetrical nature of the CML combinational logic gates in the thermometer Gray-code encoder as predicted in circuit simulation. In addition, skew in signal paths on chip might also increase the amount of systematic jitter. The transmitter output has better jitter performance with PWM-PE, as the clock signals realigns transitions at the XOR gates.



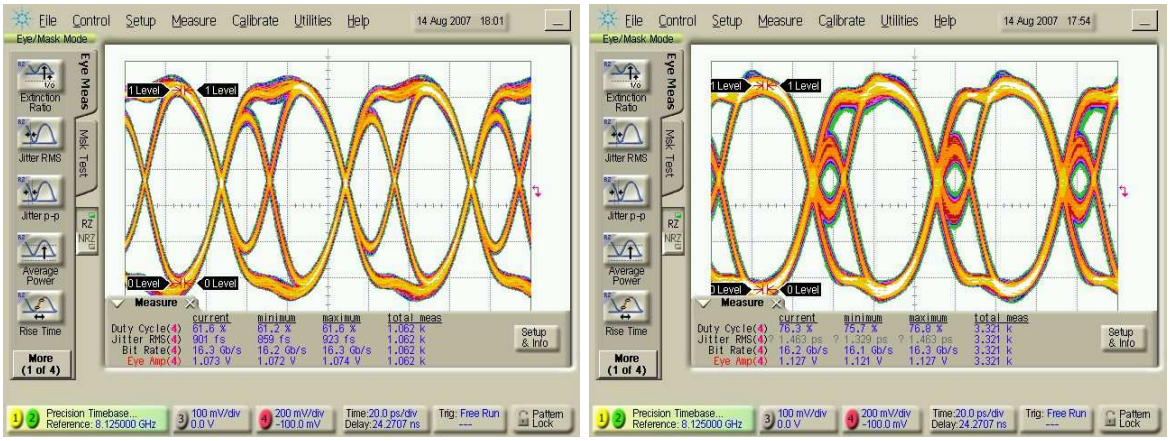
(a) 50% duty-cycle (b) NRZ

Figure 5.5: Transmitter output eye diagrams at 16.25Gb/s in binary transmit mode

Duty-Cycle Control

The transmitter output duty-cycle can be controlled externally. Fig. 5.6 illustrates the effect of duty-cycle control. A control voltage of 0V yields 50% duty-cycle whereas a voltage of 0.56V is responsible for the waveform with 76.3% duty-cycle as shown

in fig. 5.6(b). When the control voltage is further increased, the input clock signal is overwhelmed by the DC offset and the NRZ output signal shown in fig. 5.5(b) is transmitted.

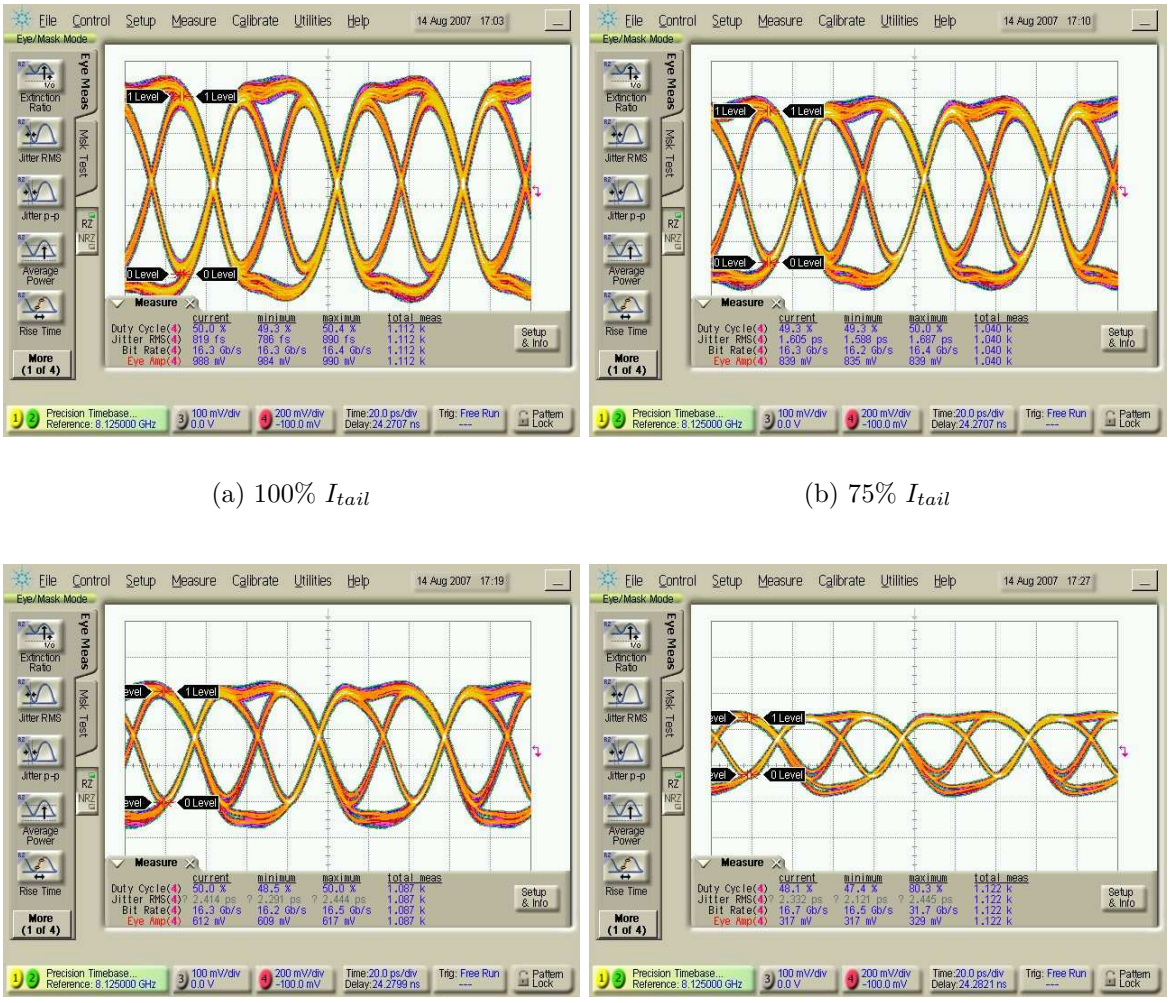


(a) 61.6% duty-cycle (b) 76.3% duty-cycle

Figure 5.6: Transmitter output eye diagrams at 16.25Gb/s in binary transmit mode: Duty-cycle control

Amplitude Control

The output swing of the transmitter can be controlled by an external bias current that is mirrored to the tail current of the cascode output stage shown in fig. 4.17. The eye diagrams shown in fig. 5.7 are obtained by adjusting the total tail current of the output stage from 100% to 25% of the maximum while keeping the duty-cycle at 50%. Fig. 5.8 is obtained with the identical tail current settings but a with duty-cycle of 61.6%.



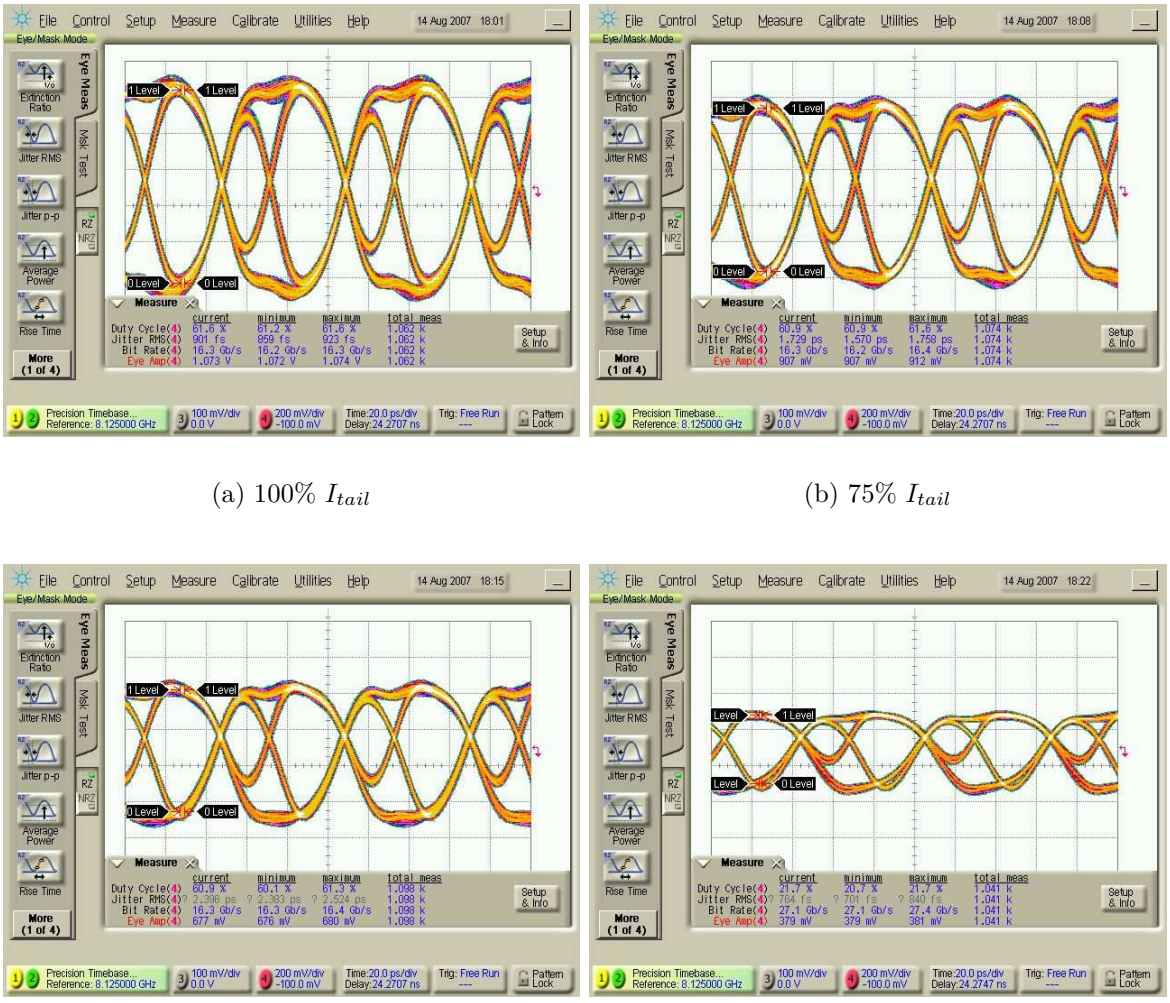
(a) 100% I_{tail}

(b) 75% I_{tail}

(c) 50% I_{tail}

(d) 25% I_{tail}

Figure 5.7: Transmitter output eye diagrams at 16.25Gb/s in binary transmit mode: Amplitude control at 50% duty-cycle



(a) 100% I_{tail}

(b) 75% I_{tail}

(c) 50% I_{tail}

(d) 25% I_{tail}

Figure 5.8: Transmitter output eye diagrams at 16.25Gb/s in binary transmit mode: Amplitude control at 61.6% duty-cycle

5.2.2 Pre-Emphasis Experiments

The goal of the pre-emphasis experiments is to find out how much channel loss can be compensated on the transmit side using PWM-PE and binary data. The setup of this experiment can be seen in fig. 5.4. Although the presence of a power divider in the output signal path is compensated by the oscilloscope software, the fact that only half the output signal swing is present at the input of the channel degrades the Signal-to-Noise Ratio (SNR) at the channel output.

Channel B at 16.25Gb/s

Channel B, which is consists of 10 meters of Belden 1694A coaxial cable with six sections of 1-meter long SMA cables and the corresponding connectors, is used in the first set of measurements at 16.25Gb/s, the same data rate as in section 5.2.1. Fig. 5.9 repeats the loss characteristics of channel B highlighting the loss at half the data rate. At 8.125GHz, the channel has a loss of 16.7dB. Fig. 5.10 shows the eye diagrams at the input and output of channel A without PWM-PE. The eye diagram at the output of the channel is completely closed.

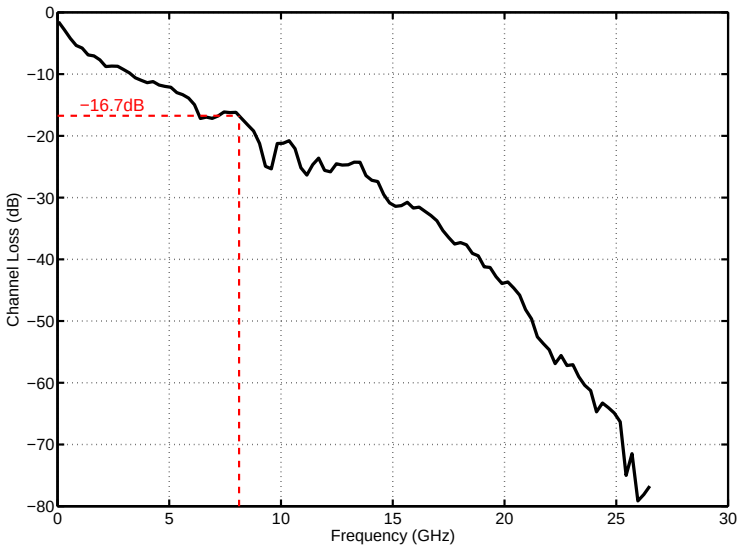
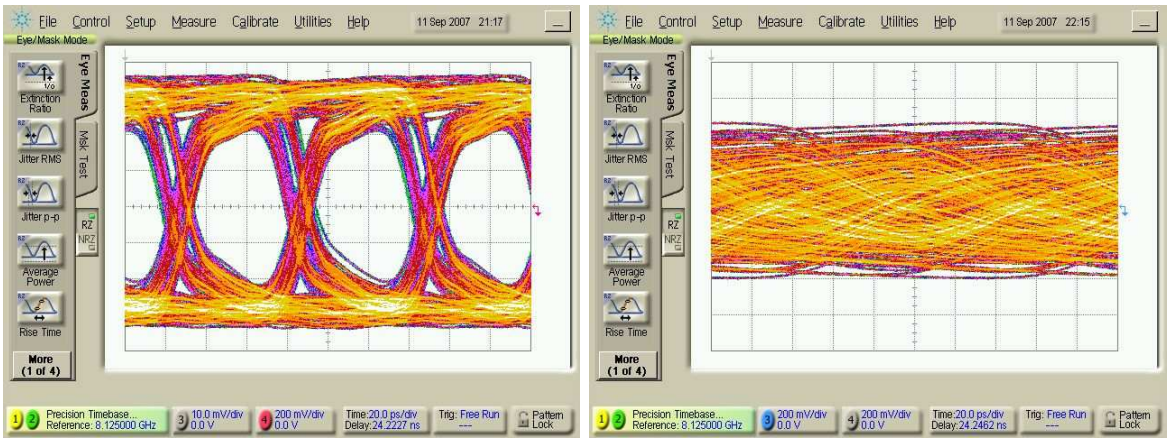


Figure 5.9: Channel B loss curve

By adjusting the duty-cycle of the transmit pulse, and thus the amount of pre-emphasis of the transmitter output, it is possible to obtained an open eye at the output of the channel. Fig. 5.11(a) illustrates the transmitter output in binary mode



(a) NRZ output of transmitter

(b) At the output of channel A

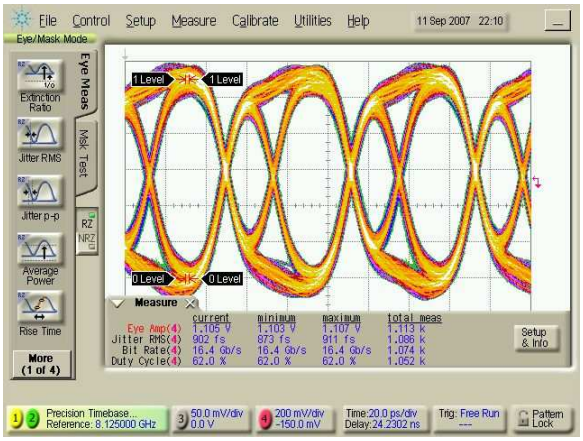
Figure 5.10: Eye diagrams for channel B at 16.25Gb/s in binary transmit mode without pre-emphasis

with 62% duty-cycle. The corresponding channel output eye diagram is shown in fig. 5.11(b). The output waveform has eye amplitude of 160mV. The BER bathtub curve is shown in fig. 5.11(c). After 2×10^7 measurements, the oscilloscope extrapolated a BER of better than 10^{-12} with 0.7UI margin at the channel output. The corresponding jitter histogram is shown in fig. 5.11(d) showing most of the jitter is data-dependent, hence due to systematic jitter in the transmitter and residual ISI.

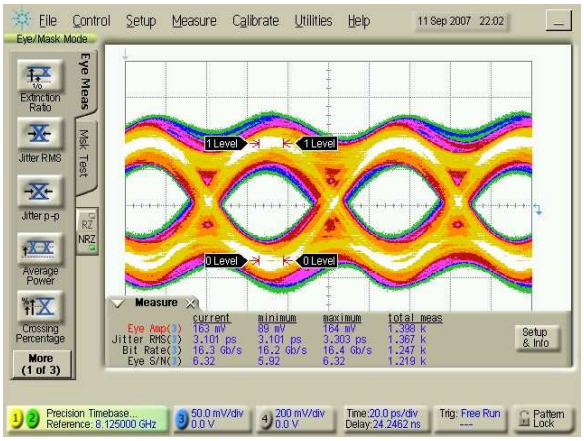
Channel C at 16.25Gb/s

The next set of measurements are performed at the same data-rate but with channel C. The coaxial cable length is increased from 10 meters to 30 meters, introducing more channel loss. Fig. 5.12 repeats the loss characteristics of channel C, highlighting the loss at half the output data rate. At 8.125GHz, the channel has a loss of 30.3dB. Fig. 5.13 shows the eye diagrams at the input and output of channel C without PWM-PE. As expected with this amount of channel loss, the eye diagram at the output of the channel is completely closed.

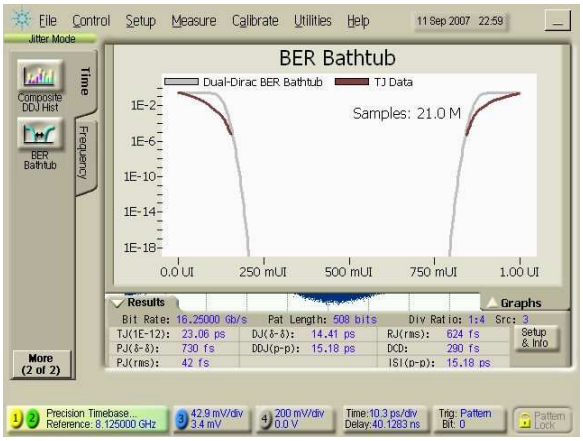
Fig. 5.14(a) illustrates the transmitter output in binary mode with 53.2% duty-cycle. The corresponding channel output eye diagram is shown in fig. 5.14(b). The output waveform has an eye amplitude of approximately 30mV. The effect of the SNR



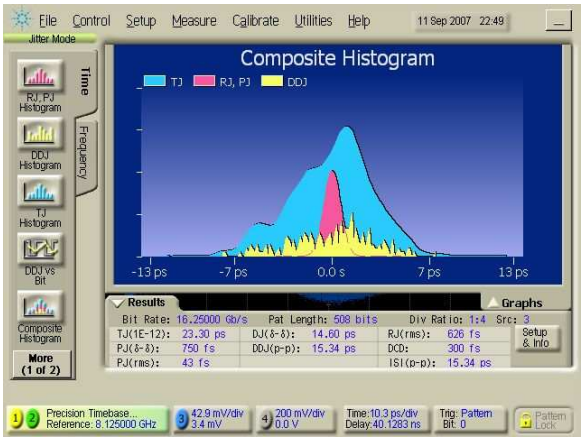
(a) Eye diagram at output of transmitter



(b) Eye diagram at output of channel



(c) BER bathtub plot of channel output data eye



(d) Jitter Histogram of channel output data eye

Figure 5.11: Channel B at 16.25Gb/s in binary signal with 62% duty-cycle

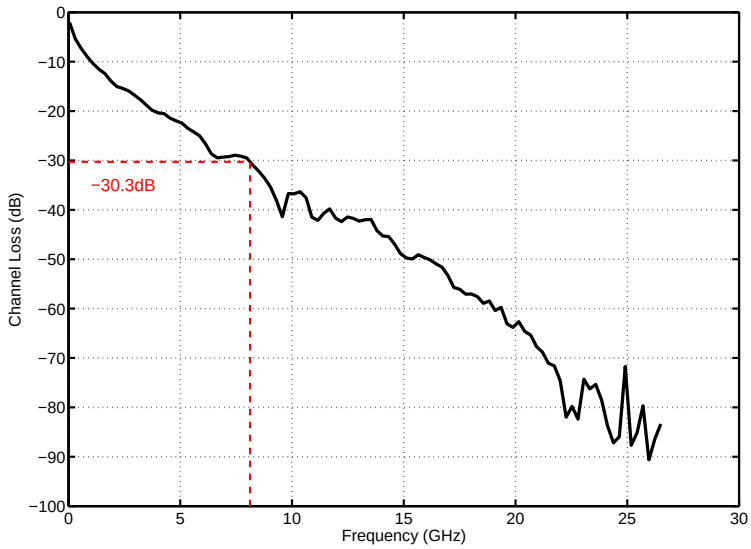
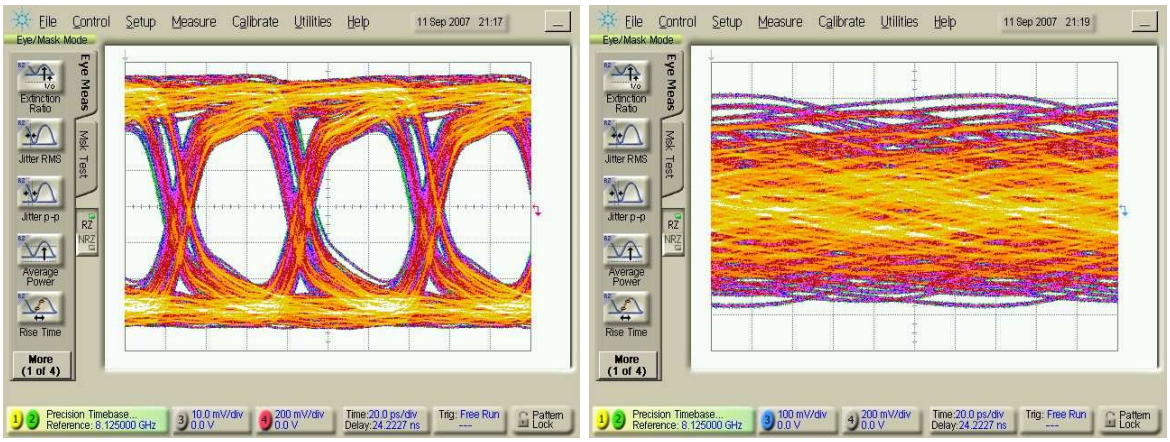


Figure 5.12: Channel C loss curve



(a) NRZ output of transmitter

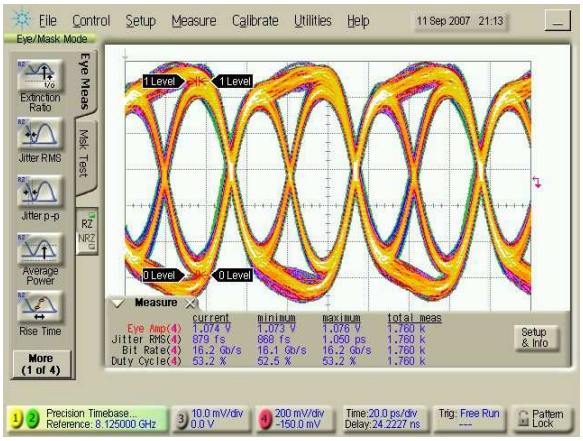
(b) At output of channel B

Figure 5.13: Eye diagrams for channel C at 16.25Gb/s in binary transmit mode without pre-emphasis

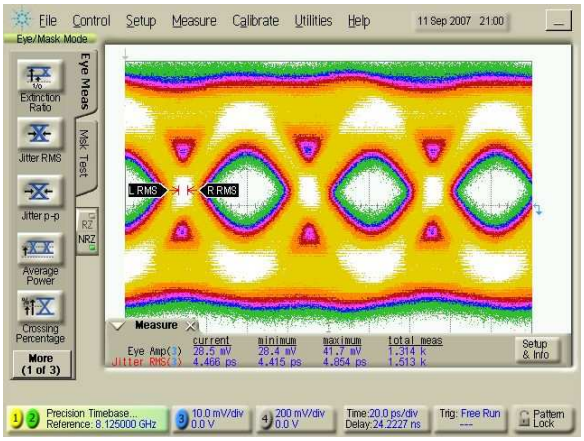
degradation due to the power divider is more visually evident in the channel output eye diagram due to its smaller voltage swing. For PWM-PE, the maximum amount of pre-emphasis that the transmitter can generate corresponds to when the duty-cycle is slightly above 50%. Therefore, at 53.2% of duty-cycle this channel presents a scenario close to the limitation to transmitter's capability to compensate for channel loss. The BER bathtub curve is shown in fig. 5.14(c). 2×10^7 measurements were taken and the oscilloscope extrapolated a BER of better than 10^{-12} with approximately 0.25UI margin at the channel output. The corresponding jitter histogram is shown in fig. 5.14(d). Notice that random jitter is now the dominant source of jitter because increased channel losses have reduced the received signal swing but the amplitude of random noise is the same as before.

5.2.3 20.4Gb/s Transient Measurements

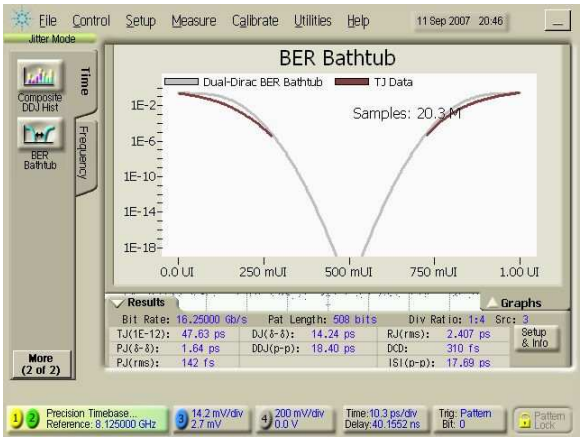
Transmitter output eye diagrams with different duty-cycles at a data-rate of 20.4Gb/s are presented in fig. 5.15. Imperfect transitions are seen at every other eye. The MUX in the PRBS setup is suspected as a possible source of such abnormal behavior, as it is the only component in the entire setup that operates at half the output symbol rate.



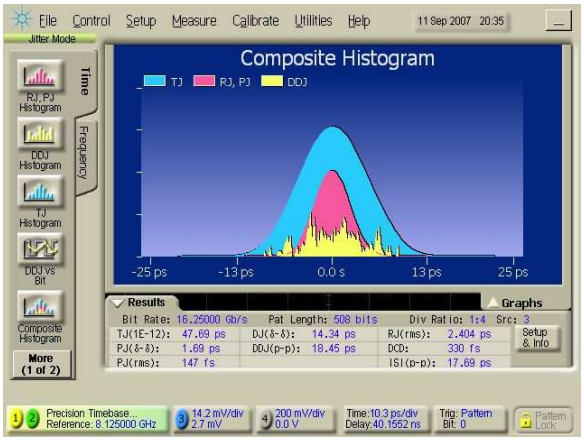
(a) Eye diagram at output of transmitter



(b) Eye diagram at output of channel

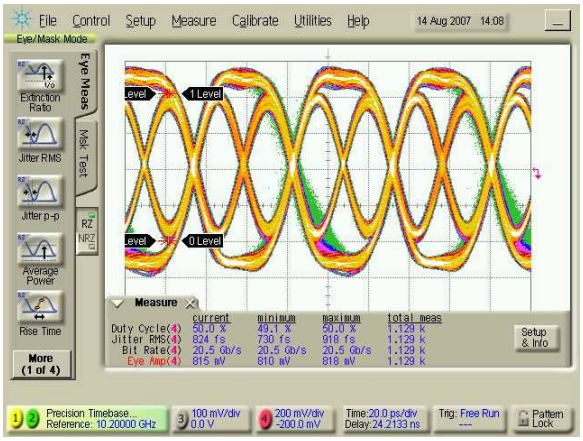


(c) BER bathtub plot of channel output data eye

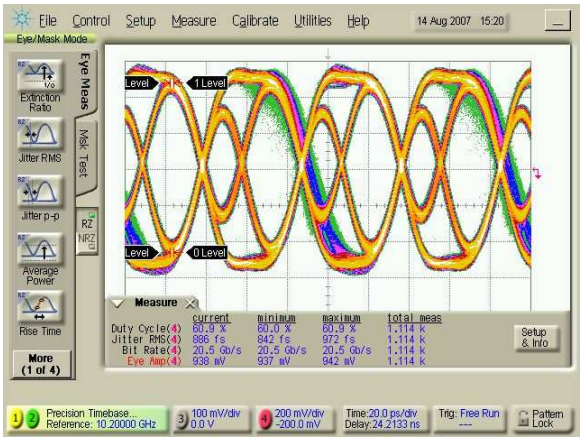


(d) Jitter Histogram of channel output data eye

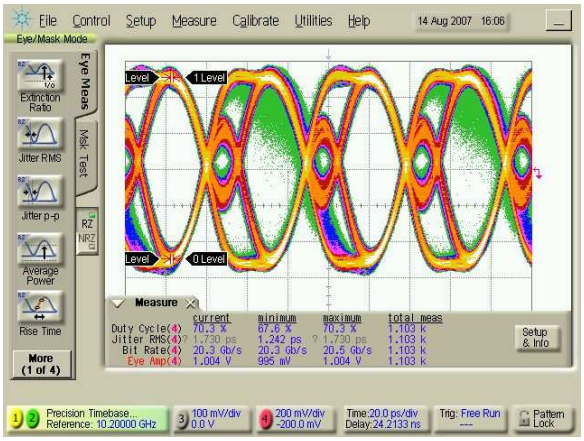
Figure 5.14: Channel C at 16.25Gb/s in binary signal with 53.2% duty-cycle



(a) 50% duty-cycle



(b) 60.9% duty-cycle



(c) 70.3% duty-cycle

Figure 5.15: Transmitter output eye diagrams at 20.4Gb/s in binary transmit mode: Duty-cycle control

5.3 4PAM Mode Measurements

Having characterized the binary mode of transmission along with pre-emphasis experiments, the next set of measurements involves the full 4PAM signals. Now, all three high-speed inputs must be carefully aligned various points of the transmitter: LSB, MSB and clock. As different lengths of cable must be used to connect the complimentary outputs of the PRBS setup to de-correlate the MSB and LSB input signals (as shown in fig. 5.2), the phase delay between the two signals becomes a function of the data-rate. This, in addition to the limited capability of the external phase-shifter, made the testing of 4PAM signals very difficult. Hence, was performed only at two data rates: 22Gb/s and 32.5Gb/s, which correspond to symbol rates of 11GSymbol/s and 16.25GSymbol/s respectively.

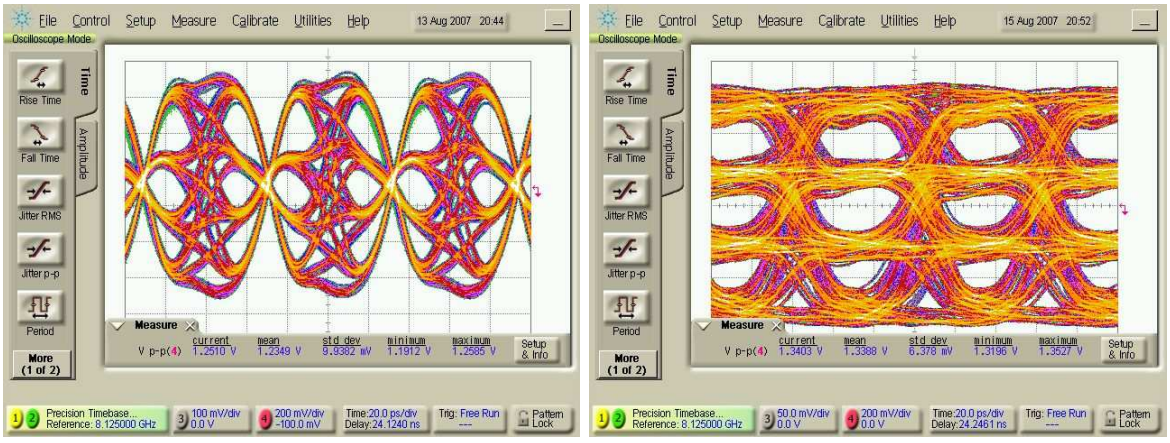
In this section, two sets of measurement results are presented. The first set of measurement results characterizes the output of the transmitter at 32.5Gb/s (16.25GSymbol/s). The second set of measurements demonstrates pre-emphasis on various coaxial cable channels at 22Gb/s and 32.5Gb/s.

5.3.1 Transmitter Output Transient Measurements

The first set of measurements is performed to characterize the transmitter output in the 4PAM mode of transmission. Key features such as NRZ transmission, PWM-PE control, and amplitude control are tested. All results are obtained with binary MSB and LSB inputs at 16.25Gb/s, and a clock signal of 16.25GHz. The oscilloscope automatic measurement functions (such as eye amplitude, duty-cycle, pattern-locking, BER bathtub curve and jitter analysis) are lost with 4PAM signals. Instead, markers are used to manually take measurements of the eye diagrams.

PWM-PE & NRZ Modes

Fig. 5.16 illustrates the transmitter output with PWM-PE (50% duty-cycle) and in NRZ mode. Similar to of binary transmit mode, jitter is much greater in NRZ mode than with PWM-PE. In addition to the asymmetrical nature of the CML AND & OR gates in the thermometer Gray-code encoder being a contributing factor to the jitter, the skew between MSB and LSB signal paths also contributes to the overall jitter performance.

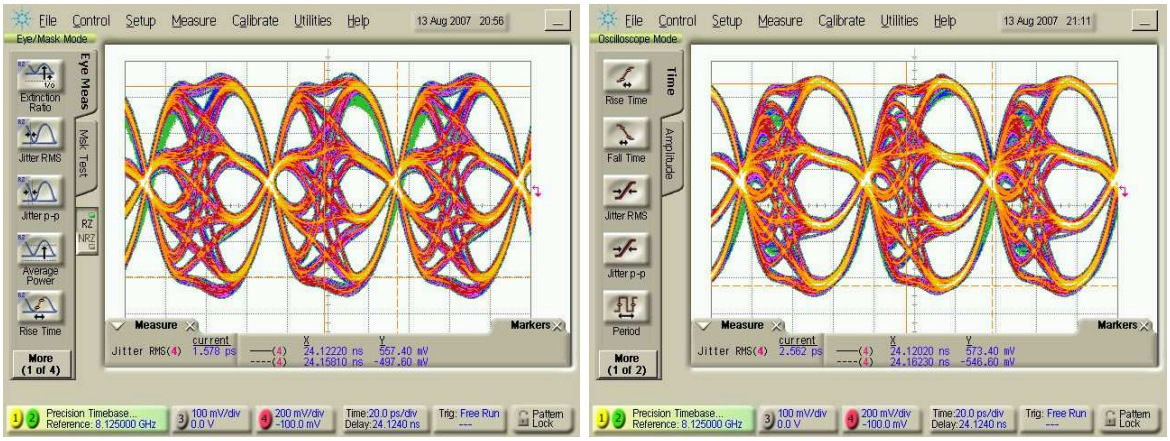


(a) 50% duty-cycle (b) NRZ

Figure 5.16: Transmitter output eye diagrams at 32.5Gb/s in 4PAM transmit mode

Duty-Cycle Control

Fig. 5.17 illustrates duty-cycle control of the 4PAM signals at the transmitter output. A control voltage of 0V yields 50% duty-cycle whereas a voltage of 0.52V provides 68.4% duty-cycle as shown in fig. 5.17(b). When the control voltage is further increased, the input clock signal is overwhelmed by the DC offset and a 4PAM NRZ output signal as shown in fig. 5.16(b) is transmitted. Note that mild imperfections appear in every other bit of the 4PAM eyes at 32.5Gb/s. These problems prevented operation at higher data rate. Again, skew problems in the PRBS MUX are suspected since that is the only place in the test setup where a half-rate clock appears.

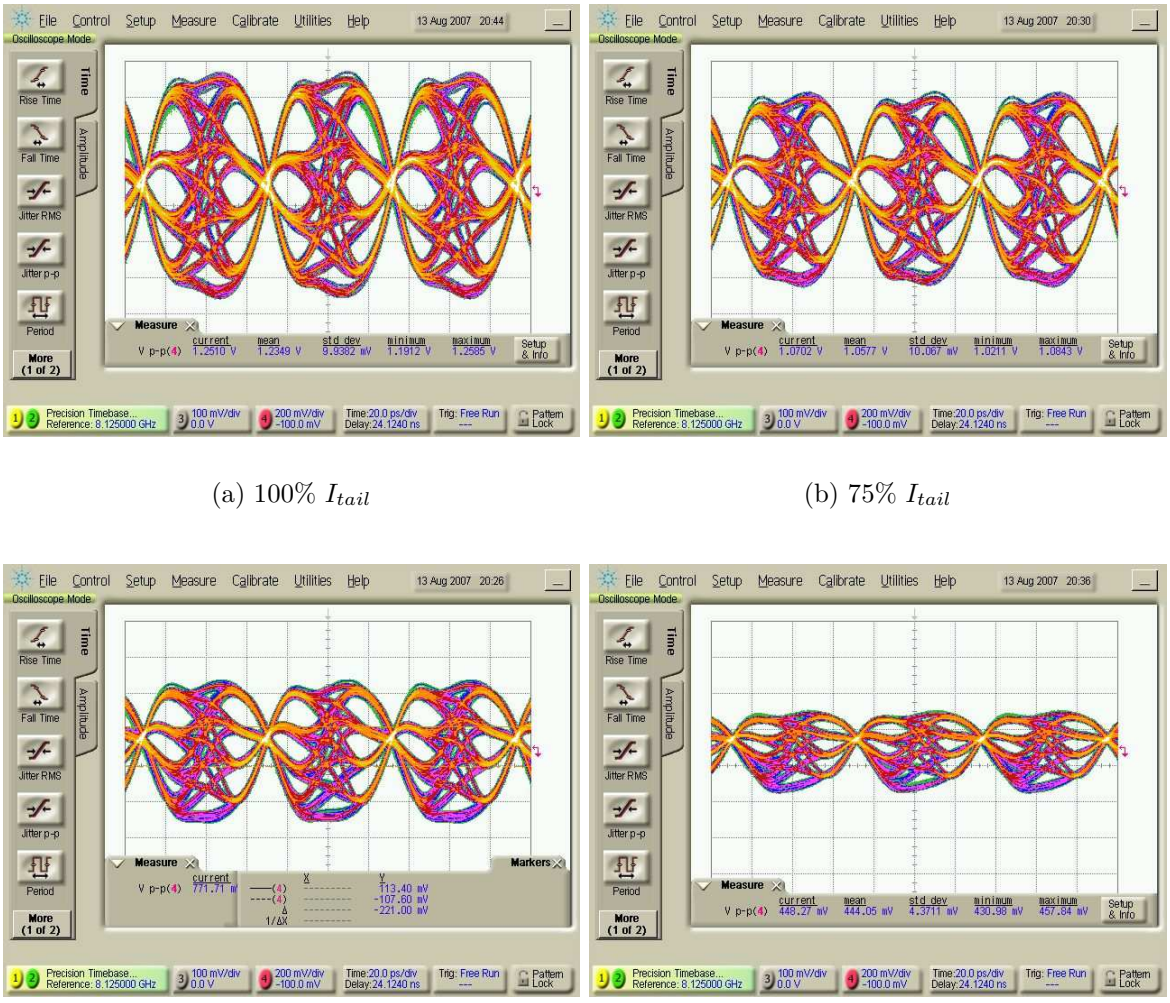


(a) 58.3% duty-cycle (b) 68.4% duty-cycle

Figure 5.17: Transmitter output eye diagrams at 32.5Gb/s in 4PAM transmit mode: Duty-cycle control

Amplitude Control

The output swing of the transmitter can be controlled by an external bias voltage that is connected to the gates of the tail current devices of the cascode output stage. The eye diagrams shown in fig. 5.18 are obtained by adjusting the total tail current of the output stage from 100% to 25% of their maximum while keeping the duty-cycle at 50%. Fig. 5.19 is performed with the identical tail current settings but with a duty-cycle of 68.4%.



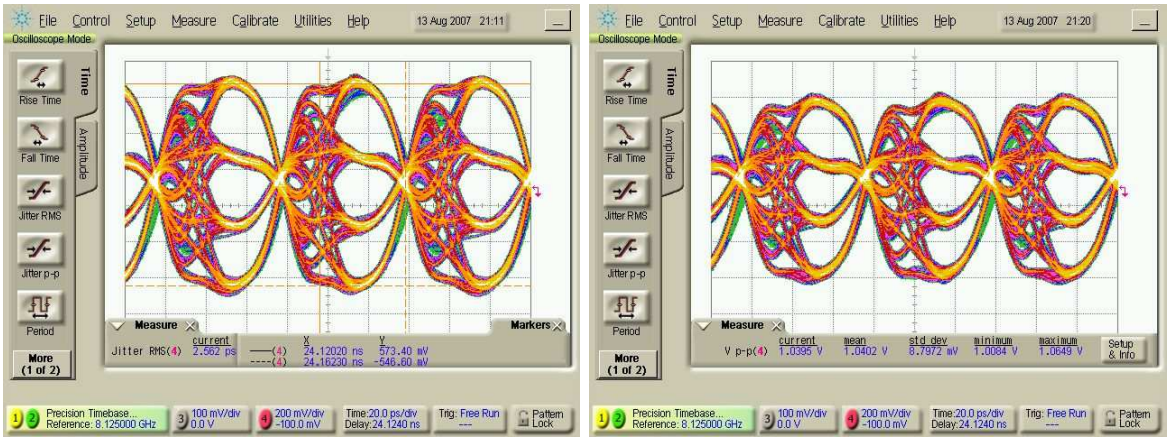
(a) 100% I_{tail}

(b) 75% I_{tail}

(c) 50% I_{tail}

(d) 25% I_{tail}

Figure 5.18: Transmitter output eye diagrams at 32.5Gb/s in 4PAM transmit mode: Amplitude control at 50% duty-cycle



(a) 100% I_{tail}

(b) 75% I_{tail}

(c) 50% I_{tail}

(d) 25% I_{tail}

Figure 5.19: Transmitter output eye diagrams at 16.25Gb/s in binary transmit mode: Amplitude control at 68.4% duty-cycle

5.3.2 Pre-Emphasis Experiments

Similar to the binary pre-emphasis experiments, the following measurements are taken with transmitter output signals passing through a coaxial cable channel to characterize the pre-emphasis performance. In this section, results are presented for 4PAM mode of operation at 22Gb/s and 32.5Gb/s with 4PAM signals through channel A.

Channel A at 22Gb/s

The frequency response of channel A, which is consists of six sections of 1-meter long SMA cables and the corresponding connectors, is shown in fig. 5.20. For 22Gb/s operation, at half the symbol rate (5.5GHz), the channel has a loss of 7.1dB and half the bit rate (11GHz) the loss increases to 14.2dB. Fig. 5.21 shows the eye diagrams at the input and output of channel C without PWM-PE. The eye diagram at the output of the channel is completely closed.

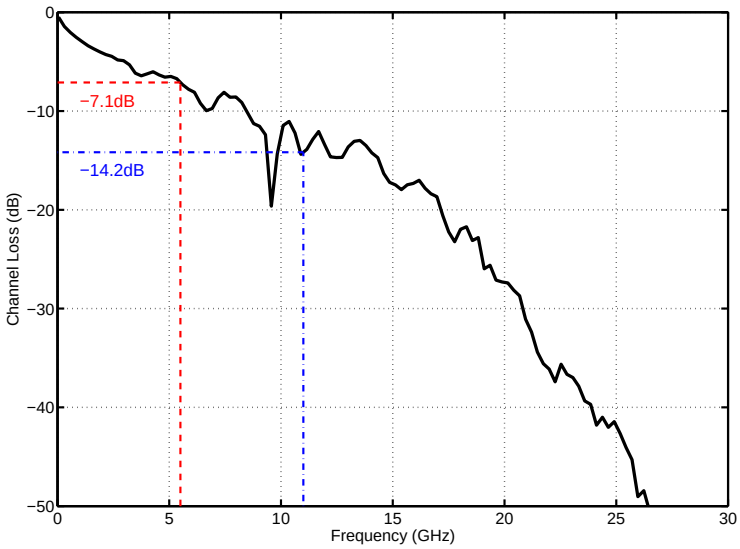
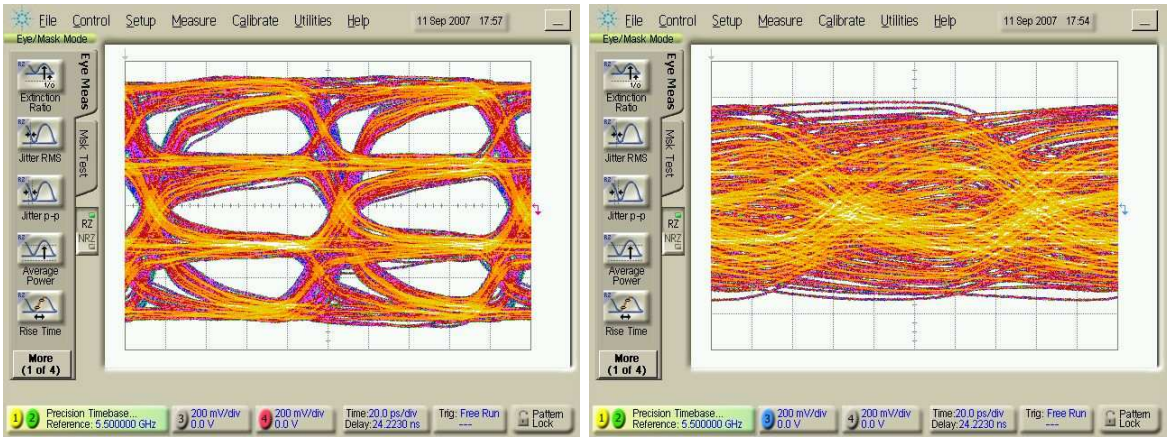


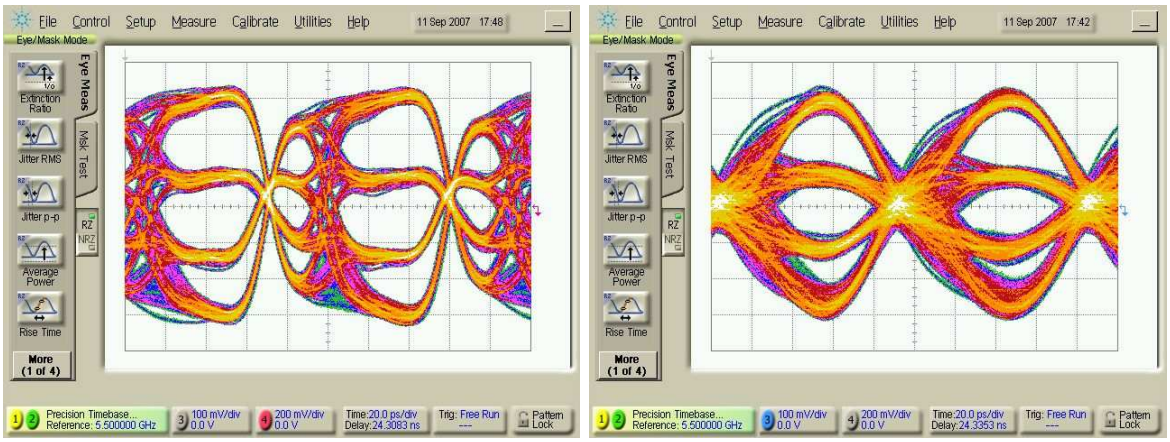
Figure 5.20: Channel A loss curve and channel loss at 5.5GHz and 11GHz

By manually adjusting the duty-cycle of the transmit pulse, and thus the amount of pre-emphasis of the transmitter output, it is possible to obtain an open eye at the output of the channel. Fig. 5.22(a) illustrates the transmitter 4PAM output with 66% duty-cycle. The corresponding channel output eye diagram is shown in fig. 5.22(b). The 4PAM level spacing at the receiver is greater than 60mV.



(a) Eye diagram at output of transmitter (b) Eye diagram at output of channel

Figure 5.21: Channel A at 22Gb/s in 4PAM transmit mode without pre-emphasis



(a) Eye diagram at output of transmitter (b) Eye diagram at output of channel

Figure 5.22: Channel A at 22Gb/s in binary transmit mode with 66% duty-cycle

Channel A at 32.5Gb/s

For a data rate of 32.5Gb/s (16.25GSymbol/s), at half the output symbol rate (8.125GHz), channel A has a loss of 8.9dB and at half the bit-rate (16.25GHz) it has a loss of 17.2dB as shown in fig. 5.23. Fig. 5.24 shows the eye diagrams at the input and output of channel A without PWM-PE. The eye diagram at the output of the channel is completely closed.

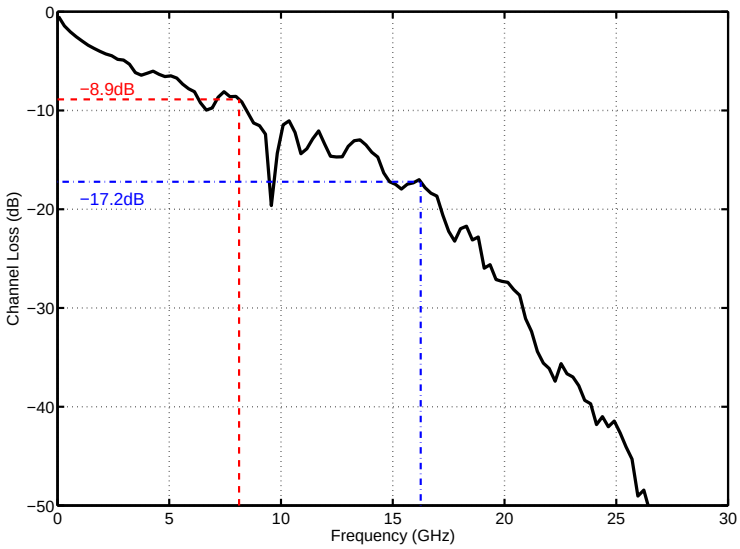
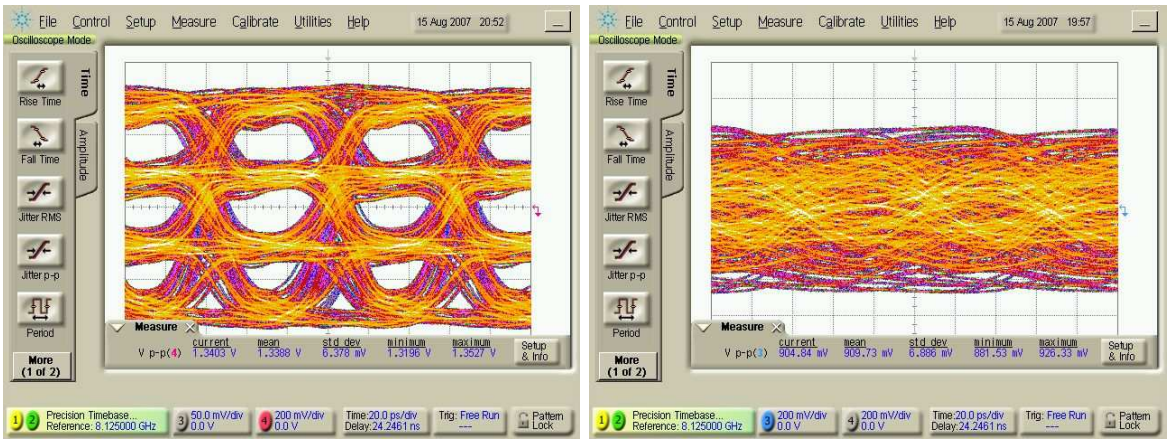


Figure 5.23: Channel A loss curve and channel loss at 8.125GHz and 16.25GHz

By manually adjusting the duty-cycle of the transmit pulse, and thus the amount of pre-emphasis of the transmitter output, it is possible to obtain an open eye at the output of the channel. Fig. 5.25(a) illustrates the transmitter 4PAM output with 64% duty-cycle. The corresponding channel output eye diagram is shown in fig. 5.25(b). The 4PAM level spacing is 30mV at the output of the channel.

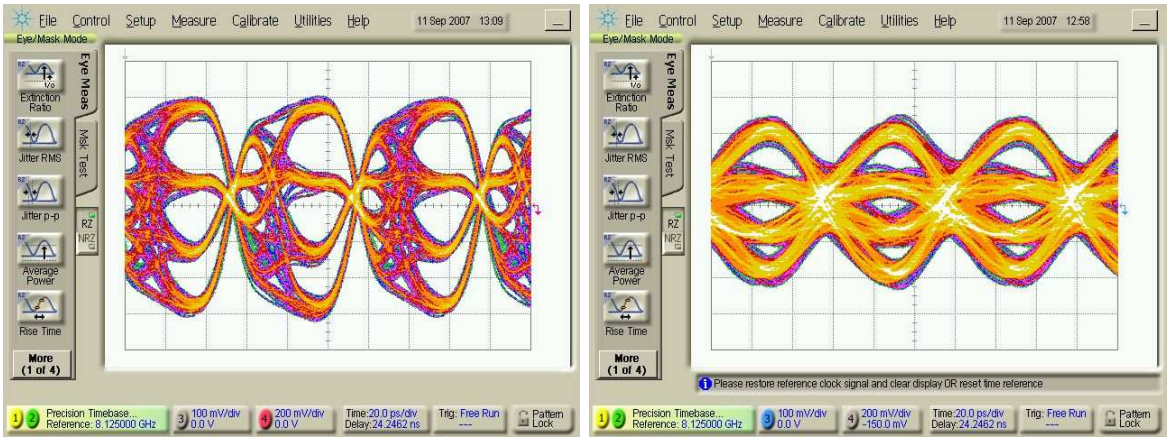
5.4 Conclusions

The maximum amount of loss compensated by the transmitter in 4PAM mode is 8.9dB at 32.5Gb/s with 64% duty-cycle pulse. In binary mode, 30.3dB of loss compensation is achieved at the same symbol rate of 16.25GSymbol/s (16.25Gb/s) with 53.2% duty cycle. The lower loss compensation and larger duty-cycle of the transmit pulse in



(a) Eye diagram at output of transmitter (b) Eye diagram at output of channel

Figure 5.24: Channel A at 32.5Gb/s in 4PAM transmit mode without pre-emphasis



(a) At output of transmitter (b) At output of channel

Figure 5.25: Eye diagrams for channel A at 32.5Gb/s in binary transmit mode with 64% duty-cycle

4PAM mode compared to binary mode demands an explanation. The large duty-cycle (64%) of the transmit pulse indicates that maximum amount of pre-emphasis is not used. Based on the channel output eye diagram shown in fig. 5.25(b), limitation to the 4PAM mode of transmission is mainly due to residual ISI in the channel-output waveform. In section 2.2, PWM-PE is shown to be a good match to the inverse of the channel loss characteristic with the channel being the Belden 1694A coaxial cable. Superior loss compensation is demonstrated in binary mode equalization experiments where channels B and C are used. In channel B, and even more so in channel C, the loss characteristic is dominated by the Belden 1694A coaxial cable. In contrast, channel A (which is used in the 4PAM equalization experiments) is made up of only six sections of 1-meter SMA cables with no Belden 1694A coaxial cable section. The poor matching of PWM-PE pulse spectrum to the SMA cable loss characteristic is suspected as a contributing factors for larger residual ISI seen in the 4PAM equalization experiments using channel A, and by extension a possible contributing factor to the lower loss compensation achieved in the 4PAM equalization experiments.

In this section, the prototype transmitter is characterized. It is shown that the transmitter can transmit up to 16.25Gb/s reliably (and 20.4Gb/s marginally) in binary mode, and 32.5Gb/s in 4PAM mode. Features such as DCC and amplitude control are also tested in both binary and 4PAM modes of operation. In addition, equalization experiments were performed to quantify the amount of loss compensation possible using PWM-PE. It is found that up to 30.3dB of loss can be compensated in binary mode at a data-rate of 16.25Gb/s, and 8.9dB of loss in 4PAM mode at data rate of 32.5Gb/s. Better SNR could be achieved if the power divider at the output path is removed. The chip consumes 1.578W of power from its two supplies, which is close to its simulated power consumption of 1.554W.

6 Conclusion

6.1 Summary

The main contribution of this thesis work is the design of a coaxial cable driver with PWM-PE with 4PAM signaling. The high-speed CML design approach discussed in this thesis enabled the circuit to operate up to 32.5Gb/s (measured) in 4PAM mode using the $0.13\mu m$ CMOS technology. Features such as duty-cycle and output amplitude controls are successfully designed and tested. Using PWM-PE, the transmitter achieved a maximum of 30.3dB of cable loss compensation at data rate of 16.25Gb/s in binary mode, and 8.9dB at 32.5Gb/s in 4PAM mode. The design occupies an area of 1.71mm x 1.83mm, and consumes a total of 1.578W.

A comparison of this work with current state of the art 4PAM transmitter is provided in table 6.1. At a maximum data rate of 32.5Gb/s, this work is the fastest CMOS implementation of 4PAM transmitter reported to date. The loss compensation of 8.9dB is secondary only to the 14.5dB reported in [5]. A suspected cause for the relatively low loss compensation of 8.9dB is the use of SMA cable as channel in the 4PAM equalization experiment. The maximum measured output swing for this work is 1.25V (shown in table 6.1). The maximum designed swing of 1.6Vpp per side under matched 75-Ω load is higher than all other 4PAM transmitters. The high power consumption of this work is due to the large output swing, complex architecture (encoder, clock distribution network, PWM-PE) and low fanout of high-speed CML stages as required for the targeted speed.

In binary mode, this transmitter achieved loss compensation of 30.3dB (@ 8.125GHz) at a data rate of 16.25Gb/s. The binary transmitter with PWM-PE in [15], implemented in the $0.13\mu m$ CMOS process, compensated 31dB[1] of cable loss at 5Gb/s. The similar maximum loss compensation ($\sim$30dB) with duty-cycle near 50% of the two transmitters employing PWM-PE indicates that they are both approaching the

[1]The reported 33dB loss includes the estimated parasitic losses in the path from chip to coaxial cable [15].

Table 6.1: Comparsion of 4PAM transmitters

	CMOS process	Maximum output swing	Maximum data rate	Maximum loss compensation	Power consumption
[4]	90-nm SOI	520mV	25Gb/s	3dB (@ 6.25GHz)	101.8mW
[5]	90-nm	800mV	24Gb/s	14.5dB (@ 6GHz)	510mW
[8]	0.4-μm	1.1V	10Gb/s	not reported	1W
[6]	0.25-μm	600mV	10Gb/s	3.7dB (@ 2.5GHz)	222mW
[36]	0.18-μm	600mV	10Gb/s	-	120mW
This work	0.13-μm	1.25V	32.5Gb/s	8.9dB (@ 8.125GHz)	1.578W

limit of loss compensation achievable using pulse-width modulation pre-emphasis. The data rate of 16.25Gb/s of this work is more than three times faster than that reported in [15] while both transmitters are implemented in the $0.13\mu m$ CMOS process. The high-speed CML design approach used in this thesis work is instrumental to its higher maximum data rate. In contrast, high fanout ($k = 3$ in the line driver) and absence of peaking inductors in [15] lead to high OCTC of its CML stages and ultimately contributed to the limitation on its maximum operating speed (and lower power consumption). Another transmitter with comparable channel loss compensation is [37][2]. Approximately 30dB of loss compensation is achieved using 5-tap FIR pre-emphasis at a data rate of 3.125Gb/s in the $0.11\mu m$ CMOS process.

High output swing is another key design aspect of this transmitter. It is challenging to design a high-speed transmitter in CMOS (above 10Gb/s) with high output swing. The modulator driver in [38], implementated in the $0.18\mu m$ CMOS process, has a single-ended swing of 4V for data rates up to 13.6Gb/s using a novel cascode topology. It consumes 600mW of power and does not include any pre-emphasis circuits. The backplane driver in [23] has a maximum swing of 350Vpp per side up to 20Gb/s with digital pre-emphasis. The 2:1 MUX output stage in [22] has an output swing of 260mVpp per side (520mVpp differential) at a data rate of 38.4Gb/s. Both [23] and [22] are implemented in the the $0.13\mu m$ CMOS process. The output driver cascode topology is instrumental to the high output swing of this work. The measured 1.25Vpp per side in this work is higher than any other transmitters above 10Gb/s in the same CMOS process. An output driver design with cascode and open-drain drain topology is reported in [20][3]. It has a target swing of 1.8Vpp per side. However, its target output swing is not verified as measurement waveform shows only 700mVpp

[2]transmitter only
[3]chip 2

(at 4Gb/s with pre-emphasis).

High data rate is another important aspect of this design. With a maximum data rate of 16.25Gb/s (20.4Gb/s with marginal performance) in 2PAM mode of operation, however, this transmitter is not the fastest binary transmitter in the $0.13\mu m$ CMOS technology. The backplane driver in [23] can operate up to 30Gb/s without pre-emphasis and 20Gb/s with digital pre-emphasis. Like this work, high (peak f_T) current density biasing was used in conjunction with inductive peaking at every CML stage. The internal swing of 450mV for CML gates in [23] is less than the soft-switching voltage of ∼780mV used in this work, as required by the large output swing specification of this work. The 2:1 MUX output stage in [22] can operate up to an impressive data rate of 40Gb/s. Shunt and double series peaking in addition to negative feedback is used in the CML MUX design to attain the target bandwidth. It is important to note that the bandwidth-limiting nodes are only present in the last two stages of the design due to the 2:1 multiplexing tree structure of the transmitter. The 40Gb/s transmitter in [22] does not incorporate pre-emphasis. As a large portion of the transmitter requires high bandwidth in this thesis design due to PWM-PE, implementation with similar circuit techniques as [22] in a transmitter with PWM-PE would be very challenging due to proper modeling of T-bridged inductors and design of feedback at the many CML stages.

Finally, the ablility to adapt to a wide range of channels is another key aspect of the design. The capability to switch between 4PAM and 2PAM mode of operation without modification (by grounding the LSB input) makes this transmitter design suitable for communication links with 4PAM and 2PAM receivers. The adjustable pre-emphasis (50%–75% duty-cycle, or NRZ) and adjustable output amplitude makes it suitable for use in a wide range of channels with different losses. The single-coefficient pre-emphasis control of this work simplifies adaptation implementation compared to the multi-tap FIR pre-emphasis approach (i.e. five-coefficients in [37]). The maximum delay of the delay cells within the digital pre-emphasis block in [23] limits the amount of loss compensation available at low data rates. On the other hand, PWM-PE used in this thesis work is able to compensate channels even at low data rates.

In summary, the 4PAM transmitter presented in this thesis work is the first of its kind to incorporate PWM-PE in addition to being the fastest reported to date. Summaries of the 4PAM and 2PAM transmitters mentioned in this section is provided in table 6.1 and 6.2 respectively. The transmitter of this thesis work compares favor-

Table 6.2: Comparsion of 2PAM transmitters

	CMOS process	Maximum output swing	Maximum data rate	Maximum loss compensation	Power consumption
[15]	0.13-μm	600mV	5Gb/s	31dB (@ 2.5GHz)	110mW
[37]	0.11-μm	800mV	3.125Gb/s	∼30dB (@1.5625GHz)	∼1W
[38]	0.18-μm	4V	13.6Gb/s	-	600mW
[20]	90-nm	700mV	4Gb/s	22dB (@ 1.25GHz)	not reported
[23]	0.13-μm	350mV	30Gb/s	not reported	150mW
[22]	0.13-μm	260mV	40Gb/s	-	∼2.7W
This work	0.13-μm	1.25V	16.25Gb/s	30.3dB (@ 8.125GHz)	1.578W

ably in terms of loss compensation, output swing, speed, and adaptability to wide range of channels with current state of the art 2PAM transmitters and drivers. The integration of all such features into one transmitter is the major contribution of this work.

6.2 Future Works

The usefulness of PWM-PE for the Belden 1694A coaxial cable channel is demonstrated in this thesis work. However, the targeted data-rate of 40Gb/s was not achieved. There exist several possibilties for future generations of this prototype design. For example, faster process in CMOS technology can be investigated. A novel circuit topology for a high-swing output driver would be necessary for CMOS implementation beyond the $0.13\mu m$ technology node in order to maintain or increase the output voltage swing. Another possible solution to further increase their speed of the CML circuits using more advanced circuit techniques such as shunt and double-series peaking [22] and active negative feedback [31]. Such circuit techniques can be used to enable higher data rates and/or higher fanout ratios between CML stages, which translates into power savings.

Adaptation for duty-cycle and output-amplitude settings in the transmitter with or without a backchannel communication from the receiver is another area for future work. The integration of the full transeiver link is an on-going project. Since just a single coefficient is required for the pre-emphasis setting, the adaptation algorithm should be much simpler than FIR implementations involving multiple tap coefficients [15].

A Square-law CML design in CMOS

The majority of published literature describing CML design is based on two main assumptions: first, MOSFETs observe a square-law voltage-current relationship in saturation; second, complete switching of the differential pair is required for proper operation [24] [25] [26] [28]. This section illustrates the approach based on these assumptions, as in the sources cited above.

As described in 2.3, the CML output differential voltage under full-switching region of operation is $\Delta V_{MAX} = I_{TAIL} \cdot R$. Generally, for high-speed operation, it is desirable to use minimum gate-lengths in all differential pair transistors. This assumption is made throughout this work. Define J as the current density of the differential pair transistors when fully-switched, given by $J = \frac{I_{TAIL}}{W}$. A CML gate is completely specified by selecting ΔV_{MAX}, W, and J; values for R and I_{TAIL} may be straightforwardly inferred. The interplay and trade-off between these parameters affect the various aspects of CML design.

First, define the differential input voltage as $\Delta V_{in} = V_{in1} - V_{in2}$ and the difference in drain currents for transistors M_1 and M_2 as $\Delta I = I_{D1} - I_{D2}$. The sum of the two drain currents is the total tail current of the CML gate, $I_{D1} + I_{D2} = I_{TAIL}$ as shown in fig. A.1. Using the circuit equation for MOSFET in saturation for M_1 and M_2:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_S - V_t)^2 \tag{A.1}$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in2} - V_S - V_t)^2 \tag{A.2}$$

Then, (A.1) and (A.2) can be re-arranged as:

$$V_{GS1} = V_{in1} - V_S = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} + V_t \tag{A.3}$$

$$V_{GS2} = V_{in2} - V_S = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}} + V_t \tag{A.4}$$

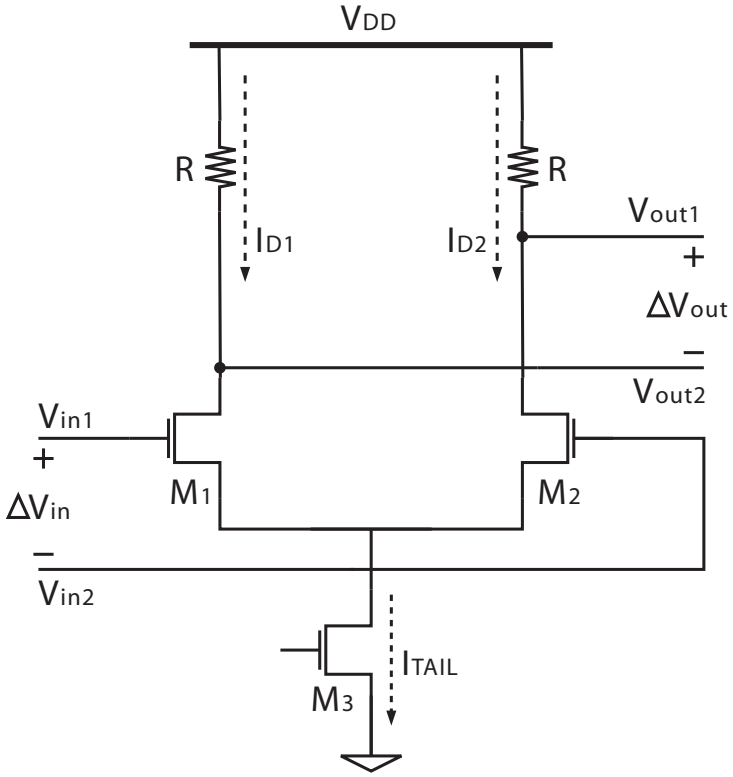


Figure A.1: Schematics of a CML buffer

The difference gives an expression for ΔV_{in},

$$\Delta V_{in} = V_{in1} - V_{in2} = V_{GS1} - V_{GS2} \tag{A.5}$$

$$\Delta V_{in} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W_1}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W_2}{L}}} \tag{A.6}$$

$${\Delta V_{in}}^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{TAIL} - 2\sqrt{I_{D1}I_{D2}}) \tag{A.7}$$

An expression for ΔI can be obtained by re-writing I_{D1} and I_{D2} in (A.7).

$$\Delta I^2 = {I_{TAIL}}^2 - (\frac{1}{2}\mu_n C_{ox}\frac{W}{L}{\Delta V_{in}}^2 - I_{TAIL})^2 \tag{A.8}$$

$$\Delta I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\Delta V_{in}\sqrt{\frac{4I_{TAIL}}{\mu_n C_{ox}\frac{W}{L}} - {\Delta V_{in}}^2} \tag{A.9}$$

This equation relates the difference in drain currents of M_1 and M_2 to the differential

input voltage ΔV_{in}. Physically it translates to switching of current to one of the differential pair devices as the differential input voltage is increased. The full-switching input voltage, $\Delta V_{in,fs}$, is achieved, then all of the tail current flows to one side of the differential pair ($\Delta I = \pm I_{TAIL}$).

$$\Delta V_{in,fs} = \sqrt{\frac{2I_{TAIL}}{\mu_n C_{ox}\frac{W}{L}}} \tag{A.10}$$

The full-switching differential input, $\Delta V_{in,fs}$, is related to the effective voltage (V_{eff}) of the differential pair transistors when they are balanced with $I_{D1} = I_{D2} = \frac{I_{TAIL}}{2}$.

$$V_{GS1} - V_t \;=\; V_{GS2} - V_t = V_{eff} \;=\; \sqrt{\frac{I_{TAIL}}{\mu_n C_{ox}\frac{W}{L}}} \tag{A.11}$$

$$\Delta V_{in,fs} = \sqrt{2} V_{eff} \tag{A.12}$$

Hence, assuming square-law behavior, the input voltage required to fully-switch a CML gate ($\Delta V_{in,fs}$) is directly related to V_{eff} at zero input, which in turn can be expressed as:

$$V_{eff} = \sqrt{\frac{L}{\mu_n C_{ox}} J} \tag{A.13}$$

So assuming a square-law MOSFET model, the full-switching voltage of a CML gate is directly proportional to its current density. Let the transconductance of the circuit be $Gm = \frac{\delta \Delta I}{\delta \Delta V_{in}}$. It is equivalent to the linearized small-signal transconductance of the differential pair devices, gm, at zero input.

$$Gm|_{\Delta V_{in}=0} = gm \;=\; \sqrt{\mu_n C_{ox}\frac{W}{L} I_{TAIL}} \tag{A.14}$$

gm can also be alternatively expressed as a function of the tail current and effective voltage:

$$gm = \frac{I_{TAIL}}{V_{eff}} \tag{A.15}$$

The conventional approach is that whenever one CML gate drives another as shown in fig. A.2, the output voltage of the first gate when fully-switched must be sufficient

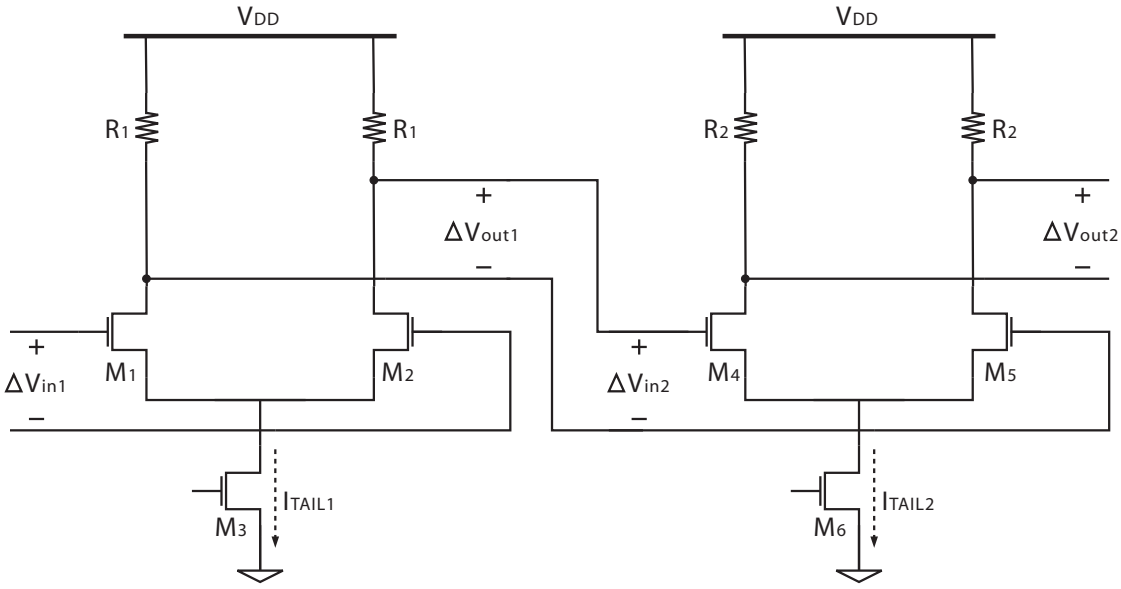


Figure A.2: Schematics of two CML buffers connected in cascade

to fully-switch the current of the second CML gate.

$$I_{TAIL1}R_1 \geq \Delta V_{in2,fs} \tag{A.16}$$

If they are biased with the same current density such that their $\Delta V_{in,fs}$ and V_{eff} are identical, then substituting (A.15) and (A.12) into (A.16) gives,

$$gm_1 V_{eff} R_1 \geq \sqrt{2} V_{eff} \tag{A.17}$$

$$gm_1 R_1 \geq \sqrt{2} \tag{A.18}$$

The left hand side of (A.18) is the small signal gain of CML stage 1, A_v, assuming the drain-source resistances are much greater than R_1. Therefore, assuming a square-law MOSFET model, in order to fully-switch each other, CML gates require a DC small-signal gain of:

$$A_v \geq \sqrt{2} \; = \; 3dB \tag{A.19}$$

Note that the small-signal gain, A_v, is determined for balanced inputs ($\Delta V_{in} = 0$).

Furthermore, according to this approach, the maximum operating frequency of a CML gate can be determined by inspecting its small-signal AC response. At high fre-

quencies the DC load R_1 in equation (A.18) is replaced by a complex load impedance and the gain, A_v, decreases. The highest operating frequency of a particular CML gate is the frequency at which its small-signal gain dips below 3dB. It is important to note that this approach assumes that all transistors are in saturation region at all times, and that their small-signal drain-source resistances are much greater than the load impedance.

In a chain of CML gates with identical output swing, in order to ensure that the devices do not enter triode region during switching, the voltage swings(ΔV_{MAX}) must be less than the threshold voltage(V_t) of the transistor [24]. Combining this condition with the full-switching requirement:

$$V_t \geq \Delta V_{MAX} \geq \Delta V_{in,fs} \tag{A.20}$$

$$V_t \geq \Delta V_{MAX} \geq \sqrt{2} V_{eff} \tag{A.21}$$

$$\frac{V_t}{\sqrt{2}} \geq V_{eff} \tag{A.22}$$

The condition imposed by (A.22) limits the effective voltage on the transistors in the CML differential pair. As the current density increases in a transistor, its V_{eff} increases, but the threshold voltage of a transistor stays more or less constant. Hence, there exists an upper limit on current density within which all differential pair devices stay within square-law region during the operations of CML circuits.

B Inductor Design

Spiral inductors with two metal layers are used throughout the design. Spiral inductors are constructed from layers 4 and 5 of the IBM CMRF8SF $0.13\mu m$ technology due to layout area considerations. Top layer metals for this particular technology requires large metal width and metal-to-metal spacing, which leads to increase in the area occupied by inductors by 400-500%. Fig. B.1 illustrates the conceptual view of a two-layer metal spiral inductor in three-dimensions. The via connection is not drawn to scale. l denotes the outer dimension of spiral, w denotes metal width of spiral, and s denotes the metal-to-metal spacing of the spiral.

The inductors were designed in the ASITIC environment. Segments at the ends of the spiral were extended by length of $\frac{l}{2}$ to better simulate the actual layout of the inductor. The s-parameters obtained from ASITIC were fitted into the $2-\pi$ model [39] in Advanced Design System (ADS) environment. The schematic used for the parameter fitting is shown in fig. B.2.

The physical parameters of the inductors are shown in table B.1. All spirals have metal-to-metal spacing of $1\mu m$. The fitted $2-\pi$ model parameters are also shown in

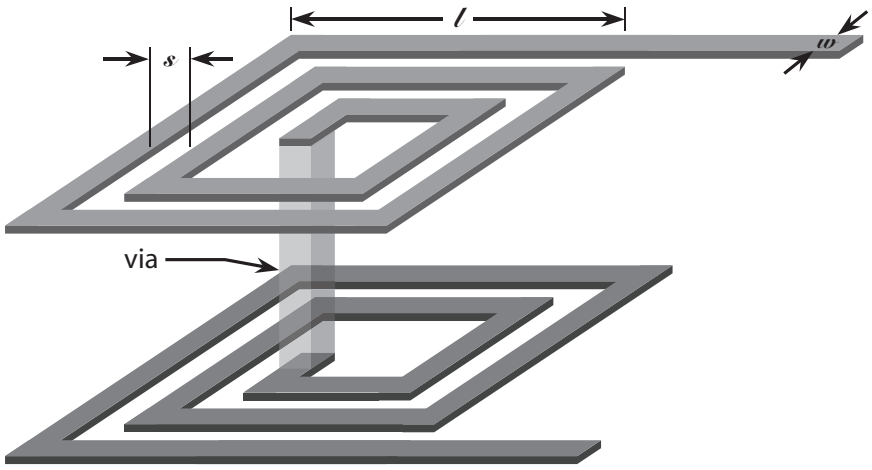


Figure B.1: Three-dimensional conceptual view of a two-layer metal spiral inductor

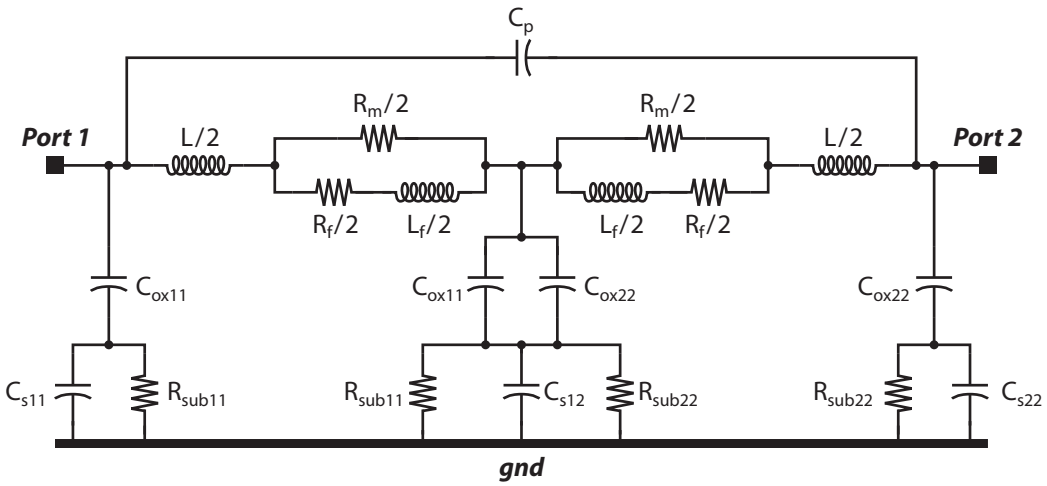


Figure B.2: Schematic of $2-\pi$ inductor model used in ADS environment

table B.1.

Table B.1: Inductor design and model parameters

Inductance		Design parameters			$2-\pi$ model parameters											
L_{target} (pH)	L_{design} (pH)	l (μm)	w (μm)	$Turns$	$\frac{L}{2}$ (pH)	$\frac{L_f}{2}$ (pH)	$\frac{R_m}{2}$ (Ω)	$\frac{R_f}{2}$ (Ω)	C_p (fF)	C_{ox11} (fF)	C_{ox22} (fF)	R_{sub11} $(k\Omega)$	R_{sub22} $(k\Omega)$	C_{s11} (fF)	C_{s22} (fF)	C_{s12} (fF)
370.0	371.4	33.5	4.7	1.75	168	96	2.431	3.231	6.183	2.732	7.307	3.561	3.104	0.200	0.200	1.728
260.0	258.0	27.7	3.6	1.5	119	57	2.394	3.216	4.033	0.825	7.450	1.837	5.528	0.297	0.541	0.665
450.0	457.7	21.8	1.6	2.25	218	78	5.873	9.516	3.359	1.264	3.518	2.993	4.103	0.489	0.664	0.735
715.7	723.9	21.5	1.1	3	344	67	14.015	12.871	3.228	0.890	4.525	1.782	8.147	2.000	0.967	0.096
206.3	206.8	17.5	2.18	2	93	48	3.186	3.764	2.588	1.000	2.741	3.376	4.269	0.200	0.309	1.345
250.8	250.8	18.5	2	2	115	51	3.746	4.674	2.608	0.452	4.803	9.454	9.339	0.484	0.481	0.706
284.3	285.4	19	1.8	2	133	55	4.162	5.975	2.637	0.978	3.158	3.287	4.645	0.246	0.483	1.181
322.3	321.9	20.2	1.8	2	152	63	4.317	6.871	2.491	1.129	2.977	3.213	4.301	0.299	0.492	1.057
385.2	382.9	19	1.5	2.5	179	59	6.500	7.486	2.749	1.109	2.957	3.104	4.310	0.400	0.571	0.949
342.8	350.0	20	1.5	2	166	58	5.317	8.354	2.637	0.387	4.952	1.314	11.415	0.200	0.409	0.851
384.9	386.1	17.8	1.2	2.5	182	49	8.038	8.782	2.182	0.713	3.338	1.901	8.492	1.260	0.745	0.354
554.0	547.1	18.8	1.1	3	257	57	12.249	10.376	2.701	0.771	3.869	1.803	8.793	2.000	0.860	0.205
477.1	485.4	18	1	2.75	229	48	11.904	10.632	2.242	0.360	4.590	1.311	15.518	0.516	0.451	0.789
568.7	572.6	18.2	0.9	3	272	54	14.156	13.255	2.774	0.431	4.524	1.374	12.702	0.661	0.552	0.634
644.5	638.8	19.2	0.9	3	305	57	15.154	14.233	2.405	0.482	4.663	1.389	14.985	0.791	0.603	0.559
675.5	679.3	19.8	0.9	3	325	57	15.663	14.900	2.601	0.906	3.748	1.946	8.140	2.000	0.977	0.085
770.4	772.2	18.9	0.8	3.25	371	61	18.012	17.652	2.463	1.005	3.013	2.326	6.339	1.661	1.028	0.070
871.7	871.0	18.3	0.6	3.5	425	46	25.105	24.756	2.382	1.282	2.206	3.499	4.153	1.376	1.100	0.018
1105.6	1105.0	20.5	0.8	4	534	75	23.025	22.105	3.366	1.476	2.915	3.345	3.890	1.366	1.130	0.025
1021.4	1025.0	19.8	0.8	4	494	75	21.947	21.105	3.092	1.388	2.769	3.278	4.052	1.401	1.116	0.020
1106.4	1105.0	21.5	0.8	4	594	72	24.541	23.556	3.380	1.619	2.994	3.468	3.767	1.354	1.156	0.010

References

[1] Peter Park. 40Gb/s 4PAM receiver. Master's thesis, University of Toronto, 2008.

[2] John R. Barry, Edward A. Lee, and David G. Messerschmitt. *Digital Communication*. Kluwer Academic Publishers, third edition, 2003.

[3] A. Ho, V. Stojanovic, F. Chen, C. Werner, G. Tsang, E. Alon, R. Kollipara, J. Zerbe, and M. Horowitz. Common-mode backchannel signaling system for differential high-speed links. *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pages 352–355, 2004.

[4] C. Menolfi, T. Toifl, R. Reutemann, M. Ruegg, P. Buchmann, M. Kossel, T. Morf, and M. Schmatz. A 25Gb/s PAM4 transmitter in 90nm CMOS SOI. *Proceedings of the 2005 International Solid State Circuits Conference (ISSCC)*, pages 77–78, 2005.

[5] A. Amirkhany, A. Abbasfar, J. Savoj, M. Jeeradit, B. Garlepp, V. Stojanovic, and M. Horowitz. A 24Gb/s software programmable multi-channel transmitter. *VLSI Circuits, 2007. Digest of Technical Papers. 2007 Symposium on*, pages 38–39, 2007.

[6] C.H. LIN and C.H. TSAI. Multi-gigabit pre-emphasis design and analysis for serial link. *IEICE Transactions on Electronics*, E88-C(10):2009–2019, 2005.

[7] Chih-Hsien Lin, Chang-Hsiao Tsai, Chih-Ning Chen, and Shyh-Jye Jou. 4/2 PAM serial link transmitter with tunable pre-emphasis. *Proceedings of the 2004 International Symposium on Circuits and Systems (ISCAS)*, 1:952–955, 2004.

[8] Ramin Farjad-Rad, Chih-Kong Ken Yang, Mark A. Horowitz, and Thomas H. Lee. A 0.4-μm CMOS 10-Gb/s 4-PAM pre-emphasis serial link transmitter. *IEEE Journal of Solid-State Circuits*, 34(5):580–585, May 1999.

[9] Ramin Farjad-Rad, Chih-Kong Ken Yang, and Mark A. Horowitz. A 0.3-μm CMOS 8-Gb/s 4-PAM serial link transceiver. *IEEE Journal of Solid-State Circuits*, 35(5):757–764, May 2000.

[10] J.T. Stonick, G.Y. Wei, J.L. Sonntag, and D.K. Weinlader. An adaptive PAM-4 5-Gb/s backplane transceiver in 0.25-/mum CMOS. *IEEE Journal of Solid-State Circuits*, 38(3):436–443, March 2003.

[11] J.L. Zerbe, C.W. Werner, V. Stojanovic, F. Chen, J. Wei, G. Tsang, D. Kim, W.F. Stonecypher, A. Ho, T.P. Thrush, et al. Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell. *IEEE Journal of Solid-State Circuits*, 38(12):2121–2130, December 2003.

[12] V. Stojanovic, A. Ho, B.W. Garlepp, F. Chen, J. Wei, G. Tsang, E. Alon, R.T. Kollipara, C.W. Werner, J.L. Zerbe, et al. Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery. *IEEE Journal of Solid-State Circuits*, 40(4):1012–1026, April 2005.

[13] Belden Wire and Cable Company. *1694A Coax - Low Loss Serial Digital Coax.*

[14] Howard W. Johnson and Martin Graham. *High Speed Signal Propagation: Advanced Black Magic.* Prentice Hall PTR, 2003.

[15] Jan-Rutger Schrader, Eric A. M. Klumperink, Jan L. Visschers, and Bram Nauta. Pulse-width modulation pre-emphasis applied in a wireline transmitter, achieving 33dB loss compensation at 5-Gb/s in 0.13-μm CMOS. *IEEE Journal of Solid-State Circuits*, 41(4):990–999, April 2006.

[16] Miao Li, T. Kwasniewski, Shoujun Wang, and Yuming Tao. FIR filter optimization as preemphasis of high-speed backplane data transmission. *Proceedings of the 2004 International Symposium on Circuits and Systems (ISCAS)*, 2:773–776, 2004.

[17] M. Horowitz, C.K.K. Yang, and S. Sidiropoulos. High-speed electrical signaling: overview and limitations. *Micro, IEEE*, 18(1):12–24, 1998.

[18] W.J. Dally and J. Poulton. Transmitter equalization for 4-Gbps signaling. *Micro, IEEE*, 17(1):48–56, 1997.

[19] J.H.R. Schrader, E.A.M. Klumperink, J.L. Visschers, and B. Nauta. CMOS transmitter using pulse-width modulation pre-emphasis achieving 33dB loss compensation at 5-Gb/s. *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on*, pages 388–391, 2005.

[20] J.H.R. Schrader, E.A.M. Klumperink, and B. Nauta. Wireline equalization using pulse-width modulation. *Proceedings of 2006 Custom Integrated Circuits Conference (CICC)*, pages 591–598, 2006.

[21] Jaeha Kim, Jeong-Kyoum Kim, Bong-Joon Lee, Namhoon Kim, Deog-Kyoon Jeong, and Wonchan Kim. A 20-GHz phase-locked loop for 40-Gb/s serializing transmitter in 0.13-μm CMOS. *IEEE Journal of Solid-State Circuits*, 41(4):899–908, April 2006.

[22] Jaeha Kim, Jeong-Kyoum Kim, Bong-Joon Lee, Moon-Sang Hwang, Hyung-Rok Lee, Sang-Hyun Lee, Namhoon Kim, Deog-Kyoon Jeong, and Wonchan Kim. Circuit techniques for a 40-Gb/s transmitter in 0.13-μm CMOS. *Proceedings of the 2005 International Solid State Circuits Conference (ISSCC)*, pages 150–151, 2005.

[23] Paul Westergaard, Timothy O. Dickson, and Sorin P. Voinigescu. A 1.5-V, 20/30-Gb/s CMOS backplane driver with digital pre-emphasis. *Proceedings of 2004 Custom Integrated Circuits Conference (CICC)*, pages 23–26, 2004.

[24] P. Heydari and R. Mohanavelu. Design of ultrahigh-speed low-voltage CMOS CML buffers and latches. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 12(10):1081–1093, 2004.

[25] P. Heydari and R. Mohavavelu. Design of ultra high-speed CMOS CML buffers and latches. *Proceedings of the 2003 International Symposium on Circuits and Systems (ISCAS)*, 2:208–211, 2003.

[26] Michael M. Green and Ullas Singh. Design of CMOS cml circuits for high-speed broadband communications. *Proceedings of the 2003 International Symposium on Circuits and Systems (ISCAS)*, pages 204–207, 2003.

[27] Timothy O. Dickson, Kenneth H. K. Yau, Theodoros Chalvatzis, Alain M. Mangan, Ekaterina Laskin, Rudy Beerkens, Paul Westergaard, Mihai Tazlauanu, Ming-Ta Yang, and Sorin P. Voinigescu. The invariance of characteristic current densities in nanoscale MOSFETs and its impact on algorithmic design methodologies and design porting of si(ge) (Bi)CMOS high-speed building blocks. *IEEE Journal of Solid-State Circuits*, 41(8):1830–1845, August 2006.

[28] John Rogers, Calvin Plett, and Foster Dai. *Integrated Circuit Design for High-Speed Frequency Synthesis*. Artech House, 2006.

[29] Yuyu Liu, Jinguo Quan, Huazhong Yang, and Hui Wang. MOS current mode logic circuits: Design consideration in high-speed low-power applications and its future trend, a tutorial. *International Journal of High Speed Electronics and Systems*, 15(3):599–614, 2005.

[30] Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee. Bandwidth extension in CMOS with optimized on-chip inductors. *IEEE Journal of Solid-State Circuits*, 35(3):346–355, March 2000.

[31] Sherif Galal and Behzad Razavi. 10-Gb/s limiting amplifier and laser/modulator driver in 0.18-/*mum* CMOS technology. *IEEE Journal of Solid-State Circuits*, 38(12):2138–2146, December 2003.

[32] Ekaterina Laskin. On-chip self-test circuit blocks for high-speed applications. Master's thesis, University of Toronto, 2006.

[33] E. Sackinger and W.C. Fischer. A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receivers. *IEEE Journal of Solid-State Circuits*, 35(12):1884–1888, December 2000.

[34] T.C. Kuo and B. Lusignan. A 1.5 W class-F RF power amplifier in 0.2 μm CMOS technology. *Proceedings of the 2001 International Solid State Circuits Conference (ISSCC)*, pages 154–155, 2001.

[35] A.-J. Annema, G.J.G.M. Geelen, and P.C. de Jong. 5.5-V I/O in a 2.5-V 0.25-μm CMOS technology. *IEEE Journal of Solid-State Circuits*, 36(3):528–538, March 2001.

[36] Kamran Farzan and David A. Johns. A CMOS 10-Gb/s power-efficient 4-PAM transmitter. *IEEE Journal of Solid-State Circuits*, 39(3):529–532, March 2004.

[37] W. Gai, Y. Hidaka, Y. Koyanagi, J.H. Jiang, H. Osone, and T. Horie. A 4-channel 3.125 Gb/s/ch CMOS transceiver with 30dB equalization. *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pages 138–141, 2004.

[38] D.U. Li and C.M. Tsai. 10-13.6 Gbit/s 0.18μm CMOS modulator drivers with 8 Vpp differential output swing. *Electronics Letters*, 41(11):643–644, 2005.

[39] Yu Cao, Rober A. Groves, Xuejue Huang, Noah D. Zamdmer, Jean-Olivier Plouchart, Richard A. Wachnik, Tsu-Jae King, and Chenming Hu. Frequency-independent equivalent-circuit model for on-chip spiral inductors. *IEEE Journal of Solid-State Circuits*, 38(3):419–426, March 2003.