14 Gb/s AC Coupled Receiver in 90 nm CMOS

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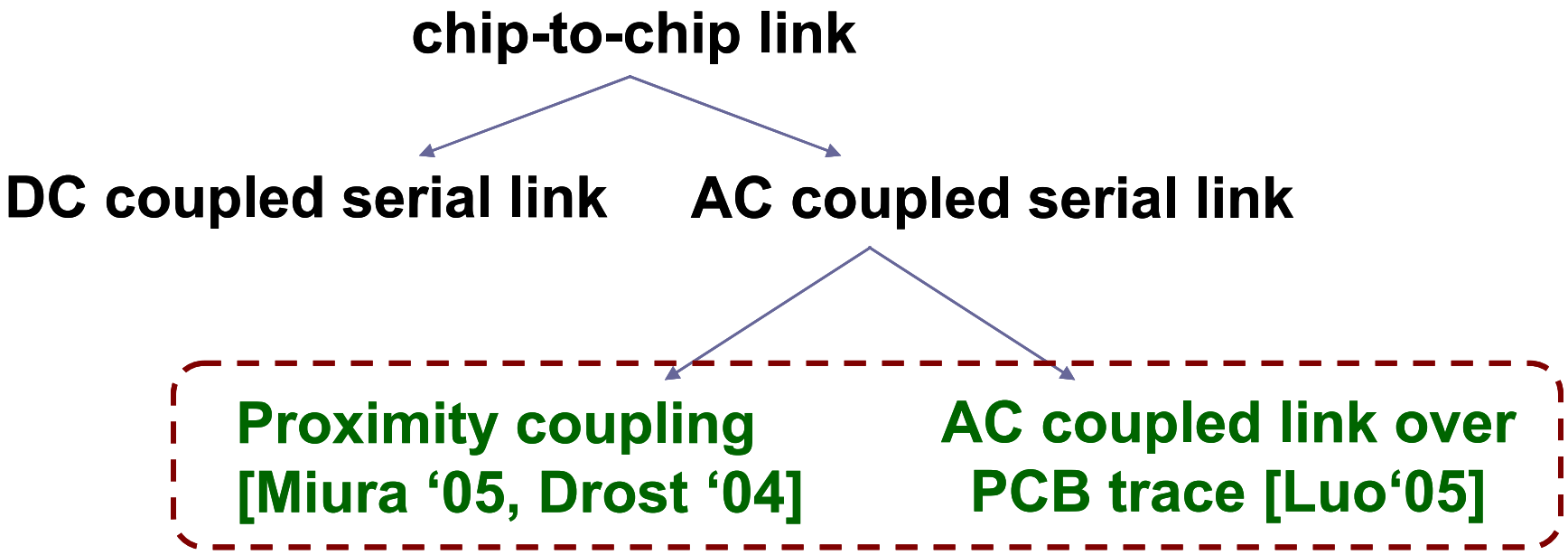
OUTLINE

- **Chip-to-Chip link overview**
- **AC interconnects**
  - Link modelling
  - ISI & sensitivity
- **AC Receiver architecture**
  - Implementation in 0.18 um CMOS
  - Measured results
- **Speed and sensitivity improvement techniques**
  - Implementation in 90nm CMOS
  - Measured results
- **Conclusion**

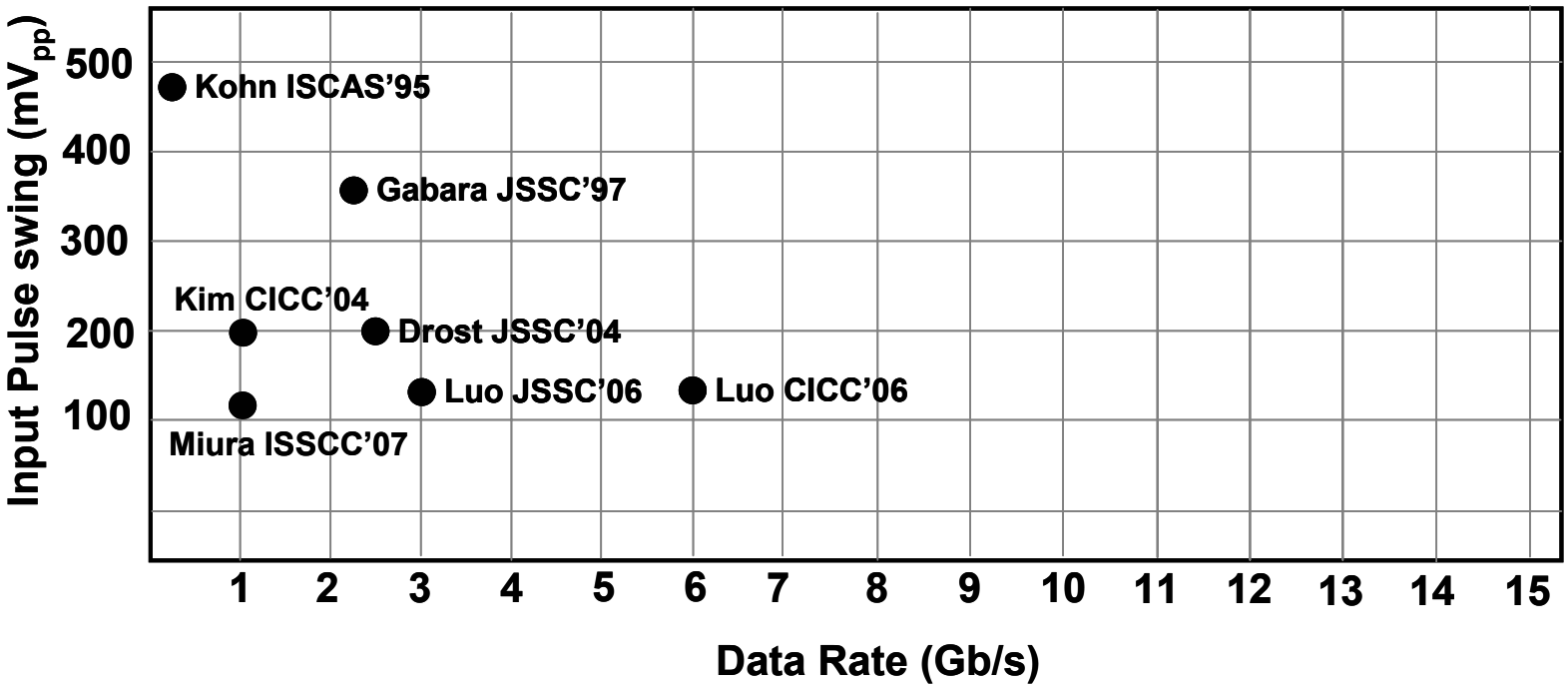
Chip-to-Chip Link Overview



Goals :

- Achieve high speed
- Small area : small coupling capacitor
- High sensitivity
- Achieve good FOM mW/Gb/s

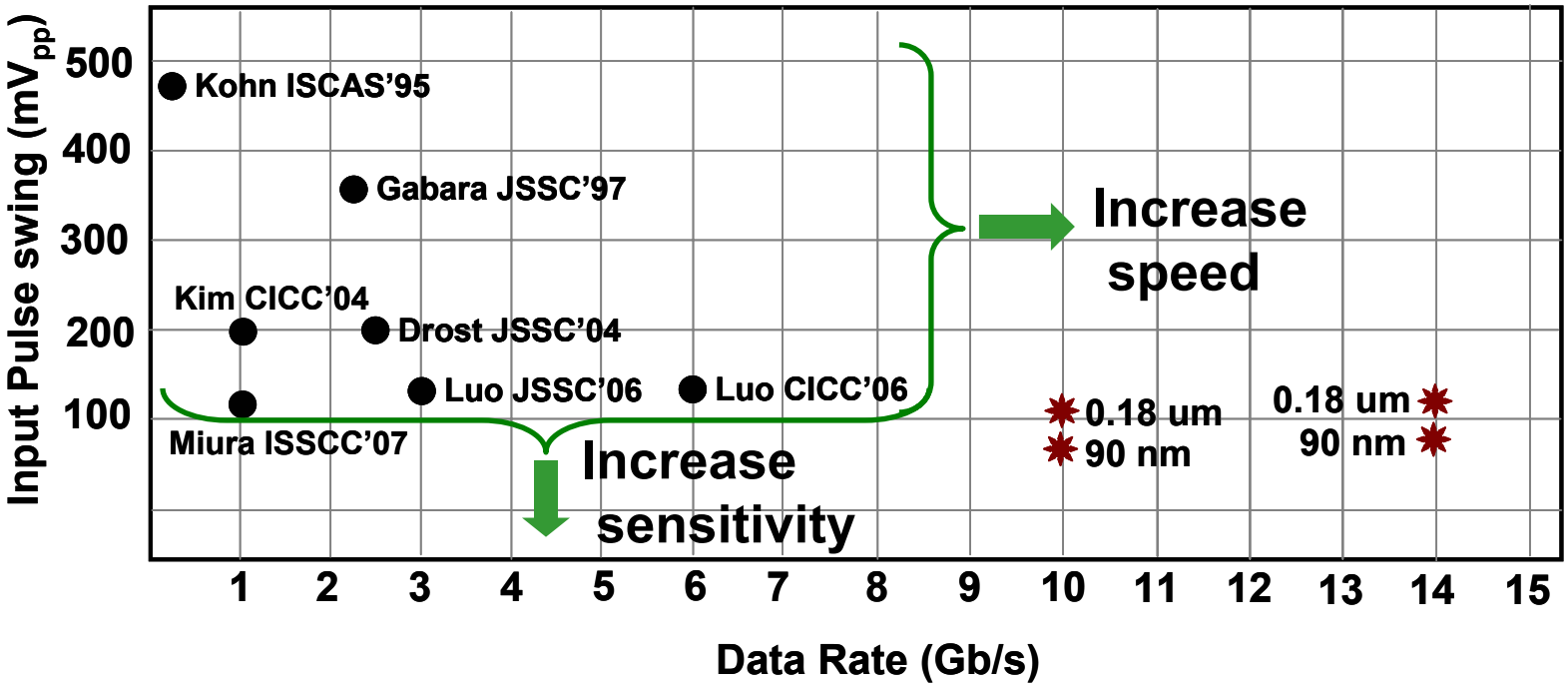
AC Coupled Link Overview



- ✓ Achieves high density
- ✓ 3-D Integration is possible
- ✓ All NMOS I/O driver
  1. Multi-standard integration
  2. Compatible common mode
  3. DC offset immune

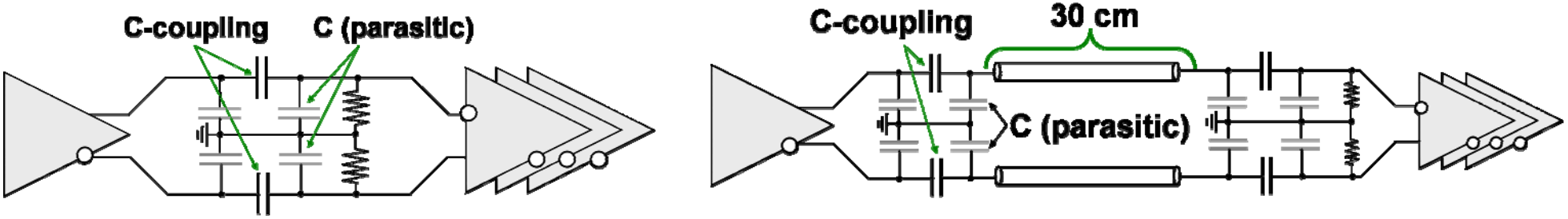
- ✖ Low speed
- ✖ Complexity increases
- ✖ Have poor FOM mW/Gb/s >10 mW/Gb/s

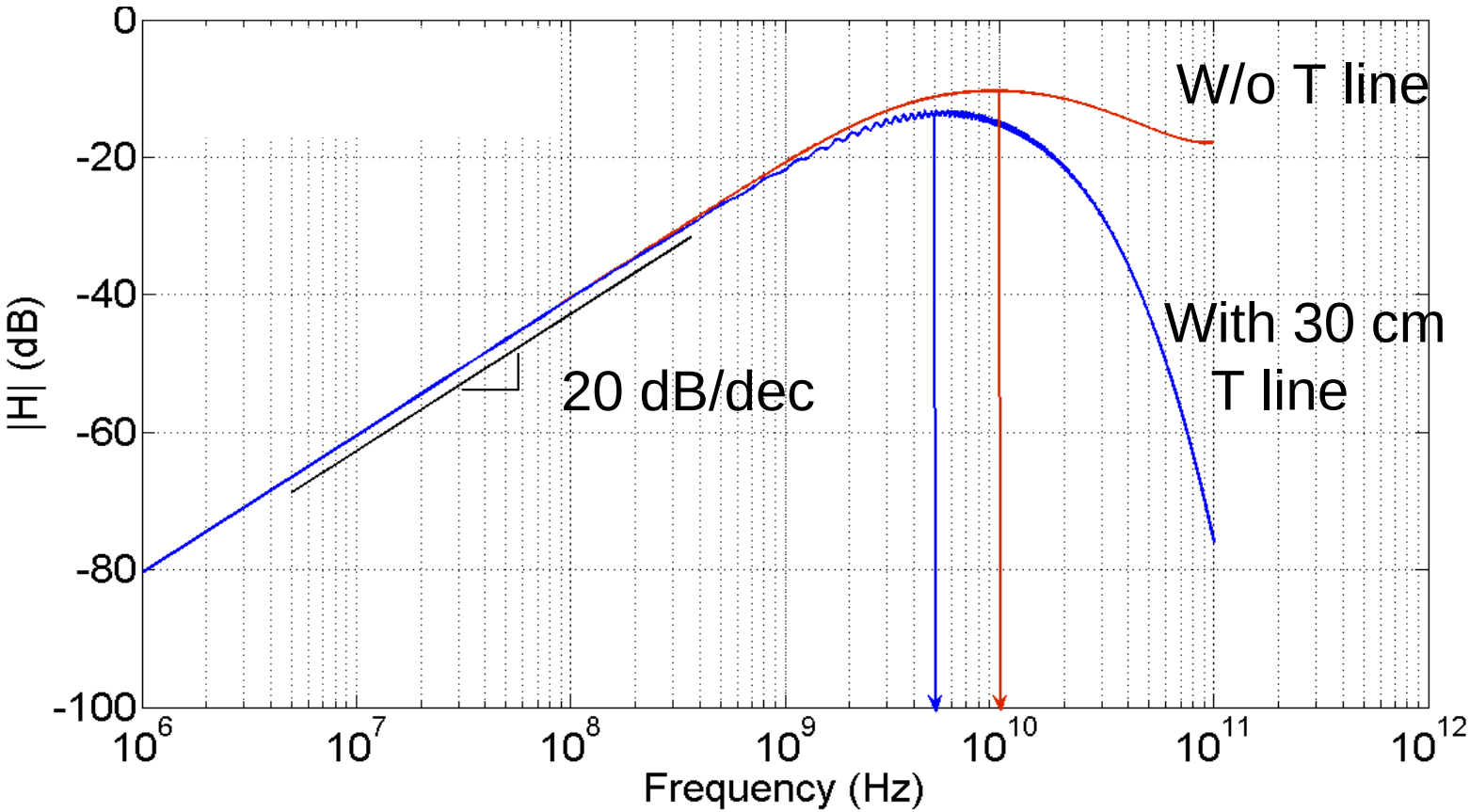
AC Coupled Link Overview



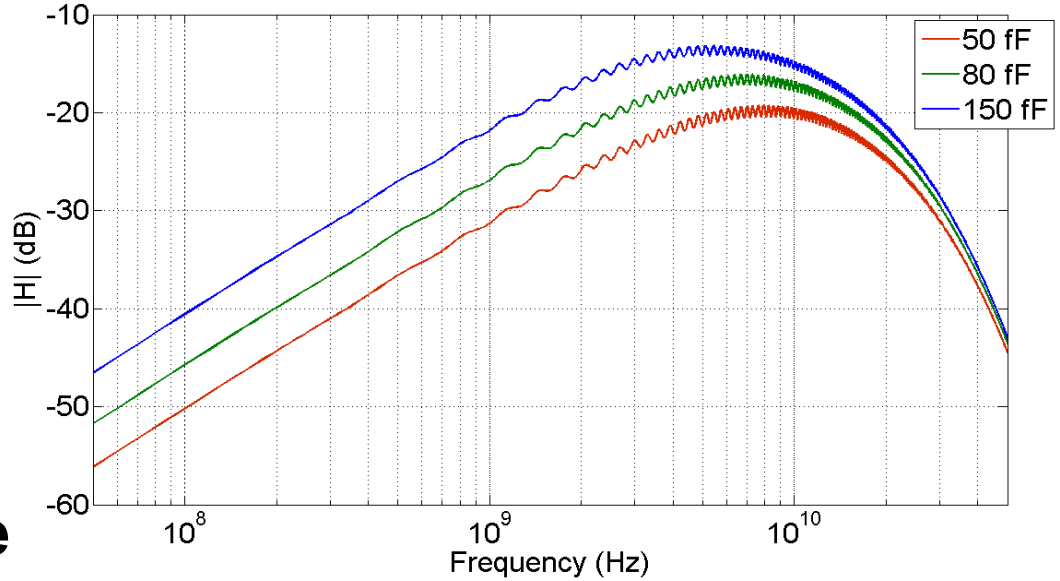
Our goal is to increase both sensitivity and speed using standard CMOS process

AC Coupled Link Modeling

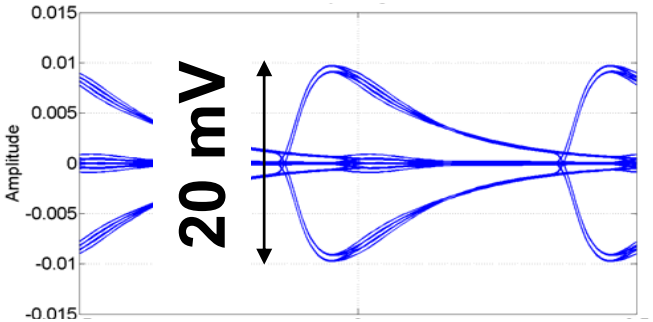




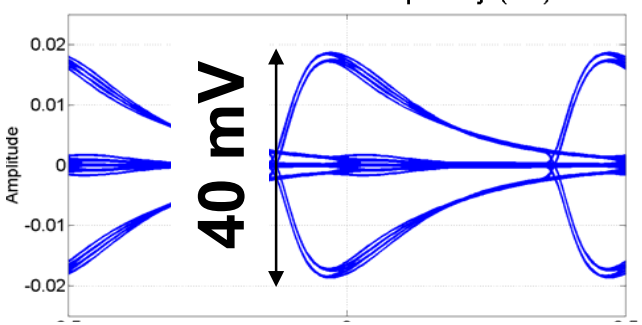
ISI & Rx Sensitivity



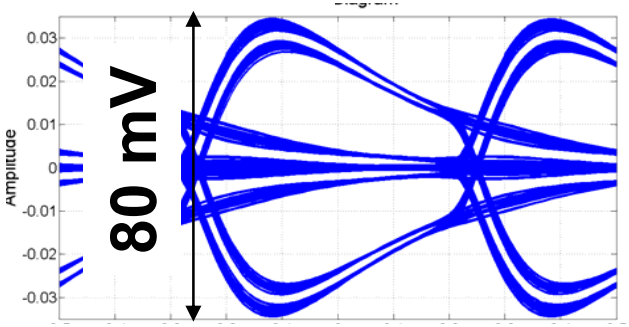
14 Gb/s input eye



C = 50 fF



C = 80 fF

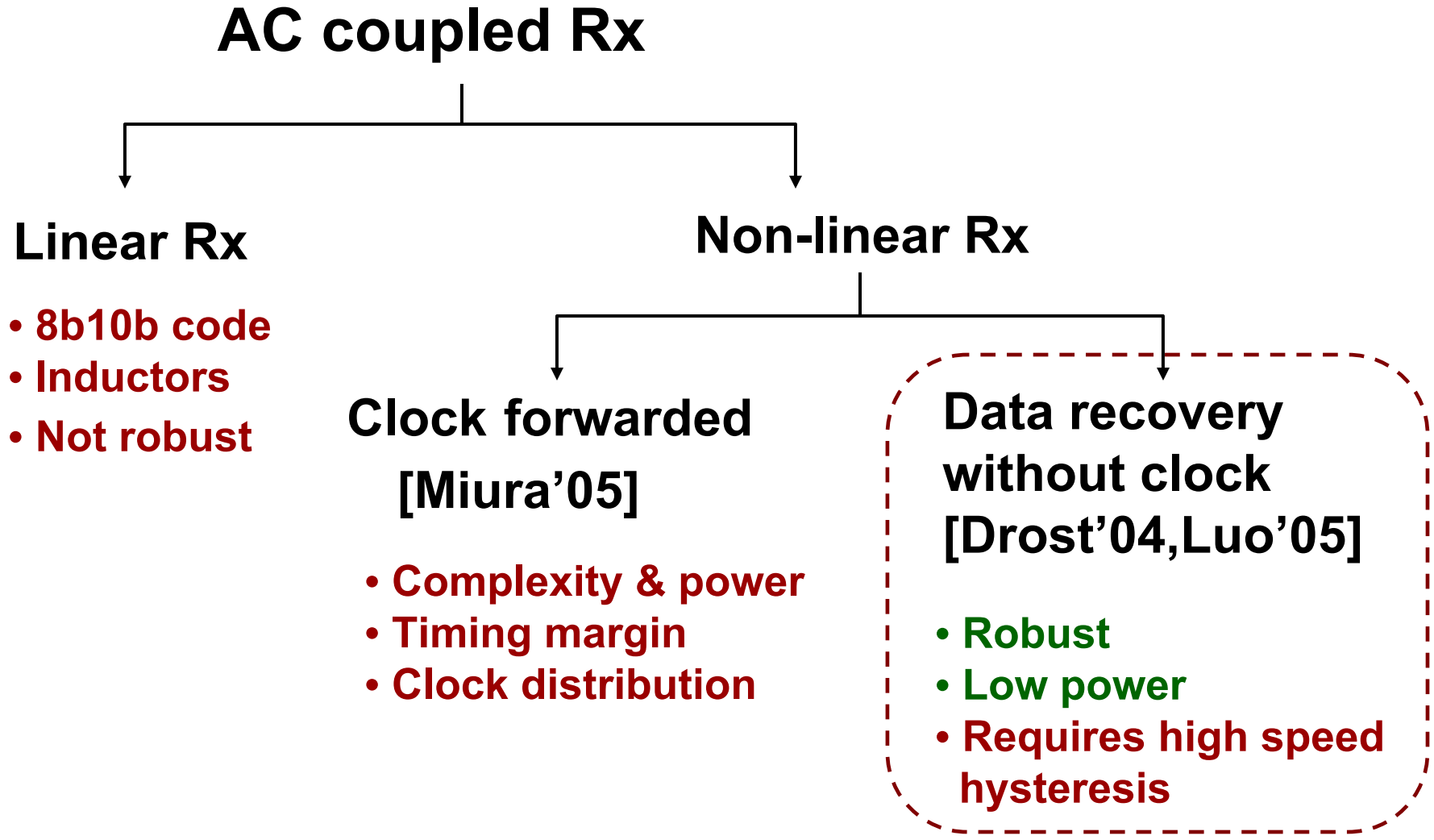


C = 150 fF

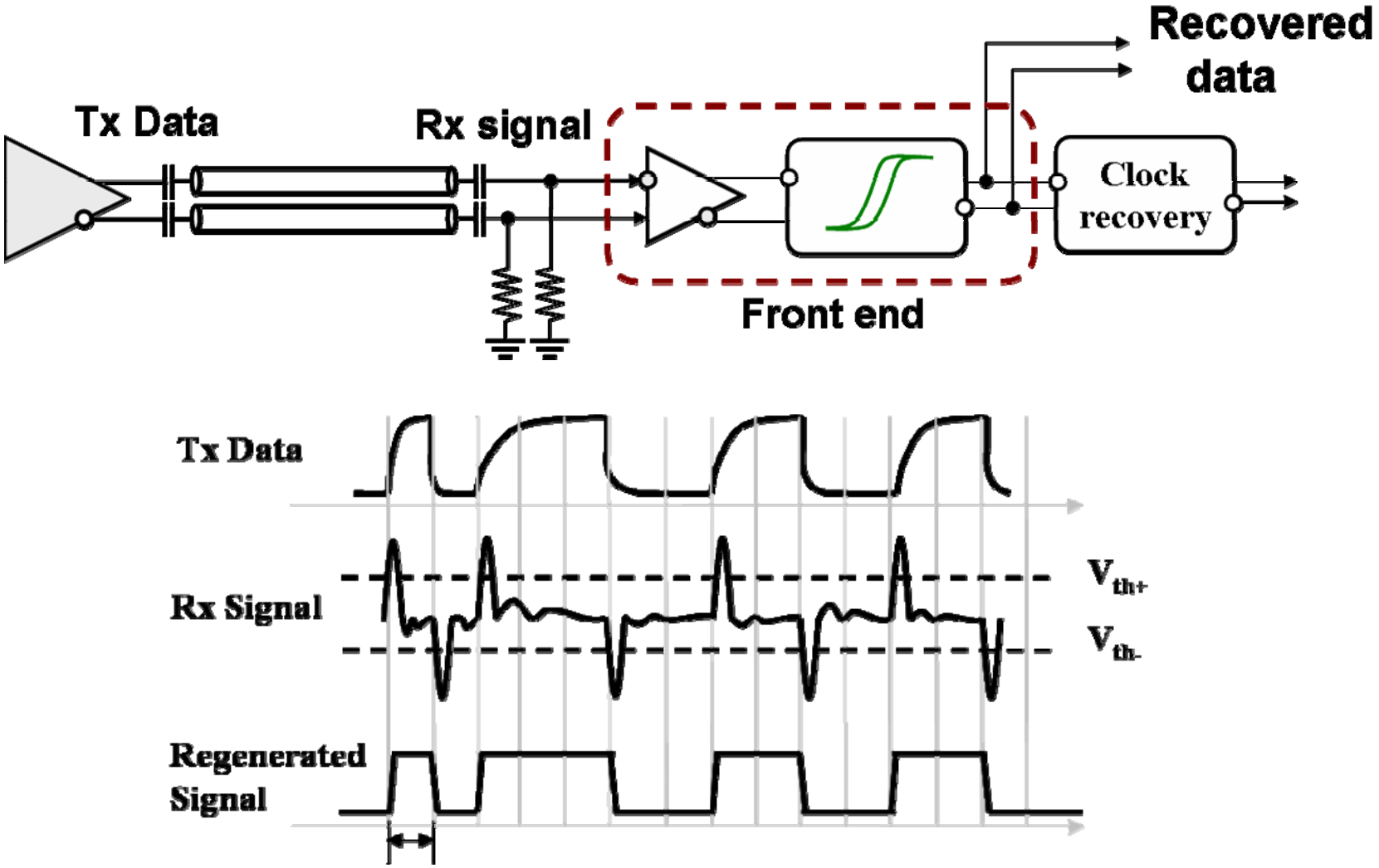
Coupling capacitor ⬆ area ⬆ ISI ⬆ sensitivity requirement ⬇

Coupling capacitor ⬇ area ⬇ ISI ⬇ sensitivity requirement ⬆

Rx Architecture

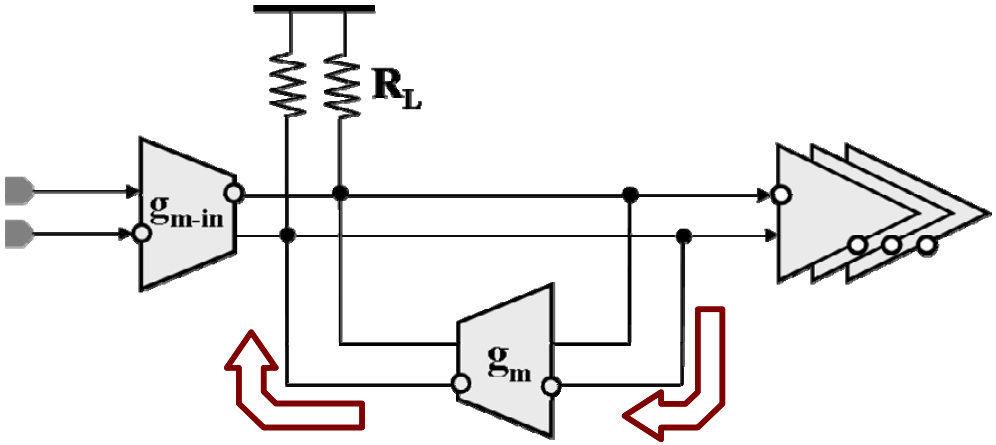


Non-linear Clock less Rx

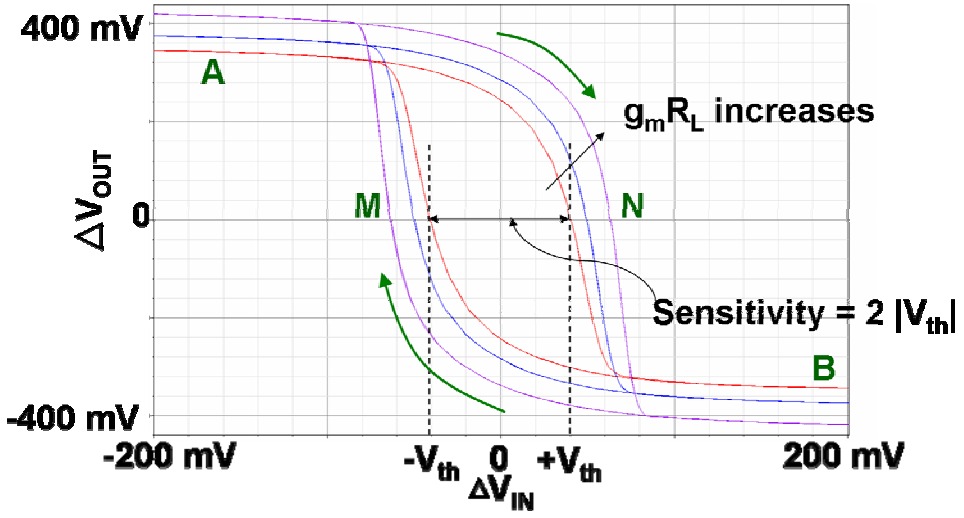


Hysteresis – Regenerates data from the transitions

Hysteresis Architecture



Positive feedback



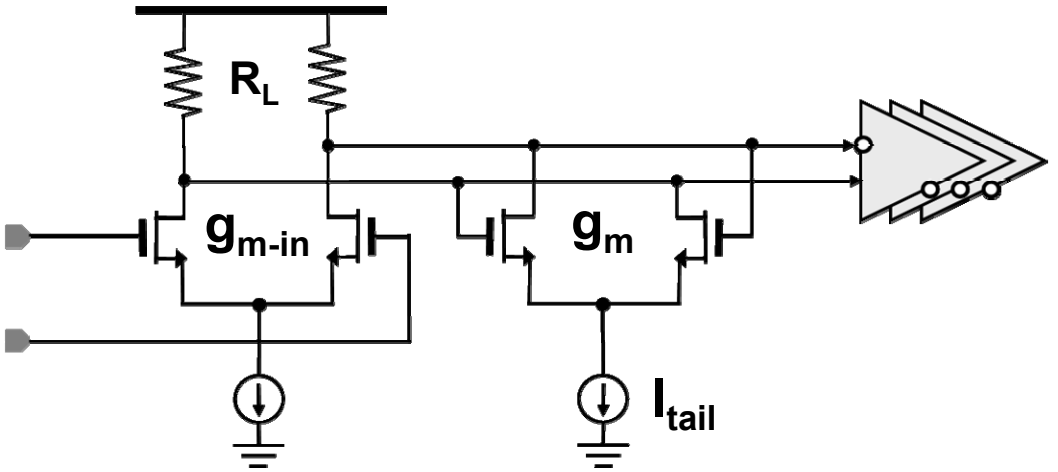
- **Hysteresis Condition : $g_mR_L > 1$**
- **Unstable points : M,N (large gain g_mR_L)**
- **Bi-Stable points : A,B (non-linear gain)**

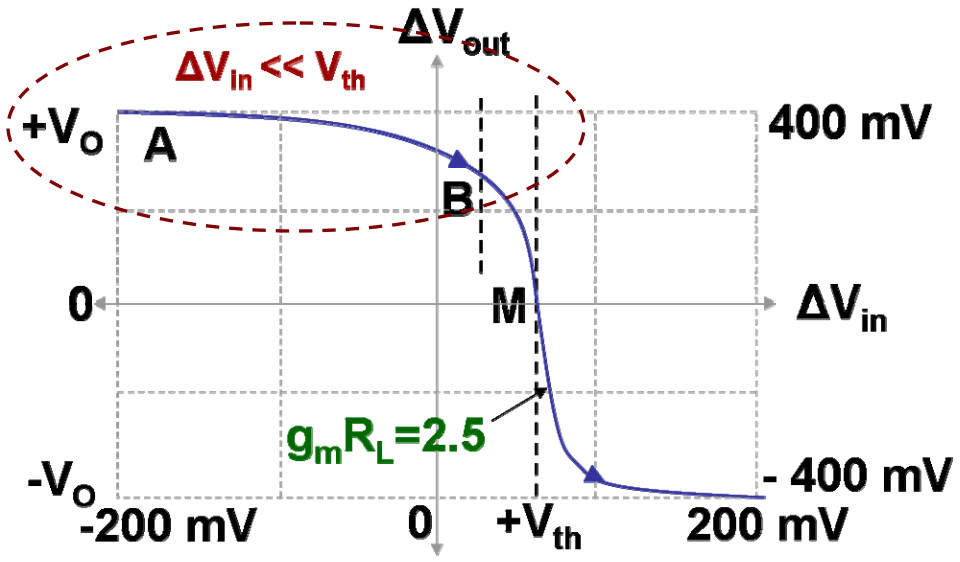
Hysteresis Analysis

Latch Mode

$\Delta V_{in} << V_{th}$

[A-B]





$$v_{out}(t) = +I_{tail}R_L - v_{in}(t)g_{m-in}R_L$$

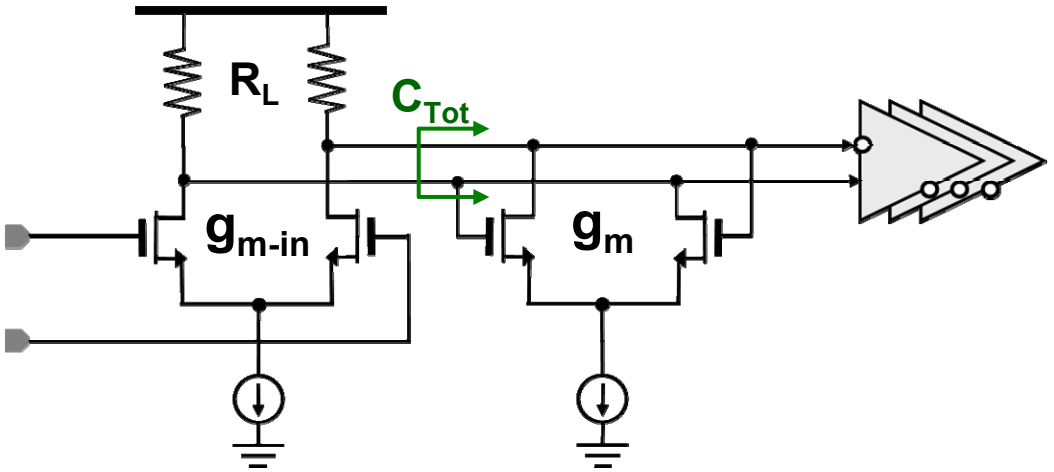
$$V_{in}(t) << V_{th} \qquad v_{out}(t) \approx +V_0$$

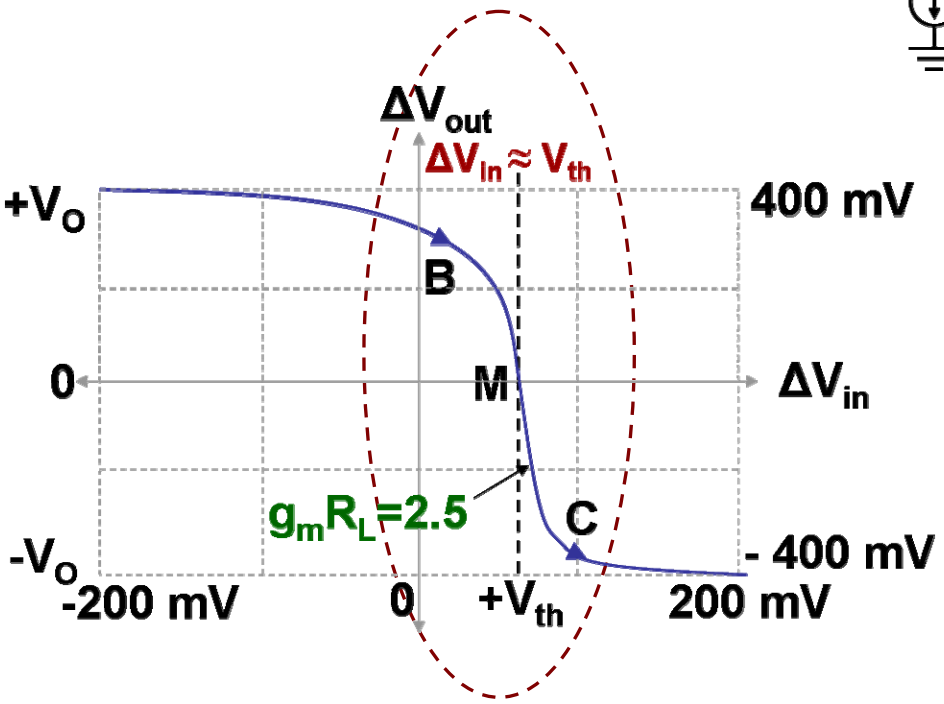
$$V_{in}(t) \approx V_{th} \quad v_{out}(t) \approx 0$$

$$\text{sensitivity} \Rightarrow 2|V_{th}| = \frac{2g_m}{g_{m-in}}|V_o|$$

Hysteresis Analysis

Switching Mode
$\Delta V_{in} \approx V_{th}$
[B-C]





$$v_0(t) = \underbrace{-V_0\, exp\left(\frac{t}{\tau_{settle}}\right)}_{\text{exponential}} \underbrace{- Kv_{in}(t)}_{\text{Linear}}$$

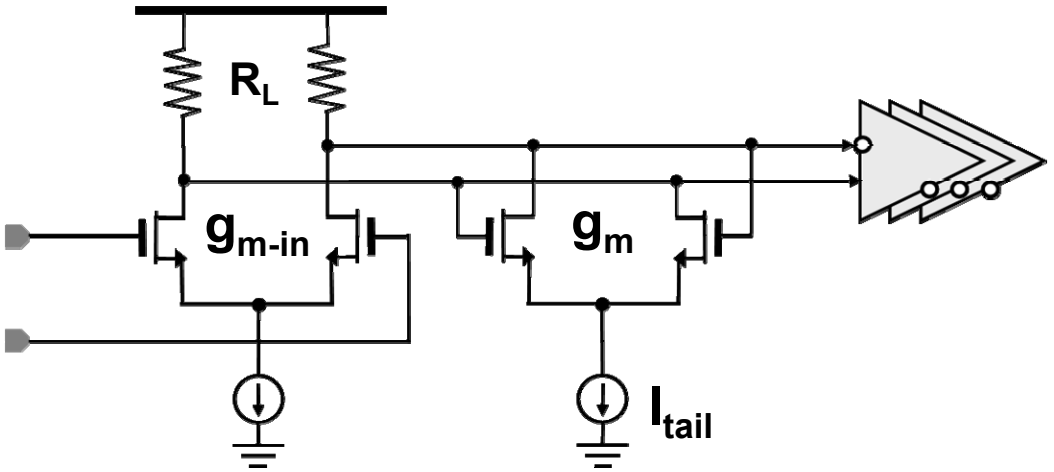
$$K = \frac{g_{m-in}R_L}{g_m R_L - 1} \qquad \tau_{settle} = \frac{R_L C_{Tot}}{g_m R_L - 1}$$

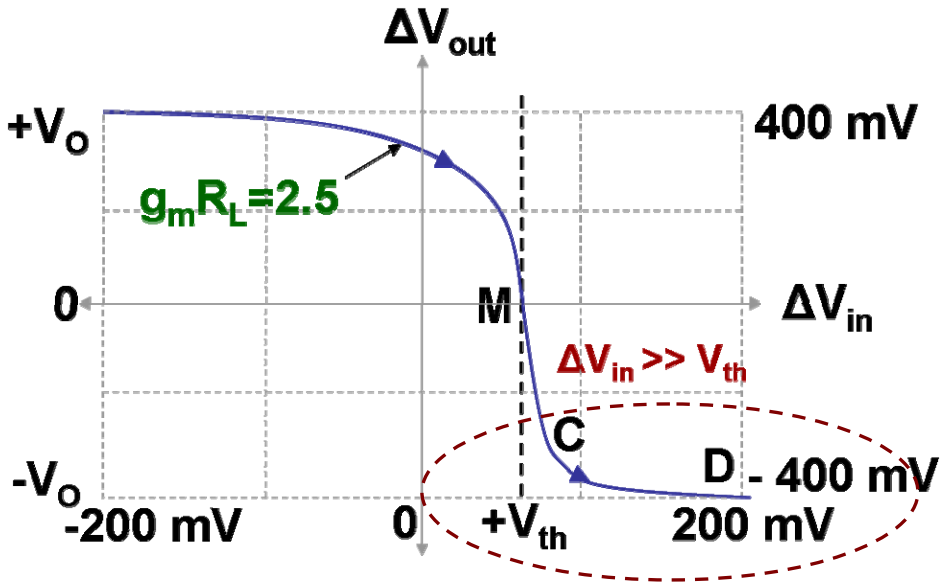
Hysteresis Analysis

Latch Mode

$\Delta V_{in} >> V_{th}$

[C-D]

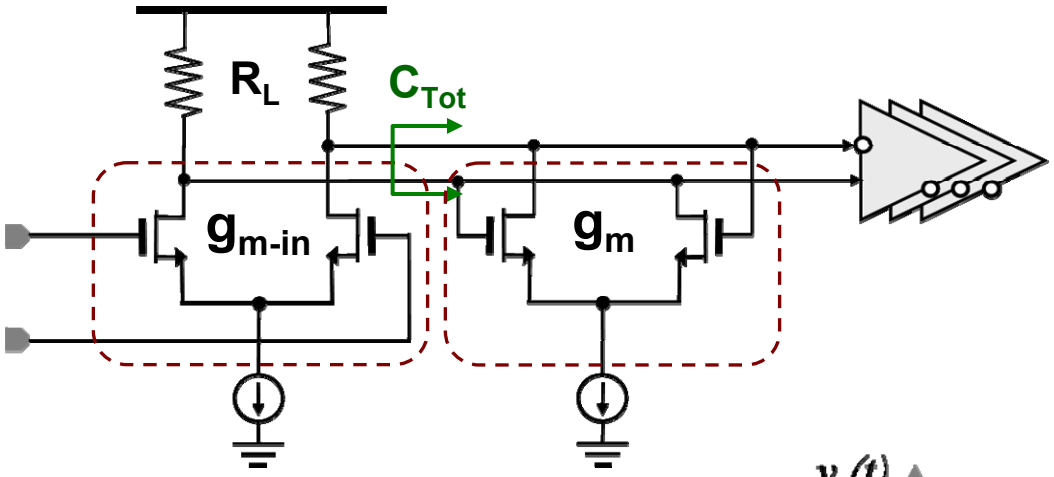


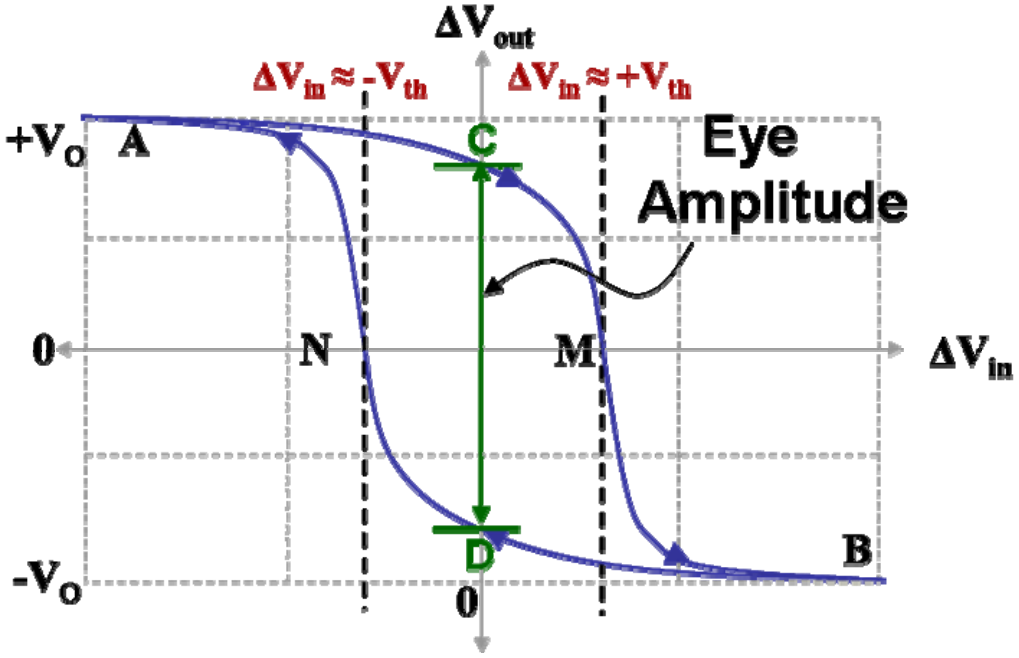


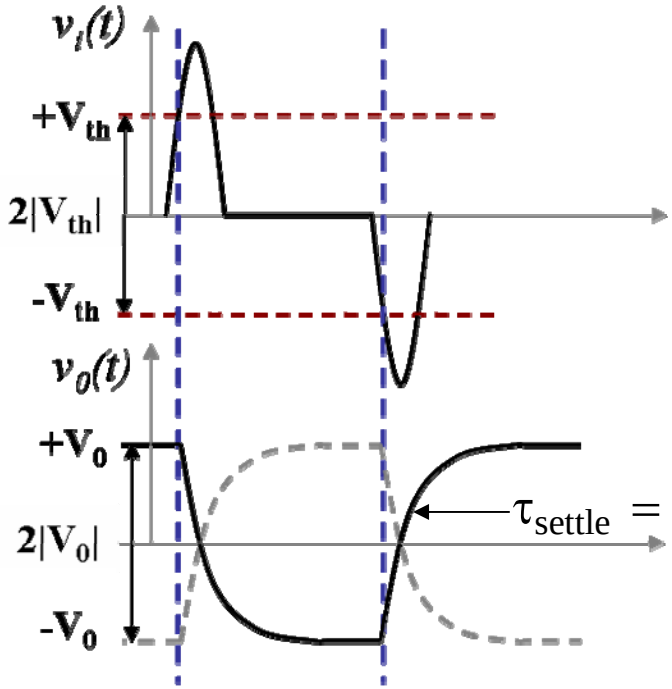
$$v_{out}(t) = -I_{tail}R_L - v_{in}(t)g_{m-in}R_L$$

$$v_{in}(t) >> V_{th} \qquad v_{out}(t) \approx -V_0$$

Hysteresis Architecture

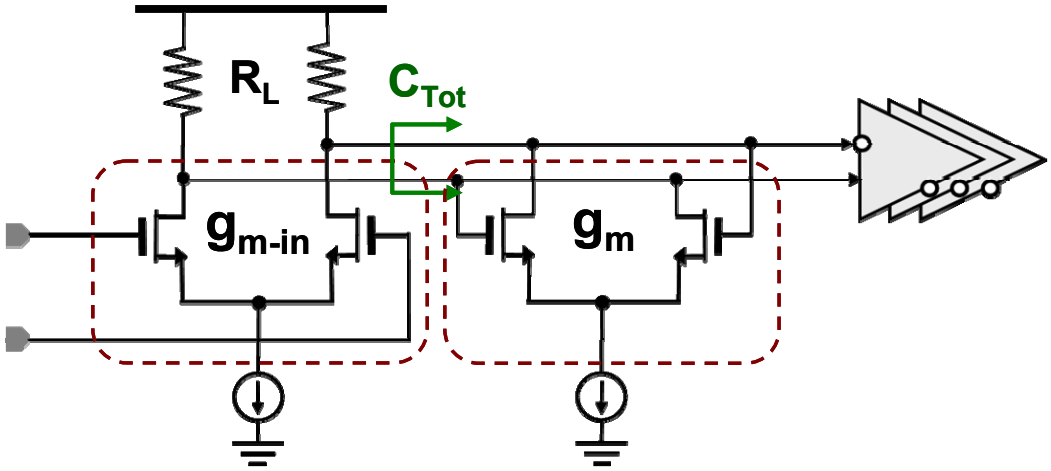






$$\tau_{settle} = \frac{R_L C_{Tot}}{g_m R_L - 1}$$

Hysteresis Design Consideration

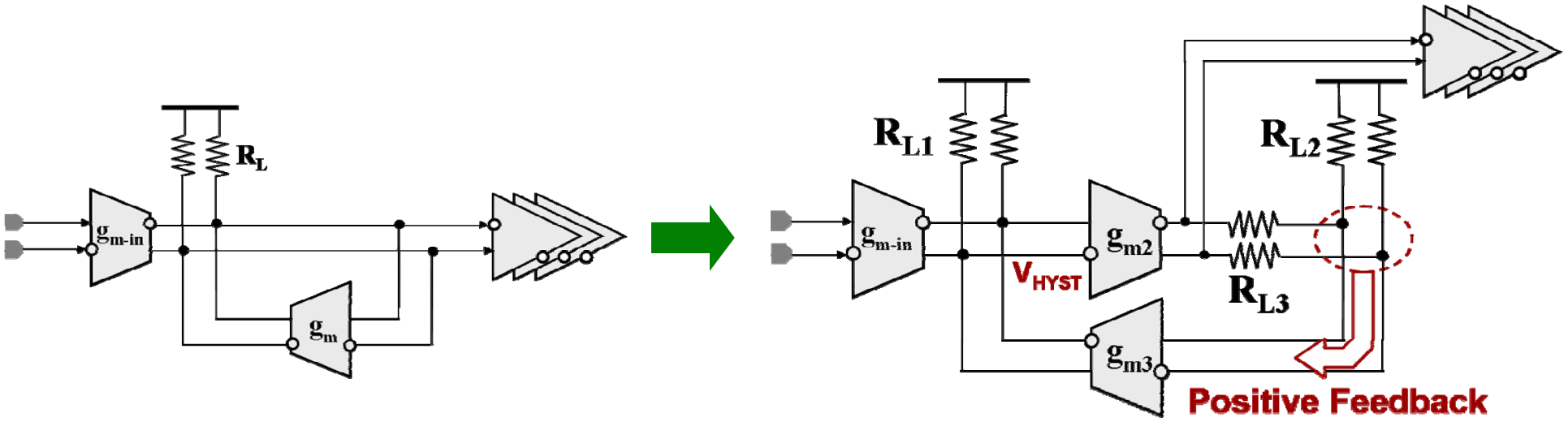


- **Speed Improvement** $\tau_{settle} = \dfrac{R_L C_{Tot}}{g_m R_L - 1}$

- **Increase $g_m R_L$** →
  - **Increase C_{Tot}**
  - **Increase power consumption**

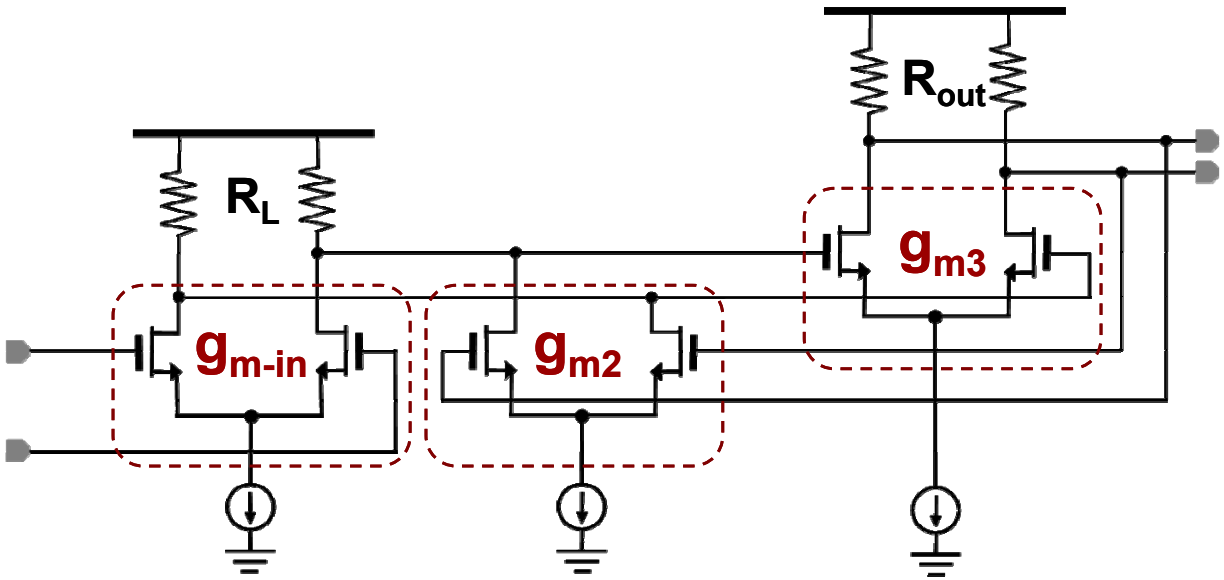
- **Reduce C_{Tot}**

Improved Hysteresis Architecture



- Condition for hysteresis : $(g_{m2}R_{L2})(g_{m3}R_{L1}) > 1$
- g_{m2} buffers node V_{HYST} from capacitive loading
- R_{L2} , R_{L3} distributes the output capacitance

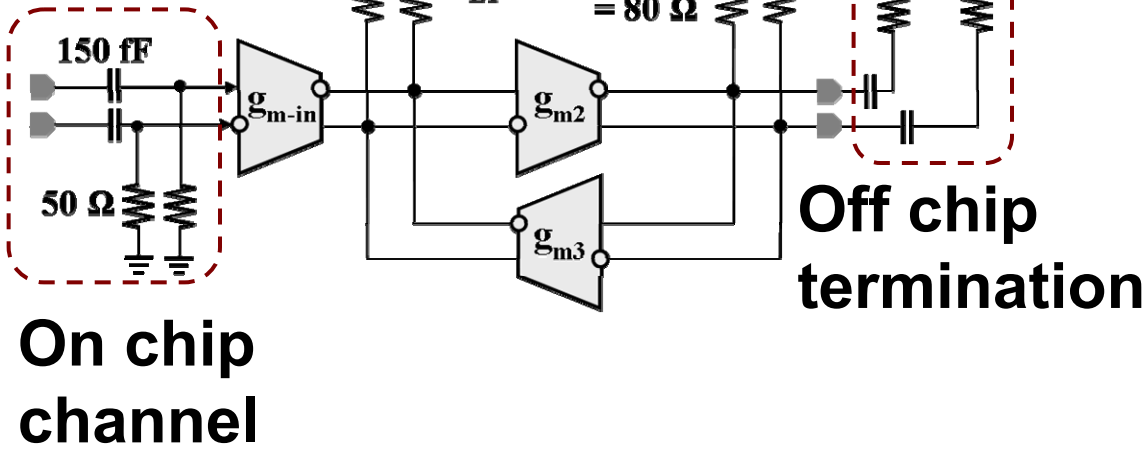
10+ Gb/s Hysteresis Design

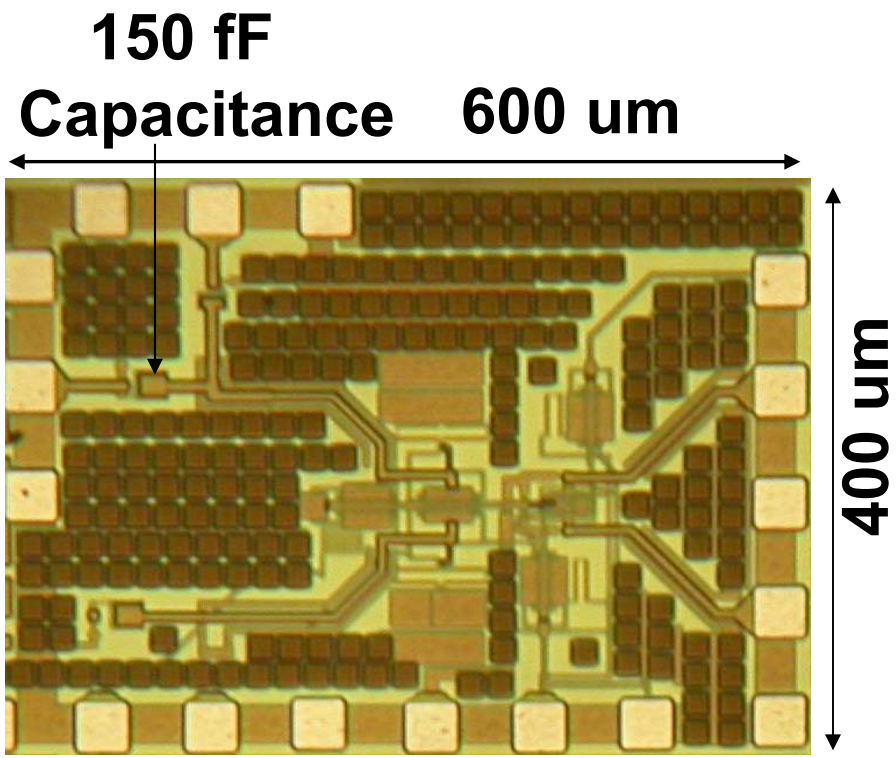


$g_{m\text{-}in}$=6.5 mS
g_{m2} =7.1 mS
g_{m3} =7.8 mS
R_L =300-ohm
R_{out} =80-ohm

- **Hysteresis condition:** $(g_{m2}R_L)(g_{m3}R_{OUT}) = 1.3347 > 1$
- **Sensitivity & Logic levels:** $|V_{th}| = 40\text{mV};\ 2|V_0| = \frac{2g_{m-in}}{g_{m2}}|V_{th}| = 76\text{mV}$
- **Rise time:** $\tau_{HYST} = R_L C_{Tot} = 18\text{ps}$
- **Power Consumption:** (1.8 X10) < 20 mW

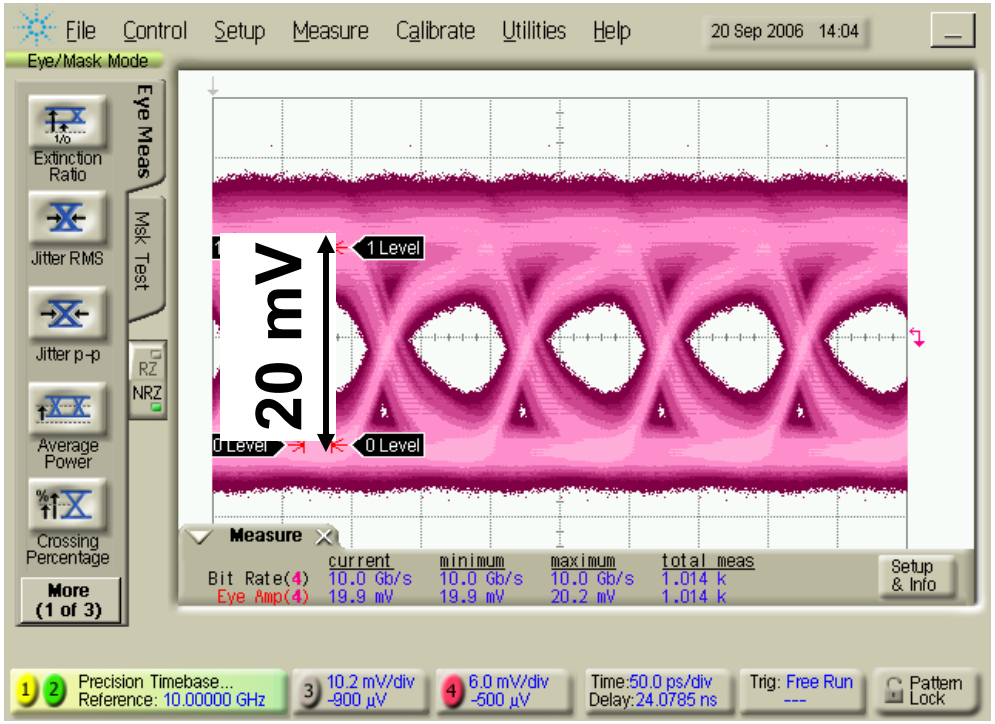
Implementation & Measurement

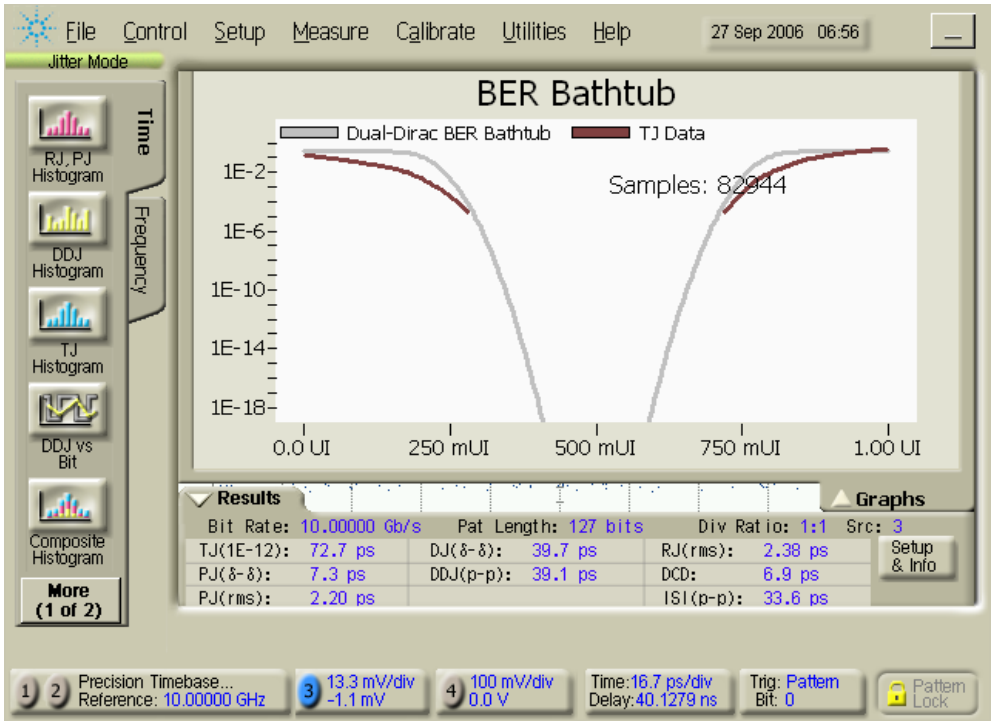




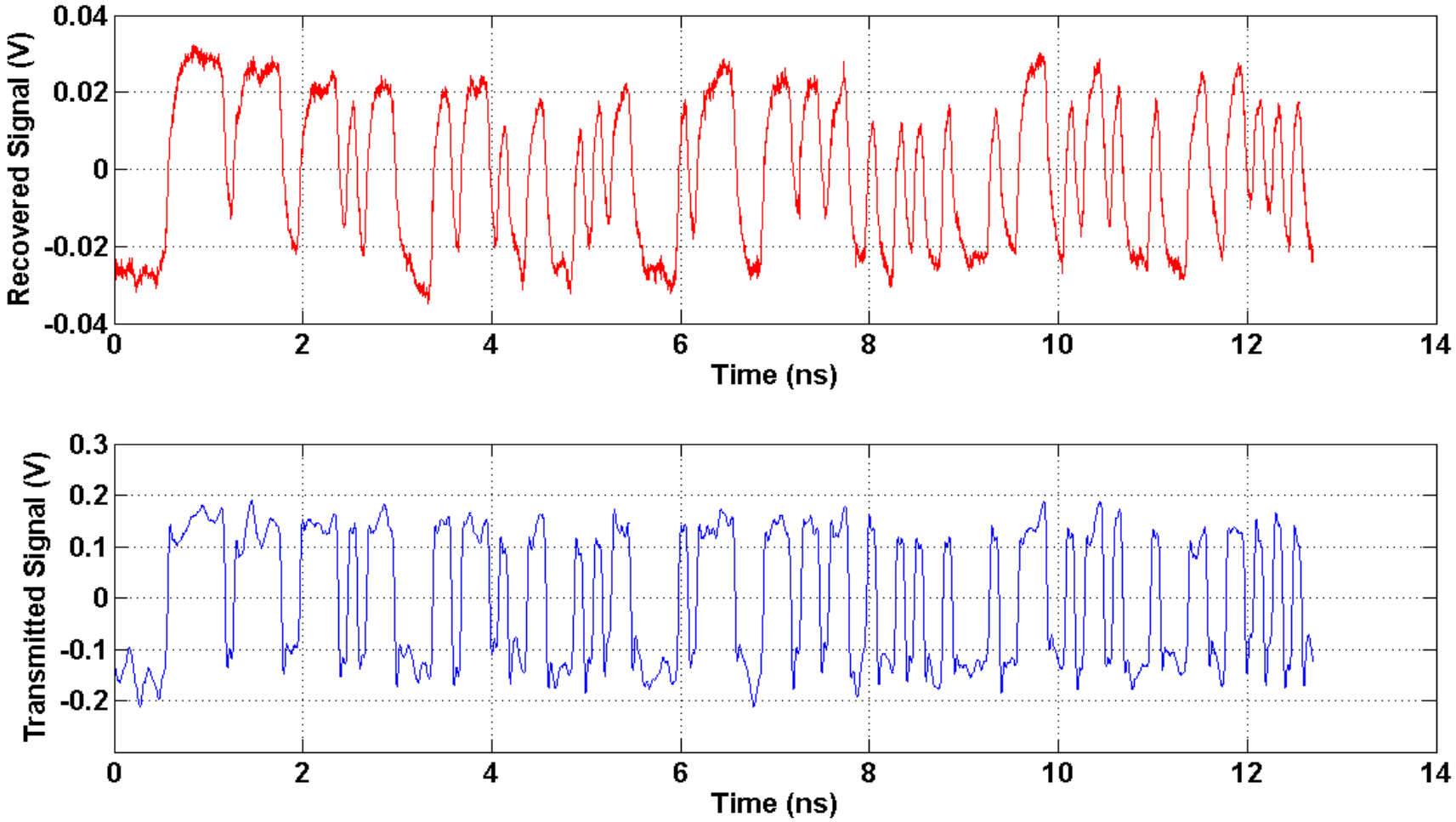
- Active area 200 um X 300 um
- Only single ended testing was possible
- Measured swing will be 25% of actual swing

10 Gb/s Measured eye





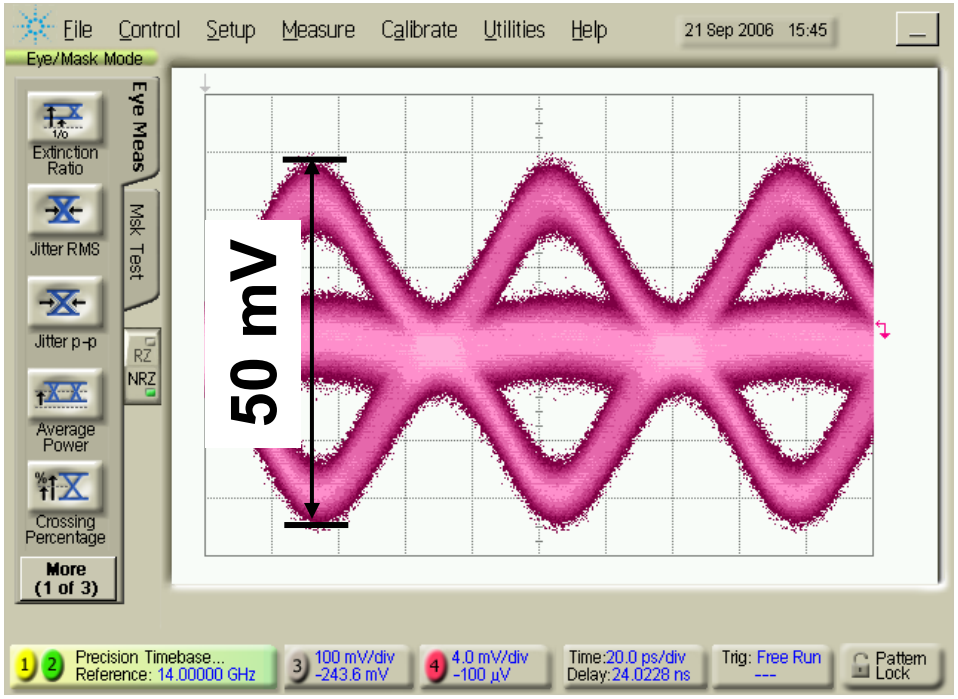
10 Gb/s Measured sequence



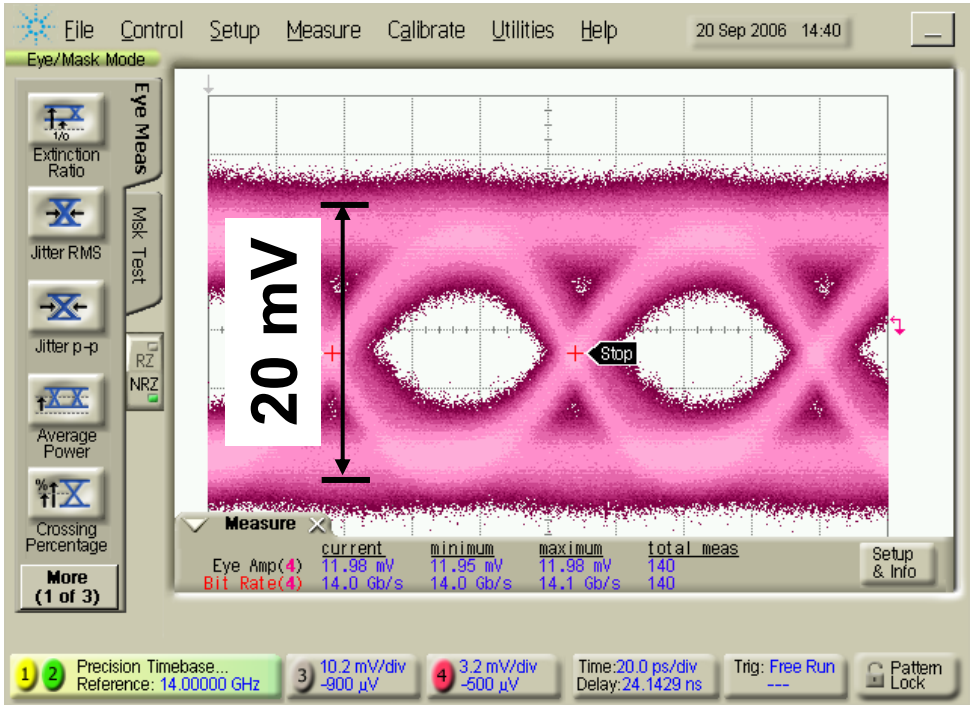
Error free operation verified with 127 bit pattern

14 Gb/s Measured eye

Rx eye



Recovered eye



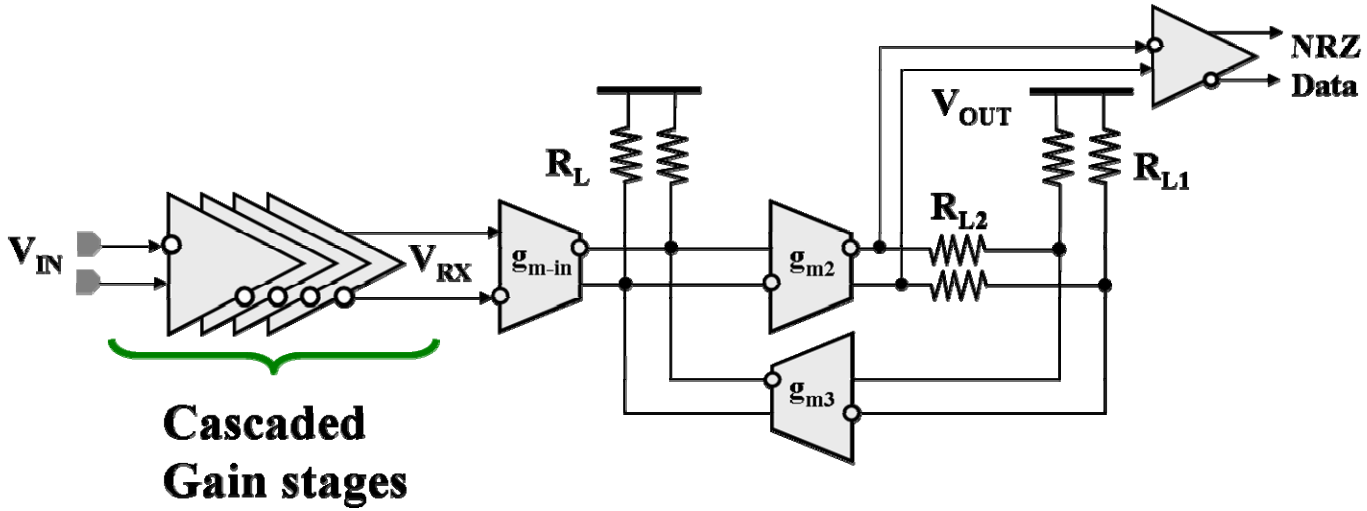
Performance Summary

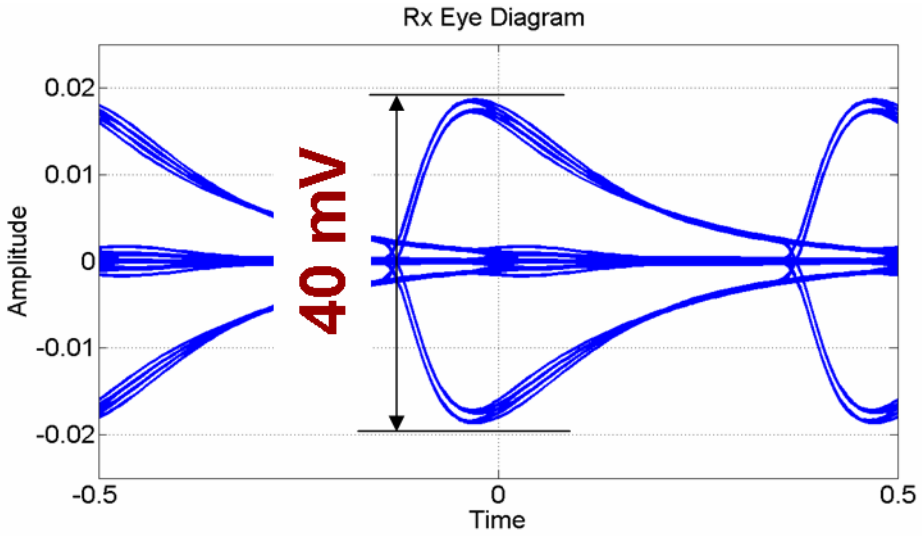
- Process 0.18 um CMOS
- Bit rate 10+ Gb/s
- Output Eye amplitude 80 mVp-p differential
- Coupling capacitor of 150 fF
- Power consumption 20 mW

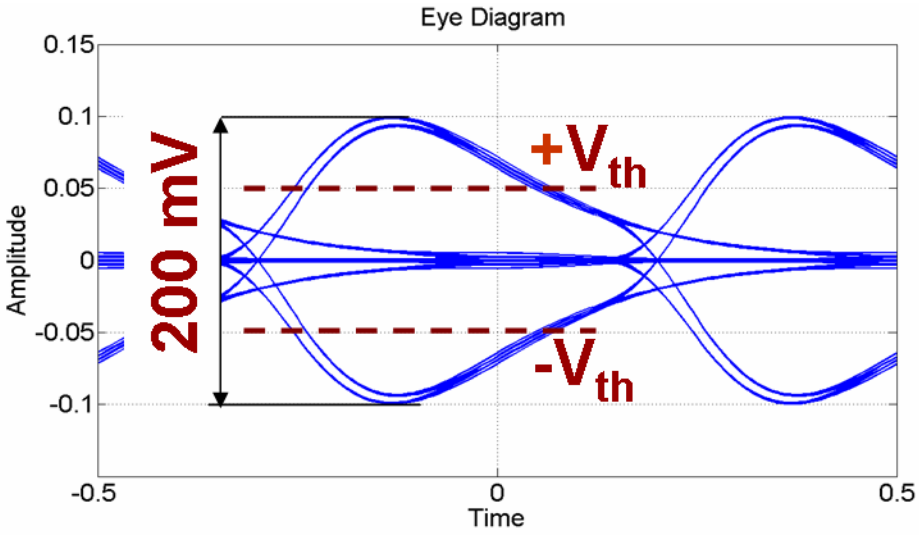
90-nm Implementation

- Coupling C = 80fF : improve sensitivity
- Eye Amplitude > 250 mV : increase output swing
- Bit Rate = 15 Gb/s : improve speed

Improving sensitivity



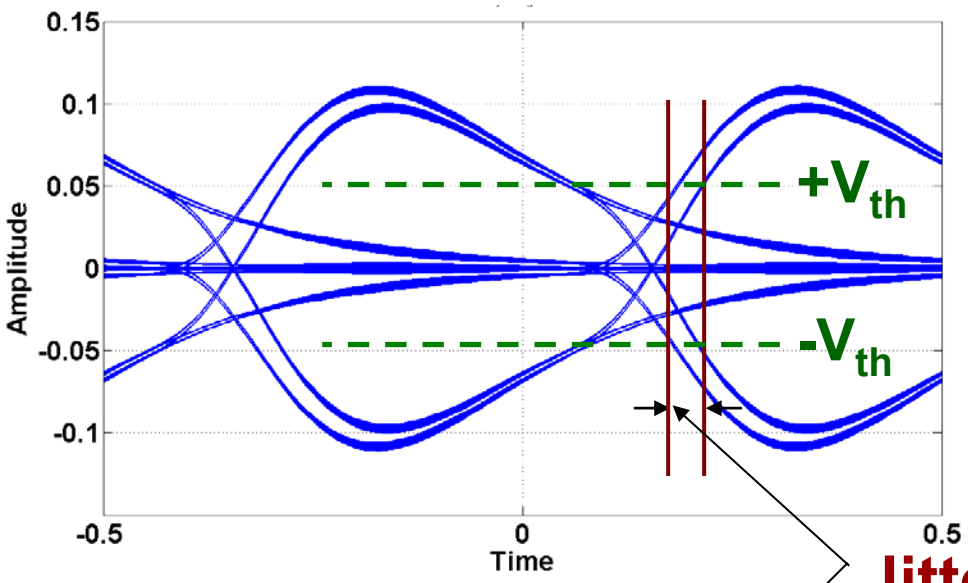




5x Improvement in sensitivity !!

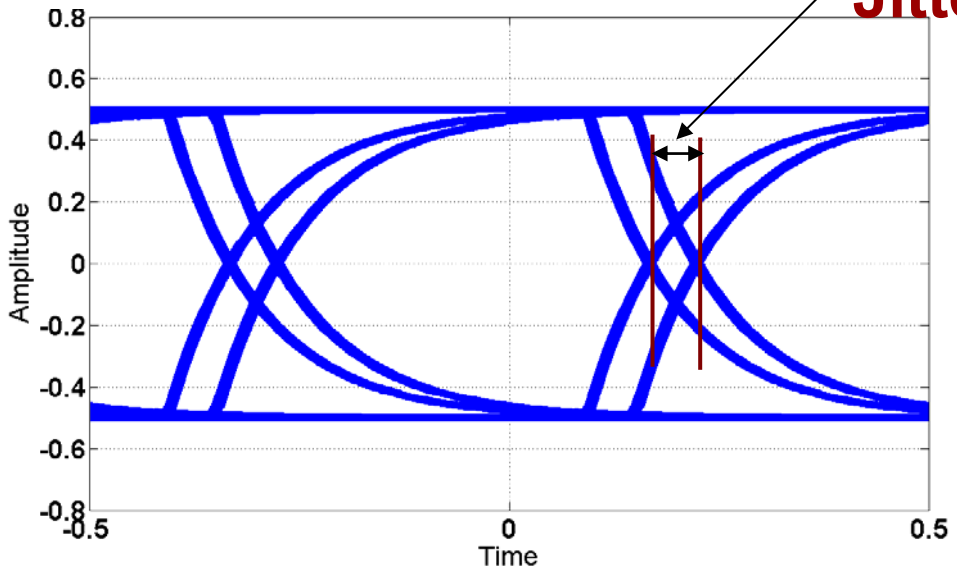
Bandwidth of the Pre-amp

Slope eye
[10 Gb/s]



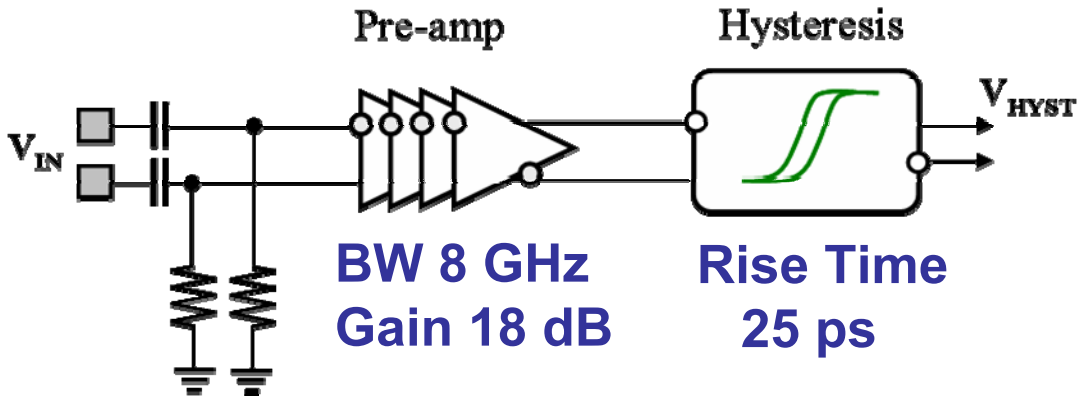
Jitter due to pre-amp
(BW = 8GHz)

Recovered
NRZ eye
[10 Gb/s]



Pre-amp requires more BW in AC coupled receivers !!!

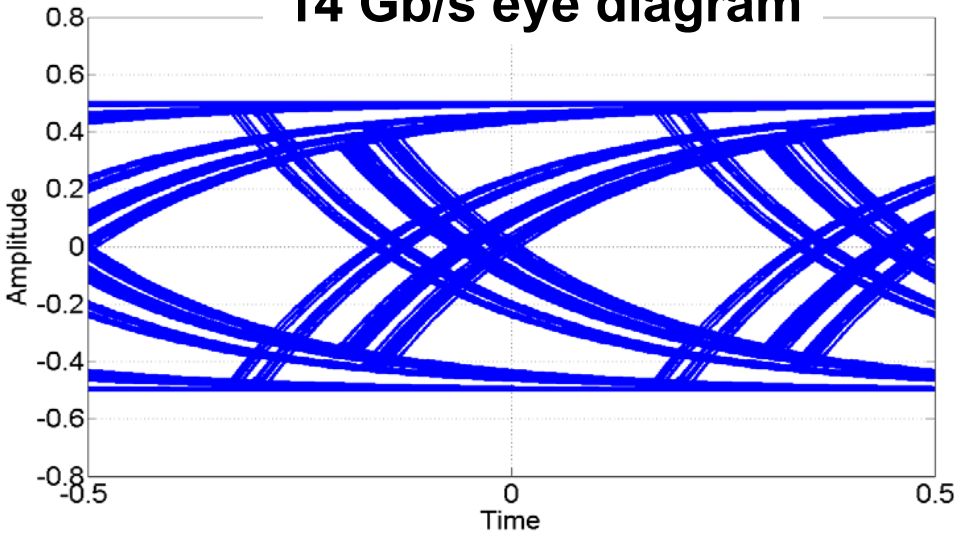
Bandwidth of the Pre-amp



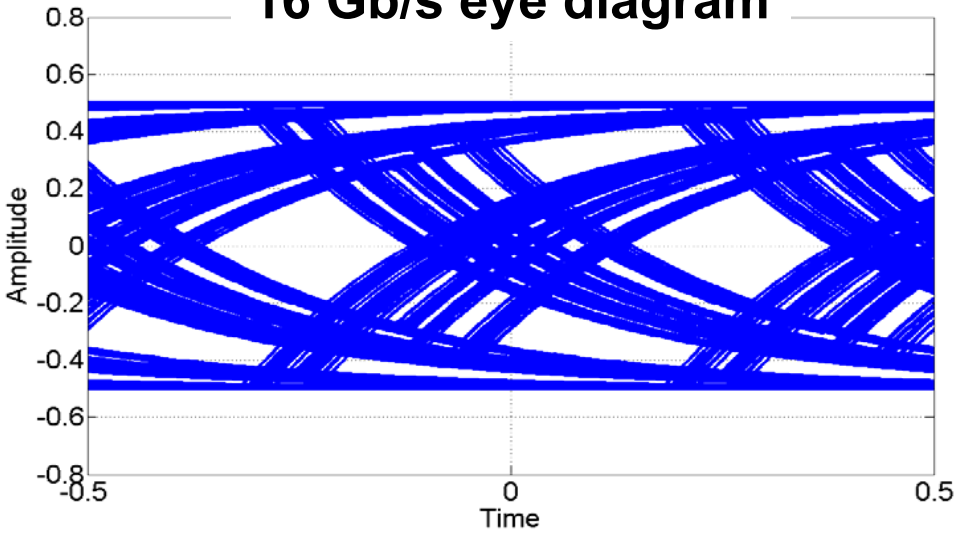
BW 8 GHz
Gain 18 dB

Rise Time
25 ps

14 Gb/s eye diagram

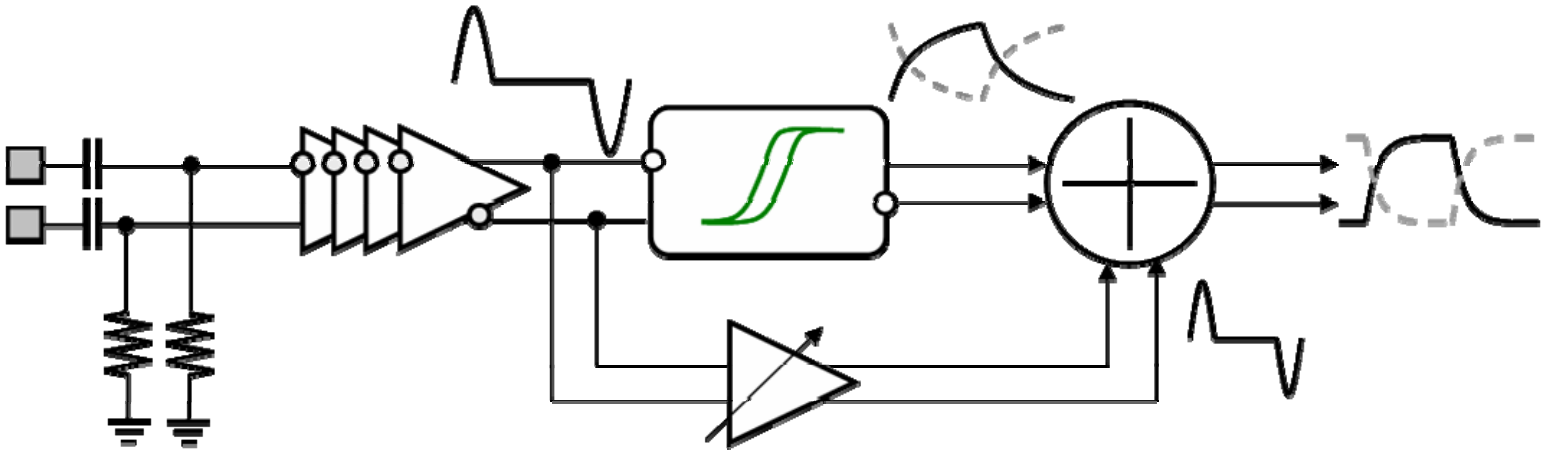


16 Gb/s eye diagram



How can we improve Jitter and ISI ??

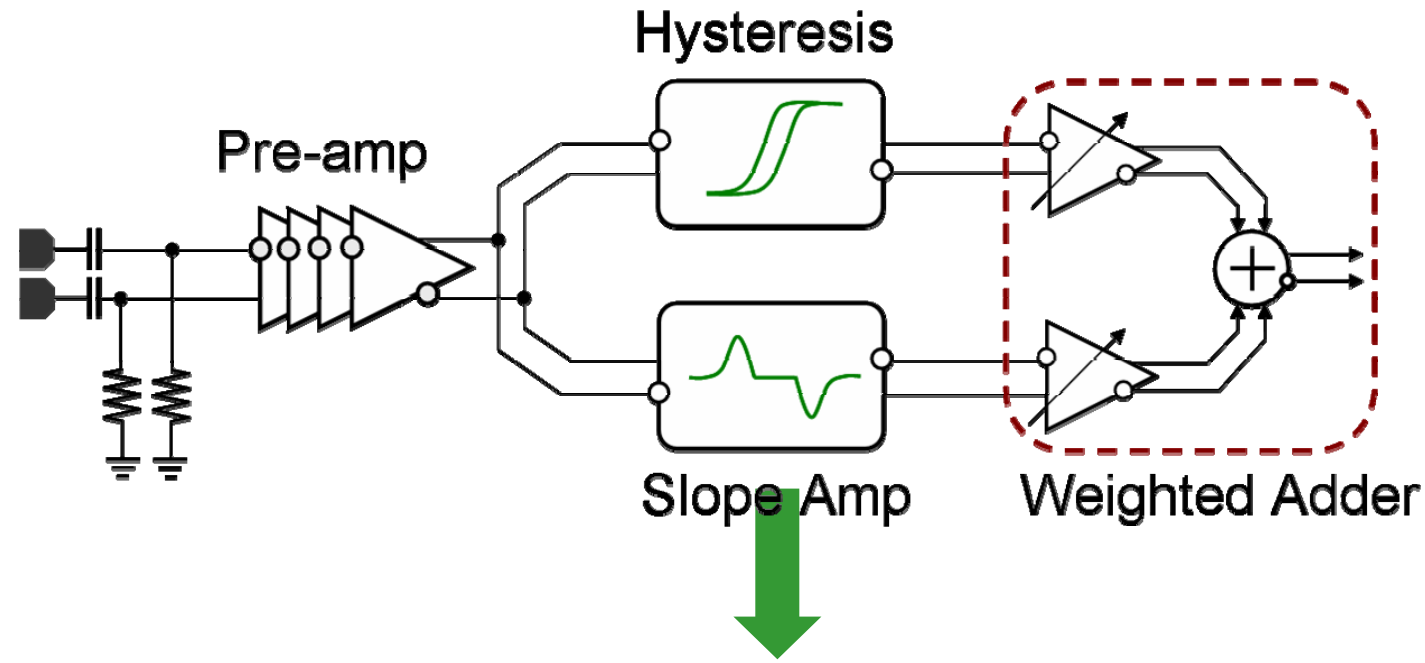
Speed Improvement

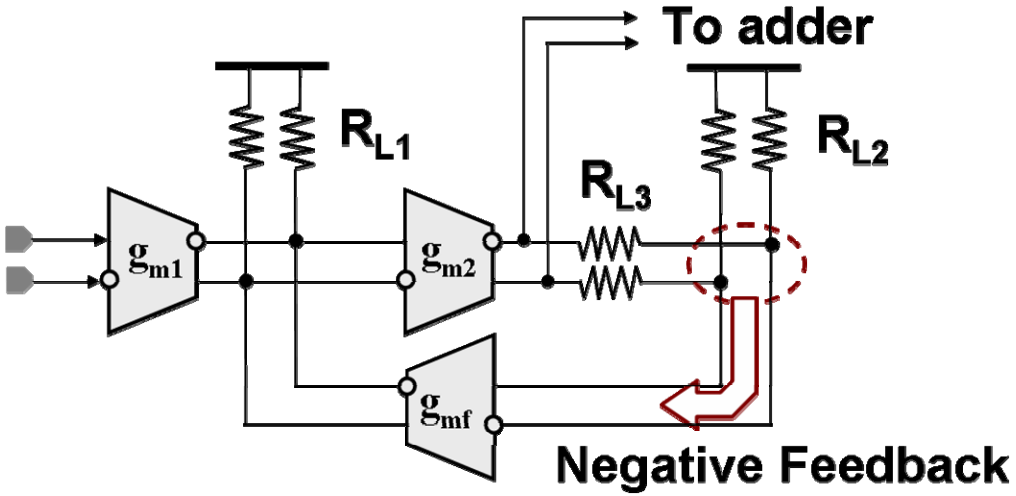


- Improve speed by using available data transitions

- How to match the latency ?
- Can we have sufficient BW ?

Speed Improvement

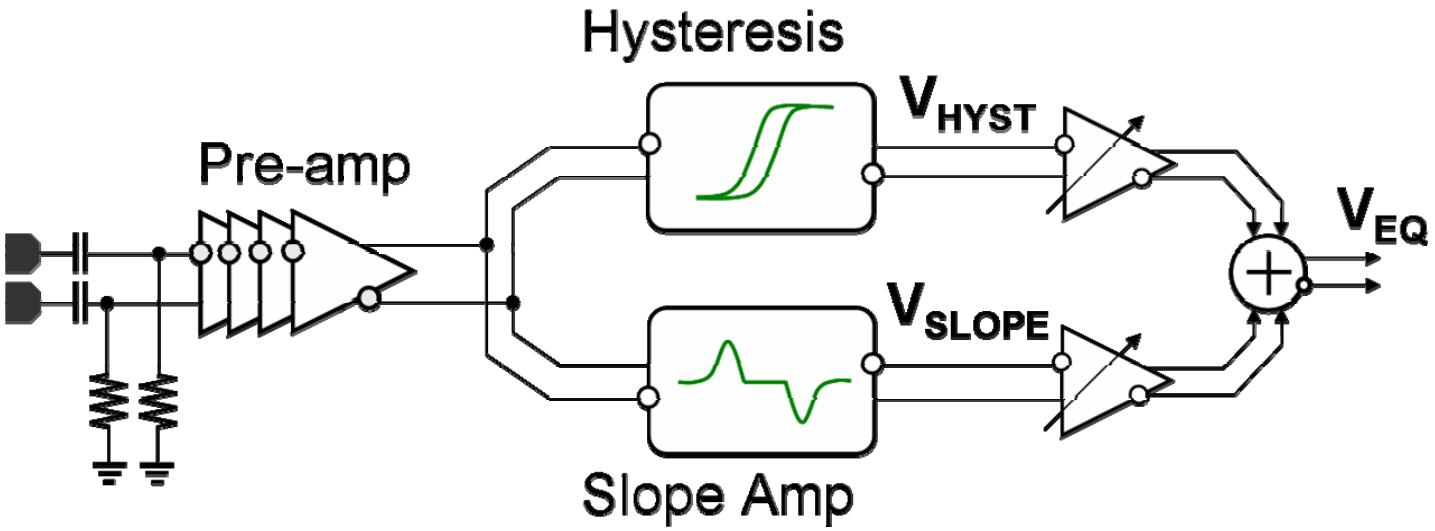




$$A_v = \frac{A_{vo}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

[Galal '02]

Speed Improvement



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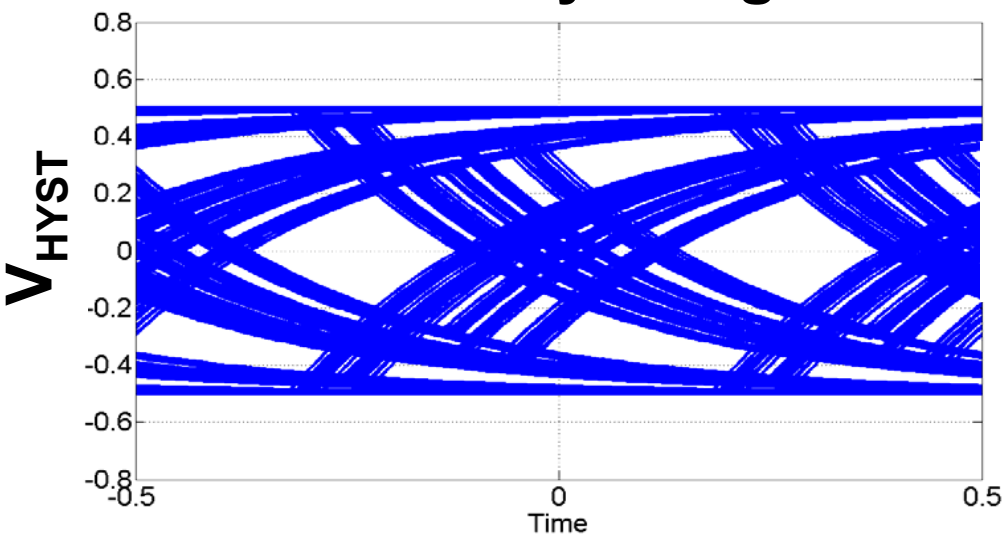
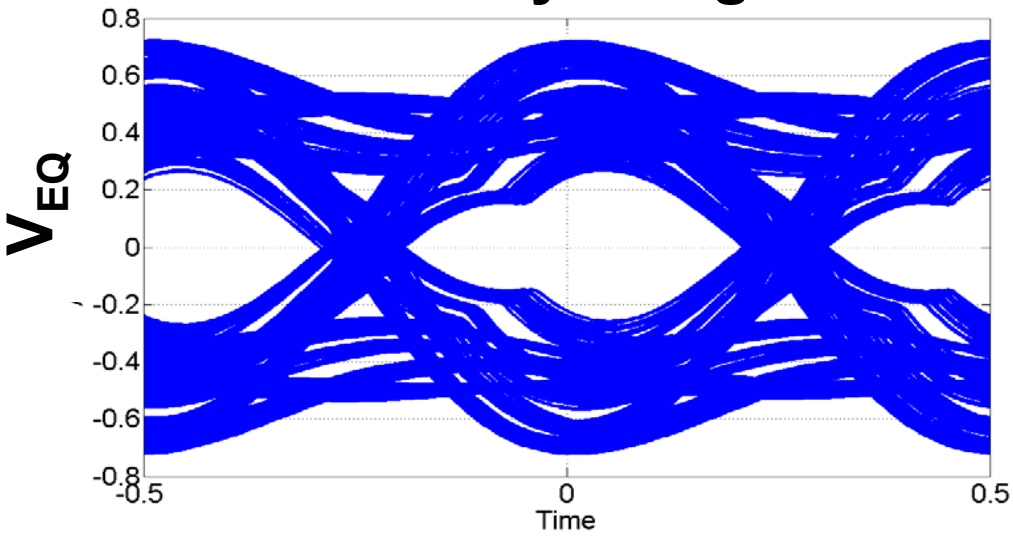
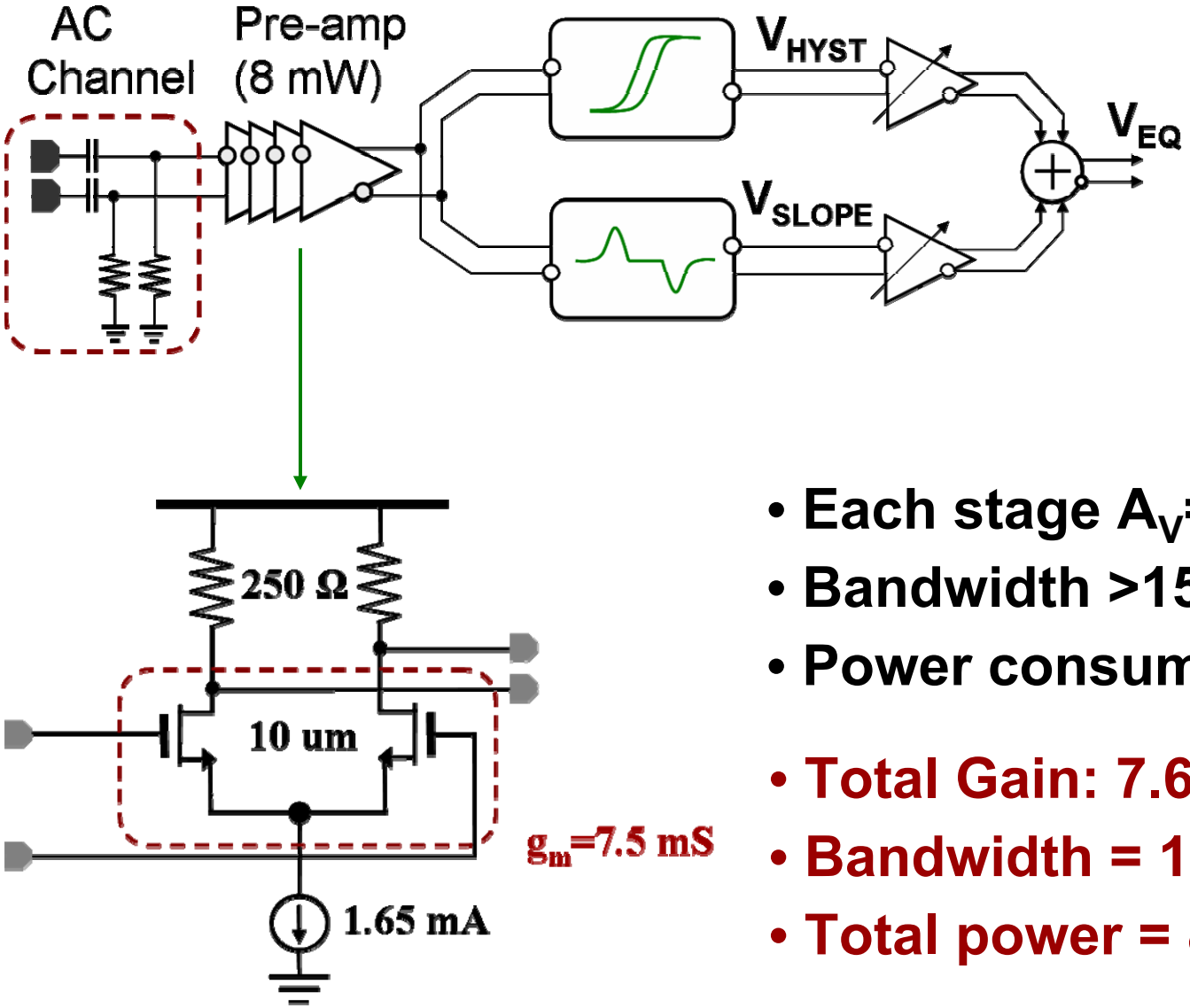


16 Gb/s eye diagram



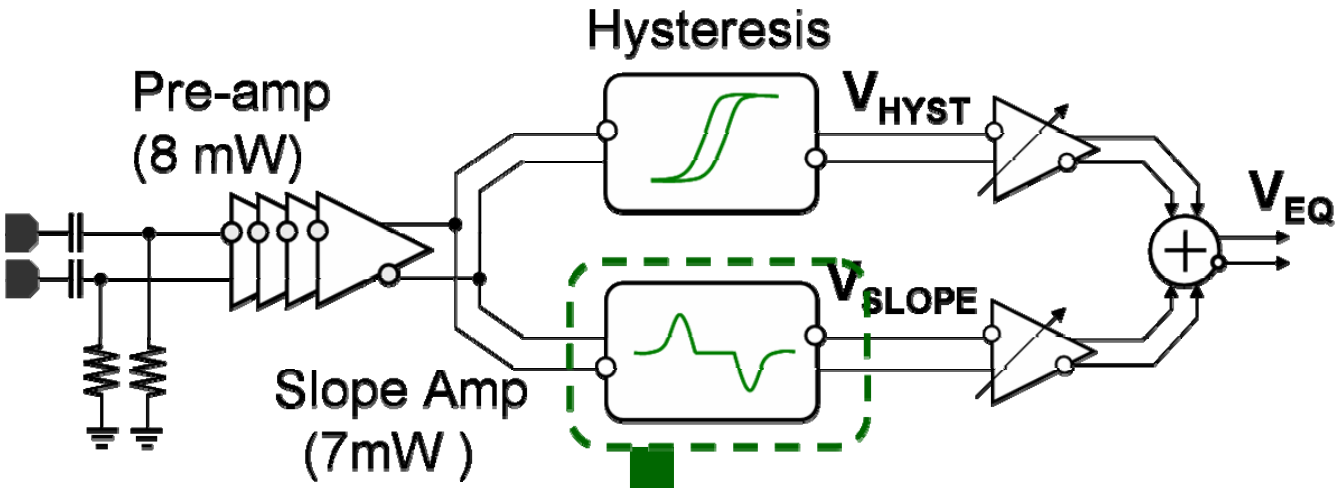
Implementation in 90-nm CMOS

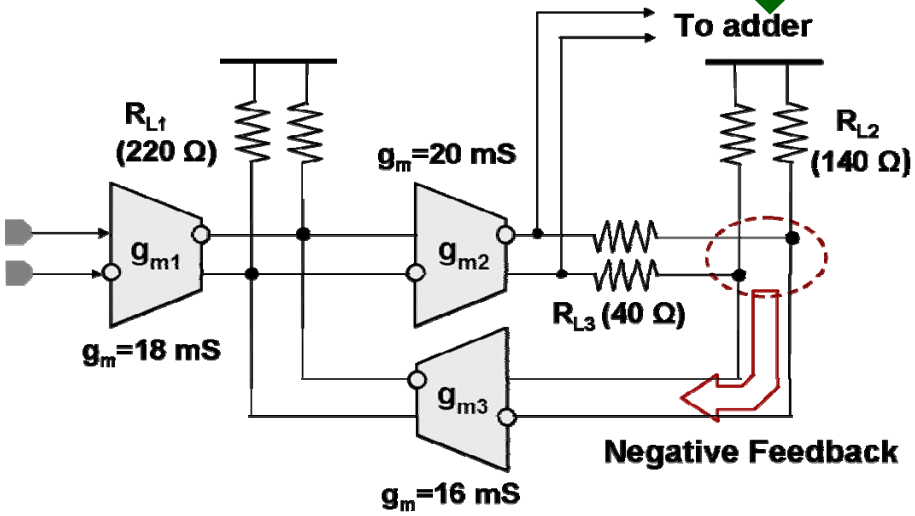


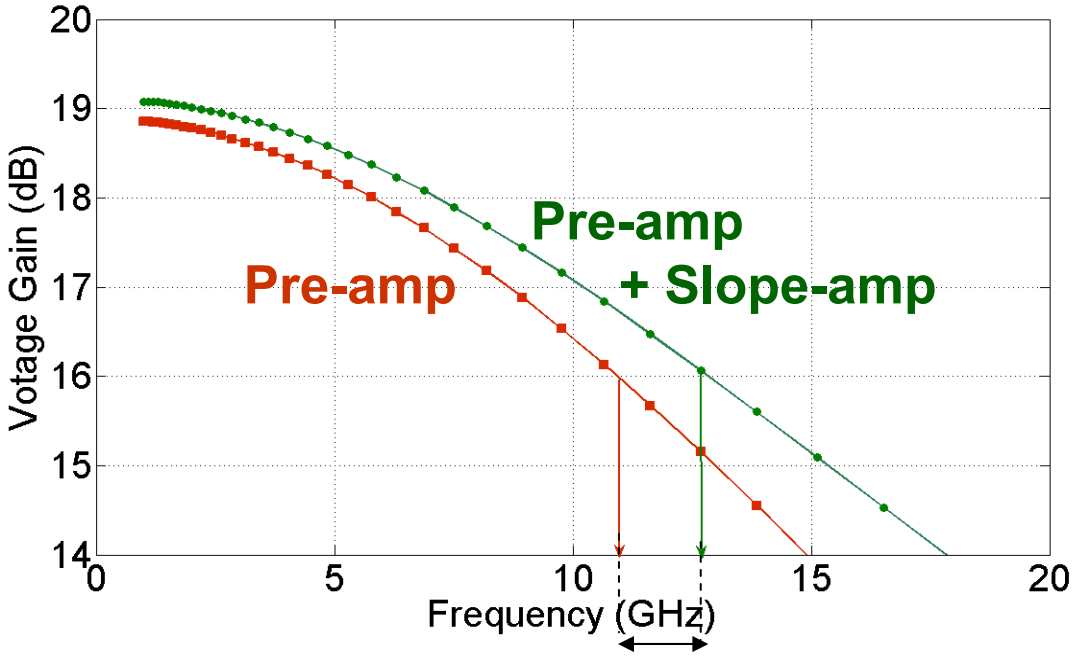
- Each stage $A_V=g_mR_L= 1.9$
- Bandwidth >15 GHz
- Power consumption 2mW

- Total Gain: 7.6 > 5
- Bandwidth = 11 GHz
- Total power = 8 mW

Implementation in 90-nm CMOS

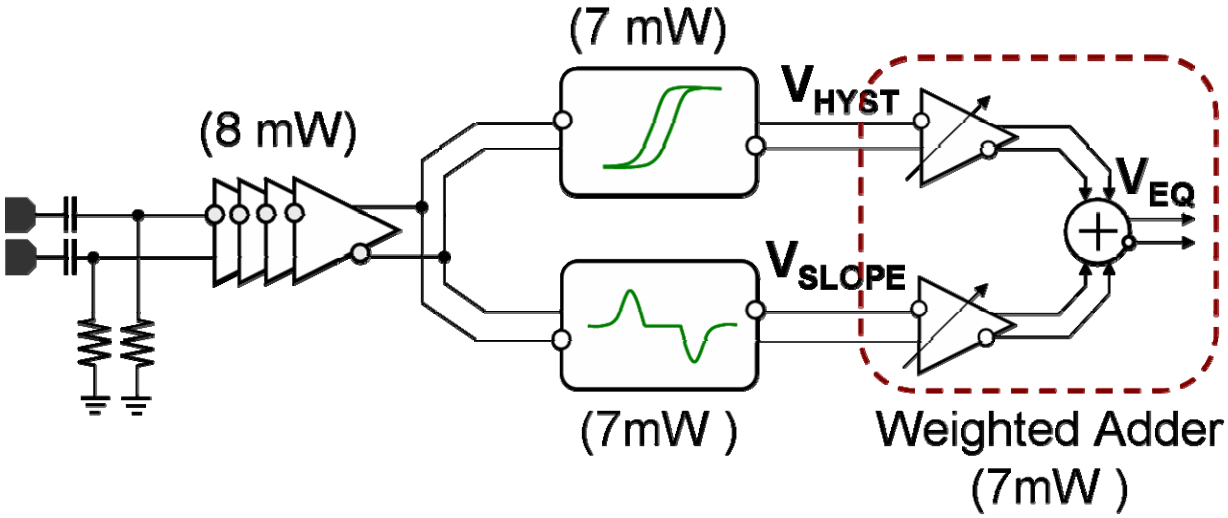


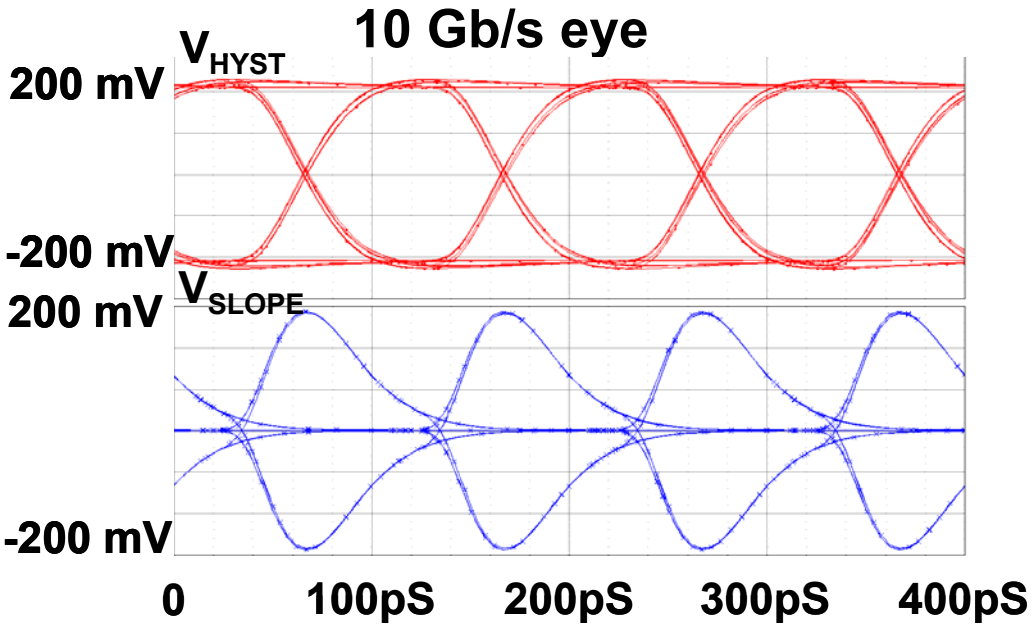


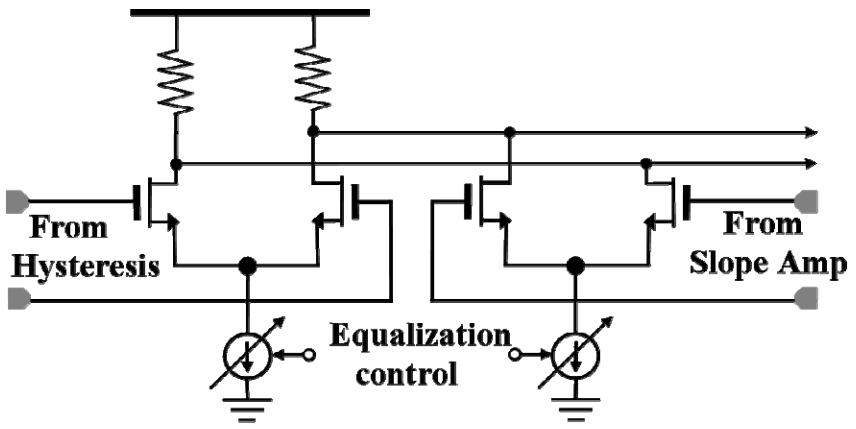


2 GHz

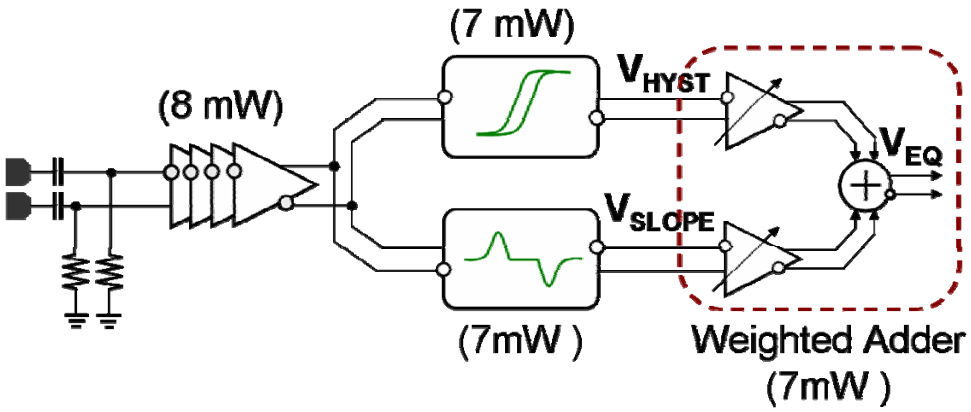
Implementation in 90-nm CMOS



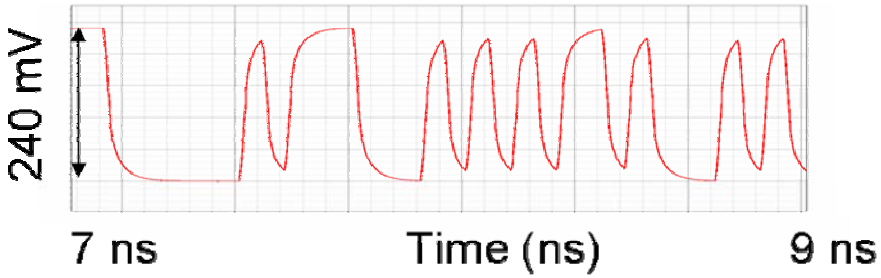




Implementation in 90-nm CMOS

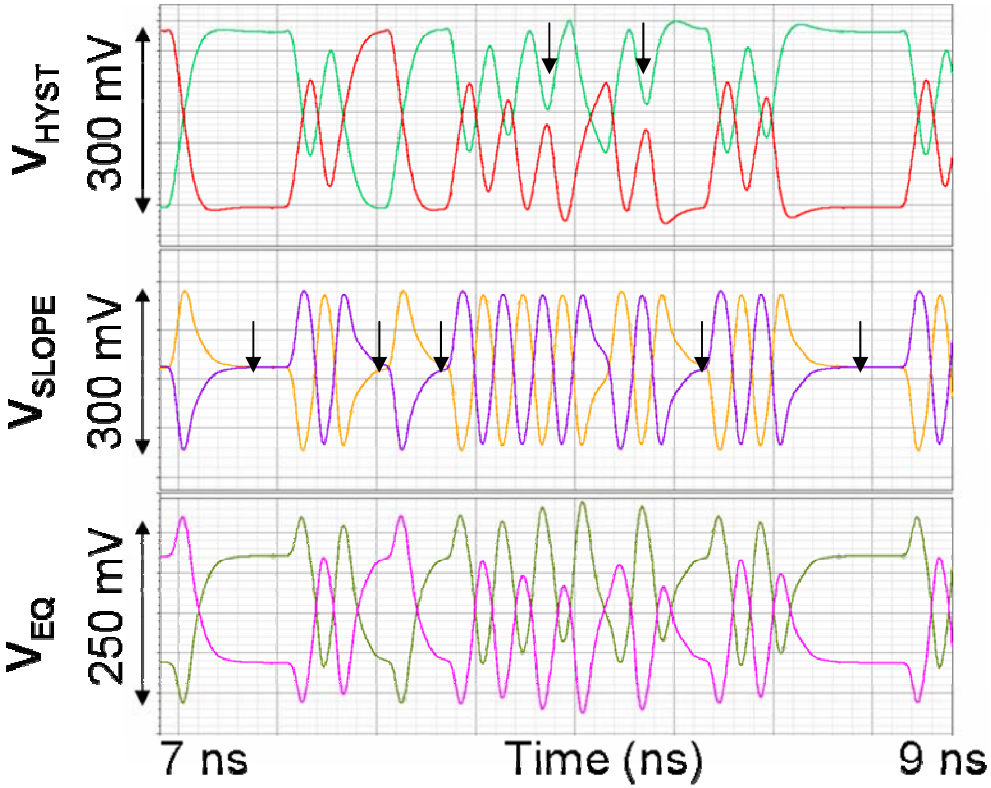


Transmitted sequence

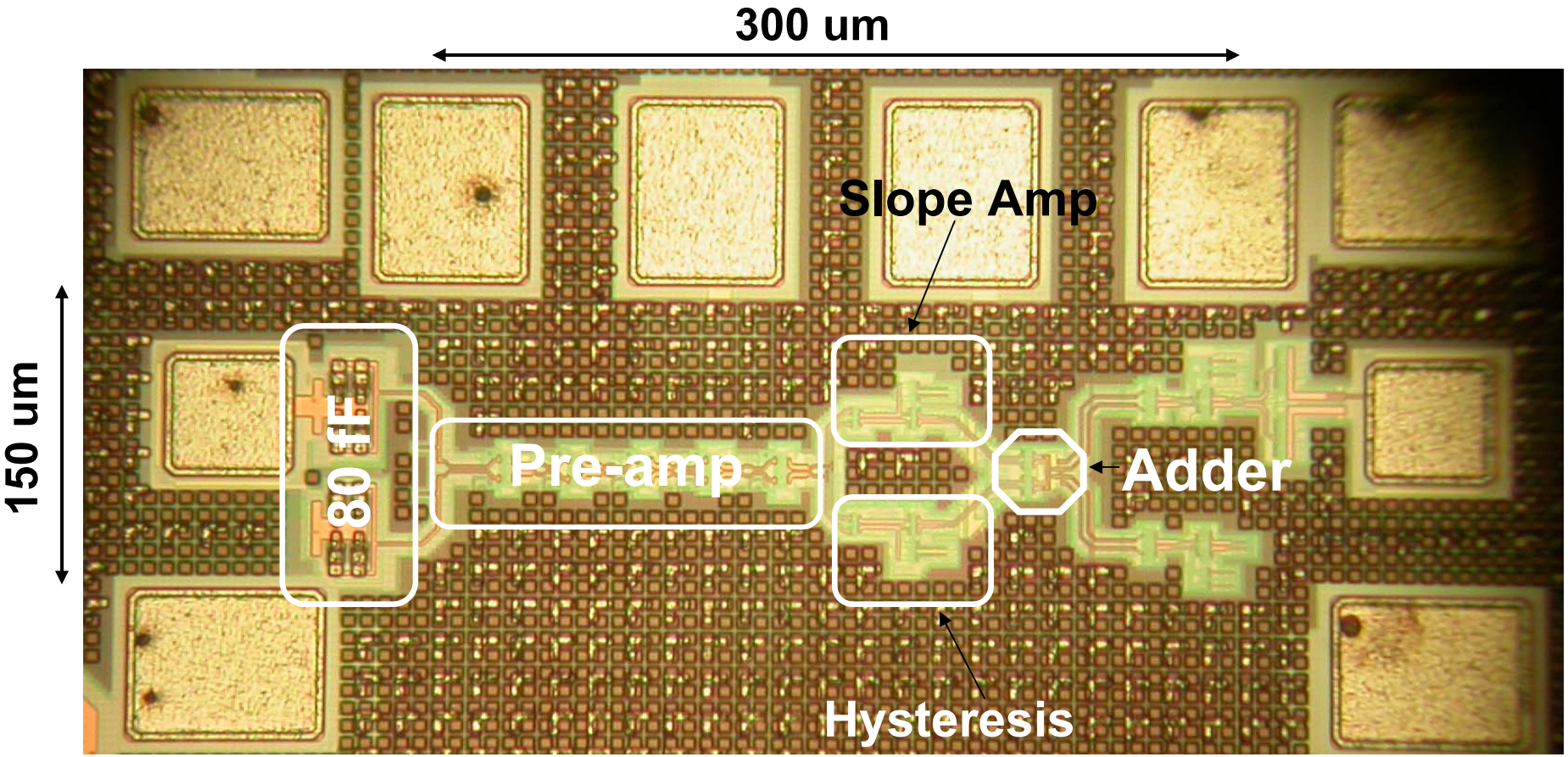


Bit period 50 ps

Arrow indicates error bits

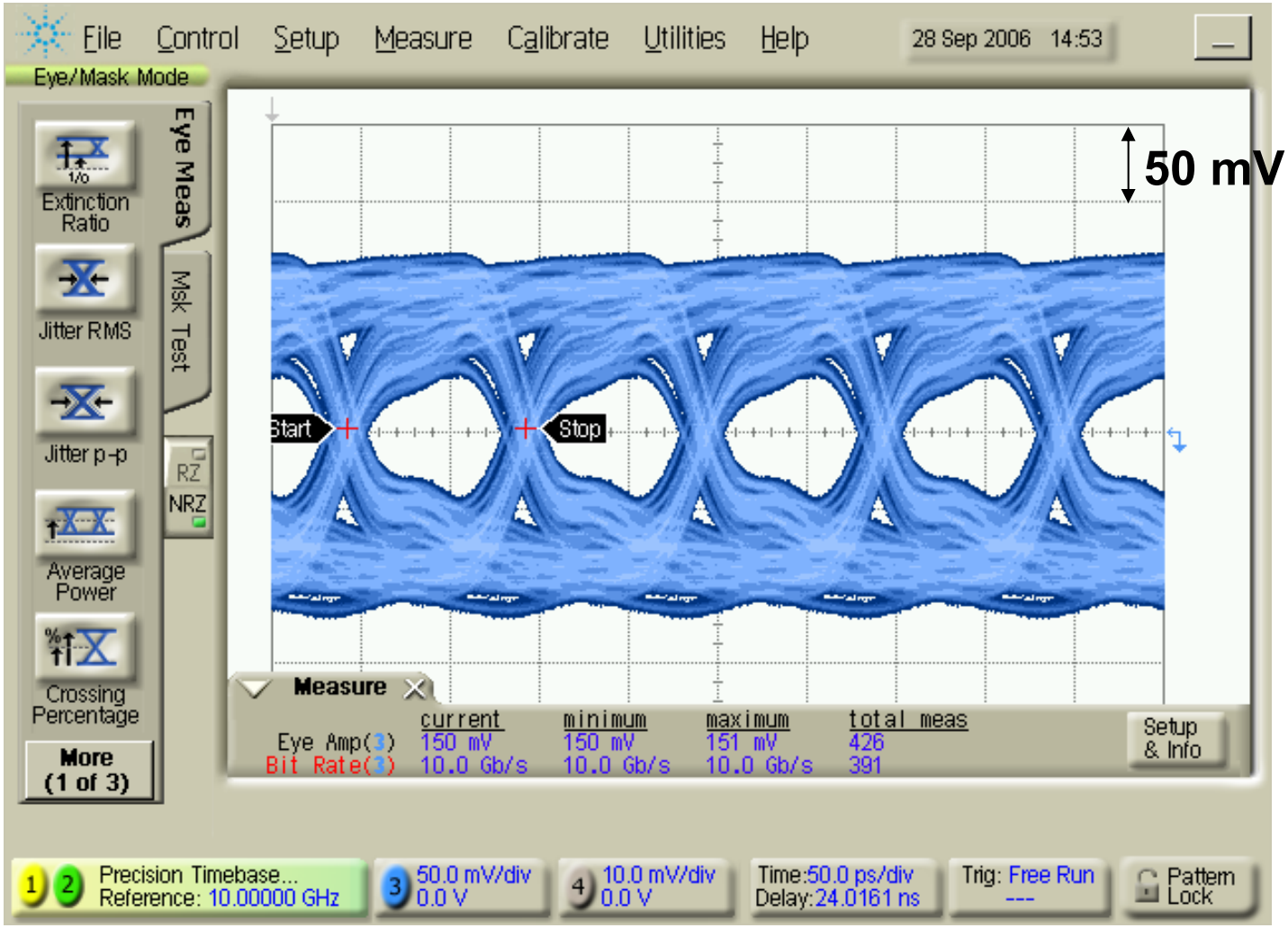


Implementation in 90-nm CMOS



- Active area 100 um X 300 m
- Total power 32 mW

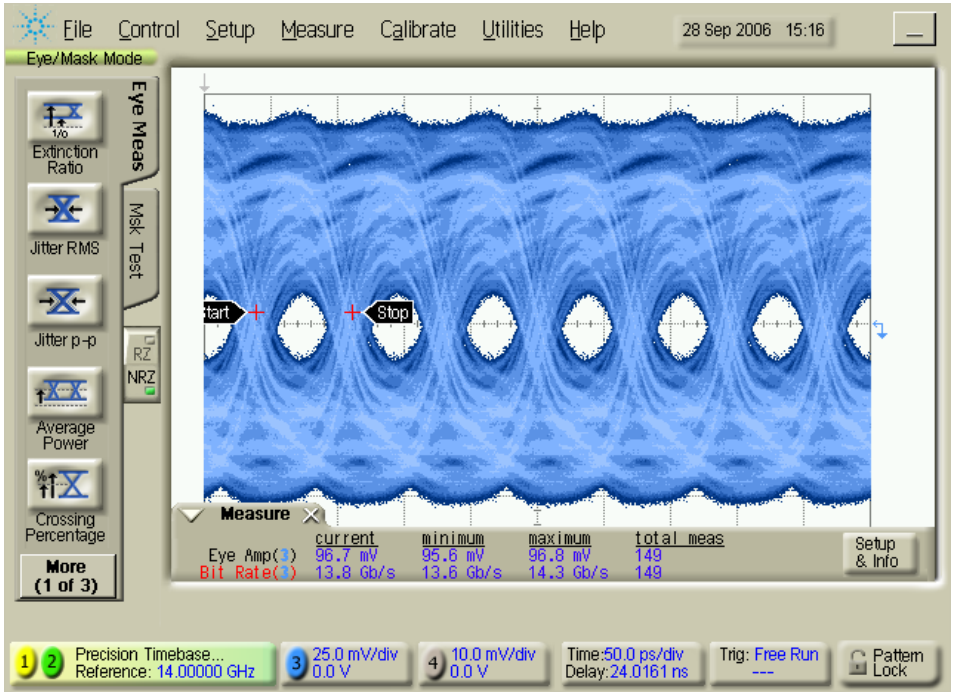
10 Gb/s Measured eye



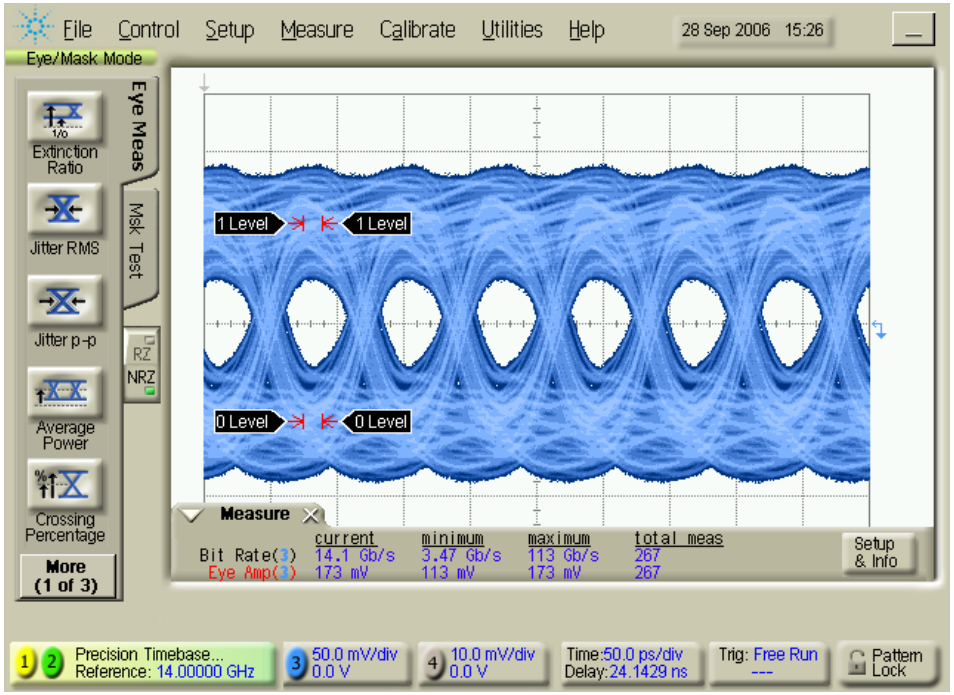
Slope path was turned off at 10 Gb/s

14 Gb/s Measured eye

Slope Path OFF



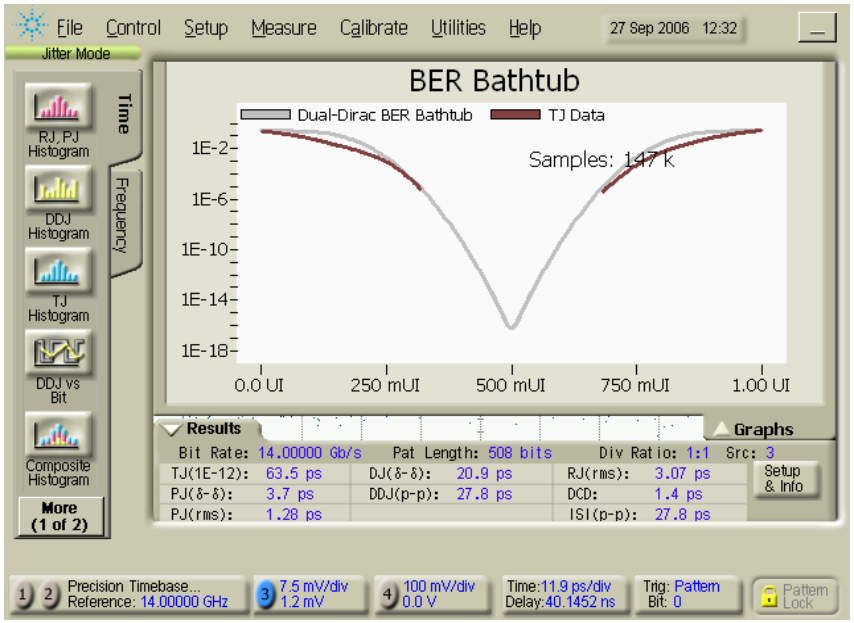
Slope Path ON



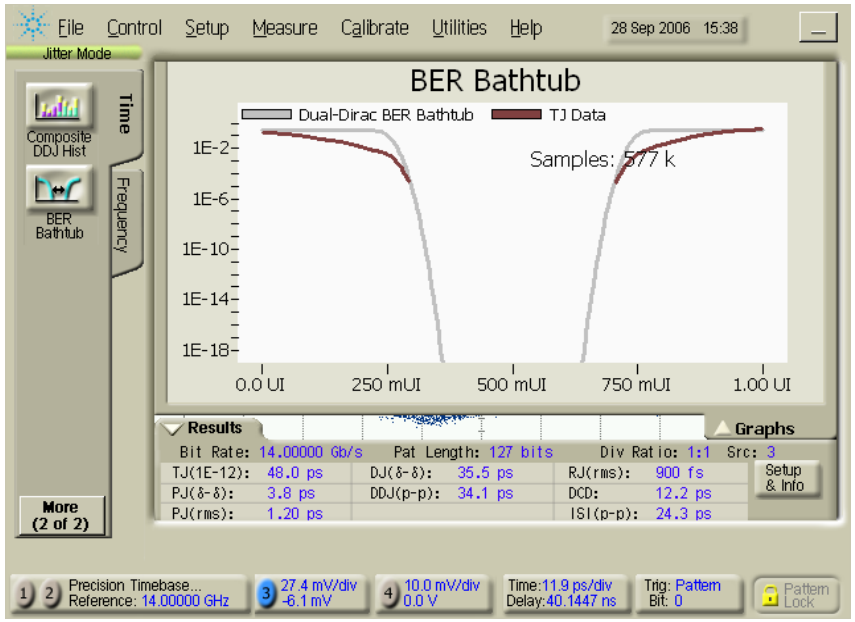
Vertical scale : 25 mV/div
Horizontal scale : 50 ps/div

Vertical scale : 50 mV/div
Horizontal scale : 50 ps/div

14 Gb/s Measured BER Bathtub



14 Gb/s recovered eye with Hysteresis only



14 Gb/s recovered eye with Hysteresis + Slope-path

Conclusion

- 10+ Gb/s hysteresis circuit topology is implemented and tested in 0.18-um CMOS process (FOM 2 mW/Gb/s)

- High speed AC coupled receiver architecture is introduced:
  1. Additional slope path reduces ISI at hysteresis output
  2. Additional slope path reduces jitter

- 14 Gb/s AC coupled receiver is implemented and tested in 90-nm CMOS
  - FOM 1.80 mW/Gb/s @ 10 Gb/s
  - FOM 2.28 mW/Gb/s @ 14 Gb/s