A 5-Gbps Optical Receiver with Monolithically Integrated Photodetector in 0.18-μm CMOS

Tony Shuo-Chun Kao and Anthony Chan Carusone
Edward S. Rogers, Sr. Department of Electrical & Computer Engineering, University of Toronto
10 Kings College Rd., Toronto, Ontario, M5S 3G4, Canada

***Abstract*—This paper describes an optical receiver with monolithically integrated photodetector in 0.18-μm CMOS technology using a combination of spatially modulated light detection and an analog equalizer. A transimpedance amplifier employing negative Miller capacitance is introduced to increase its bandwidth without causing gain peaking. Occupying a core area of 0.72 mm^2, the fully integrated optical receiver achieves 4.25 Gbps and 5 Gbps with a power consumption of 144 mW and 183 mW respectively.**

***Index Terms*—CMOS integrated circuits, equalizers, monolithically integrated photodiode, negative Miller capacitance, photodetector, transimpedance amplifier**

I. Introduction

Optical receivers have become an active area of research as they can be used in short-distance communication systems such as local-area networks (LAN), fiber-to-the-home (FTTH), and automotive interconnects. Optical interfaces are also required in optical storage systems such as CD-ROM, DVD, and Blu-ray Disc. In all these applications, a photodetector is necessary to establish the conversion from light to electrical signal for further processing. Monolithically integrated photodetectors in standard CMOS technology are attractive since the extra overhead and cost during assembly for multi-chip solutions can be avoided. In addition, ESD problems and parasitics associated with bond wires can also be eliminated.

In general, light detection in CMOS technology is performed by a reverse biased PN junction which creates a depletion region to collect the electron-hole pairs generated by incident photons. However, the penetration depth of 850-nm light is much greater than the location where the depletion region occurs in standard CMOS technology (typically 1 um to 2 um below the surface). Consequently, photons are absorbed and carriers are generated deep in the silicon substrate. They slowly diffuse to the depletion region. This slow diffusion mechanism limits the data rate to only a few hundreds of Mbps if no compensation techniques are employed [1]. Several methods have been proposed to eliminate the slow diffusive carriers and improve the speed of monolithically integrated photodetectors. In standard CMOS technology without any modification to the process, speed can be increased by applying a high reverse bias voltage, often higher than the power supply, to generate a thick depletion region [2], [3]. This approach however seriously impacts the reliability of the photodetector. A spatially modulated light (SML) detector comprising alternating covered and exposed diodes has also been used to eliminate the slow diffusive carriers [4]. Alternatively, equalization can be applied to directly compensate the low intrinsic bandwidth of the photodiode [1].

This paper describes the design of a 5-Gbps fully integrated optical receiver including photodetector, transimpedance amplifier (TIA), equalizer, and post amplifier (PA). To the authors' knowledge, it is the fastest fully integrated optical receiver implemented in a standard CMOS technology. A TIA employing negative Miller capacitance to extend its bandwidth without causing gain peaking is also introduced.

II. Photodetector

A simplified cross section of the SML detector consisting of an exposed and a covered photodiode with a light-blocking metal is shown in Fig. 1. When the light is incident on the surface of the detector, carriers generated in the depletion region are immediately collected by the exposed photodiode. Carriers generated in the deep substrate will diffuse towards the depletion region and have equal probability of reaching either the exposed or the covered photodiode. Hence, when the signal currents collected by these two photodiodes are subtracted, the slow diffusive carriers are cancelled and a faster response is obtained. The cancellation however reduces the responsivity of the photodetector, and a low-noise TIA is necessary to amplify differential currents in the range of a few microamperes from the SML detector without degrading the sensitivity. The actual layout of the SML detector consists of alternating fingers of exposed and covered photodiodes with the dimensions shown in Fig. 1. The area of the SML detector is 75 um × 75 um to facilitate coupling to multimode fibers.

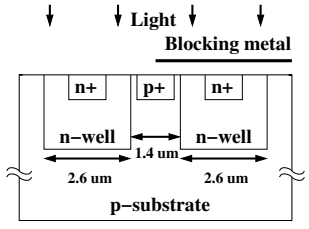


Fig. 1. Cross section of the SML detector.

III. Circuit Design

The architecture of the proposed optical receiver is shown in Fig. 2. It begins with the SML detector which converts the incident optical power into two currents. A differential TIA converts the two currents from the photodiodes into

two voltages. The supply of the TIA was 3.3 V in order to provide a high reverse bias voltage for the photodiodes so that a large photodetector bandwidth and responsivity can be achieved simultaneously. AC coupling with a cutoff frequency of 100 kHz was used to connect the TIA to the rest of the circuit blocks which operate from a 1.8 V supply. Since the current from the exposed photodiode is always larger than that from the covered photodiode, the AC coupling link has the added benefit of eliminating any difference between the common-mode levels of the two signals. A subtracter follows to further improve common-mode rejection and cancel the slow diffusive carriers generated by photon absorption deep in the substrate. The resulting signal after the subtracter is completely differential. An equalizer and a PA follow to further remove inter-symbol interference (ISI) and increase the signal swing respectively. For testing purposes, an output buffer was used to drive the signal to the oscilloscope.

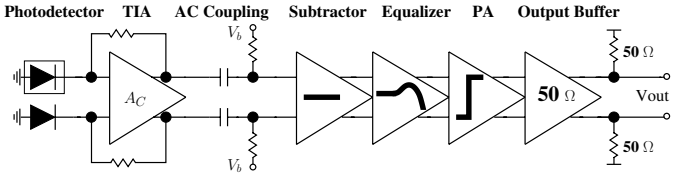


Fig. 2. Optical receiver block diagram.

A. Transimpedance Amplifier

A regulated cascode (RGC) stage has often been employed to alleviate bandwidth reduction of the TIA due to parasitic capacitance of the photodetector [2], [5]. This topology however degrades the sensitivity due to the added components directly at the input of the TIA. The schematic of the proposed TIA is shown in Fig. 3. A large R_F is chosen to provide a high transimpedance gain which is desirable as noise contributions from later stages can be kept small compared to that from the TIA. The bandwidth of the TIA can be approximated as [6]

$$BW_{TIA} = \frac{A_C}{2\pi R_F C_{in}} \tag{1}$$

where A_C is the open-loop gain of the core amplifier, and C_{in} includes the input capacitance of the core amplifier and the parasitic capacitance of the photodetector. Since the bandwidth of the TIA varies inversely proportional to R_F, A_C must be made large to keep the bandwidth high. Increasing A_C however leads to gain peaking in the frequency response due to an insufficient phase margin. Gain peaking must be removed so that the amount of overshoot in the time domain can be minimized. A capacitor can be added in parallel with R_F to eliminate the gain peaking but at the expense of a reduced TIA bandwidth [7]. Instead, the topology used in this work employs a negative Miller capacitance in the core amplifier, which extends the dominant pole of this stage and leads to an increase in the overall TIA bandwidth. In addition, the improvement in phase margin created by this shift of the core-amplifier pole allows A_C to be increased without sacrificing stability. This further increases the bandwidth of the TIA as shown in (1). Illustrated in Fig. 4, the bandwidth of the TIA is increased with the negative Miller capacitance while ensuring a flat frequency response. The TIA has a simulated transimpedance gain of 74.6 dBΩ and a bandwidth of 2.9 GHz. The gate-source and gate-drain voltages of all transistors are kept within 1.8 V to guarantee reliability of the operation under the 3.3 V supply.

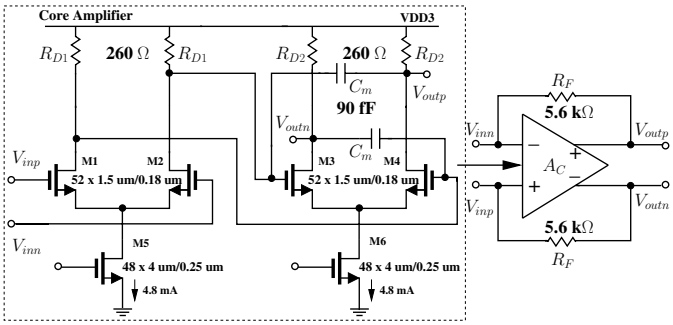


Fig. 3. Schematic of the TIA.

B. Subtracter

The schematic of subtracter is shown in Fig. 5. The implementation of the gain cell is based on the Cherry-Hooper amplifier with active feedback [8]. The subtracter has a simulated DC gain of 10 dB and a bandwidth of 12.4 GHz.

C. Equalizer

The schematic of the equalizer is shown in Fig. 6. It uses capacitive degeneration to generate boosting at high frequencies. The degeneration capacitors were implemented as MOS devices in accumulation mode by placing NMOS transistors inside an n-well. The equalizer has a simulated DC gain of 0 dB with a maximum boosting of 5.8 dB.

D. Post Amplifier

The architecture of the PA is shown in Fig. 7. It consists of an input stage which performs offset cancellation, 4 identical gain cells to provide the necessary gain, and an offset cancellation network to low-pass filter the output and sense any DC offset. Each gain cell was implemented using the same topology as the one for the subtracter, shown in Fig. 5, but with 2.8 mA, 2.8 mA, and 0.4 mA flowing through M7, M8, and M9 respectively. The PA has a simulated DC gain of

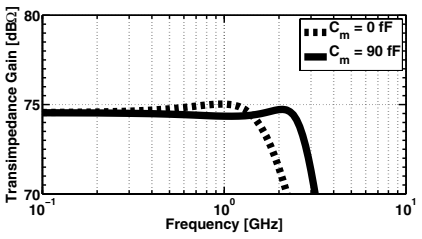


Fig. 4. Simulated frequency response of the TIA with and without negative Miller capacitance.

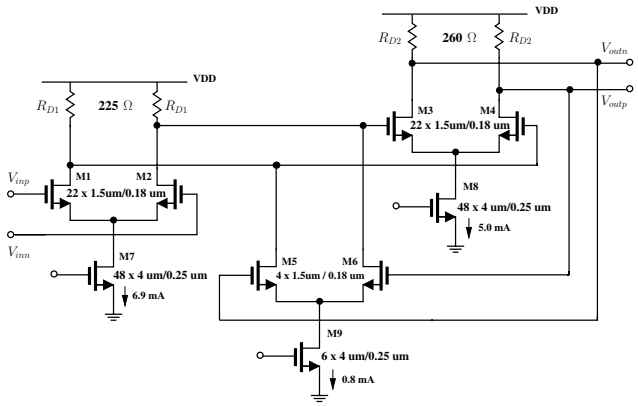


Fig. 5. Schematic of the subtracter.

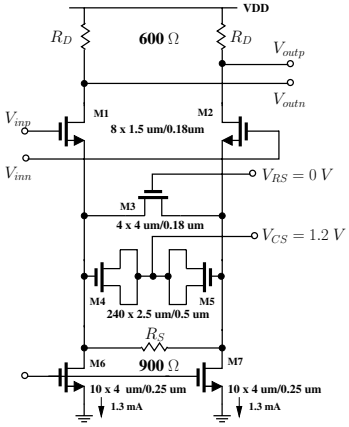


Fig. 6. Schematic of the equalizer.

39 dB, a small-signal bandwidth of 4.7 GHz through the first three stages, and an overall bandwidth of 3.7 GHz through all five stages. The cutoff frequency due to the offset cancellation must be low enough to avoid baseline wander; with a nominal value of 40 kHz.

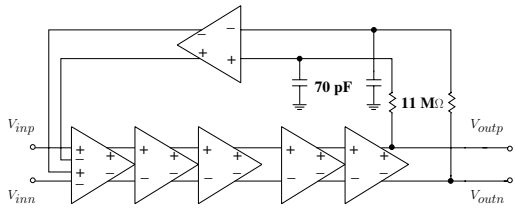


Fig. 7. Architecture of the PA.

IV. Measurement Results

The optical receiver was implemented in a one-poly six-metal 0.18-µm CMOS technology without the use of additional masks or anti-reflective coatings to enhance the optical performance of the photodetector. It occupies a core area of 0.72 mm^2. The die photo of the circuit is given in Fig. 8. An output buffer with 50 Ω on chip termination was employed to provide matching. A pattern generator (MP1701A) was used

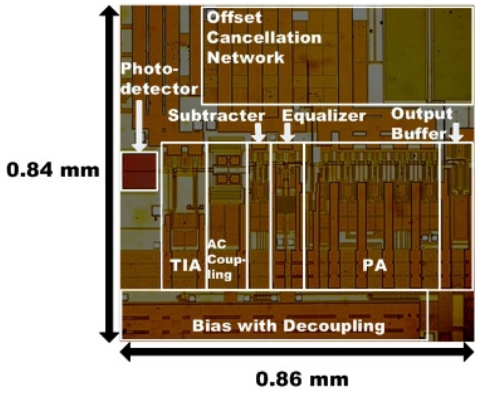
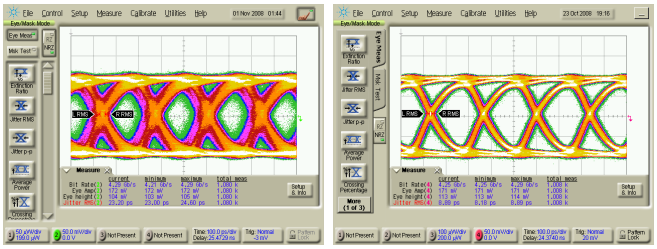


Fig. 8. Die photo of the fully integrated optical receiver.

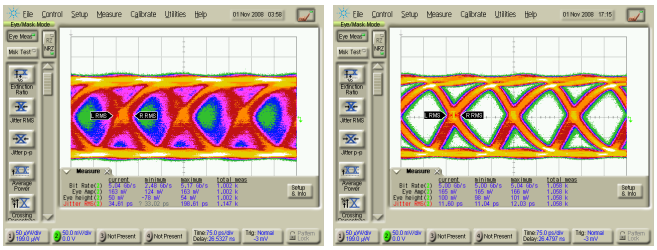


(a) (b)

Fig. 9. Measured eye diagrams in LP mode at 4.25 Gbps for a $2^{31}-1$ PRBS pattern and an average P_{opt} of -3 dBm with (a) equalization off and with (b) equalization on (horizontal scale: 100 ps/div, vertical scale: 50 mV/div).

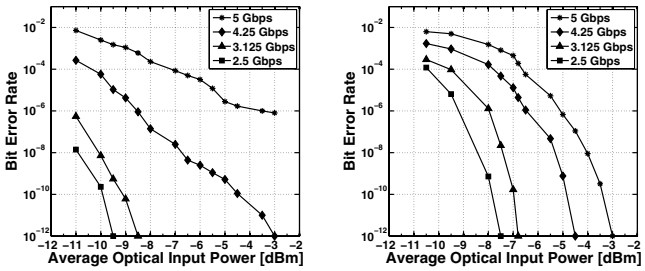
to modulate an 850-nm VCSEL as an optical source. A bit error rate (BER) tester (Anritsu MP1800A) was used for BER measurements.

The optical receiver was operated in two modes which differ only in the current consumption of the TIA. Hence, two sets of measurement were obtained. The first set of measurements (low-power, or LP) corresponds to a total current consumption of 9 mA in the TIA. The second set of measurements (high-performance, or HP) corresponds to a total current consumption of 20 mA in the TIA. A $2^{31}-1$ PRBS pattern was used to modulate the VCSEL. For the LP mode, the highest data rate with a BER less than 10^{-12} and an average optical input power, P_{opt}, of -3 dBm is 4.25 Gbps. In order to verify the performance improvement provided by the equalizer, the boosting must be eliminated. This was achieved by pulling both V_{RS} and V_{CS} to 1.8 V. The eye diagrams with equalizer off and equalizer on are shown in Fig. 9(a) and Fig. 9(b) respectively. For the HP mode, the maximum data rate with a BER less than 10^{-12} and an average P_{opt} of -3 dBm is 5 Gbps due to a larger TIA bandwidth. Shown in Fig. 10(a) and Fig. 10(b) are the eye diagrams with equalizer off and equalizer on respectively. The boosting of the equalizer was deactivated using the same approach done in the LP mode. The measured BER as a function of average P_{opt} at different data rates is shown in Fig. 11(a) and Fig. 11(b) for the LP mode and HP mode respectively.



(a) (b)

Fig. 10. Measured eye diagrams in HP mode at 5 Gbps for a $2^{31}-1$ PRBS pattern and an average P_{opt} of -3 dBm with (a) equalization off and with (b) equalization on (horizontal scale: 75 ps/div, vertical scale: 50 mV/div).



(a) (b)

Fig. 11. Measured BER as a function of average P_{opt} at different data rates under (a) LP mode and (b) HP mode.

V. Conclusion

The design of an optical receiver with monolithically integrated photodetector was investigated. A combined approach of a SML detector with an analog equalizer was used to extend the state-of-the-art data rate to 5 Gbps. To the authors' knowledge, it is the fastest photodetector integrated in a standard CMOS technology using standard supplies below 3.3 V. A low-noise TIA with high bandwidth and high transimpedance gain was also proposed. By employing negative Miller capacitance, the bandwidth of the TIA can be extended while keeping a flat frequency response. The measurement results of the optical receiver operating in two modes are compared with recently published photodetectors built in standard CMOS technology in Table I. Among the references mentioned in Table I, [2], [5], and [9] are the only ones that have an integrated TIA and PA together with the photodetector on chip. A more detailed comparison between these fully integrated optical receivers with this work is summarized in Table II. Although 5 Gbps was reported in [3], it used a very high supply at 13.9 V to reverse-bias its photodiode through a bias-T. In addition, the authors failed to report the sensitivity at 5 Gbps. Moreover, since TIA and PA were not integrated on chip with the photodetector, an external TIA was used for testing. In conclusion, the optical receiver achieves a better sensitivity at 2.5 Gbps and 3.125 Gbps at a BER less than 10^{-12} compared to [2] and [5] in both HP and LP modes. When operating in the LP mode, the optical receiver accomplishes so with less power consumption than [5]. The improvement in sensitivity justifies the design of the proposed low-noise TIA compared to the RGC stage. With a maximum data rate of 5 Gbps, it is the only fully integrated optical receiver operating at speeds exceeding 3.125 Gbps.

TABLE I
Photodetectors in standard CMOS technology

	Technology	Responsivity	Highest Supply	Data Rate
[1]	0.18-µm CMOS	-	1.8 V	3 Gbps
[2]	0.18-µm CMOS	-	6 V	2.5 Gbps
[3]	0.18-µm CMOS	0.38 A/W	13.9 V	5 Gbps
[4]	0.6-µm CMOS	0.1 A/W	5 V	250 Mbps
[5]	0.18-µm CMOS	0.07 A/W	3.3 V	3.125 Gbps
[9]	0.18-µm CMOS	0.03 A/W	1.8 V	1.2 Gbps
This work (LP)	0.18-µm CMOS	0.05 A/W	3.3 V	4.25 Gbps
This work (HP)	0.18-µm CMOS	0.05 A/W	3.3 V	5 Gbps

TABLE II
Detailed comparison of fully integrated optical receivers including photodetector, TIA, and PA

	Power	Data Rate	Sensitivity	Area
[2]	138 mW	2.5 Gbps	-4.5 dBm	0.53 mm^2
[5]	175 mW	3.125 Gbps	-4.2 dBm	0.7 mm^2
[9]	250 mW	1.2 Gbps	-8 dBm	4.5 mm^2
This work (LP)	144 mW	2.5 Gbps 3.125 Gbps 4.25 Gbps	-9.5 dBm -8.5 dBm -3 dBm	0.72 mm^2
This work (HP)	183 mW	2.5 Gbps 3.125 Gbps 4.25 Gbps 5 Gbps	-7.5 dBm -6.8 dBm -4.5 dBm -3 dBm	0.72 mm^2

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