A 15Gb/s AC-coupled VCSEL Driver with Waveform Shaping in 65nm CMOS

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***Abstract* — A Vertical Cavity Surface Emitting Laser (VCSEL) driver in 65nm CMOS selectively-enables parallel low-power CMOS drivers to shape the output current waveforms and compensate VCSEL nonlinearities. The CMOS waveform-shaping drivers are AC-coupled allowing them to operate from a 1-V supply to save power, while parallel low-frequency paths provide programmable DC biasing from a 3-V supply. The measured VCSEL driver is able to achieve 15Gb/s with up to 5.1dBm OMA at a total power dissipation of 60mW, or 2.1dBm OMA at 28mW corresponding to 1.9pJ/bit. The driver occupies 250 × 160µm including the on-die AC-coupling.**

I. Introduction

Directly modulated Vertical Cavity Surface Emitting Lasers (VCSEL) diodes can offer low cost and high density parallel communication links above 10Gb/s when assembled in linear or 2D arrays. However, to fully realize the benefits of parallel VCSEL-based optical links, a CMOS laser diode driver (LDD) can permit integration alongside CMOS logic and ultimately lower cost. Commercially-available low-cost VCSEL arrays are designed on n-doped substrates, making it impossible to independently modulate the cathode terminals. Thus, recent efforts have focused on anode-driving LDD architectures [1,2,3].

Slow VCSEL transient optical effects, device capacitance and nonlinear asymmetrical rise/fall-times can degrade performance above 10Gb/s. Additionally, packaging parasitics provide a complex impedance load to the LDD. Waveform shaping the LDD output current can provide a wider eye opening [4]. This work describes a CMOS LDD combining on-die AC-coupling and programmable waveform shaping for VCSEL-based optical links above 10Gb/s.

II. Transmitter Architecture Background

The LDD architecture depends significantly upon the VCSEL array type. Common-anode VCSEL arrays can be driven with all-NPN or all-NMOS cathode-driving LDDs, as shown in Fig. 1(a), achieving very high speed modulation due to the relatively low parasitic capacitance of those devices [5]. However, the majority of VCSELs are fabricated as common-cathode arrays due to lower defect densities of n-type substrates [6], requiring anode-driving LDDs.

The anode-driving architecture shown in Fig. 1(b) must source the sum total of the bias and modulation currents (I_{bias}+I_{mod}) from a high supply voltage V_{DDH}, which must exceed than the typical VCSEL operating voltages of 1.6–2.4V. Moreover, transistors in modern CMOS technologies have breakdown voltages below this range, requiring complicated biasing of the output stage.

Both issues can be addressed by AC-coupling the LDD to the VCSEL as shown in Fig. 1(c). In this configuration, the driver is shielded from the DC bias voltages at the VCSEL anode by a coupling capacitor. Hence, the LDD can use a voltage supply compatible with nanoscale CMOS logic transistors, since the AC voltage swing required for VCSEL modulation does not exceed 0.7 V. Lower power consumption is thereby attained, since LDD now sources only (I_{bias}+I_{mod}/2) from the high supply voltage, V_{DDH}, which is I_{mod}/2 less than in Fig. 1(b). The dynamic power required to charge the output node capacitance is sourced from the low supply voltage, V_{DDL}.

AC-coupling introduces an undesired lower cut-off frequency to the LDD's data transmission. Traditionally, a large, discrete coupling capacitor was required to minimize the resultant pattern-dependent vertical jitter. This issue can be addressed by modulating the current source between I_{bias} and I_{bias}+I_{mod} via a low-frequency driver (LFD) as shown in Fig. 1(d), thereby providing an additional path for any low-frequency signal content. For DC-balanced input data, the average power provided from the high-voltage power supply will remain V_{DDH}(I_{bias}+I_{mod}/2), which is the same as in (c). An AC-coupled VCSEL driver with on-chip integrated coupling capacitance was first introduced in [1], but lacked any pre-emphasis or waveform shaping capability, limiting its speed to 10Gb/s. In this work, programmable waveform shaping is incorporated into the high-frequency driver (HFD) operating from the low supply voltage, V_{DDL}.

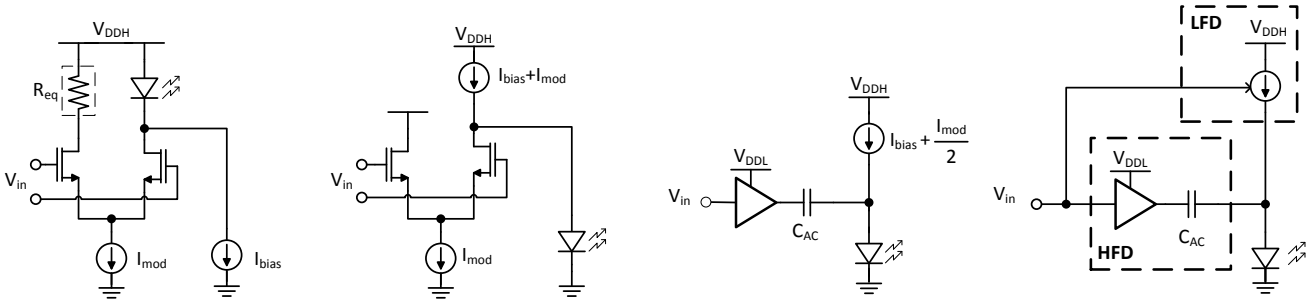


Fig. 1. (a) Common-anode VCSEL driver design; (b) Common-cathode VCSEL driver design; and (c) Common-cathode AC-coupled VCSEL driver design.

III. Circuit Design

The proposed LDD architecture consisting of an AC-coupled HFD and current-sourcing LFD is illustrated in Fig. 2(a). The input signal is buffered by a 50Ω CML buffer and amplified to CMOS logic swing levels by a CML/CMOS converter prior to being distributed to the various driver blocks. Example output driver waveforms are illustrated in Fig. 2(b). The LFD outputs a DC current (I_{bias}) required to bias the VCSEL above its lasing threshold, and the low-frequency component of the modulation current (I_m). The high-frequency components of the modulation current I_{mod} is generated by the HFD.

In order for the LDD to produce a flat broadband output current, the LFD and HFD cut-off frequencies (f_c), amplitudes, and switching times must match. In [1], the cut-off frequencies are matched by tuning the LFD bandwidth by means of an adjustable capacitor. In this work, both the LFD and HFD cut-off frequencies are determined by the output node time constant, thus achieving frequency matching automatically without the need for tuning. A high-speed current mirror LFD has allowed the cut-off frequency to be increased to 3–5GHz and permitted the use of a smaller AC-coupling capacitor than in [1], where the cut-off frequency is between 100–500MHz.

LFD modulation current (I_m) is made programmable from 0 to 12mA by partitioning the PMOS current mirror and CML pre-drivers into thermometer-coded slices. Circuit detail of one LFD output stage slice is shown in Fig. 3. The LFD sources I_m (and I_{bias}) from 2.5V thick-oxide PMOS current mirrors to prevent device breakdown from overvoltage when operating from a 3.0V supply. The DC output on-current is determined by the 1:8 mirror ratio. A capacitively-coupled CMOS inverter rapidly

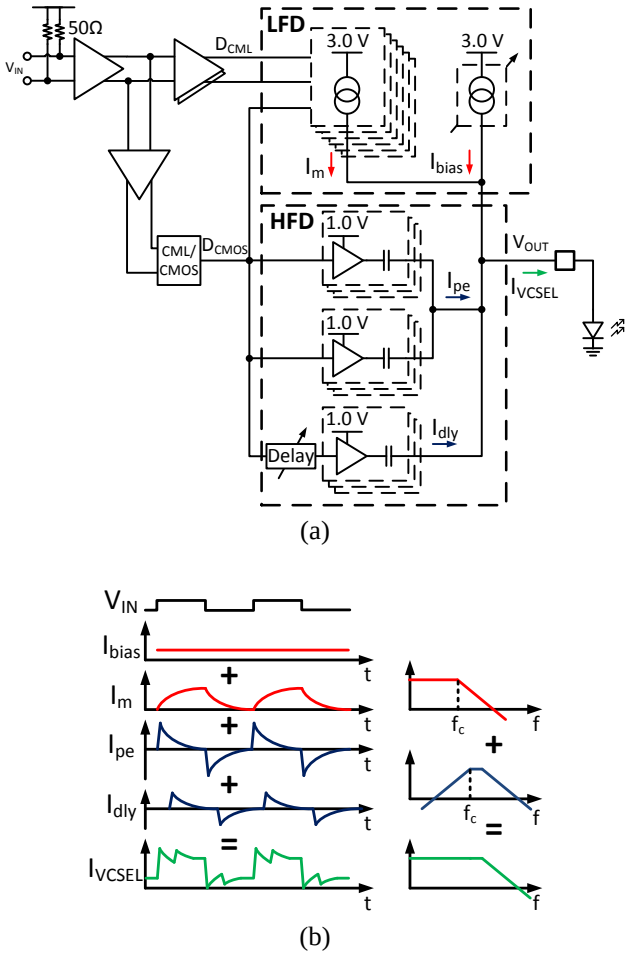


Fig. 2. (a) Top level schematic; (b) Waveform illustrations.

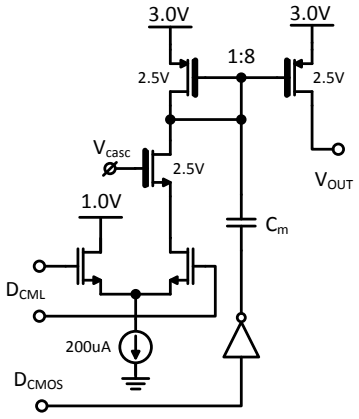


Fig. 3. LFD output stage schematic.

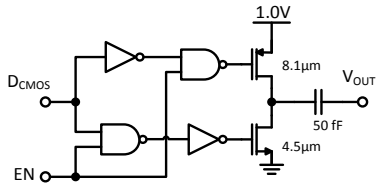


Fig. 4. HFD output LSB slice schematic.

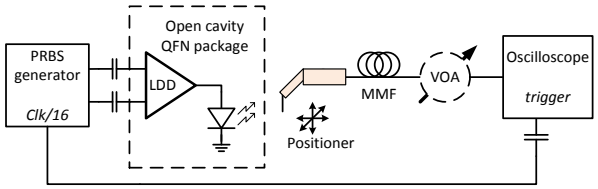


Fig. 6. Test setup diagram.

modulates the gate voltage of a current mirror slice, increasing the intrinsic bandwidth of the LFD to 10-15GHz, depending on the temperature and process corner. The coupling capacitor C_m is sized such that the voltage swing generated by the inverter is sufficient to completely switch off the current in the PMOS device. Since the LFD transitions is triggered by the CMOS signal D_{CMOS} used by the HFD path, the transition instant of the HFD and LFD drivers are guaranteed to be concurrent.

HFD circuits use thin-oxide transistors operating from a standard 1.0V CMOS logic supply. As shown in Fig. 2, the HFD is partitioned into 3 groups of 3-bit programmable binary-weighted parallel slices, with an LSB unit capacitance of 50fF. Unlike the design in [1], where the gain of the HFD is tuned by the means of an adjustable voltage regulator, HFD gain is digitally programmed by enabling the desired fraction of available capacitor slices. This approach is more efficient since it does not require a programmable LDO. Additionally, since the gain of the HFD is no longer dependent on the supply voltage, this design allows the LDD to operate with a smaller modulation current without any decrease in speed. In order to minimize the capacitive loading on the output node, unused coupling capacitor slices are disabled by tri-stating the driver slice's output, as shown in Fig. 4.

In addition to the main emphasis driver that switches concurrently with the LFD, a 350fF portion of the coupling capacitance is allotted to generate a secondary emphasis pulse I_{dly}. The double-emphasis technique is used to mitigate any optical ringing caused by the VCSEL's relaxation oscillation [4]. The secondary emphasis delay is generated with programmable CMOS logic, which consumes considerably less power than the CML logic in [4]. This type of pre-emphasis would be impossible with a larger coupling capacitance.

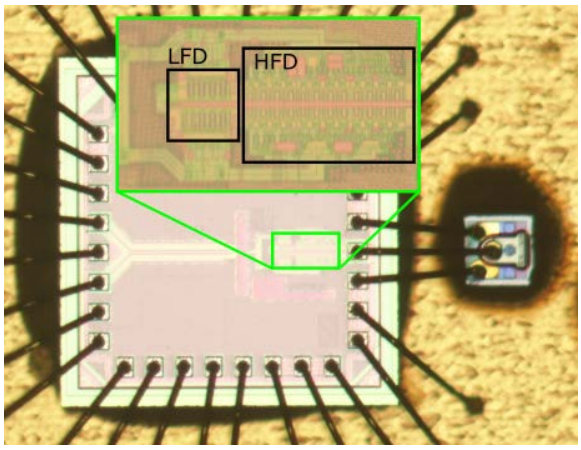


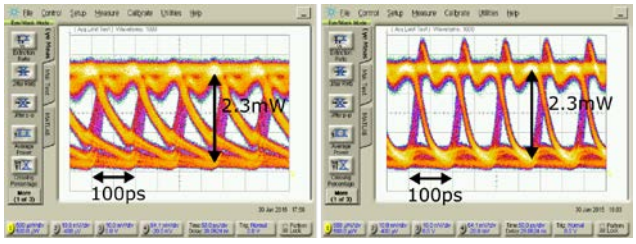
Fig. 5. Microphotograph of VCSEL driver fabricated in TSMC 65-nm technology. Inset shows an annotated close-up of the LDD layout.

IV. Fabrication and Measurement Results

The proposed driver was fabricated in a standard 65-nm bulk CMOS process. Fig. 5 shows the LDD directly wire-bonded to a common-cathode VCSEL chip. The VCSEL ground pads are wire-bonded back to the LDD to reduce the packaging inductance. The pre-driver and LDD occupy an area of 250 × 160 µm^2 including the HFD coupling capacitance.

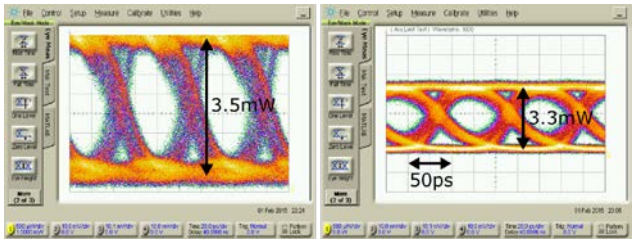
Fig. 6 shows the test setup. A 300mV$_{pp}$ swing PRBS input sequence was generated by a Keysight N4960 BERT. Whereas PRBS7 testing was used in [1], in this work PRBS31 NRZ sequences were used for all measurements in order to capture the effect of many consecutive identical digits through the AC-coupled HFD. A Keysight 86100C oscilloscope was used to directly capture the optical eye diagrams using a Keysight 86105D 20-GHz optical module. Some optical coupling losses are expected due to the manual VCSEL-fiber lens alignment.

Fig. 7(a) demonstrates the asymmetrical VCSEL step response when driven only by the LFD with 10Gb/s data. A slow falling edge and the VCSEL's relaxation oscillation during the rising edge can be observed. An improved eye opening due to pre-emphasis compensation from the HFD is shown in (b).



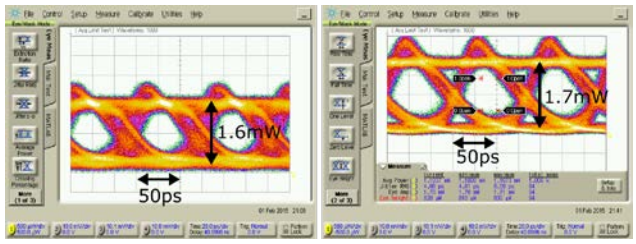
(a) (b)

Fig. 7. Optical measurements of VCSEL step response (a) LFD only (b) LFD and HFD primary emphasis.



(a) (b)

Fig. 8. Optical eye diagram at 15Gb/s and 12mA modulation current: without (a) and with (b) secondary emphasis applied.



(a) (b)

Fig. 9. Optical eye diagram at 15Gb/s and 6mA modulation current: without (a) and with (b) secondary emphasis applied.

The 15Gb/s optical eye diagram taken for the maximum 12mA LDD modulation current setting is shown in Fig. 8. A variable optical attenuator was inserted as indicated in Fig. 6 to display the 5.1dBm optical modulation amplitude (OMA) on the oscilloscope shown in subfigure (b). A clear eye opening could be obtained with a bias current of only 1.1mA by applying an appropriately-timed secondary emphasis pulse to compensate for the undershoot at the rising and falling edges.

At a similar bias current setting, the transmitter could be configured into a low power mode by decreasing the modulation current. Fig. 9 shows the measured optical eye diagram for a modulation current of 6mA, resulting in a measured OMA of 2.3dBm and 8.9dB ER. With secondary emphasis applied, the eye-opening height and width were 48% and 63%, respectively. For this measurement, the HFD was programmed to 350fF for the first primary emphasis and 200fF secondary emphasis. Excluding the 50Ω input buffer power, the LDD and VCSEL consume 28.1mW.

TABLE I
COMPARISON TABLE OF ANODE-DRIVING LDDS

Reference	This work		[1]	[2]	[3]
Topology	AC-coupled			DC-coupled	
Technology	65nm CMOS		65nm CMOS	65nm CMOS	8HP BiCMOS
Bit rate (Gb/s)	15	15	10	26	25
Power (mW)	28.1	59.8	69.5	46.9	60
Efficiency (pJ/bit)	1.9	4.0	6.9	1.8	2.4
Supply voltages	1.0,2.5	1.0,3.0	1.2,3.3	1.0,3.0	2.5,3.3
Area (mm^2)	0.04		0.128	0.024	0.09
OMA (dBm)	2.3	5.1	6.4	1.8	N/A
I_{mod} (mA_{pp})	6	12	8	8	4
I_{bias} (mA)	1.1	1.1	3	6	2

VII. CONCLUSION

In this paper, an anode-driving VCSEL transmitter was demonstrated at a data rate of 15Gb/s with on-chip AC-coupling and programmable waveform shaping. The LDD was fabricated in a standard TSMC 65nm GP CMOS process. Recently reported anode-driving LDDs are listed in Table 1. Compared to the AC-coupled architecture in [1], this work was able to achieve a higher efficiency and faster data rate by including waveform shaping, and the use of a fixed low supply voltage eliminating the need for a programmable LDO for the HFD supply. At a high OMA setting, the two drivers have comparable power consumption due to the large modulation current being a major fraction of the overall power. Compared with DC-coupled works, this driver has a smaller circuit area and higher OMA. Moreover, since this architecture relies only upon core nanoscale CMOS transistors operating from a 1V supply for the signal path, it is expected to benefit significantly from scaling to more advanced CMOS technology nodes, which will afford higher data rates, smaller area and improved energy efficiency in the future.

ACKNOWLEDGMENT

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