Two-tap travelling-wave infinite impulse response filter with 12 dB peaking at 24 GHz

G. Ng, F.A. Musa and A.C. Carusone

A two-tap infinite impulse response (IIR) filter using travelling-wave architecture is presented. The filter utilises poles as a means of frequency boosting, contrasting the conventional finite impulse response technique of utilising zeros and is the first ever implementation of an IIR filter using a double-loop multi-delay topology. Implemented in a 90 nm CMOS process, the filter achieves a 12.1 peak at 24 GHz when both filter taps are set to maximum peaking and consumes 55.2 mW from a 1.2 V supply.

Introduction: Distributed circuit techniques have been studied extensively for the implementation of finite impulse response (FIR) filters. The 'travelling-wave filter' architecture was first presented for this purpose in [1] and has recently been applied to the design of integrated circuit equalisers operating at 10s of Gbit/s [2]. Modifications to the architecture have been suggested in [3–5], but have always focused on FIR filters. This Letter considers the use of travelling-wave filter techniques for the implementation of an infinite impulse response (IIR) filter.

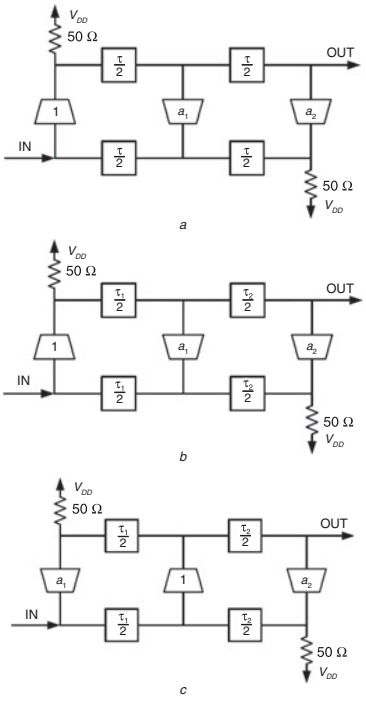

Fig. 1 *All pole travelling-wave IIR filter topologies with two-taps*

a Direct form (uniform delay)
b Multi-delay
c Double-loop multi-delay

IIR filter topology: Fig. 1*a* shows a top-level block diagram of a direct form two-tap IIR filter that uses a travelling-wave topology with only poles in its transfer function. Owing to the absence of a feed-forward path, zeros are eliminated from the transfer function of the filter thus simplifying the hardware required to implement the filter. The total loop delay from the input to the output through the first tap a_1 is τ and the total loop delay from the input to the output through the second tap a_2 is 2τ. Ideally the frequency at which peaking is observed in the magnitude response of the all pole IIR filter is given by

$$f_{peak} = \frac{1}{2\tau_d} \tag{1}$$

where τ_d is the total delay around a feedback loop that includes an active amplifier. Thus, ideally tap a_1 produces a peak at $1/(2\tau)$ whereas tap a_2 produces a peak at $1/(4\tau)$.

A drawback of the direct form all pole IIR topology is the double-peaking behaviour observed when utilising the low frequency tap, a_2, with the high frequency tap, a_1, turned off. This arises from the periodic nature of the filter peaks and the finite bandwidth of the delay line segments. Moreover, with the high frequency peak twice as large as the low frequency peak, it becomes difficult to place both peaks within the frequency band of interest. Practically, it would be desirable to bring the low and high frequency peaks close enough to each other to permit them to create a single peak, providing frequency boosting over a broader range. To bring the peak frequencies closer, the direct form all pole IIR can be modified into the multi-delay IIR section as shown in Fig. 1*b*. Here the delay section τ_1 determines the peak location for tap a_1 while the delay section $\tau_1 + \tau_2$ determines the peak location for tap a_2. By allowing different segment delays, the multi-delay IIR filter allows two peak frequencies to be placed in close proximity to each other while suppressing any undesired secondary peak with the low frequency tap on. A major drawback of this topology is that τ_2 cannot be selected independently from τ_1. Consequently, the delay τ_2 would be forced to be small in order to bring the peaking frequencies close together. To alleviate this problem, the multi-delay IIR filter can be modified as shown in Fig. 1*c* to form a double-loop. By introducing two independent feedback loops, the delays τ_1 and τ_2 can be sized independently according to the desired peak frequencies.

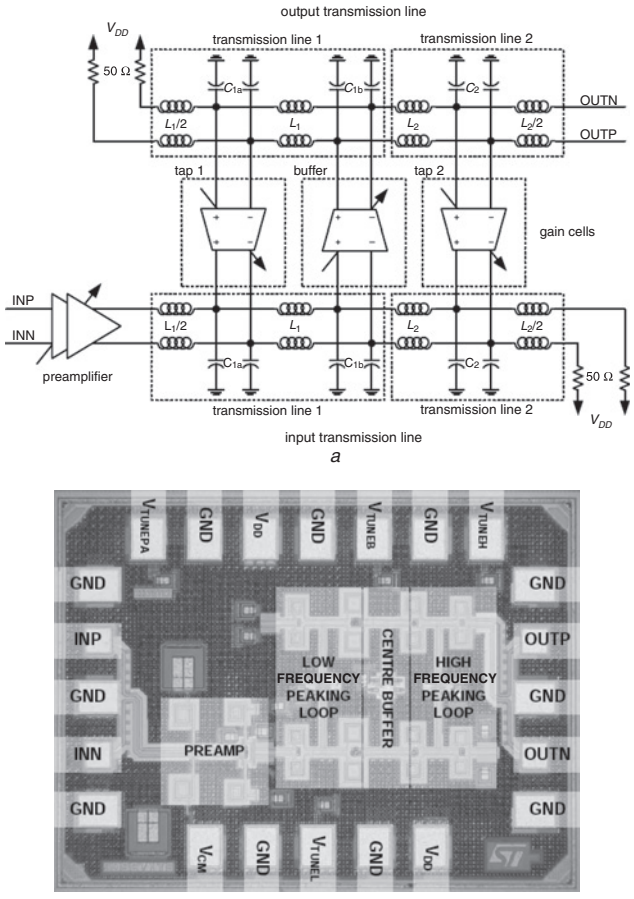

Fig. 2 *Double-loop multi-delay IIR filter*

a Schematic diagram
b Die photo

Double-loop multi-delay IIR filter design: Fig. 2*a* shows the top-level block diagram of the double-loop multi-delay all pole IIR filter that uses a travelling-wave architecture. The filter delays are realised using lumped LC transmission sections. Ideally an LC transmission line can be used to introduce a delay ΔT and characteristic impedance Z_o:

$$\Delta T = \sqrt{LC} \tag{2}$$

$$Z_o = \sqrt{\frac{L}{C}} \tag{3}$$

Rearranging (2) and (3), the values of L and C can be determined to realise a certain delay ΔT and characteristic impedance Z_o:

$$L = Z_o \Delta T \tag{4}$$

$$C = \frac{\Delta T}{Z_o} \tag{5}$$

Referring to Fig. 2*a*, the loop containing transmission line 1, tap 1 and buffer forms the low frequency peaking path while the loop containing transmission line 2, tap 2 and buffer forms the high frequency peaking path. Both transmission line segments were designed to have 50 Ω characteristic impedance. The first segment, transmission line 1, is designed to have 9.375 ps delay. Using (4) and (5), initial values for L_1 and C_{1a} (or C_{1b}) were chosen as 468 pH and 178 fF, respectively. Similarly, transmission line 2, is designed to have a 5 ps delay resulting in 250 pH and 100 fF for L_2 and C_2, respectively. The filter utilises two differently sized gain cells. The centre buffer gain cell is larger than the feedback gain cells. The gain cells are sized such that the device and parasitic capacitances account for a maximum of 60% of the total node capacitance. The final values of inductance and capacitances were: $L_1 = 370.1$ pH, $L_2 = 220.1$ pH, $C_{1a} = 79.6$ pF, $C_{1b} = 35.4$ pF and $C_2 = 26$ pF. A lumped two-stage preamplifier that is matched to a 100 Ω differential system impedance precedes the filter. The tail currents of the preamplifier and the gain cells were made adjustable through current mirrors to control their gains.

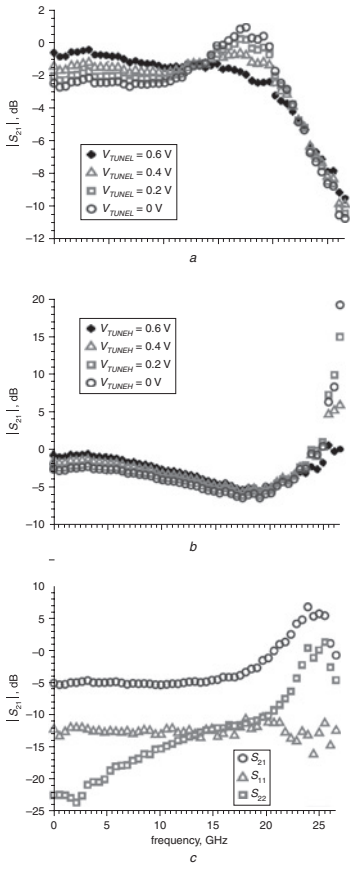

Fig. 3 *S_{21} measurements results*

a High-frequency tap off, low frequency tap gain is varied through on-chip current mirror

b Low-frequency tap off, high frequency tap gain is varied through on-chip current mirror

c Both low and high frequency taps are varied to achieve maximum peaking

Measurement results: The IIR filter was implemented in a 90 nm CMOS process and occupied an area of 0.85 × 0.625 mm. Fig. 2*b* shows the die photo. All circuit measurements were performed on-wafer. Fig. 3*a* plots the measured S_{21} of the filter with the high frequency tap off and for varying gain settings for the low frequency tap. A maximum peak gain of 3.4 dB is observed at 17 GHz. With the high frequency tap on and low frequency tap off, the maximum peak gain is 21.7 dB at 26.5 GHz. This is shown in Fig. 3*b*. With both taps on, the filter produces a 12.1 dB peak at 24 GHz. Under these conditions the filter consumes 55.2 mW from a 1.2 V supply.

Conclusion: The ability of IIR filters to produce peaking at high frequencies is demonstrated. A novel double-loop multi-delay two-tap IIR filter toplogy is developed that removes undesired double peaks and potentially decouples the taps from each other so that the taps can define the high and low frequency peaks independently. Implemented in 90 nm CMOS, the filter produces a peak of 12.1 dB at 24 GHz with both taps on.

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