# A 38-Gb/s 2-tap Transversal Equalizer in 0.13-μm CMOS using a Microstrip Delay Element

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***Abstract*—This paper describes a single-ended integrated transversal 2-tap feed-forward equalizer implemented using a commercial 0.13-μm CMOS process. Equalization of a 38-Gb/s data stream over SMA cables with 14.3 dB of channel loss is demonstrated on-wafer. The equalizer features a microstrip transmission line as the delay element and "line inductors" for improved impedance matching. The IC measures 1.5 mm × 0.26 mm, and consumes 30 mW of power from a 1.2 V supply.**

***Index Terms*—Equalizers, CMOS integrated circuits, transversal filters, finite impulse response, microstrip**

## I. Introduction

As data transmission rates continually increase into the tens of gigabits range, frequency dependent channel losses pose a significant challenge to successful data transmission. Finite impulse response (FIR) equalizers serve an important role in many of these communication links by compensating for the inter-symbol interference (ISI) introduced by these channels. This paper presents the design of a 2-tap transversal FIR filter in a commercial 0.13-μm CMOS process which could be used for such an application. A simple 2-tap FIR equalizer can be applied to compensate for frequency dependent losses in chip-to-chip backplanes, cable channels, as well as modal dispersion in short multimode fiber links.

## II. Transversal Filter

A 2-tap FIR equalizer can be implemented in two ways: as a traveling wave filter (TWF) or as a transversal filter (TVF). The traveling wave filter splits the delay element between the input and output, whereas the transversal filter uses a single delay element between the taps.

For passive implementations, each topology offers its own advantages and disadvantages. There are several benefits of using the traveling wave filter topology. Most notably, a TWF has been demonstrated to be robust in its ability to compensate for reflections caused by termination impedance mismatch and series loss [1]. In the case of a TWF the presence of termination impedance mismatches only result in reflections within the span of the equalizer, thus can be compensated for by adjusting the tap weights accordingly. In the case of a TVF the presence of termination impedance mismatches result in reflections that appear outside the span of the equalizer, which cannot be compensated for by adjusting the tap weights.

Compared to traveling wave filters, transversal filters can offer a gain advantage. It is difficult to design an integrated transmission line with characteristic impedances higher than several hundred ohms that is also low loss at frequencies in the tens of gigahertz. Since the output side of a traveling wave filter is a transmission line delay element, it must have an output impedance that is at maximum several hundred ohms, terminated by a matching lumped load at the output. This restriction does not exist for a transversal filter, as the outputs of the transversal filter are directly tied to the lumped load. This situation is advantageous when driving on-chip loads where impedance matched terminations are not necessary. This advantage exists only in a transversal filter due to the co-location of the tap outputs, making it unnecessary to connect the tap outputs to each other and to the load through a transmission line. All previous implementations of FIR equalizers above 10 Gb/s with passive delay elements have employed a traveling wave structure [2], [3] or variants thereof [4], [5].

A single-ended design of the equalizer was chosen over a differential design. This allows the equalizer to be cascaded directly after the transimpedance amplifier (TIA), which is also single-ended in optical fiber or coaxial cable communication applications. Otherwise, the design may be straightforwardly modified into a fully differential circuit.

The delay element between the taps of the TVF can be implemented passively in two ways: using an artificial L-C transmission line or a microstrip transmission line. Other options for the distributed transmission line would be a strip line or a grounded coplanar waveguide (CPW), but both were ruled out since they result in more resistive conductor traces for the same characteristic impedance, thus would be more lossy. For the current circuit implementation, a microstrip transmission line was selected as the delay element. Utilizing a microstrip transmission line can offer advantages over a lumped L-C transmission line. A microstrip delay line allows the transmission line to be wrapped in a "U" shape making it simple to route both equalizer taps to a common summation node. This long narrow shape may be easier to fit in some receiver layouts. Since there are no inductors, it is easier to accommodate metal fill rules, especially if the inductor is large. Microstrip lines also have an inherently higher bandwidth due to their distributed nature. Whereas it is necessary to use special techniques to achieve baud-spacing with sufficient bandwidth due to the lumpiness of artificial transmission lines [4], [5], a single length of microstrip line can simply be used to achieve baud-rate tap spacing. This simplifies both the design and modeling of the interconnects.

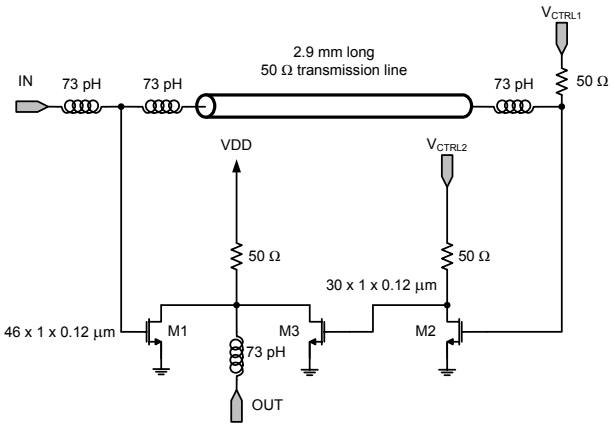



Fig. 1. 2-tap transversal FIR filter circuit schematic.

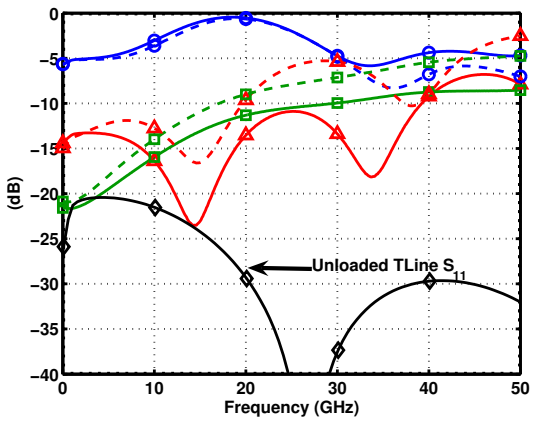



Fig. 2. Simulated transversal equalizer impedance matching. Unloaded transmission line $S_{11}$ (diamond solid line). S-Parameters for $V_{CTRL1} = 0.82$ V, $V_{CTRL2} = 0.85$ V. $S_{21}$ (circle), $S_{11}$ (triangle), and $S_{22}$ (square). Before addition of line inductors (dashed lines). After addition of line inductors (solid lines), the $S_{11}$ and $S_{22}$ are below -10 dB for frequencies up to 30 GHz.

Previous FIR equalizers at these speeds that use microstrip delay lines have employed a TWF structure with fractional tap spacing, (for example, $T_{baud}/4$ in [2]). In this design, small "line inductors" are used so that a single distributed element can provide baud-rate tap spacing while maintaining a very constant input impedance up to 30 GHz.

## III. Circuit Design

The full circuit schematic of the implemented single-ended 2-tap transversal FIR equalizer is shown in Fig. 1. Common-source amplifiers are used as the tap transconductors. Located at the input of the equalizer, transistor *M1* forms the first equalizer tap. The cascaded transistors *M2* and *M3* form the second tap of opposite polarity, a condition needed to create peaking. Signal inversion was performed with an additional common-source stage at the end of the transmission line instead of at the beginning to introduce additional signal delay, thus increasing the effective inter-tap delay and shortening the required transmission-line length. The majority of the inter-tap delay is provided by a 50 Ω microstrip transmission line that is terminated by a matching load resistor. In this design the tap outputs are summed in the current domain on a 50 Ω resistor which also provides output impedance matching, although a higher load resistance could have been used to provide high gain if driving on-chip loads only.

Transistor *M1* is the main tap, thus it is chosen slightly larger than the secondary tap transistors *M2* and *M3*, since greater gain is desired through the main tap of the equalizer. Transistor *M1* is biased near peak $f_T$ current density at 0.26 mA/µm with a nominal gate voltage of 0.82 V. The bias current densities of *M2* and *M3* depend on the tuning voltage $V_{CTRL2}$. Transistor *M2* is biased at a maximum current density of 0.27 mA/µm when 0.82 V is applied at the gate of *M2* via $V_{CTRL1}$ and the tuning voltage $V_{CTRL2}$ is set at 1.2 V. The nominal supply voltage $V_{DD}$ for the equalizer is 1.2 V.

Two analog voltages, $V_{CTRL1}$ and $V_{CTRL2}$, are used to control the tap gains. The voltage $V_{CTRL1}$ provides the gate voltages of both *M1* through the transmission line and *M2*. Tuning the DC voltage on $V_{CTRL1}$ adjusts the gain through the first (main) equalizer tap. Adjusting the voltage on $V_{CTRL2}$ changes the gate voltage on *M3*, which in turn adjusts the amount of peaking produced by the equalizer. No peaking is produced when $V_{CTRL2}$ is set to 0 V (transistor $M3$ and, hence, tap 2 turned off) and maximum peaking when set to 1.2 V.

### A. Microstrip Transmission Line

The 50 Ω microstrip line is 2.9 mm in length and provides 18.2 ps of group delay. The microstrip width is 9 µm. The transmission line utilizes a "U" shaped layout to allow both equalizer taps to be easily routed together.

As shown by the diamond solid line Fig. 2, the unloaded transmission line input impedance is well matched with the $S_{11}$ below -20 dB for all frequencies. However, once the transconductors are connected to both ends of the transmission line, the capacitive loading degrades the input impedance match of the equalizer. From the dotted line S-parameters shown in Fig. 2, the $S_{11}$ of the equalizer is degraded such that it is above -10 dB at frequencies greater than 20 GHz. A $S_{22}$ above -10 dB at frequencies greater than 20 GHz is caused by the large capacitance associated with tying the output of the transconductors together.

### B. Line Inductors

In order to improve the input and output matching of the TVF, a small amount of inductance was added around the nodes where the transconductors are connected. This tunes out the lumped parasitic capacitances of the MOS devices and hence the impedance mismatch caused by the transconductors can be reduced [6]. To keep the equalizer layout long and narrow, "line inductors" instead of regular spiral inductors were employed. The "line inductors" are simply long narrow strips of metal which are inductive due to the skin effect. The

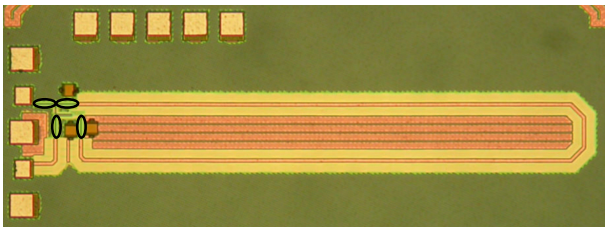


Fig. 3. 2-tap transversal FIR filter die photo. Line inductors are circled.

"line inductors" used measure 60 µm in length and 1.5 µm in width. Their inductance simulated by *ADS Momentum* is 73 pH. The "line inductors" are shown in the circuit schematic in Fig. 1 and are circled in the die photo in Fig. 3.

The improvement in matching with the addition of the "line inductors" can be seen from the solid lines in Fig. 2 for arbitrary tap control voltages $V_{CTRL1}$ = 0.82 V and $V_{CTRL2}$ = 0.85 V. Both the $S_{11}$ and $S_{22}$ are now below -10 dB for frequencies below 30 GHz. The addition of the "line inductors" did not impact the frequency or the magnitude of the peaking as shown by the $S_{21}$ curve. The simulated peak frequency of the equalizer remains at 18.5 GHz with a maximum peaking of 9 dB when $V_{CTRL2}$ is set at 1.2 V.

### C. Circuit Layout

The die photo of the circuit is given in Fig. 3. The size of the equalizer IC excluding pads is 1.5 mm × 0.26 mm.

## IV. Measurement Results

All circuit measurements were made on-wafer. A 1.2 V supply was used, and tuning voltage $V_{CTRL1}$ was fixed at the nominal voltage of 0.82 V.

One-port S-parameter measurements were made to characterize the input and output impedance match $S_{11}$ and $S_{22}$. Fig. 4 shows both the measured and simulated impedance match when the FIR equalizer is operated with maximum peaking. This is the worst case operating condition for matching as there is increased capacitance due to the Miller effect of the common-source amplifiers. The plot of $S_{22}$ shows excellent agreement between the measurements and simulations, staying below -10 dB up to the maximum measured frequency of 26.5 GHz. The measured $S_{11}$ matches simulations reasonably well, largely remaining below -10 dB, except at 5.6 GHz where it peaks at -9.2 dB. This may be caused by un-modeled interactions between the line inductors and the surrounding layout.

When operated with no peaking, the equalizer consumes 14.4 mW from a 1.2 V supply. With maximum peaking, the equalizer consumes 30 mW from a 1.2 V supply.

Channel equalization measurements were performed at 38 Gb/s. The input pattern was generated by multiplexing four $2^7 - 1$ independent NRZ PRBS sequences at various bit rates.

Fig. 5 shows the measured frequency response of the channel comprising 6-ft of SMA cable (a cascade of two 3-ft SMA cables) and a 3-ft section of 50 GHz cable.

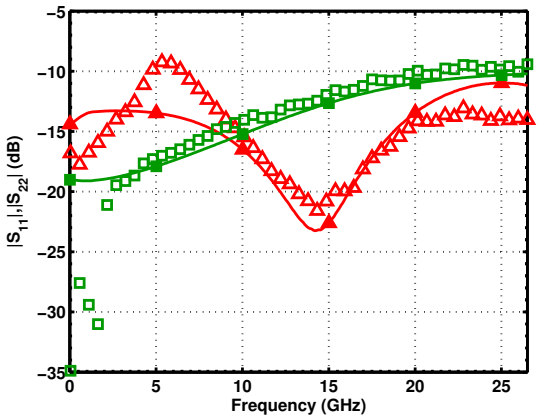



Fig. 4. Measured FIR input and output impedance match for maximum peaking mode of operation. Measured $S_{11}$ (triangle), $S_{22}$ (square). Simulated $S_{11}$ (solid line filled triangle), $S_{22}$ (solid line filled square).

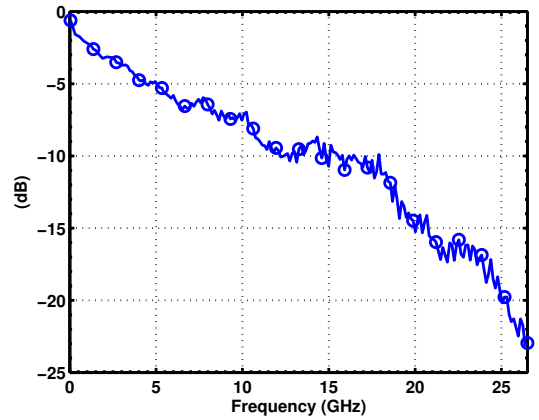
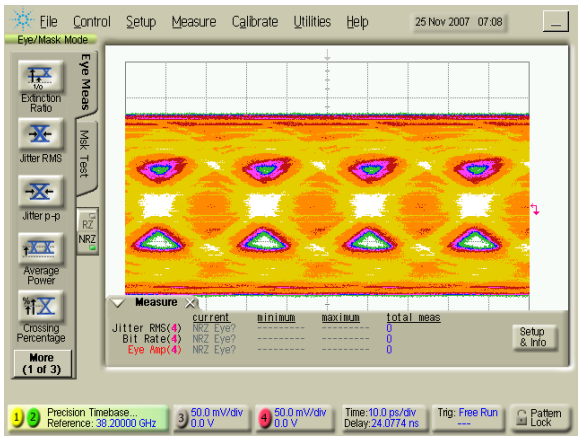


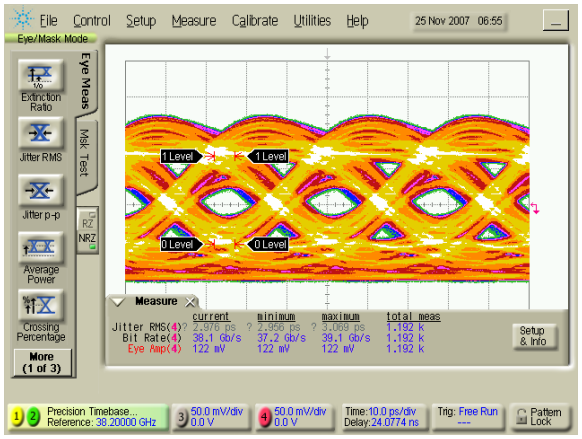

Fig. 5. Channel frequency response. Channel consists of 6-ft of SMA cable and a 3-ft section of 50 GHz cable.

Channel equalization was performed at 38.2 Gb/s. Based on the channel frequency response, a 38.2-Gb/s signal experiences 14.3 dB of attenuation at one-half the bit rate (19.1 GHz). Fig. 6(a) shows the closed and unequalized eye through the channel. Setting the tuning voltages $V_{CTRL1}$ at 0.82 V and manually tuning the peaking control voltage $V_{CTRL2}$ to 0.88 V, results in the equalized eye shown in Fig. 6(b). The equalized eye shows a significant improvement in eye opening. Similar experiments were performed at other data rates showing similar or better performance from 30 - 38 Gb/s.

Although the power gain $S_{21}$ could not be directly measured to determine the peak frequency, the transient eye diagram measurements provides some insight into the FIR equalizer's frequency response. The ability for the equalizer to compensate for channel loss at data rates between 30 and 38 Gb/s indicates that the equalizer has a peaking frequency in the range between 15 to 19 GHz which corresponds well with the simulated peak frequency at 18.5 GHz.




(a)




(b)

Fig. 6. Measured 38.2-Gb/s eye diagrams. (a) Unequalized eye. (b) Equalized eye.

The 1-dB compression point of the FIR equalizer was measured for the no peaking mode of operation. The losses of the input and output cables, decoupling capacitor, and bias-tee were manually de-embedding from the presented results using spectrum analyzer measurements. Only the probe losses are unaccounted for in the results. A plot of the 1-dB compression point as well as the second and third harmonics HD2 and HD3 respectively is shown in Fig. 7 for a 2 GHz input tone. The measured input referred 1-dB compression point is 1.8 dBm. The total harmonic distortion (THD) at the 1-dB compression point is -27.5 dB.

Based on the input and output power measurements, the DC gain of the FIR equalizer is determined to be approximately 0.3 dB, subject to de-embedding errors.

## V. Conclusion

This paper shows the design and measurement of a 2-tap transversal equalizer in 0.13-µm CMOS. The equalizer utilizes a "U" shaped microstrip transmission line as the lone delay element with small series "line inductors" to maintain a constant input and output impedance up to 30 GHz. The fabricated die measures 1.5 mm × 0.26 mm and consumes a maximum of 30 mW from a 1.2 V supply. Equalization of a 38-Gb/s data stream with 14.3 dB of channel attenuation was successfully demonstrated. A comparison with other recently reported IC equalizers is presented in Table I.

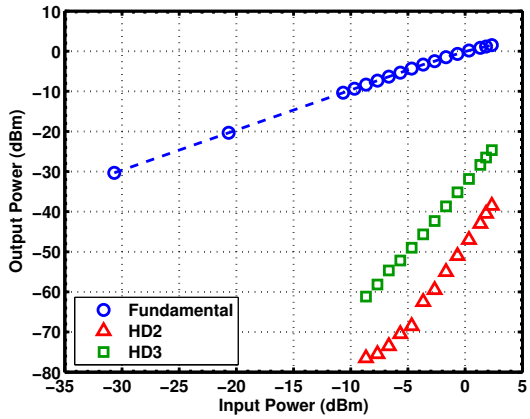



Fig. 7. Measured 1-dB compression point and harmonics.

TABLE I
Comparison with other recently reported IC equalizers

| | **This Work** | [4] | [5] | [2] | [3] |
|---|---|---|---|---|---|
| Technology | 0.13-µm CMOS | 0.18-µm CMOS | 90-nm CMOS | 0.18-µm SiGe BiCMOS | InP-HBT |
| Data rate (Gb/s) | 38 | 40 | 30 | 49 | 43 |
| Channel Type | SMA | SMA | SMA | SMA (6.5 ft) | SMF (405 km) |
| Channel Loss (dB) | 14.3 | 15 | 14.4 | - | - |
| Tap Spacing (ps) | 18.2 | 25 | 35 | 6.75 | 12.5 |
| Number of Taps | 2 | 3 | 3 | 7 | 4 |
| Delay Type | µstrip | L-C | L-C | µstrip | CPW |
| Supply (V) | 1.2 | 1.8 | 1 | 5 | -5.2 |
| Power (mW) | 30 | 70 | 25 | 750 | 1500 |
| Area (mm × mm) | 1.5×0.26 | 1.0×1.0 | 0.6×0.5 | 2.0×1.0 | 1.5×3.0 |

## Acknowledgment

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