

Session RMO3B-2

A 38-Gb/s 2-tap Transversal Equalizer
in 0.13- μm CMOS using a Microstrip
Delay Element

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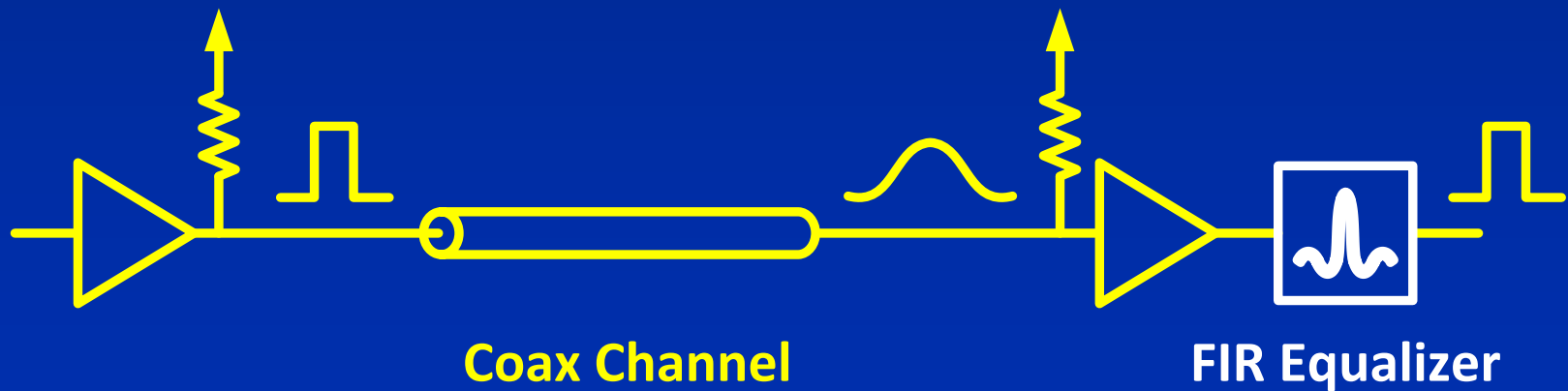
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Outline

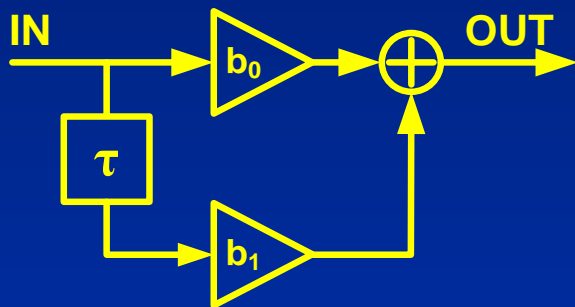
- Motivation
- 2-tap FIR equalizer topologies
- Circuit design
- Measurement results
- Conclusion

Motivation

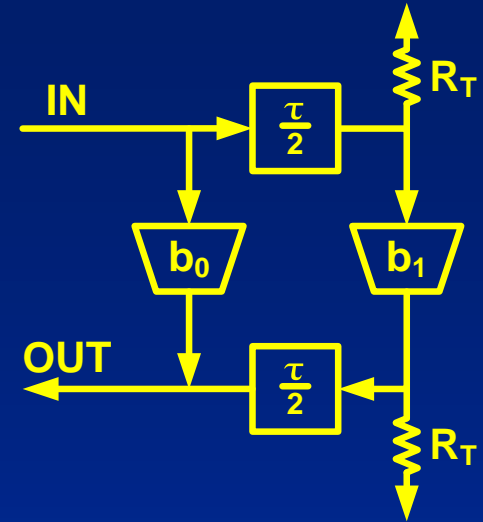
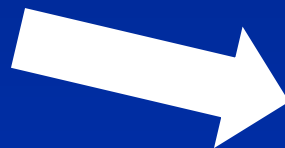
- Frequency dependent channel losses results in inter-symbol interference (ISI) at receiver
- A simple 2-tap finite impulse response (FIR) equalizer can be used to compensate the channel losses



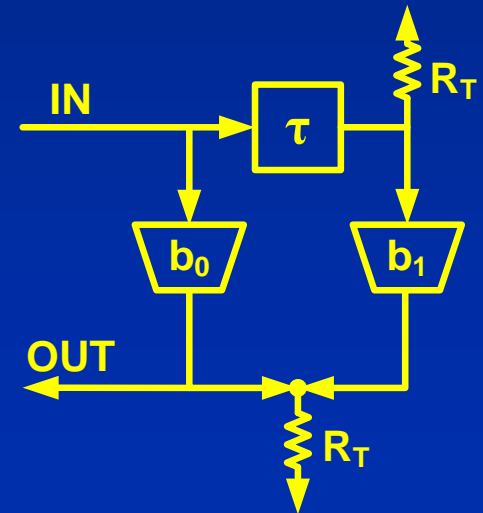
2-Tap FIR Equalizer



Discrete Filter



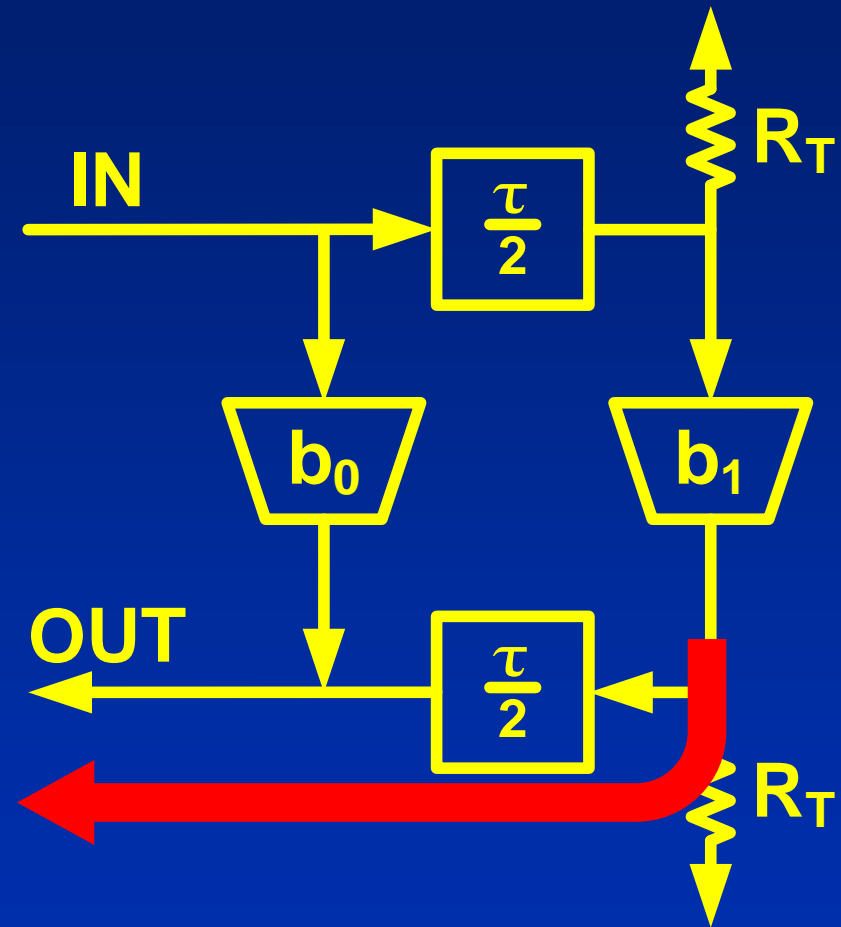
Traveling Wave Filter



Transversal Filter

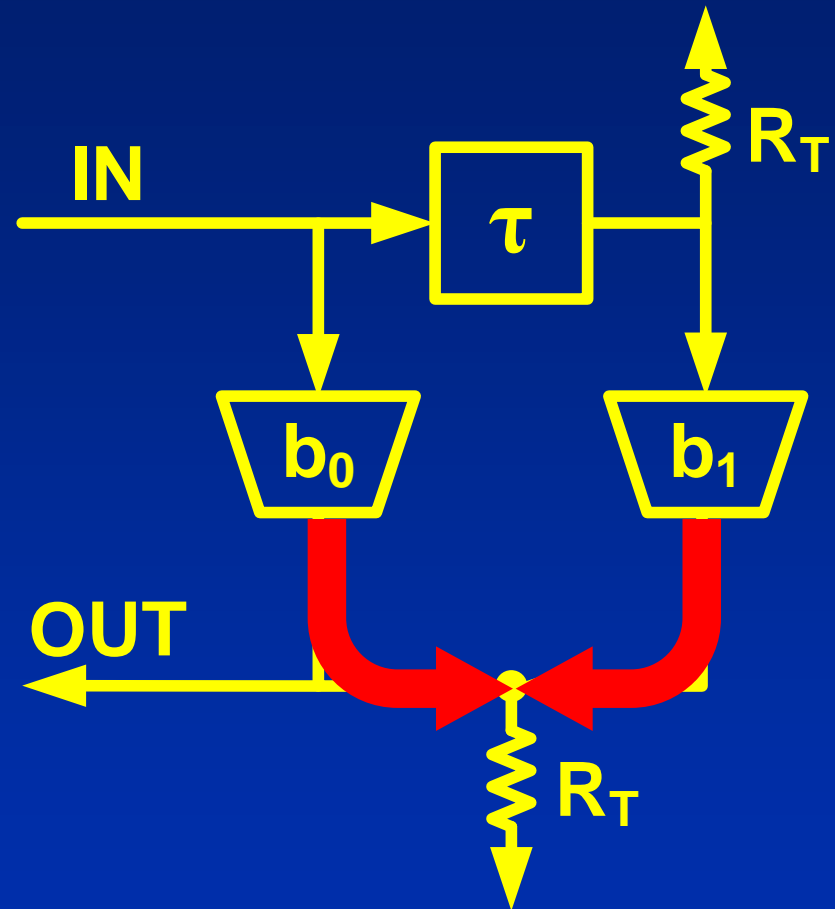
Traveling Wave Filter

- Compensates for reflections due to termination impedance mismatch
- Difficult to get gain due to output side delay element



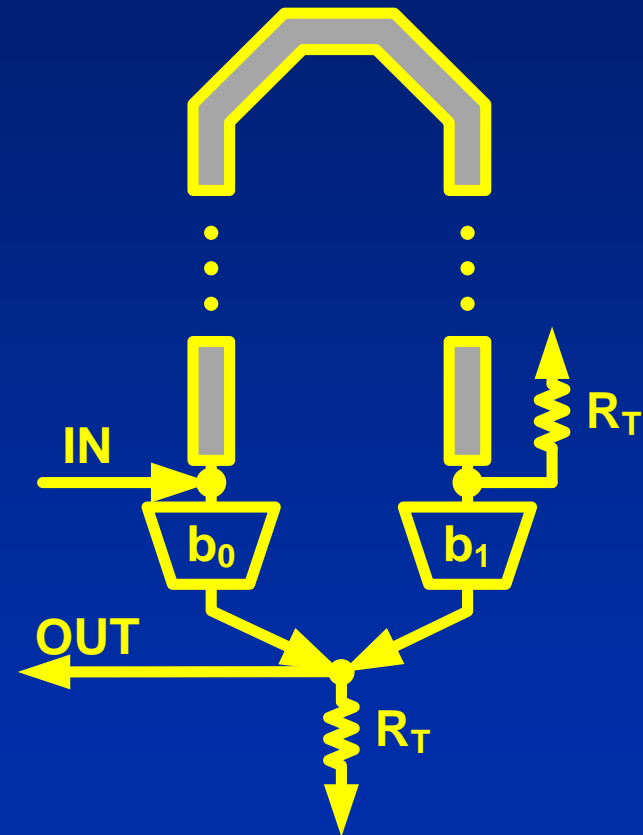
Transversal Filter

- Cannot easily compensate for termination mismatch reflections
- Offers gain advantage due to co-location of tap outputs

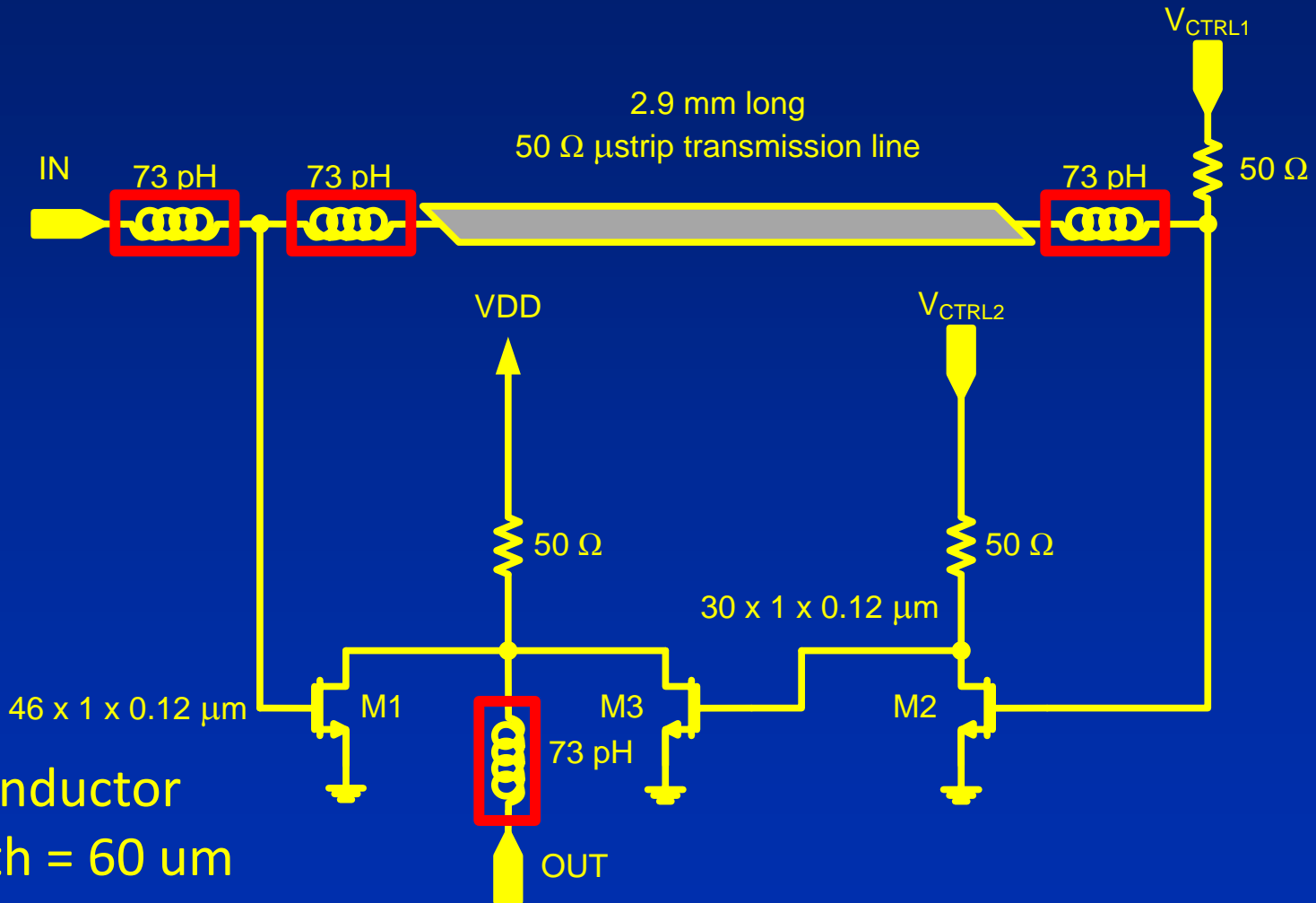


Microstrip Passive Delay Line

- “U” shape simplifies routing to taps
- Easier to accommodate metal fill rules
- Higher bandwidth than lumped L-C delay line

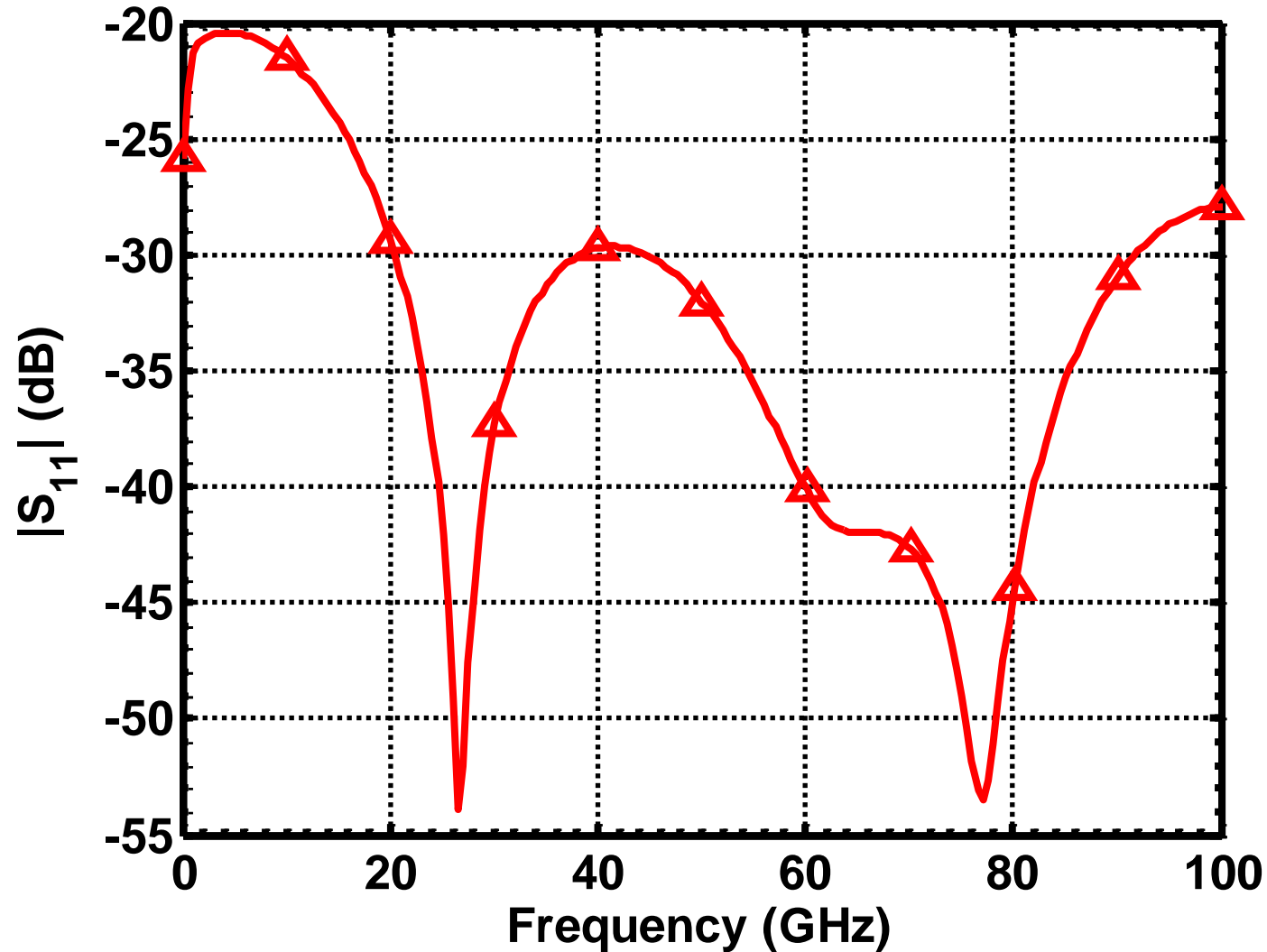


2-Tap Transversal Equalizer

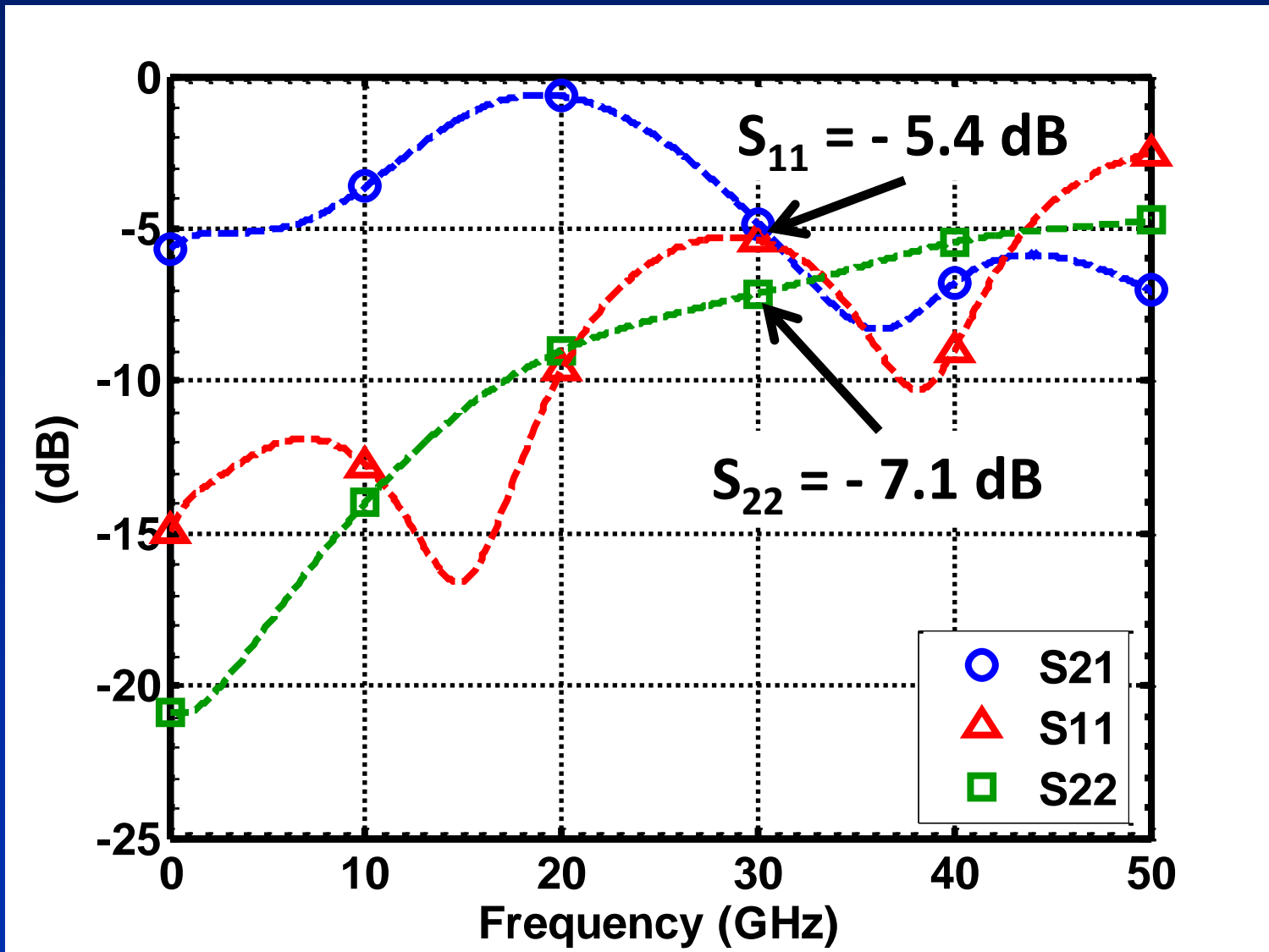


Line Inductor
Length = 60 μm
Width = 1.5 μm
Inductance = 73 pH

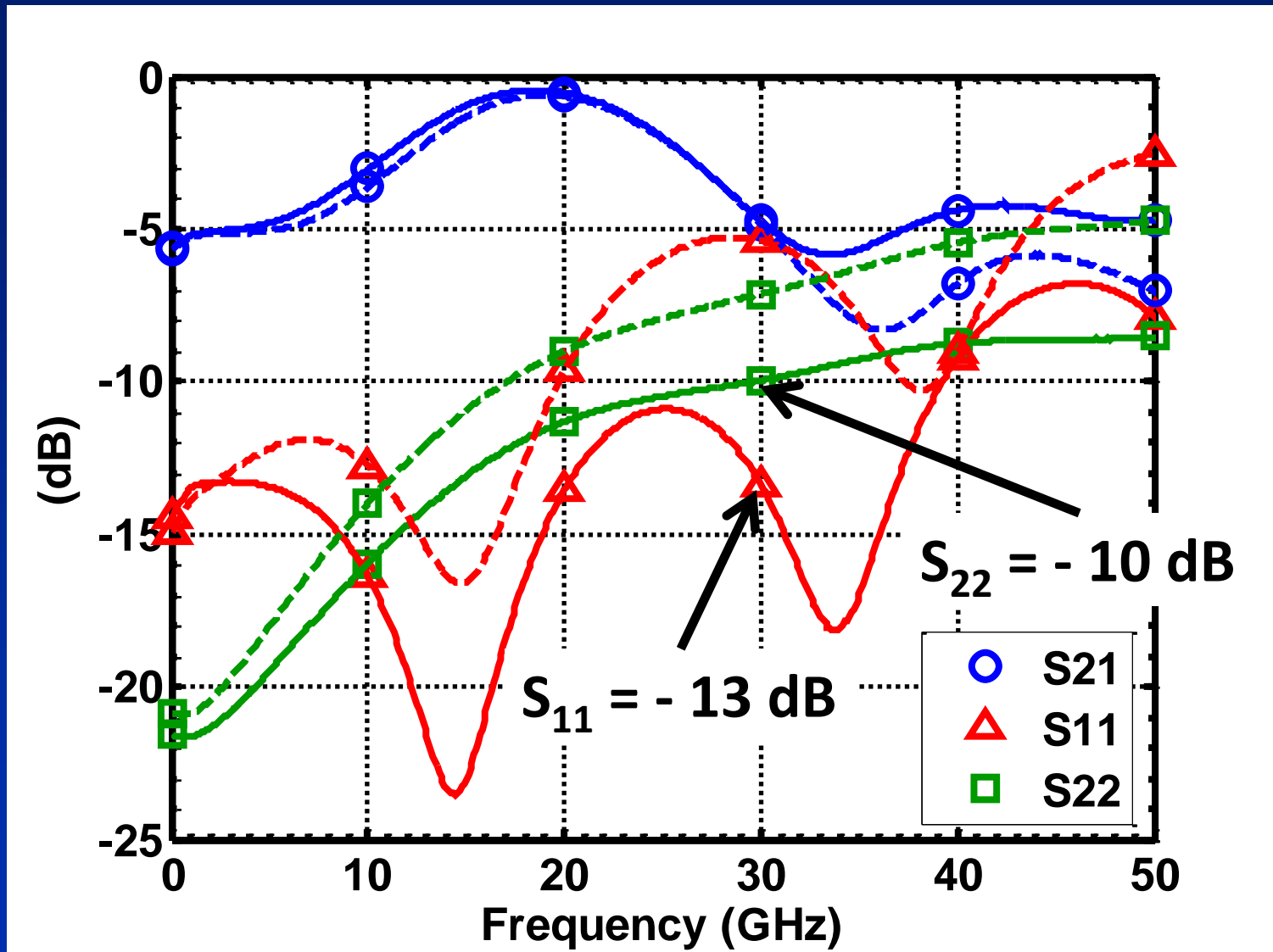
Unloaded Microstrip Line



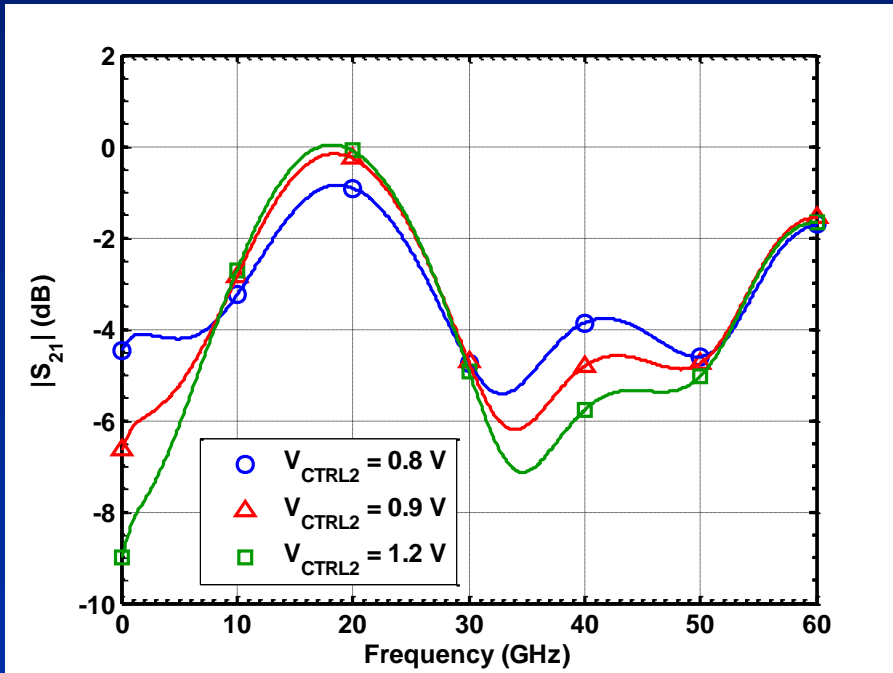
2-Tap without Line Inductors



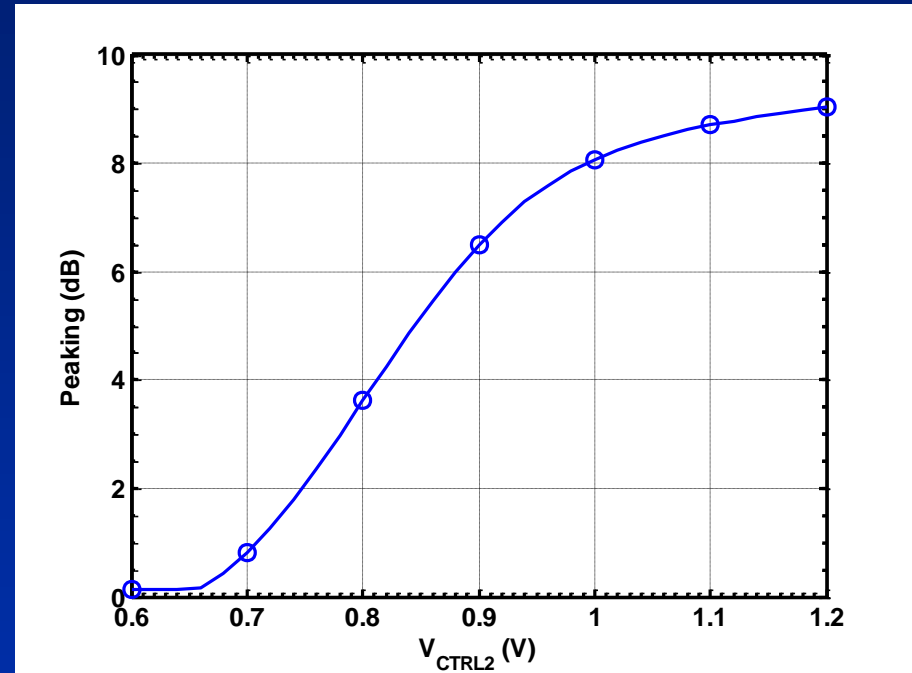
2-Tap with Line Inductors



Simulated Peaking

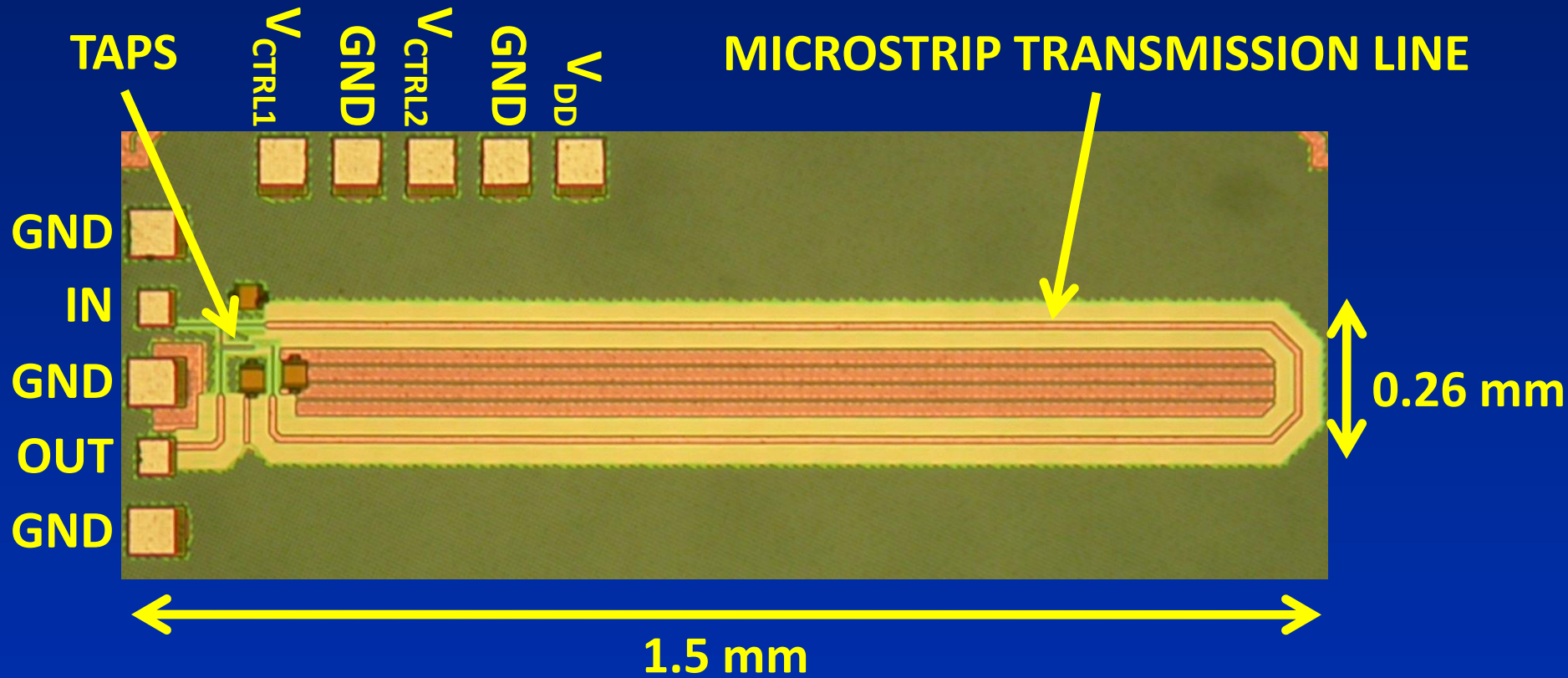


S_{21} versus frequency



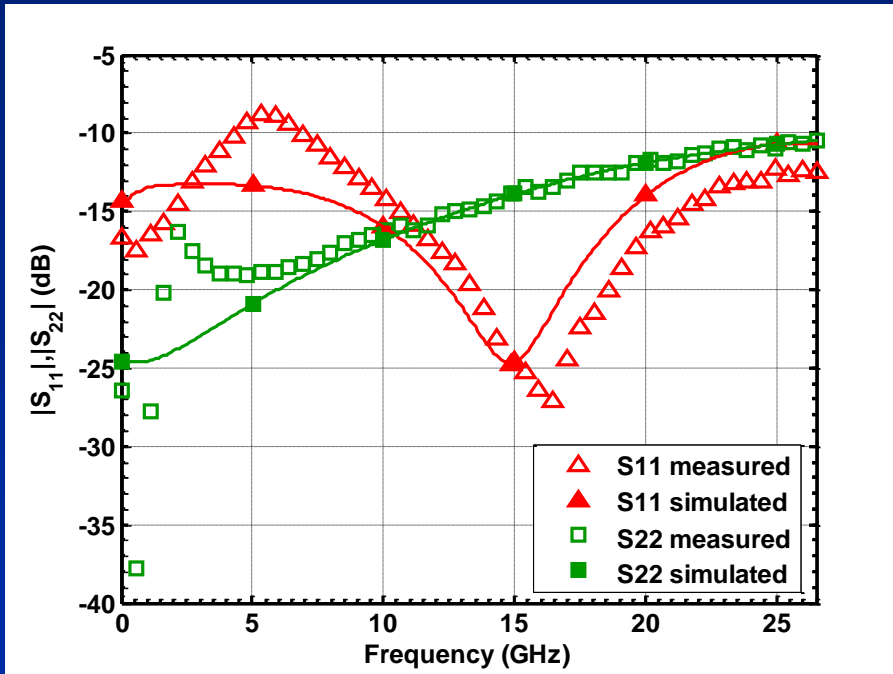
Peaking at maximum frequency versus peaking control voltage (V_{CTRL2})

Die Photo

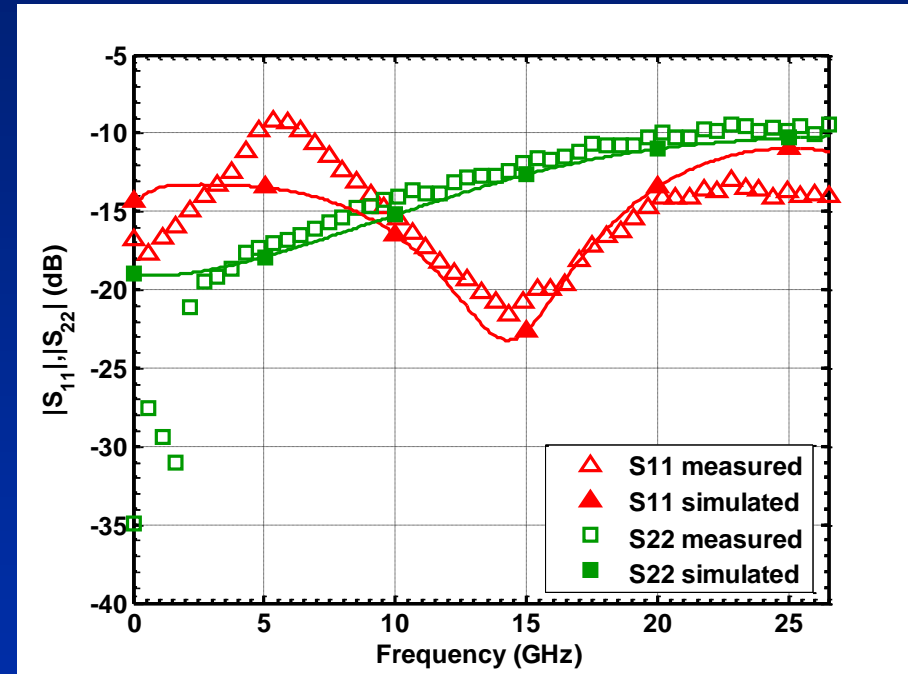


UMC 0.13- μ m CMOS process

S-Parameter Matching

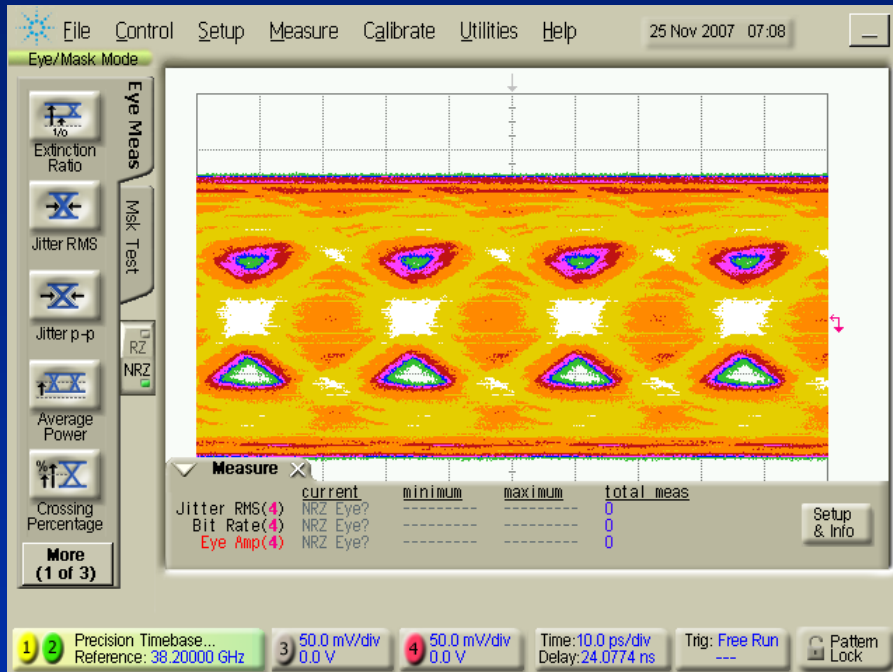


No Peaking

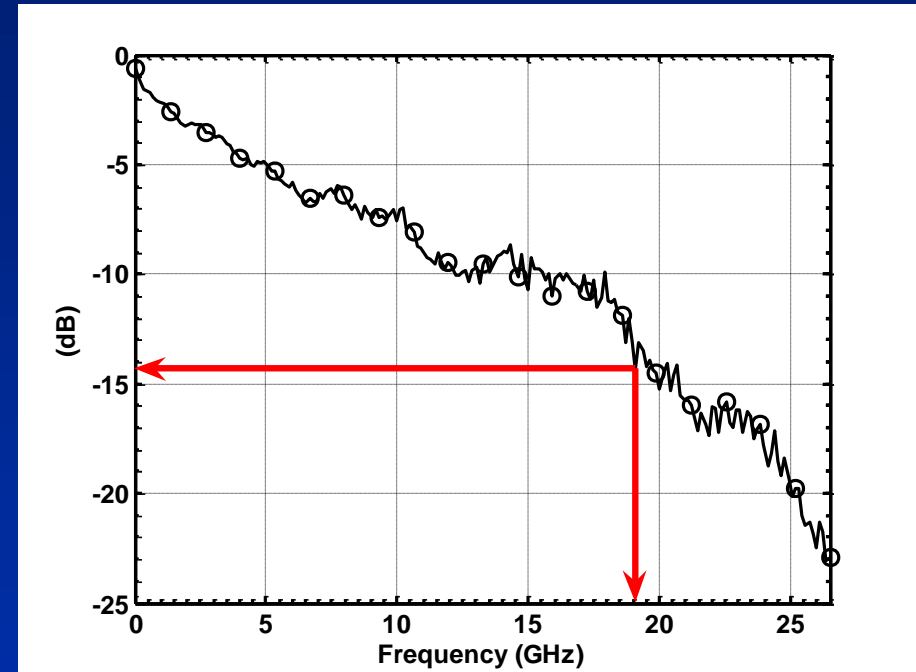


Maximum Peaking

Eye Diagrams – 38 Gb/s



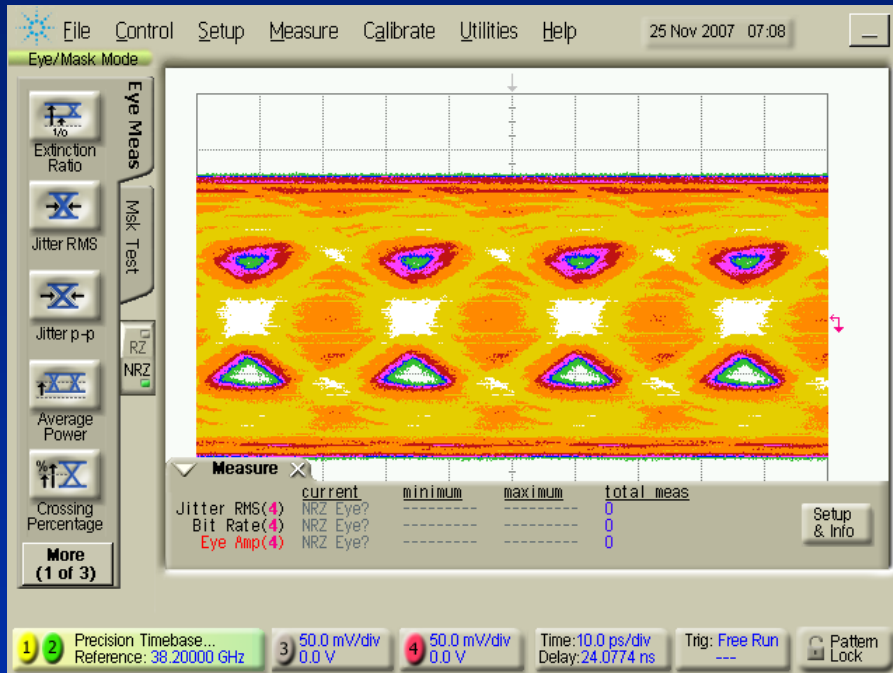
Unequalized Eye



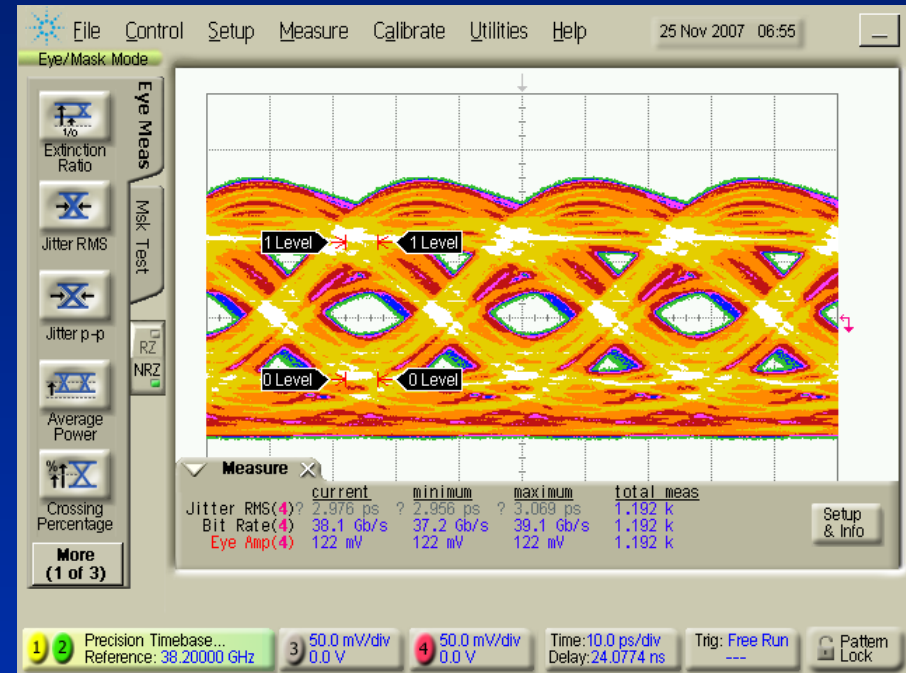
Channel Loss @ 19 GHz: 14.3 dB
(one-half bit-rate)

Channel Type: 6-ft SMA &
3-ft 50-GHz cable

Eye Diagrams – 38 Gb/s



Unequalized Channel Eye



Equalized Eye

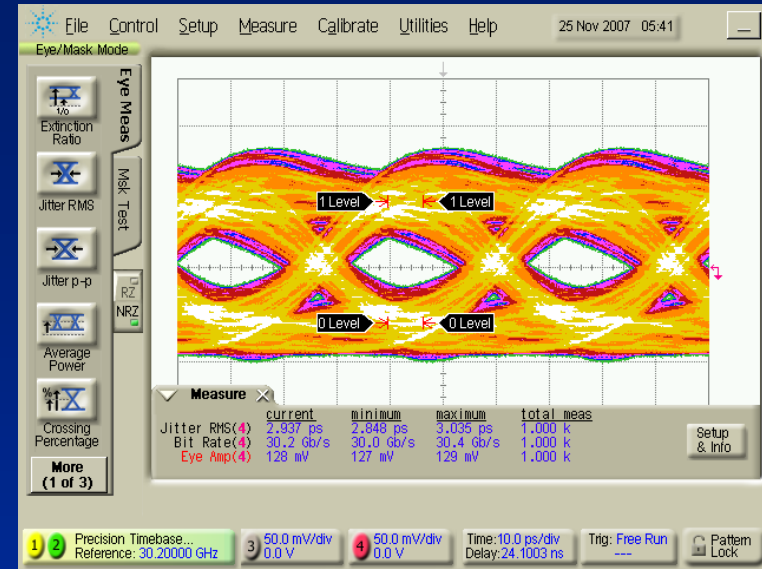
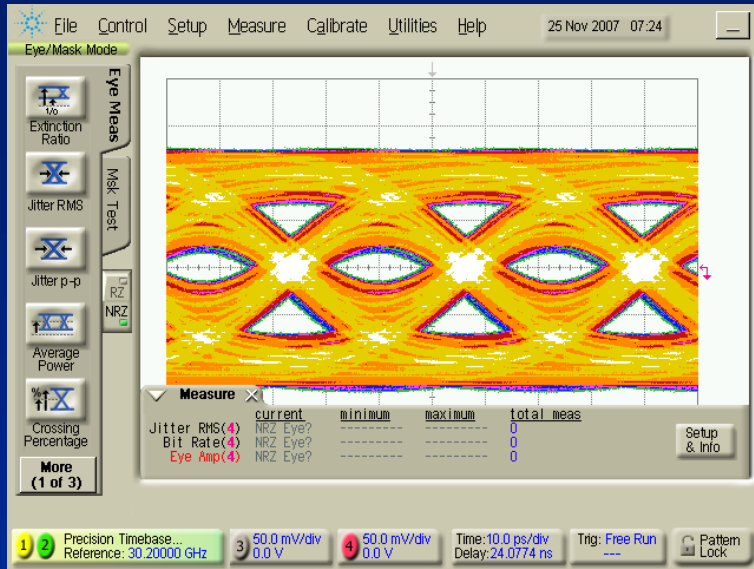
$$V_{DD} = 1.2 \text{ V}$$

$$V_{CTRL1} = 0.82 \text{ V}$$

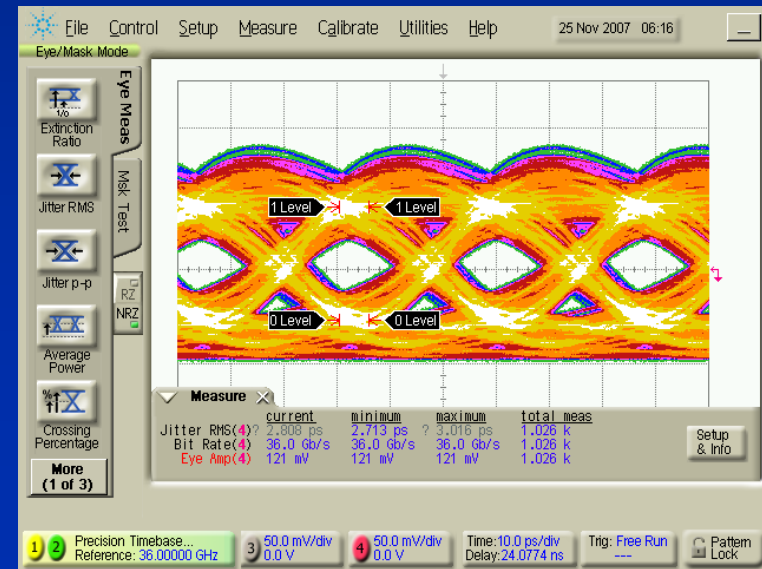
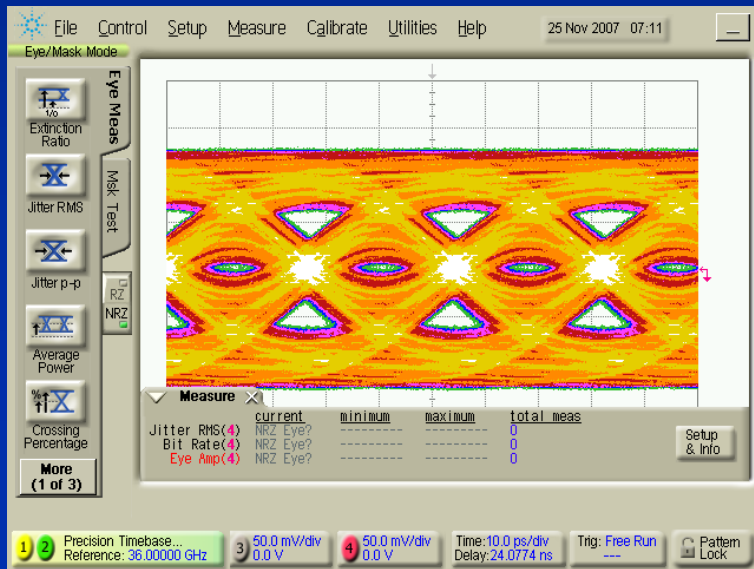
$$V_{CTRL2} = 0.88 \text{ V}$$

Eye Diagrams 30 & 36 Gb/s

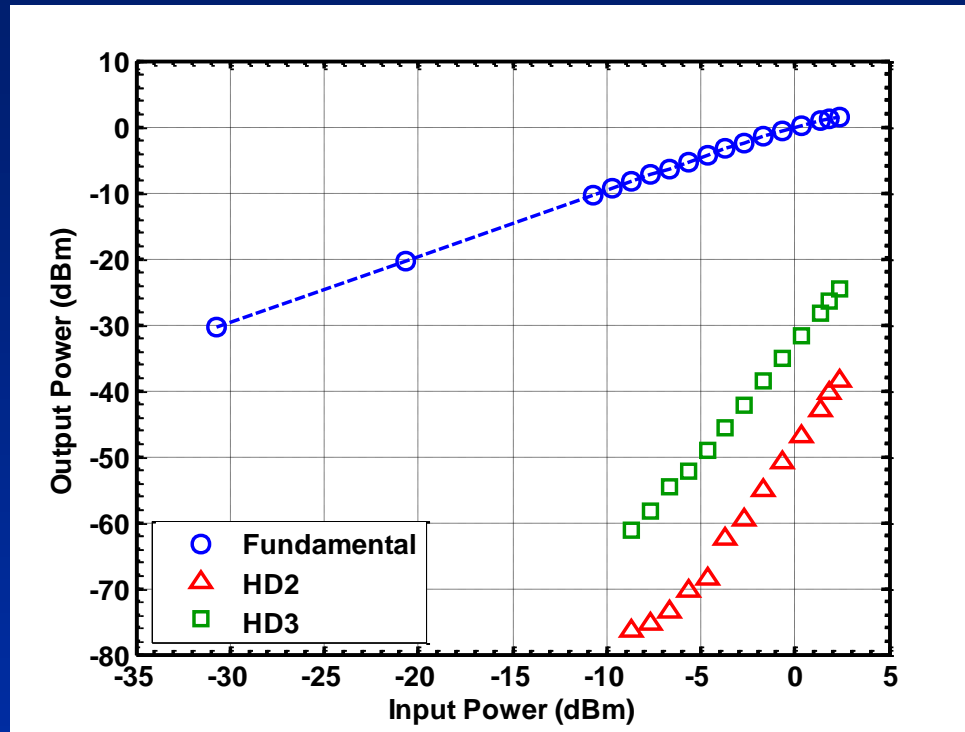
30 Gb/s



36 Gb/s



Linearity



Mode	No peaking
Input Tone (GHz)	2
Input Ref. 1 dB Comp. Pt. (dBm)	1.8
THD @ Comp. Pt. (dB)	-27.5

Measurement Summary

Specification	Measured Result
Process	UMC 0.13- μ m CMOS
Nominal Operating Supply (V)	1.2
Nominal I_{DD} (mA)	12 (no peaking), 17 (max peaking)
Nominal I_{CTRL2} (mA)	0 (no peaking), 8 (max peaking)
Maximum Power Consumption (mW)	30 mW 14 mW (tap 1) 16 mW (tap 2)
S_{11} (peaking off) (dB)	> -9.2 dB up to 26.5 GHz
S_{22} (peaking off) (dB)	> -10 dB up to 26.5 GHz
Maximum equalized channel attenuation (dB)	14.3
Maximum equalized bit-rate (Gb/s)	38
Input ref. 1-dB compression point (no peaking) (dBm)	1.8

Conclusion

- Presented a 2-tap transversal FIR equalizer
- Utilizes “U” shaped microstrip transmission line to achieve baud-tap spacing
- Series “line inductors” maintain constant input and output impedance up to 30 GHz
- Demonstrated equalization of 38-Gb/s data stream with 14.3 dB of channel attenuation

Acknowledgments

- Gennum Corporation for IC fabrication
- Broadcom Corporation for financial support

Questions?