A Dead-Zone Free and Linearized Digital PLL

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***Abstract*—This paper implements a novel digital solution to avoid the problem of dead-zone behavior in digital phase locked loop (DPLL) caused by the quantization effect of time-to-digital converter (TDC). The dead-zone behavior results in chaotic limit cycle behavior causing higher than expected in-band phase noise and strong spurious tones. This behavior is dependent on the initial phase difference between the output and reference clock which makes the DPLL performance inconsistent and unpredictable. To alleviate this problem, a noise shaped offset is added to the phase error, in the digital domain to keep the TDC active and away from the dead-zone. The proposed solution is verified by extensive simulation and using a DPLL prototype in a 0.13 μm CMOS process.**

I. Introduction

Digital phase locked loops (DPLLs) have shown several advantages over analog PLLs in terms of noise immunity, small area, testability, and programmability [1]. A simplified diagram of DPLL architecture is shown in Figure 1, where the time-to-digital converter (TDC) and the digitally-controlled oscillator (DCO) introduce unwanted quantization noise.

The TDC works as a fractional counter that measures the phase difference between the output clock, F_{out}, and the reference clock, F_{ref}. The phase difference is quantized with a limited resolution of Δt_{res}, as shown in Figure 2. The estimated phase difference is averaged and normalized to the instantaneous F_{out} period and expressed as fixed-point number. In the presentence of enough phase noise at the TDC inputs, the quantization noise can be scrambled which will effectively linearize the TDC transfer function. The scrambling of the quantization noise lowers the chance of chaotic limit cycle behavior due to TDC nonlinearities and makes linear analysis of DPLL valid.

If the DPLL is operating as a fractional-N synthesizer, the phase relationship between DCO output and reference input is scrambled over time, the quantization error introduced by the TDC, Δt_Q in Figure 2, may be approximated as white noise [2]. However, if the DPLL is locked in an integer-N mode (or with a simple fractional component, for example 1/2), the phase relationship between the TDC inputs is fixed (or periodic). In this case, the limited resolution of the TDC has an effect similar to the classic dead-zone behavior observed in analog phase detectors. The dead-zone has the effect of periodically opening the loop and letting the phase drift which creates a substantial amount of deterministic jitter [3].

Recently published work [4] demonstrated an analog approach to avoid the dead-zone behavior for low bandwidth DPLLs by randomizing the phase of the reference clock, F_{ref}. In this work, the reference buffer is modified by adding 16 bias

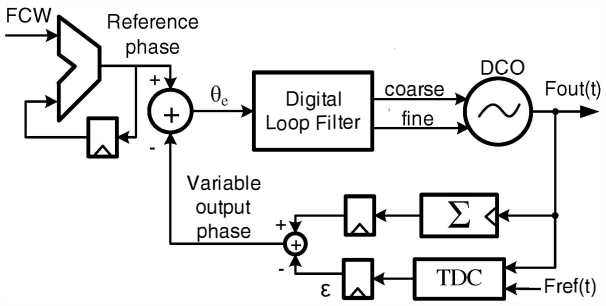

Fig. 1. Digital PLL Architecture

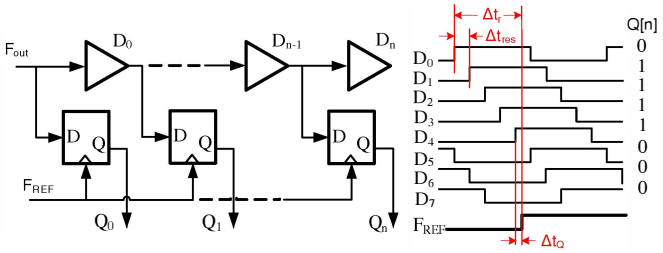

Fig. 2. TDC: simplified schematic view (left); timing diagram(right). The raw $Q[i]$ is pseudo-thermal code to be converted into a normalized binary word representing the fractional phase error.

elements controlled by short dithering sequence. This requires custom modification of the reference buffer and accurate sizing of the bias elements. Furthermore, due to its analog nature, the effectiveness of this approach is affected by the PVT variations and so calibration is needed. Moreover, this approach allows F_{out} to lock to F_{ref} with an arbitrary phase offset. The GRO-TDC in [2] intrinsically scrambles the quantization noise with first-order noise sapping. However, the TDC design is complex and it consumes high power and a small dead-zone was still measured for some special cases.

In this paper, we elaborate on the dead-zone behavior of a DPLL caused by TDC finite resolution, focusing on integer-N operation. Also, we present a pure simple programable digital solution to the dead-zone problem that achieves a consistently low in-band phase noise operation regardless of the initial condition while maintaining high loop bandwidth. This solution is not affected by PVT variations and ensures phase locking with minimal phase offset. The paper is structured as follows. In Section II, an overview of TDC operation is given along with a discussion of the inconsistent performance of DPLLs caused by dead-zone behavior. Dithering algorithm and comprehensive simulation results are presented in Section

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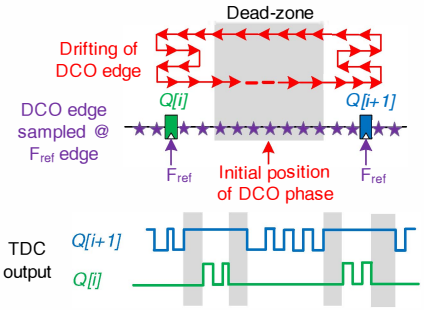
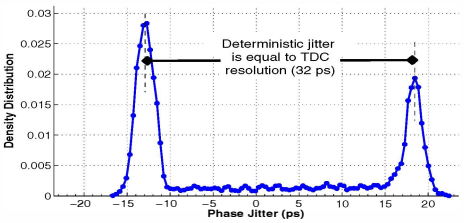
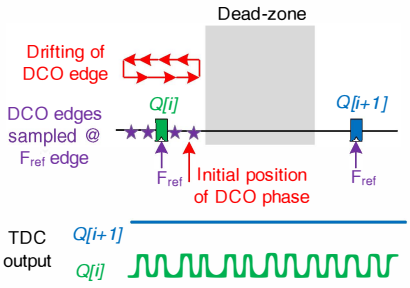


(a) Explanation diagram.

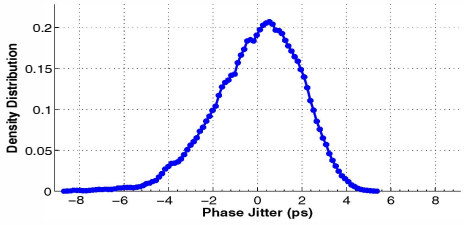


(b) PDF of the phase jitter from a behavioral simulation.

Fig. 3. Dead-zone behavior of Integer-N DPLL



(a) Explanation diagram.



(b) PDF of the phase jitter from a behavioral simulation.

Fig. 5. Bang-Bang behavior of Integer-N DPLL

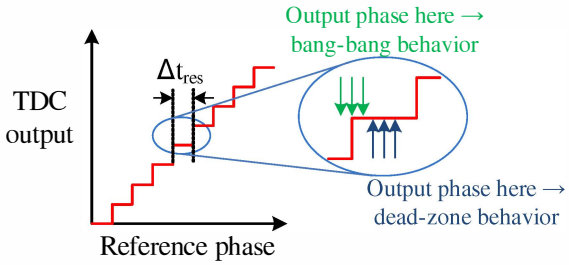


Fig. 4. The DPLL nonlinearity.

III. Finally, measurement results of the DPLL prototype are shown Section IV.

II. TDC Dead-Zone Behavior

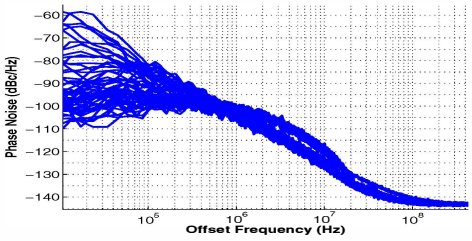
The TDC compromises a chain of buffers with a resolution that ranges from approximately 32 ps in a 0.13-μm CMOS process to 8 ps in a 28-nm process. The output clock, F_{out}, propagates through this chain such that many delayed versions of F_{out} are sampled at the rising edge of the reference clock, F_{ref}. The TDC reads out the normalized time difference, $\Delta t_r/\Delta t_{res}$, between the rising edge of F_{ref} and the previous rising edge of F_{out}. The DPLL reacts to the time-varying values of the TDC readout to keep the DPLL locked [4].

Due to the TDC's staircase nonlinearity, different types of nonlinear behavior are observable depending upon the relationship between the reference phase and DCO output phase in lock, as illustrated in Figure 4. The DPLL will try to enforce the TDC output to track the reference phase provided by the digital phase accumulator on the left side of Figure 1. In integer-N mode, the fractional part of the frequency control word (FCW) is zero while the accumulated reference phase, θ_{ref}, might have arbitrary fractional value depending upon the accumulator's initial condition.

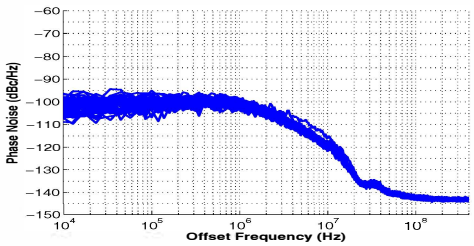
When that fractional part of the reference phase coincides with a flat-part of the TDC staircase, the DPLL will try to lock to a phase where the TDC has low effective gain and, hence, the DPLL has low loop bandwidth. In this case, F_{out} edge initially lies in the middle of TDC step anywhere within the gray dead-zone region, as shown in Figure 3(a). It takes long time for F_{out} edges to drift toward F_{ref} edges such that the DPLL appears as an open loop during the phase drift within the dead-zone. Moreover, dead-zone behavior results in large spurs, similar to analog PLLs with a dead-zone.

On the other hand, if the fractional part of the reference phase is constant at a value coinciding with a transition in the TDC staircase, the TDC will operate similar to a bang-bang phase detector as illustrated in Figure 5(a), where a TDC bin keeps toggling between 0 and 1 and produces late or early phase difference without being able to quantify the value of that phase difference. This happens when the initial phase difference between F_{out} and F_{ref} is small compared to the DCO time resolution and jitter such that the F_{out} edges drift over time can be quickly detected and corrected as shown in Figure 5(a). The TDC will stay active bouncing back and forth at high frequency and so the TDC output will be filtered by the loop dynamics. In this case, the probability density function (PDF) of the phase jitter follows a Gaussian distribution as shown in Figure 5(b).

During the bang-bang mode of operation, the DPLL will exhibit a loop bandwidth that depends upon the instantaneous phase error as well as other noise sources in the loop [5]. It also has the potential for limit-cycle behavior, again resulting in spurs. Based on non-linear analysis of bang-bang PLL, the smaller the phase difference between F_{ref} and F_{out}, the higher

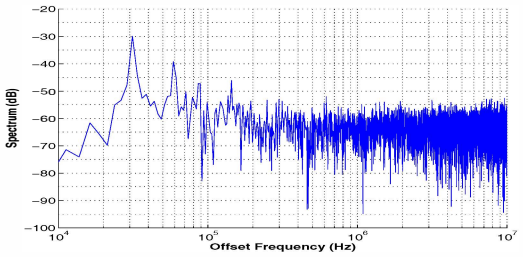


(a) Uncompensated Integer-mode DPLL.

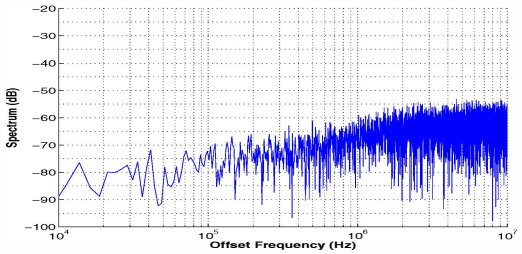


(b) After applying random offset with noise shaping and disabling ZPR.

Fig. 6. Phase noise of the same output clock for 60 different initial conditions



(a) During dead-zone operation.



(b) After applying random offset with noise shaping.

Fig. 7. Spectrum of TDC normalized output

the loop gain and bandwidth [4].

The more serious of these problems observed is the dead-zone behavior. The dead-zone behavior increases the spread of phase jitter and degrades the loop bandwidth due to the degradation of the loop gain. The spread of phase jitter is determined by the DCO jitter performance as well as its frequency resolution and more importantly by the TDC resolution. In extreme cases, F_{out} might need to span one whole TDC step before phase and frequency error is detected and correction is applied. Figure 3(b) shows the PDF of the DPLL phase jitter while exhibiting dead-zone operation where the simulated phase error is concentrated around -14 ps and 18 ps with a large separation of 32 ps. This ensembles a deterministic jitter at low frequency offset that is equals to the TDC resolution.

Many DPLLs have coarse control loop to set the DCO close to the desired frequency range and fine control loop to achieve accurate frequency and phase lock. To avoid any discontinuities in the DCO control word during gear shifting from coarse to fine operation, a zero-phase restart (ZPR) mechanism proposed in [1] is used to zero-out the phase detector output. The ZPR resets the reference phase accumulator in Figure 1 to an arbitrary value depending on the initial condition. In this work the fractional part of the ZPR is disabled so that the fractional part of the reference phase can be set to ensure the TDC's dead-zones are avoided.

Figure 6(a) shows the phase noise, based on simulation results, for the same integer-mode DPLL for 60 different initial conditions with the ZPR enabled illustrating how very different loop bandwidths can result. The simulation environment employs high level model of DCO phase noise as well as the reference noise as shown in [6]. The in-band phase noise varies from -60 dBc/Hz to -100 dBc/Hz and the loop bandwidth changes by an orders of magnitude.

III. Noise-Shaped Dithering

Even with the TDC dead-zones avoided, bang-bang-like operation can still result in inconsistent loop bandwidth and potentially spurs due to limit cycle behavior. To alleviate the inconsistent behavior of integer-mode DPLL, F_{ref} edges can be randomized with respect to F_{out} edges to ensures that TDC is kept busy enough as demonstrated in [4]. This solution needs custom modification of the reference buffer and careful choice of delay circuits. Furthermore, mismatches between the delay elements could reduce the usefulness of this approach.

Alternatively, we propose to dither the phase difference, ϵ, estimated by TDC and represented as fixed-point number by using purely digital techniques. By observing the transient behavior of phase difference, ϵ, as well as its spectrum, we found that ϵ changes slowly and continually from 0 to 1 during dead-zone operation. The spectrum of ϵ exhibiting such behavior is shown in Figure 7(a) where the large spur of -33 dB at 30 kHz offset is evident. Once a random digital offset, generated by 20-bit LFSR, is added to ϵ, the spurs disappeared and the in-band spectrum drops to -60 dB. This random offset solution ensures consistent but sub-optimal DPLL performance.

The proposed optimal solution dithers the phase difference, ϵ, using a 10-bit third-order delta-sigma modulator. The dithering algorithm is sampled by F_{ref} and it only requires 230 digital gates for implementation. The dithering scrambles the quantization noise of the TDC and linearizes its response. The offset value, as shown in Figure 8, is chosen to be 0.5 to ensure that the falling edge of F_{out} is always locked to the rising edge of F_{ref} at a phase difference around a step in the TDC response. A small random offset, generated by LFSR, is introduced to ensure acceptable noise shaping as well as to

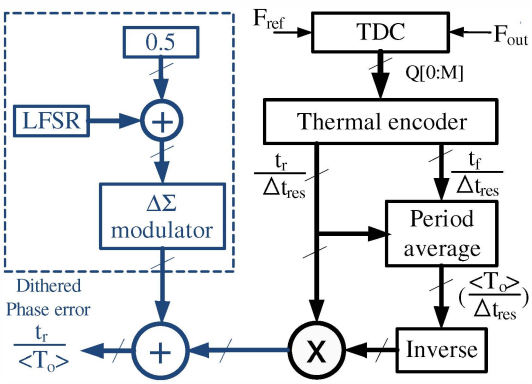


Fig. 8. The proposed circuit to estimate and dither the phase error

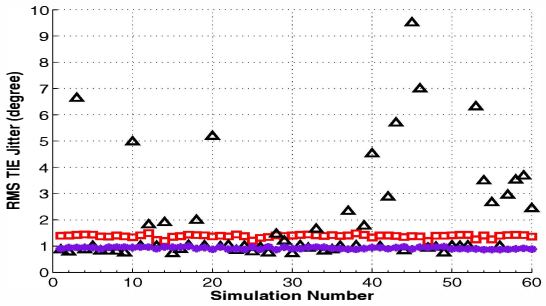


Fig. 9. Time Interval Error (TIE): △ No dithering, □ Random dithering, ∗ Noise-shaped dithering

get rid of unwanted reference spurs.

Finally, the phase noise spectrums after applying the noise-shaped offset for 60 different initial conditions are shown in Figure 6(b) where the loop bandwidth is high and consistent. Plot of the time-interval error (TIE) for 60 different initial conditions is presented in Figure 9. The average RMS TIE of the 60 different initial conditions after applying the proposed noise-shaping offset is 0.92 degree with only 0.04 degree standard deviation. Without dithering, the average RMS TIE is 1.59 degree with 0.67 degree deviation.

IV. Measurement Results

A prototype DPLL in 0.13-μm technology is used to demonstrate the TDC dithering linearization technique. Complete details on the DPLL are available in [7], except for this dithering linearization which was not reported on there. Figure 11 shows phase noise measurement results when the carrier is 2 GHz while the reference is 20 MHz, using a HP8565C spectrum analyzer. For the same frequency and same loop settings, we captured different loop responses by simply resting the DPLL many times. Dead-zone operation is drawn in blue while the medium activity TDC response is shown in green. Large in-band spurs at 40 kHz and 80 kHz offset frequency are readily seen. The optimal performance of the integer-mode DPLL after applying noise shaped offset is drawn in red. The average integrated RMS jitter is 1.25 ps for 10 different initial

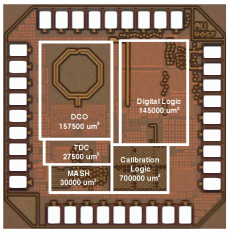


Fig. 10. Die photo of the DPLL [7] (active area is 0.36 mm^2).

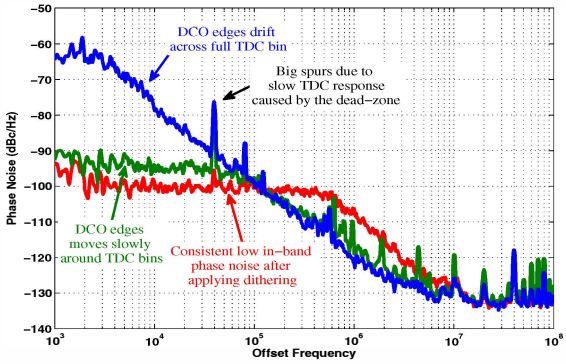


Fig. 11. Phase noise measurement using HP8565C analyzer showing different behaviors of integer-mode DPLL

condition after applying the proposed dithering algorithm with a consistent DPLL loop bandwidth of 700 kHz.

V. Conclusion

This paper presents a detailed explantation of dead-zone behavior in DPLL's operated in integer mode. Based on that understanding, a simple purely-digital dithering solution is also demonstrated to ensure the DPLL avoids its dead-zones. The solution employs a third-order noise-shaping phase offset to linearize the bang-bang behavior. The proposed solution ensures phase lock with minimum offset. Extensive simulation results as well as a prototype of DPLL achieve a consistent low in-band noise operation regardless of the initial condition while maintaining high bandwidth loop.

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