Cycle-Slipping Pull-In Range of Bang-Bang PLLs

Amer Samarah, Anthony Chan Carusone
Edward S. Rogers Sr. Department of Electrical and Computer Engineering
University of Toronto, Toronto, CANADA

***Abstract*—An analysis of the cycle slipping behavior of a bang-bang phase locked loop (PLL) far from its lock provides expressions for the pull-in frequency range. Behavioral simulation is used to validate the analytical results which estimate the pull-in range at least 40% more accurately than prior work.**

I. Introduction

Phase-locked loops (PLLs) are essential blocks in many systems such as clock and data recovery, data conversion, frequency synthesis and clock synchronization. PLLs employing a binary "bang-bang" phase detector (BBPD) have become more commonly used due to their simplicity compared to PLLs with a linear phase detector allowing them to operate at the highest possible speed. Also, BBPDs are preferred over time-to-digital converters (TDCs) for integer-mode digital PLLs for their low power consumption.

However, bang-bang PLLs in general suffer from three major drawbacks. Firstly the loop gain and the associated loop characteristics are hard to define due to the highly nonlinear phase detector. Secondly they have a limited pull-in frequency range. Thirdly there is a trade-off between pull-in frequency range and jitter performance of bang-bang PLLs [1]. The focus of this brief is on the analysis of cycle slipping behavior and frequency pull-in process of bang-bang integer PLLs.

There is a lot of literature dealing with the small-signal steady-state behavior of bang-bang PLLs [2], [3]. Those works focus on the jitter performance and stability of such PLLs. The pull-in process during frequency acquisition of bang-bang PLL is very non-linear and a large signal analysis is needed. An early attempt to quantify pull-in range of binary bang-bang PLLs was done by [4] where an asymptotic formula was derived for the pull-in range under certain constraints. That analysis is only valid for lag-lead loop filters and it does not provide an intuitive understanding of design trade-offs. In [5], a step-by-step description of oscillator phase and frequency during locking is presented. However, [5] provides formula for the frequency lock range before the occurrence of the first cycle slip, which is much smaller than pull-in range. More recently, [6] provides a closed loop formula for pull-in frequency range but it is very conservative and it under estimates the pull-in range.

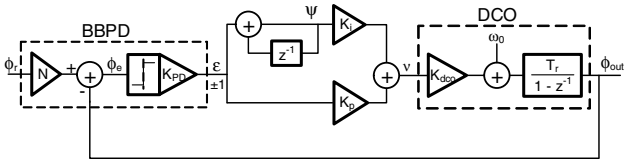


Fig. 1. Phase domain model of DPLL with bang-bang phase detector.

In this paper, we will analyze the transient behavior of bang-bang PLLs far from their lock point. A closed form will be derived to accurately predict PLL pull-in frequency range which is more accurate than prior literatures.

II. Timing Model of Bang-Bang PLL

Fig. 1 shows a z-domain phase model of PLL with BBPD. The output clock is sampled directly by the reference clock without being divided down. Accordingly, the reference phase must be multiplied by the frequency ratio between output and input clock i.e. N. The BBPD output is $\varepsilon[k] = K_{PD} \cdot \text{sgn}(\phi_e[k]) = \text{sgn}(\phi_e[k])$ assuming $K_{PD} = 1$ without loss of generality.

Let ω_0 be the free running angular frequency of the oscillator output and K_{dco} be the oscillator gain expressed in $rad/s/step$. Also, denote the instantaneous output frequency by $\omega_{out}[k]$. Then,

$$\omega_{out}[k] = \omega_0 + K_{dco}K_p \cdot \varepsilon[k] + K_{dco}K_i \cdot \psi[k] \quad (1)$$

Based on Eq. 1 and Fig. 1, the change in the output phase is,

$$\Delta\phi_{out}[k] = T_r\omega_0 + T_rK_{dco}K_p \cdot \varepsilon[k] + T_rK_{dco}K_i \cdot \psi[k] \quad (2)$$

For simplicity, we will consider separately the phase contribution of the proportional path, $\phi_p[k]$, and integral path, $\phi_i[k]$, as follows:

$$\begin{aligned}\phi_p[k] &= T_rK_{dco}K_p \cdot \varepsilon[k] \\ &= T_rK_{dco}K_pK_{PD} \cdot \text{sgn}(\phi_e[k]) \Rightarrow \quad (3)\end{aligned}$$

$$\boxed{\phi_p \equiv T_rK_{dco}K_pK_{PD} \Rightarrow \phi_p[k] \approx \phi_p \cdot \text{sgn}(\phi_e[k])} \quad (4)$$

$$\phi_i[k] = T_rK_{dco}K_i \cdot \psi[k] \quad (5)$$

$$\textit{but} \quad \Delta\psi[k] = \varepsilon[k] \Rightarrow \Delta\phi_i[k] = T_rK_{dco}K_i \cdot \varepsilon[k] \quad (6)$$

978-1-4799-8893-8/15/$31.00 © 2015 IEEE

$$\boxed{\omega_i \equiv K_{dco}K_iK_{PD} \Rightarrow \Delta\phi_i[k] \approx T_r\omega_i \cdot \text{sgn}(\phi_e[k])} \quad (7)$$

Hence, ω_i represents the angular frequency correction provided by the integral path in one reference period. Now, substitute Eq. 4 and Eq. 7 back into Eq. 2 to get:

$$\Delta\phi_{out}[k] = T_r\omega_0 + \phi_p[k] + \phi_i[k] \quad (8)$$

The initial frequency offset, ω_{off}, is defined as the difference between the ideal locked output frequency, $N\omega_r$, and the oscillator free running frequency, ω_0

$$\omega_{off} = N\omega_r - \omega_0 \quad (9)$$

$$\Rightarrow T_r\omega_{off} = T_rN\omega_r - T_r\omega_0 = 2\pi N - T_r\omega_0 \quad (10)$$

If ω_{off} is within the pull in range, then the output frequency error will converge to zero. The phase error is defined as the difference between the reference phase and output phase

$$\phi_e[k] = N\phi_r[k] - \phi_{out}[k] \quad (11)$$

$$\Rightarrow \Delta\phi_e[k] = N\Delta\phi_r[k] - \Delta\phi_{out}[k] \quad (12)$$

For a fixed reference frequency, $\Delta\phi_r[k] = 2\pi$. Substituting Eq.8 into Eq.12,

$$\Delta\phi_e[k] = 2\pi N - T_r\omega_0 - \phi_p[k] - \phi_i[k] \quad (13)$$

and Eq. 10 into Eq. 13 to finally get

$$\boxed{\Delta\phi_e[k] = T_r\omega_{off} - \phi_p[k] - \phi_i[k]} \quad (14)$$

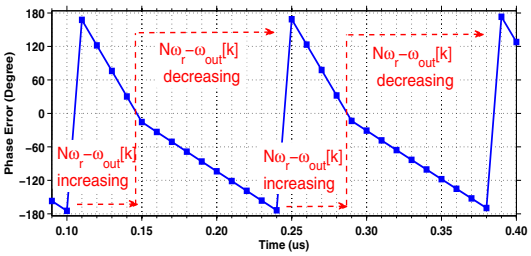
Eq. 14 has three terms: the first contributes phase slipping due to the frequency error between the free-running and lock frequencies; the second and third account for the phase corrections of the proportional and integral paths, respectively.

III. Cycle Slipping Phenomena

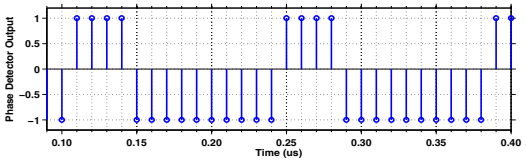
A PLL is said to exhibit cycle slipping if the phase error at the input of BBPD exceeds the range $\pm\pi$. This phenomena slows down frequency acquisition and limits the pull-in frequency range of PLL [5].

Whether a PLL will exhibit cycle slipping or not is dependent on the relation between the phase shift caused by the initial frequency offset, $T_r\omega_{off}$ and the available phase correction by the proportional path, ϕ_p. If $T_r\omega_{off} < 2\phi_p$[1], then a PLL will lock relatively quickly without cycle slipping, assuming the loop is stable. On the other hand, if the frequency offset is big enough such that $T_r\omega_{off} > 2\phi_p$, but still within the pull-in range described below, then the PLL will exhibit cycle slipping during frequency acquisition until the induced phase shift due to frequency error is reduced to below $2\phi_p$.

[1]The choice of factor 2 is based on an analogy between a BB-PLL and $\Delta\Sigma$ modulator not discussed further here. Reference [5] predicts similar limit.



(a) Phase error at the input of BBPD



(b) BBPD output

Fig. 2. Illustration of cycle slipping and frequency acquisition during pull-in process.

IV. Analysis of Pull-In Frequency Range

Pull-in frequency range is defined as the maximum initial frequency offset, ω_{off}, for which a PLL acquires lock, generally after experiencing many cycle slips. To guarantee locking, the frequency error, $N\omega_r - \omega_{out}[k]$, must reduce in each cycle slip in response to the phase detector outputs [4]. If the frequency error remains constant over successive cycle slipping periods, or increases after a cycle slip period, the PLL will wander around an intermediate metastable frequency [4].

Assume that a PLL has large enough positive frequency error which causes a phase drift from $-\pi$ to $+\pi$ over several reference periods i.e. cycle slipping, as shown in Fig. 2(a). When the phase error is positive, the phase detector output is positive as shown in Fig. 2(b). These positive pulses will push the phase error toward zero. But, they will cause the frequency error to increase rather than decrease since they are positive pulses. The phase error will then drift below zero and the BBPD will then produce negative pulses. As long as frequency error is large enough, the phase error will keep decreasing, though at a slower rate compared with positive phase errors, toward $-\pi$ where a cycle slip happens.

To quantify the pull-in range, denote the number of up pulses in a cycle slipping period at the edge of pull-in range as N_{up} and the number of down pulses in a cycle slipping period as N_{dn}.

Assume that $\omega_0 > N\omega_r$ which will cause a negative phase shift in each reference period until it gets corrected by the integral path. Also assume the initial phase error is just slightly below π, and so the initial output of the phase detector is positive and stays positive for another

N_{up} reference periods. Recall Eq. 7 to find the phase shift due to the frequency correction of the integral path over the next N_{up} periods:

$$\begin{aligned}\phi_i[0] &= 0\\ \phi_i[1] &= \phi_i[0] + T_r\omega_i = 1T_r\omega_i\\ \phi_i[2] &= \phi_i[1] + T_r\omega_i = 2T_r\omega_i\\ &\dots\end{aligned}$$

Also, recall Eq. 14 to express the change in phase error during these N_{up} periods:

$$\begin{aligned}\Delta\phi_e[1] &= -T_r\omega_{off} - \phi_p - T_r\omega_i\\ \Delta\phi_e[2] &= -T_r\omega_{off} - \phi_p - 2T_r\omega_i\\ &\dots\\ \Delta\phi_e[N_{up}] &= -T_r\omega_{off} - \phi_p - N_{up}T_r\omega_i\end{aligned}$$

At the end of N_{up}^{th} period, the frequency error increases from ω_0 to $\omega_0 + N_{up}\omega_i$. Once the phase error changes its sign from positive to negative, then the phase detector will produce negative pulses that move the frequency error in the correct direction. In order to cause sign inversion of the phase detector output, the sum of the phase shift contribution of the positive pulses, $\sum_{1}^{N_{up}} \Delta\phi_e[k]$, shall be in the neighborhood of $-\pi$:

$$\sum_1^{N_{up}} \Delta\phi_e[k] = -N_{up}T_r\omega_{off} - N_{up}\phi_p - \frac{N_{up}(N_{up}+1)}{2}T_r\omega_i \approx -\pi$$

$$\Rightarrow \quad N_{up}\left(T_r\omega_{off} + \phi_p + \frac{N_{up}+1}{2}T_r\omega_i\right) \approx \pi \quad (15)$$

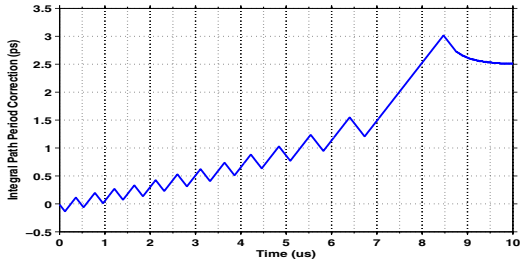
The frequency/ phase correction by the integral path can be ignored to approximate N_{up}. This assumption is valid since N_{up} is small at the edge of pull-in range and since K_i is usually $\ll K_p$ to maintain stability and to avoid strong ringing in the step response.

$$N_{up} \approx \frac{\pi}{T_r\omega_{off} + \phi_p} \quad (16)$$

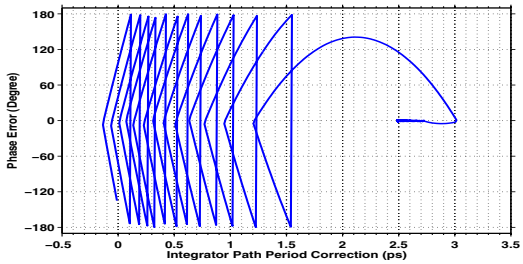
Now, when there is a negative phase error for the following N_{dn} periods, one can write

$$\begin{aligned}\Delta\phi_e[N_{up}+1] &= -T_r(\omega_{off} + N_{up}\omega_i) + \phi_p + T_r\omega_i\\ \Delta\phi_e[N_{up}+2] &= -T_r(\omega_{off} + N_{up}\omega_i) + \phi_p + 2T_r\omega_i\\ &\dots\\ \Delta\phi_e[N_{up}+N_{dn}] &= -T_r(\omega_{off} + N_{up}\omega_i) + \phi_p + N_{dn}T_r\omega_i\end{aligned}$$

From the last equation, it is obvious that the frequency correction at the end of a cycle slipping period is merely $(N_{dn} - N_{up})\omega_i$. To guarantee frequency acquisition, $N_{dn} \geq N_{up}+1$ to ensure the frequency error is reduced by at least ω_i at the end of the cycle slipping period. Otherwise, the frequency error will remain unchanged and not converge to zero with time. Similar to the phase shift by up pulses, the summation of the phase shift contribution by down pulses, $\sum_{N_{up}+1}^{N_{up}+N_{dn}} \Delta\phi_e[k]$, shall be in the neighborhood of $-\pi$ and it is equal to the following:



(a) Integral path output



(b) Trajectory of phase error vs. period correction

Fig. 3. Transient simulation of bang-bang PLL using time-based behavioral model, when frequency offset is 2.5 MHz.

$$\sum_{N_{up}+1}^{N_{up}+N_{dn}} \Delta\phi_e[k] = -N_{dn}T_r(\omega_{off} + N_{up}\omega_i) + N_{dn}\phi_p + \frac{N_{dn}(N_{dn}+1)}{2}T_r\omega_i \approx -\pi$$

By substituting $N_{dn} = N_{up} + 1$ in the above equation. we get the following simplified form

$$(N_{up}+1)\left(T_r\omega_{off} - \phi_p + \frac{N_{up}-2}{2}T_r\omega_i\right) \approx \pi \quad (17)$$

Adding Eq. 17 to Eq. 15 to get the total phase shift during the first cycle slip:

$$(2N_{up}+1)T_r\omega_{off} - \phi_p + (N_{up}^2 - 1)T_r\omega_i = 2\pi \quad (18)$$

Assume that $(N_{up}^2 - 1)T_r\omega_i \ll \phi_p$ (which is the case when $K_i < K_p/64$) such that the effect of ω_i can be ignored in Eq. 18. Now, substitute Eq. 16 into Eq. 18

$$\left[\frac{2\pi}{T_r\omega_{off} + \phi_p} + 1\right]T_r\omega_{off} - \phi_p \approx 2\pi \quad (19)$$

Rearranging Eq. 19 will result in quadratic equation in terms of ϕ_p that is easy to solve

$$T_r\omega_{off} \approx \sqrt{(2\pi + \phi_p)\phi_p} \quad (20)$$

From Eq. 20, the pull-in range can be expressed as

$$\boxed{f_{pull-in} = \frac{\omega_{off}}{2\pi} \approx f_{ref}\frac{\sqrt{(2\pi + \phi_p)\phi_p}}{2\pi}} \quad (21)$$

The pull in range formula can be simplified further without losing accuracy by recalling that $\phi_p \ll 2\pi$ (as required to achieve stability and low peak to peak jitter performance).

$$\boxed{f_{pull-in} \approx f_{ref}\sqrt{\frac{\phi_p}{2\pi}} = \sqrt{\frac{f_{ref}K_{dco}K_pK_{PD}}{2\pi}}} \quad (22)$$

Despite the simplicity of Eq.21 and Eq.22, they both do not capture the effect of K_i on pull-in range which could underestimate it especially if K_i is not very small relative to K_p. To include this effect, substitute Eq. 16 into Eq. 18 without ignoring ω_i. This will lead to cubic equation that can be solved for ω_{off}

$$\begin{aligned}(T_r\omega_{off})^3 &+ (\phi_p - T_r\omega_i)(T_r\omega_{off})^2 \\ &- (2\pi + \phi_p + 2T_r\omega_i)\phi_p T_r\omega_{off} \\ &+ (\pi^2 T_r\omega_i - \phi_p^3 - T_r\omega_i\phi_p^2 - 2\pi\phi_P^2) = 0 \end{aligned} \quad (23)$$

The exact solution to Eq. 23 is not provided here but it is plotted in Fig. 4. It is obvious that Eq. 21 and Eq. 23 are in general more accurate for high K_p/K_i ratio.

V. Analysis and Simulation Comparison

The pull in range as defined in Eq. 21 and Eq. 23 is proportional to the square root of the loop gain. This is similar to the conclusion presented in [6] but Eq. 21 and Eq. 22 is at least 40% more accurate than [6] when it compared with behavioral simulations in MATLAB/ Simulink (example of these simulations is shown in Fig. 3). Table I presents a comparison of pull-in range (normalized to reference frequency) for different combinations of K_p and K_i. Based on those results, we notice that when $K_i = K_p/300$, Eq. 21 estimates the pull-in range within +2% and when $K_i = K_p/75$ the estimation error increases to -7%. However, the estimation error increases to -23% once $Ki = K_p/4.4$. Using Eq. 23, this error reduces to 16%.

VI. Conclusion

This paper investigates the operation of binary bang bang PLLs in the far from lock region of operation. By analyzing the cycle slipping behavior of second-order PLLs in this region, a closed form is derived to accurately predict PLL pull-in frequency range. The same analysis can be extended to accurately estimate locking time though it is outside the scope of this paper. The analytical results are in good agreement with simulation results and 40% more accurate than previous work [6]. Our analysis tracks the change in phase error during each reference period within the first cycle slip.

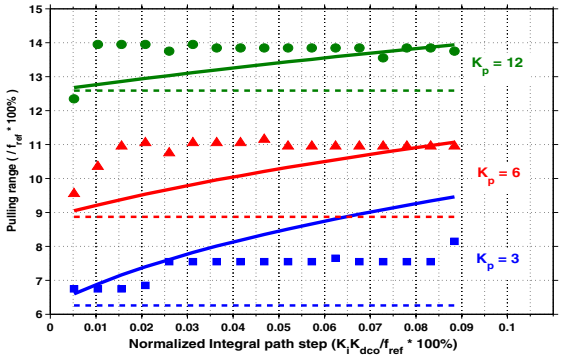


Fig. 4. Pull in range vs. different values of K_i and K_p. Dashed lines obtiained by Eq. 21, solid lines obtained by Eq. 23, and symbols are based on simulations.

K_p	K_i	Sims	Eq. 21	Eq. 23	[6]
3	0.04	6.75%	6.26%	6.60%	4.43%
3	0.68	8.15%	6.26%	9.46%	4.66%
12	0.04	12.35%	12.59%	12.68%	8.84%
12	0.68	13.75%	12.59%	13.94%	8.86%

TABLE I
THE LOCK-IN FREQUENCY BASED ON SIMULATION AND PRESENTED THEORY VERSUS RESULTS FROM OTHER REFERENCES

On the other hand, [6] estimates change in phase error on average and it evaluates pull-in range during the first and the second half of cycle slip which results in higher rounding error compared to our analysis.

Finally, Eq. 21 suggests the possibility of using a quantized phase detector with dynamic gain, K_{PD}, that varies according to the phase and frequency error. Such detector will have higher pull-in range and faster locking time, compared to BBPD, without affecting the steady state performance during phase locking.

References

[1] B. Razavi, Ed., *Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design*. Wiley-IEEE Press, 1996.

[2] N. Da Dalt, "Linearized Analysis of a Digital Bang-Bang PLL and its Validity Limits Applied to Jitter Transfer and Jitter Generation," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, no. 11, pp. 3663–3675, 2008, ISSN: 1549-8328.

[3] G. Marucci *et al.*, "Analysis and Design of Low-Jitter Digital Bang-Bang Phase-Locked Loops," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 61, no. 1, pp. 26–36, 2014, ISSN: 1549-8328.

[4] J. F. Oberst, "Pull-In Range of a Phase-Locked Loop with a Binary Phase Comparator," *Bell System Technical Journal, The*, vol. 49, no. 9, pp. 2289–2302, 1970, ISSN: 0005-8580.

[5] M. Ramezani *et al.*, "Analysis of a Half-Rate Bang-Bang Phase-Locked-Loop," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 49, no. 7, pp. 505–509, 2002, ISSN: 1057-7130.

[6] M. Chan and A. Postula, "Transient Analysis of Bang-Bang Phase Locked Loops," *Circuits, Devices Systems, IET*, vol. 3, no. 2, pp. 76–82, 2009, ISSN: 1751-858X.