A 10Gb/s 4.1mW 2-IIR + 1-Discrete-tap DFE in 28nm-LP CMOS

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***Abstract*—A half-rate decision feedback equalizer (DFE) with two infinite impulse response (IIR) filters and one discrete-time tap is presented. The two IIR filters have different time constants to cancel the long tail of the pulse response. The discrete-tap cancels the first post-cursor inter-symbol interference term. The system can operate with a low transmit swing of 150mVpp-diff and 24 dB channel loss at the Nyquist frequency while consuming 4.1mW at 10 Gb/s. The receiver, including the DFE, clock buffers and clock phase adjustment, occupies an area of 8,760 μm^2 and was fabricated in an ST 28nm LP CMOS process.**

I. Introduction

Chip-to-chip links over lossy PCB substrates (~1m in length at 10Gb/s), die-to-die links over silicon interposers (up to a few centimeters in length at 10+Gb/s), or coaxial cable links (whose maximum length depends upon the cable cross-section) have between 20-30dB loss at one-half the bitrate, often without any major channel discontinuities. Hence the primary impairments to signal integrity are noise, crosstalk and a long smooth tail in the pulse response resulting in inter-symbol interference (ISI) spanning more than 10 UI. A passive equalizer followed by a gain stage (e.g. [1]) can be used to cancel the long tail of the pulse response. Alternatively, a continuous time active linear equalizer may be used [1]. However, significant extra power is consumed and high frequency noise is amplified relative to the received signal amplitude. A transmit swing of several hundred mV can overcome the noise enhancement, but also increases crosstalk. Another approach to cancel the numerous post-cursor ISI terms of the channel is a decision feedback equalizer (DFE). A traditional DFE will allow the post-cursor ISI to be removed without enhancing noise or crosstalk but can consume a large amount of power for channels with a large number post-cursor ISI. Recent work has shown that infinite impulse response (IIR) DFE taps can efficiently cancel many post-cursor ISI terms [2], [3]. For example, [2] demonstrated 1 IIR + 1 discrete-tap DFE as shown in Fig. 1A. Here, we extend that DFE architecture to comprise of 2 IIR + 1 discrete-time taps, Fig. 1B, affording more flexibility to match the channel's pulse response while maintaining a low power consumption of 0.41mW/Gb/s.

The remainder of the paper is organized as follows. Section II discusses the DFE architecture chosen to compensate for a channel with a long pulse response while keeping the power consumption low. Section III shows the circuit implementation details followed by measurement results in section IV. Finally, section V concludes the paper.

II. DFE Architecture

The benefit of an IIR DFE is that a single tap can cancel many UI of ISI. However, whereas a discrete-time DFE remains effective as long as the loop delay is less than 1 UI (Fig. 2A), the performance of an IIR-DFE varies with loop delay, degrading significantly even for loop delays less than 1

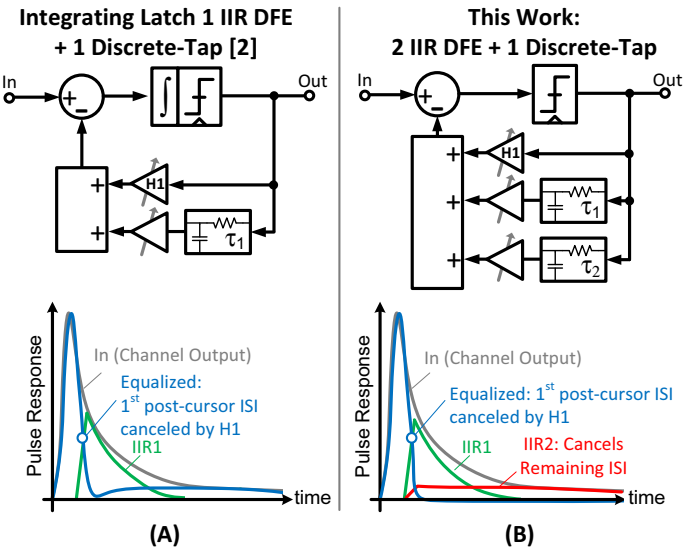


Fig. 1. Receiver equalizer architecture comparison: (A) Integrating latch with 1-IIR and 1 discrete-tap [2]. (B) 2-IIR and 1 discrete-tap [this work].

UI. Post layout simulations in a 28nm LP CMOS technology show that a 10% decrease in V_{DD} results in a ~0.2UI increase in latch clock-to-output delay at 10Gb/s shown in Fig. 2F (delays are normalized to a V_{DD} of 1V at the typical (TT) corner). Process variation will also affect the latch-delay and can cause significant increases. The increase in latch-delay reduces the eye opening anywhere from 0.1UI to 0.3UI in an IIR DFE system with no discrete-tap (Fig. 2B). However, combining one discrete-time DFE tap with the IIR-DFE makes it much more robust to delay variations (Fig. 2C) [2], [3]. Although the sensitivity to delay variations is addressed in [2] with the discrete-tap, since only one IIR filter is used there is limited freedom to shape the DFE response. Moreover, the windowed integration attenuates the signal by 3.92 dB at a frequency of one-half the bitrate creating more loss that needs to be equalized.

Using 2-IIR DFE taps provides a significant improvement over 1 IIR filter [4] as seen in Fig 2B vs. Fig. 2D. In [5] 2-IIR DFE taps are implemented with two separate feedback paths to minimize feedback loop delay. The additional feedback path necessitates a second 2:1 mux operating at the full data rate and consuming extra power. Even so, because there is no discrete-time tap in that work, the architecture's performance remains sensitive to latch clock-to-output delay which is in turn sensitive to V_{DD} and process variations (Fig 2F).

This work is the first to combine the benefits of 2 IIR-DFE taps plus one discrete-time DFE tap as shown in Fig 1B. The two IIR DFE taps cancel the long tail of the channel pulse response better than one tap can and the discrete-time DFE tap makes its performance insensitive to latch timing delays (Fig. 2E). Moreover, unlike past work, the proposed design is implemented in a low-power (LP) process suitable for devices

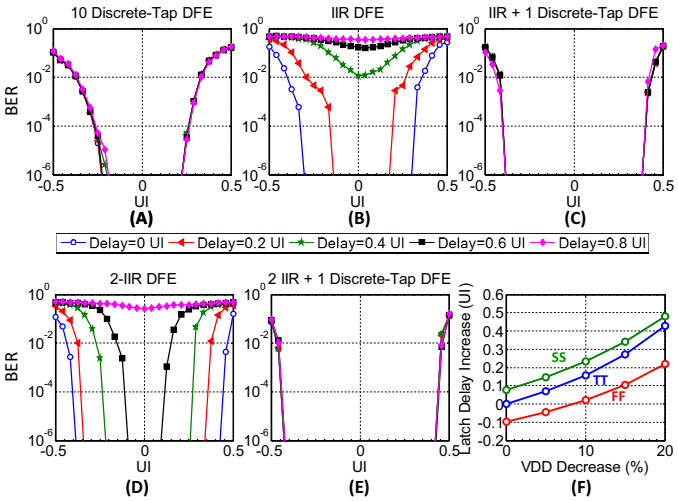


Fig. 2. (A) - (E) Simulated Bathtub curves with various latch-delays for different DFE architectures for a 32" backplane channel. (F) Post-layout simulations of latch-delay increase as a function of reduction in V_{DD}.

requiring low standby power, but where in general it can be difficult to realize the high gain-bandwidth product required for analog equalization.

III. Proposed Receiver

Fig. 3 is a block diagram of the proposed half-rate receiver. The front-end comprises of a passive equalizer and preamplifier. The passive linear equalizer can be disabled to compare different methods of equalization. Dynamic logic is used throughout. Unlike [2], a current integrating latch is not used, eliminating its inherent 3.92dB loss at the Nyquist rate. The 1 discrete-time plus 2 IIR DFE taps all feed directly into additional latch inputs. A single 2:1 mux, shown in Fig. 4 and followed by cross-coupled buffers, is used to drive both IIR filters. By contrast, [5] used two 2:1 muxes to minimize the loop delay for the fast IIR filter, and allow more settling time for the second IIR filter. In this work, the architecture includes a discrete-time tap making the performance relatively insensitive to small variations in loop delay and obviating the need for the additional mux.

A. Data re-muxing & IIR Filters

The implementation of the 2:1 differential mux is shown in Fig. 4. Two single-ended 2:1 muxes choose between each of the even and odd inputs and are followed by cross-coupled buffers. The clock is placed closer to the output of the mux to have a shorter delay to the output with respect to the data. Since the clock is aligned to sample the data in the middle of the eye opening, the data has been stable for some time and minimizing the delay from the clock to the output creates a faster mux.

The IIR filter time constants can be adjusted to fit the DFE response to that of the channel as shown in Fig 5. The two IIR filters have time constants an order of magnitude apart; hence, one is intended primarily to cancel the first 6 UI of post-cursor ISI while the other is primarily intended to cancel ISI that persists for more than 6 UI beyond the main cursor. The higher bandwidth filter, IIR1, can be adjusted between 200MHz to 3.2GHz while the lower bandwidth filter, IIR2, can be adjusted between 20MHz to 320MHz. Fig. 5A shows the IIR filter with a faster time constant (IIR1), which can be adjusted with 3 binary-weighted switched capacitors as well

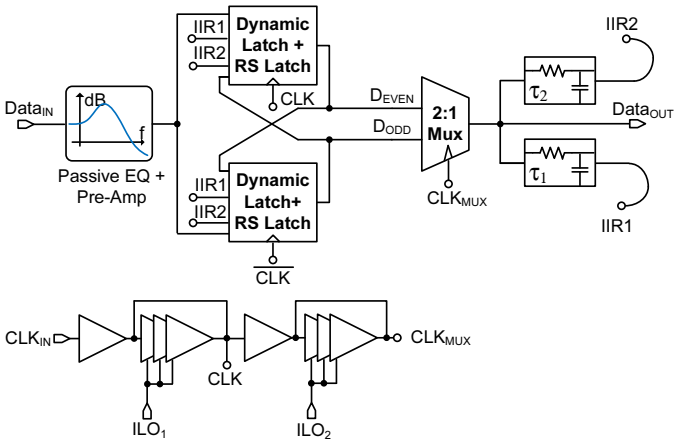


Fig. 3. Block diagram of the receiver

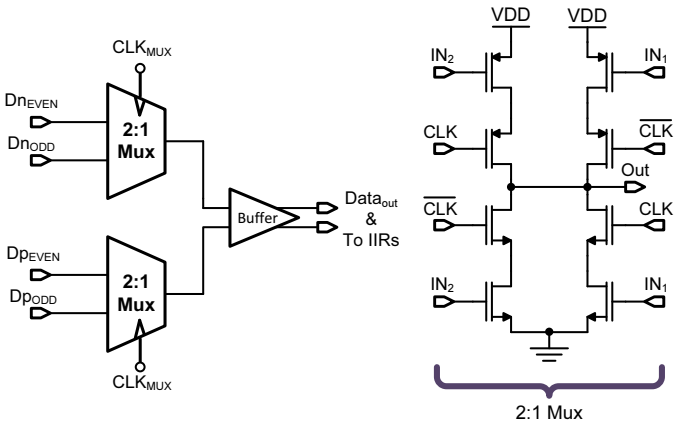


Fig. 4. Two dynamic 2:1 muxes are used to create a differential 2:1 mux

as a varactor. Since the DFE performance is more sensitive to the first few large post-cursor ISI contributors, having the varactor allows for finer tuning of the time constant to better match the pulse response. The tuning range of the varactor was designed to be larger than the LSB capacitor value to allow for tuning to any time constant within the range 200MHz to 3.2GHz. The filter IIR2, shown in Fig. 5B, has a 4-bit binary-weighted switched capacitor bank for tuning its time constant, but no varactor since the accuracy of this time constant is not as critical. The time constant of the IIR2 filter only needs to roughly match the long tail of the response to cancel the remaining post-cursor ISI.

B. Input Stage

Fig. 6 shows the CMOS inverter with resistive feedback used as a pre-amp. At the input, C1 and R1 provide attenuation

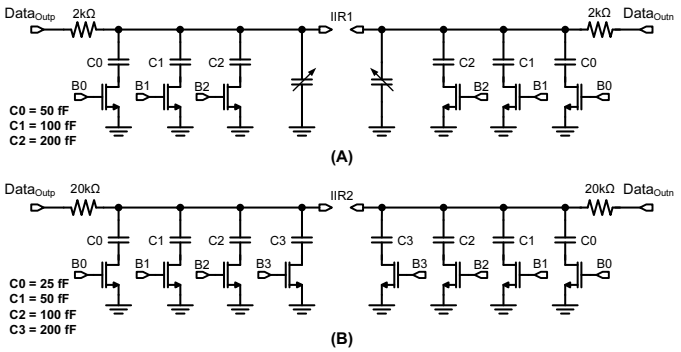


Fig. 5. IIR filters created using a resistor and switched capacitor circuits. The faster time constant IIR1 (A) includes a varactor to allow for finer tuning.

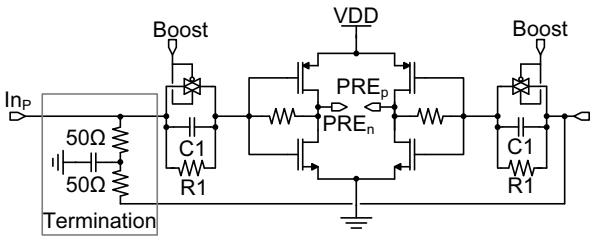


Fig. 6. Input termination, passive equalizer with disable, and preamplifier.

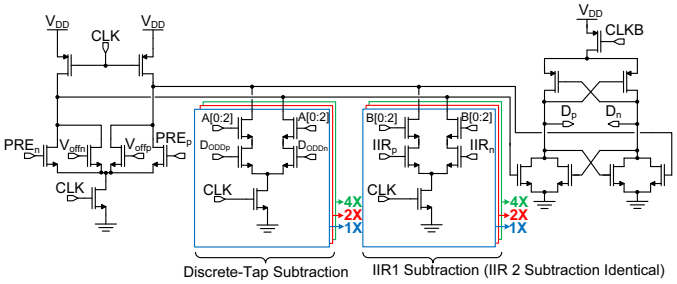


Fig. 7. Double-tail latch with DFE subtraction directly performed inside the latch. The subtraction for IIR2, not shown, is identical to and in parallel with IIR1.

at low-frequencies creating a relative boost at high-frequencies. The boost can be turned off by activating the transmission gate which shorts out C1 and R1. The input resistance to the pre-amp is designed to be more than 10X larger than the required 50 ohm termination resistance to minimize its impact on the matching network. The input common-mode is also set by the pre-amp assuming the incoming data is AC coupled.

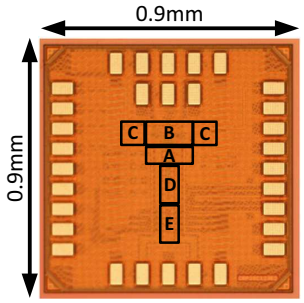
C. Summing and Latches

Fig. 7 shows a double-tail latch implementation [6] with additional differential inputs subtracting the DFE feedback signals [5]. Three binary-weighted transistor pairs sized 1X, 2X and 4X relative to the input pair can be selectively enabled to set the tap gains. In this work, the gain adjusting transistors are placed closer to the output to reduce the coupling from the fed-back data in the DFE (D_{ODDp}, D_{ODDn}, IIR_p, IIR_n, etc.) to the latch summing node. There are three subtraction paths, one for the lone discrete-tap and one for each of the 2 IIR filter outputs. A pair of transistors are introduced in parallel with the input pair to allow for offset compensation in the latch by adjusting V_{offp} & V_{offn} as shown in Fig. 7. The offset compensation transistor sizes were determined by post-layout monte-carlo simulations and were set to ensure the DC offset can be compensated well beyond 3σ.

IV. Measurement Results

The chip die photo along with an area breakdown is shown in Fig. 8. The measured channel attenuations are shown in Fig. 9 A, B for a 6 meter coax channel and a 34" backplane channel, respectively. The plots also contain the simulated losses of the characterization PCB and the QFN package which are ~2.5dB at 5GHz.

Fig. 10 shows an eye diagram at the output of the chip and Fig. 11 C, F show measured eye diagrams at the output of the channel at two different amplitudes. With the passive equalizer disabled, the DFE can successfully equalize a signal launched with a swing of only 150mVpp differential (mVpp-diff) and transmitted over a backplane channel with 24 dB attenuation,



	Block Description	Area (um^2)
A	Pre-Amp	2,030
B	DFE Core	1,620
C	IIR Filters	3,240
D	ILO 1	802
E	ILO 2	1,070
	Total	8,762

Fig. 8. Prototype 28nm-LP CMOS Die photo.

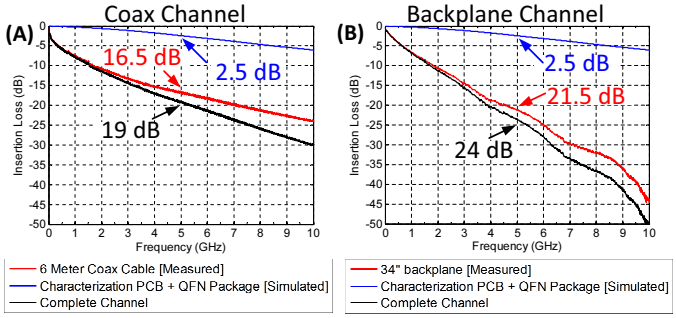


Fig. 9. A, B) Channel insertion loss including the receiver characterization PCB and QFN package loss. C) Model for the Characterization PCB + QFN Package.

or a 19 dB-loss coax cable driven single-endedly with only 75mVpp swing.

Fig. 11A, B show measured bathtub curves for the system employing only the passive equalizer for various transmit swing amplitudes and the two channels. Fig. 11D, E show the bathtub curve for the system with the passive equalizer disabled and only the DFE enabled at a transmit swing of 75mVpp (single-ended), and 150mVpp-diff (shown in Fig. 11F), respectively. For the backplane channel, to obtain similar horizontal eye openings, the passive equalizer requires an input swing which is 8X higher than using the DFE (1.2Vpp-diff shown in Fig. 11C). The larger swing is required to compensate for the low frequency attenuation of the signal used to relatively boost high frequencies. A continuous-time linear equalizer (CTLE) with gain could have been used to provide similar input sensitivity [7], but the additional power consumption of a CTLE is expected to be approximately 0.27 mW/Gbps [7]. In comparison, the power overhead for the proposed DFE is only that of the 2:1 CMOS mux and the extra dynamic power of the differential pairs performing subtraction in the DFE, both totaling only 0.074 mW/Gbps based upon post-extraction simulations. Furthermore, a CTLE amplifies crosstalk and high frequency noise whereas the proposed DFE-

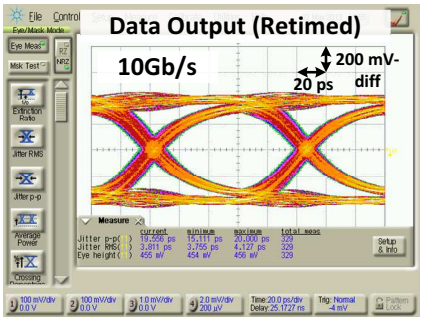


Fig. 10. Full-Rate retimed output from the chip.

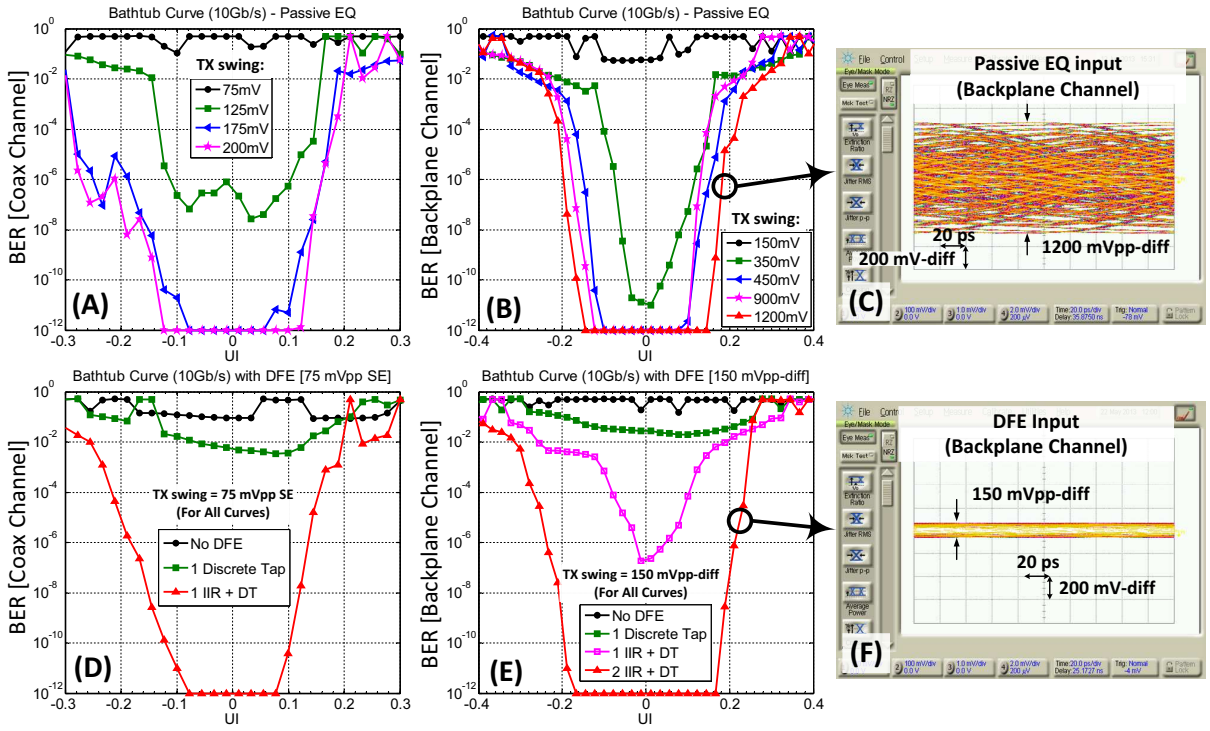
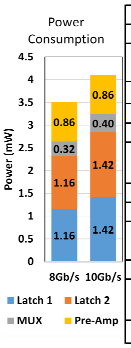


Fig. 11. (A,B) Bathtub curves at 10Gb/s using the passive EQ only for various TX swings. (C) Input to the receiver when the passive equalizer is used to equalize the signal with a swing of 1200 mVpp-diff. (D,E) Bathtub curves at 10 Gb/s for various DFE settings and with the passive EQ disabled. (F) Eye diagram at the channel output and input to the receiver with a swing of 150mVpp-diff when the DFE is used for equalization.



	This work	[2]	[3]	[5]	[7]	[8]
Data Rate (Gb/s)	10	10	5	10	16	6
Architecture	2 IIR + 1 DT DFE	1 IIR + 1 DT DFE	1IIR + 1DT + Pass. EQ	2 IIR DFE	TX EQ & RX CTLE	1 IIR DFE
Transmit Swing (mVpp-diff)	**150**	**700**	**NA**	**700**	**360**	**1000[b]**
Technology	**28nm (LP)**	**65nm**	**65nm (LP)**	**65nm**	**32 nm**	**90nm**
Attenuation @ Nyquist	24 dB	27 dB	15 dB	35 dB	18 dB	32.7 dB
Equalized Eye Width @ BER	33% @ 10^{-12}	28% @ 10^{-9}	66% @ 10^{-9}	31% @ 10^{-12}	40% @ 10^{-9} [b]	NA
PRBS Length	7	7	7	7	NA	7
Supply (V)	1	1	1.2	1	1.08	NA
Power (mW) [Excluding Clock Buffers]	4.1	3.5	2.3	9.9	12.64[c]	4
mW / Gbps	**0.41**	**0.35**	**0.46**	**0.99**	**0.79**	**0.67**
Required TX power (mW)[#] [Calculated into 50Ω load]	3	14	NA	14	7.78	20
Area (μm^2)	8,760	17,250	23,321	30,400[a]	20000[d]	89,000

[a] Area of DFE core only. [b] Calculated from Figure, [c] Includes CTLE & Samplers, [d] per lane
[#] Power consumed in final TX driver stage (doubly-terminated)

Fig. 12. Power breakdown and comparison to previous work

based receiver does not. The improved receiver sensitivity here can be translated into a minimum of 11mW (1.1mW/Gbps) power savings at the transmitter assuming a 150mVpp-diff driver instead of 700mVpp-diff over a doubly-terminated 50-Ohm-per-side link.

Fig. 12 shows a power breakdown of the receiver along with a table of comparison to previous work. The DFE power consumption consists of only dynamic power and as a result scales with frequency. Among the compared receivers, this work occupies the least area and can offer the lowest overall link power consumption owing to the greatly reduced transmit swing requirement.

V. Conclusion

Behavioural simulations showed that the large impact of feedback loop delay in IIR-based DFEs has a tremendous impact on the receiver performance, but a discrete-time tap was shown to make the architecture robust. An all dynamic power DFE with two IIR taps and one discrete-time tap was developed in a 28nm-LP process. It consumes 4.1 mW at 10Gb/s. The design has a lower input swing requirement and smaller circuit area than all previous designs as well as a lower area. The DFE was able to compensate 24dB of loss with a transmit swing of only 150mVpp-diff which is 8X lower than the swing required for a passive equalizer.

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