A 0.41pJ/bit 10Gb/s Hybrid 2 IIR and 1 Discrete-Time DFE Tap in 28nm-LP CMOS

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Abstract

An ideal infinite impulse response (IIR) decision feedback equalizer (DFE) can have an effect on wireline received waveforms similar to a continuous-time equalizer, but without the associated amplification of noise and crosstalk. However, an IIR DFE's performance degrades significantly as the feedback loop delay increases. Fortunately, adding a single discrete-time tap can eliminate the degradation. The implementation of a half-rate DFE with two IIR taps and one discrete-time tap is presented here. The two IIR filters have different time constants to accommodate a variety of channel pulse responses having a long tail. The discrete-time tap cancels the first post-cursor inter-symbol interference (ISI) term and alleviates feedback loop timing issues. The DFE can receive data transmitted with a low swing of 150mVpp-diff through 24dB of channel loss at half the bitrate while consuming 4.1mW at 10 Gb/s. Digital foreground calibration of clock phase shifters and offset cancellation is described. The receiver, including the DFE, clock buffers and clock phase adjustment, occupies an area of 8,760μm^2 in an ST 28nm LP CMOS process.

I. Introduction

In many high-speed (10+Gb/s) chip-to-chip links, the primary impairments to signal integrity are noise, crosstalk, and a smooth tail in the pulse response resulting in inter-symbol interference (ISI) spanning more than 10 unit interval (UI). As the aggregate bandwidth inside high-performance computing, networking infrastructure and mobile platforms increases, data rates must be increased throughout the communication hierarchy. Hence, the energy efficiency of all links must improve to stay within limited power envelopes, requiring low-power receivers that can overcome channel impairments. Chip-to-chip links over lossy printed circuit boards (approximately 1m in length at 10Gb/s) [1], die-to-die links over silicon interposers [2] (up to a few centimeters in length at 10+Gb/s), or coaxial cable links (whose maximum length for robust communication at 10+Gb/s data depends upon the cable cross-section) have between 20-30dB loss at one-half the bitrate [1], [2], [3]. In many cases, these links do not exhibit major discontinuities. Even backplane links may employ high-frequency connectors and/or backdrilling to mitigate the impact of the daughtercard-backplane discontinuity [4]. Hence, the pulse response for such links does not suffer from major reflections, but rather exhibits predominantly a long smooth tail of post-cursor ISI spanning 10 UI or more. These links require equalization to overcome the channel ISI and allow for data recovery at the receiver with low power consumption. Moreover, a receiver with improved sensitivity in the presence of noise and crosstalk can permit lower transmit swings thereby improving the links' energy efficiency [5], [6]. This paper addresses these needs describing the implementation of a low-power and robust DFE architecture combining continuous-time infinite impulse response (IIR) and discrete-time feedback filters.

The remainder of the paper is organized as follows.Section II provides background from prior art and compares different equalization architectures, including the one used in this work.

Section III shows the circuit implementation details followed by measurement results in section IV. Finally, section V concludes the paper.

II. BACKGROUND

Fig. 1 shows various equalization architectures that can be used for the links discussed in section II.

A. Continuous Time Linear Equalization

Although often simple in their implementation, continuous time linear equalizers amplify high-frequency noise and crosstalk and consume extra power. For example, a passive equalizer followed by a gain stage (e.g. [7]) can be used to cancel the long tail of the pulse response shown in Fig. 1A. Equivalently, the two can be combined into a continuous time active linear equalizer [6]. In both cases, high frequencies experience more gain in the receiver's linear front end than do low frequencies. Since low frequencies determine the baseline received eye opening, this means that the noise (which is broadband) and crosstalk (typically concentrated at high frequencies) are amplified with respect to the eye opening. Alternatively, the amplification can be performed at the transmitter so that a wider dc swing is transmitted and only a passive equalizer used at the receiver as shown in Fig. 1B resulting in the same eye opening as in Fig. 1A. In this case, the receiver's input-referred noise is not amplified but assuming near- and/or far-end crosstalk arises from similarly architected links, the wider transmit swing will still mean more high-frequency crosstalk. Furthermore, transmit swing cannot be increased indefinitely since it is ultimately limited by the power supply voltage of the transmitter.

B. Decision Feedback Equalization

A conventional discrete-time decision feedback equalizer (DFE), shown in Fig. 1C, is well-suited and power efficient for channels with a few dominant post-cursor ISI terms. Since the input to the DFE is the recovered digital data pattern free from channel noise and crosstalk, it is able to cancel ISI without amplifying noise or crosstalk and without attenuating the channel's main-cursor response. Fig. 2 shows the energy efficiency of some of the best DFE implementations plotted against the amount of attenuation they compensate. State-of-the-art DFE implementations consume 0.083-0.25 pJ/bit/tap [8], [9], [10], [11], [12]. Hence, DFEs are an efficient equalizer for the cancellation of a few taps of post-cursor ISI compared to a continuous-time linear equalizer which have recently been reported at 0.27 mW/Gbps [6]. For the cancellation of reflections, DFE taps with programmable delays, called roving taps, have been used [3], [13], [14]. Roving taps allow the system to cancel the most significant post-cursor ISI terms while only adding a few extra DFE taps; for example, additional taps in [3].

It is important to note that the channel loss at one-half the bitrate alone does not indicate the number of post-cursor ISI terms that are present. Fig. 3A shows the frequency response of two exemplar channels normalized to an arbitrary bitrate, f_{bit}: one dominated by skin effect loss and another dominated by dielectric loss. Both channels have 25dB of loss at one-half the bitrate. Fig. 3B shows the pulse responses of both channels with a transmitted pulse amplitude of 1 and 1 UI in duration with the post-cursor ISI terms shown. Channels dominated by dielectric loss have a faster-roll off (proportional to frequency) in their frequency response and a few dominant post-cursor ISI terms. The channel dominated by skin effect loss has a slower roll off in its frequency response (proportional to $\sqrt{f}$) and hence many more post-cursor ISI terms, in spite of having the same magnitude response at one-half the bitrate.

For channels exhibiting a long tail of ISI, discrete-time DFE complexity becomes prohibitive. For example, consider the channel response for the skin effect loss channel (Fig. 3B); note that 10 UI of post-cursor ISI terms exceed 5% of the main-cursor's amplitude. Based upon the state-of-the-art 0.083-0.25 pJ/bit/tap, at 10Gb/s a 10-tap DFE will consume 8.3-25 mW.

An alternative approach, illustrated in Fig. 4A(left), shows an integrating IIR DFE to equalize long pulse responses [2], [15], [16], [17]. In this approach, several discrete-time DFE taps are replaced by a single feedback tap with an infinite impulse response. The feedback path's response is designed to match and cancel the tail of the channel response shown in Fig. 4A(right).

C. Continuous-Time Equalization vs. IIR DFE

A continuous-time equalizer and IIR DFE can be shown to have similar effect on the received signal. Let $H(s)$ represent the transfer function of the channel, $G(s)$ represent the transfer function of a continuous-time (in this case, passive) equalizer as shown in Fig. 5A. The circuit parameters of the passive equalizer, R_{G1}, R_{G2}, and C_G are defined in Fig. 5C. Let $\alpha = R_{G2}/(R_{G1} + R_{G2})$, $\omega_{GZ} = 1/(R_{G1} \times C_G)$, and $\omega_{GP} = 1/(C_G \times (R_{G1}//R_{G2})$, then the passive equalizer transfer function can be written as

$$G(s) = \alpha \times \frac{1 + s/\omega_{GZ}}{1 + s/\omega_{GP}}. \tag{1}$$

If the recovered data is error free, the slicer output in the receiver is identical to the transmitted data. Hence, in Fig. 5B the IIR DFE is modeled as having access to the transmitted data. The circuit parameters of the DFE, R_1 and C_1 are defined in Fig. 5D. Let $I(s)$ represent the transfer function of the IIR DFE tap. If $\omega_{IP} = 1/(C_1R_1)$ then the transfer function for the IIR filter can be written as

$$I(s) = \beta \times \frac{1}{1 + s/\omega_{IP}}. \tag{2}$$

To compare the effect of the passive equalizer with the IIR DFE, we set $H(s) = 1$ so that only the equalizer transfer functions are compared. In that case, the overall link response in Fig. 5A is simply $G(s)$, whereas the overall response of the IIR DFE link in Fig. 5B is,

$$1 - I(s) = (1 - \beta) \times \frac{1 + s/(\omega_{IP} \times (1 - \beta))}{1 + s/(\omega_{IP})}. \tag{3}$$

The two approaches (continuous-time linear equalizer and IIR DFE) will be equivalent when (1) and (3) are equal. The DC gain and the pole of the two transfer functions are equal when β is set to $1 - \alpha$ and $\omega_{IP} = \omega_{GP}$ which means that $C_I = C_G$ and $R_I = R_{G1}//R_{G2}$. Under these conditions, it may also be shown that $\omega_{IP} \times (1 - \beta) = \omega_{GZ}$, as follows:

$$\begin{aligned} \omega_{IP} \times (1 - \beta) &= \frac{1}{C_G \times (R_{G1}//R_{G2})} \times \frac{R_{G2}}{R_{G1} + R_{G2}} \\ &= \frac{1}{C_G \times R_{G1}} \\ &= \omega_{GZ}. \end{aligned} \tag{4}$$

From (4) it can be seen that both the passive equalizer and IIR DFE are performing similar signal conditioning on the link, except that the IIR DFE operates on the recovered data, free from noise and crosstalk. When $H(s) \neq 1$, the continuous-time linear equalizer and IIR DFE can still be made equivalent if the IIR DFE is modified taking into the account the response of $H(s)$. The one provisio is that the model in Fig. 5B does not include the delay of the channel which will impact the DFE response, $I(s)$. The phase shift due to the delay will capture the fact that the DFE can only cancel post-cursor ISI. This model also does not capture the effect of error propagation.

If there is a continuous-time equalizer in front of the DFE, it alters the pulse response and often

makes it difficult to precisely cancel the ISI with a simple IIR DFE. If the channel attenuation is high and both a continuous-time equalizer and an IIR DFE are to be used, special care needs to be taken to make sure the IIR DFE can still match the shape of the pulse response after the continuous-time equalizer.

Depending on the shape of the pulse response, a single time constant IIR DFE filter may not be able to provide a good fit to cancel all of the post-cursor ISI. However, it has been shown that two IIR DFEs are well suited to a variety of coaxial cable and even backplane channels [14] shown in Fig. 4B(left). One filter is used to cancel the first few prevalent post-cursor ISI terms while the second filter will cancel the remaining pulse response tail as shown in Fig. 4B(right). In this text two IIR filters refers to having two parallel 1st-order IIR filters in the DFE. For channels with significant reflections, additional discrete-time taps can be used. The IIR filters can cancel the general shape of the pulse response while the additional discrete-time taps cancel remaining ISI due to reflections. Using a continuous-time linear equalizer with multiple discrete-time DFE taps to cancel the reflections is also possible, however, the reflections would be boosted by the continuous-time linear equalizer. This may require the system to have more discrete-time taps since even small reflections may be boosted and become significant.

D. IIR DFE Performance Analysis

The benefit of an IIR DFE is that a single tap can cancel many UI of post-cursor ISI. However, the performance of an IIR-DFE varies with loop delay, even for loop delays less than 1 UI , whereas a discrete-time DFE remains effective as long as the feedback loop delay is less than 1 UI. To illustrate this, Fig. 6A shows a 1 discrete-tap DFE with loop delay Δ which models the delay through the flip-flop, gain path and summer. It can be seen that as the loop delay (Δ) increases, the retimed data (V_{DT}) is shifted by the amount of the delay. However, the 1st

post-cursor ISI term can still be canceled as long as the delay is less than 1 UI. Fig. 6B shows the same analysis for the 1 IIR DFE architecture. As the loop delay is increased, the IIR gain and time constant are readjusted to best fit the shape of the pulse response. However, it is evident that as the delay increases, the amount of residual uncanceled 1st post-cursor ISI increases. Therefore, even for feedback loop delays less than 1 UI the performance of the receiver will degrade significantly. It should be noted that the rising slope of the IIR filter output (V_{IIR}) which is $1/\tau_1 \times \beta$ is limited by the time-constant (τ_1) that is selected so that the decaying V_{IIR} matches the shape of the channel. Any additional loop delay (Δ) decreases the cancellation which the IIR DFE tap can provide for the first post-cursor ISI; the reduction is given by $1/\tau_1 \times \beta \times \Delta$. The performance analysis remains the same if the loop delay is split between the flip-flop, summer, and gain path since this feedback path is linear.

Fig. 7A shows a simulated bathtub curve for a 10 discrete-tap DFE and it can be seen that the loop delay does not affect the horizontal eye opening. By contrast, the loop delay is much more critical in an IIR DFE. Fig. 7B shows the bathtub curve for an IIR DFE with increasing amounts of delay in the critical path and it is evident that the performance is heavily dependent on the loop delay. To minimize the effect of the delay in the critical timing path, a single 1st post-cursor discrete-time tap is dedicated to the cancellation of the first post-cursor ISI term. Specifically, the simulated horizontal eye opening, shown in Fig. 7C, remains similar for varying loop delays because the first post-cursor ISI is effectively canceled. This approach has been implemented in [2], [18] and although the sensitivity to delay variations is addressed with the discrete-tap, since only one IIR filter is used there is limited freedom to shape the DFE response. Moreover, in [2] the design requires a sample and hold in order to avoid the 3.92dB loss at half the bitrate, which can be difficult to achieve at high speeds in a bulk LP CMOS process, whereas in this design

the sampling is done directly by the latches without the 3.92dB penalty. The block diagram for this implementation is shown in Fig. 9A.

Using 2-IIR DFE taps provides a significant improvement over 1 IIR filter [19] as seen in Fig 7B vs. Fig. 7D for a 32" backplane channel with ~20dB of loss at one-half the bitrate. In [20] 2-IIR DFE taps are implemented with two separate feedback paths to minimize feedback loop delay, as shown in Fig. 9B. The additional feedback path necessitates a second 2:1 multiplexer operating at the full data rate and consuming extra power. Even so, because there is no discrete-time tap in that work, the architecture's performance remains sensitive to latch clock-to-output delay which is in turn sensitive to V_{DD} and process variations. Post layout simulations in a 28nm LP CMOS technology show that a 10% decrease in V_{DD} results in a ~0.2UI increase in latch clock-to-output delay at 10Gb/s, shown in Fig. 7F. (Delays are normalized to a V_{DD} of 1V at the typical (TT) corner.) Process variations can also cause significant increases in the latch delay. Increasing latch-delay by 0.2UI reduces the eye opening anywhere from 0.1UI to 0.3UI in a single tap IIR DFE without a discrete-tap for a ~20dB loss channel (Fig. 7B).

Under identical operating conditions, the 2-IIR DFE is not only more sensitive to loop delay than the 2-IIR + 1 DT DFE, it is also more sensitive to coefficient variations. Fig. 8 directly compares the 2-IIR DFE architecture (Fig. 8A) with a 2-IIR + 1-DT DFE (Fig. 8B). The black curve shows the bathtub curve for a $V_{DD} = 1V$ and $T = 25^oC$, where the loop delay is conservatively chosen to be $0.5UI$. As the V_{DD} drops to 0.9V and the temperature drops to -40^oC (blue curve), the loop delay increases by 0.2UI based on post-layout extracted simulations of the latch. Under this condition, the 2-IIR DFE eye is completely closed, however, there is only a minor degradation to the 2-IIR + 1 DT DFE. Finally, the red curve shows both systems at the reduced V_{DD} and temperature but the coefficients of the DFE have been re-optimized

for minimum post-cursor ISI. The eye opening of the 2-IIR DFE is partially restored but not completely, whereas the 2-IIR + 1 DT DFE is completely restored back the original eye opening, once again showing the insensitivity to loop delay. This analysis also shows that the 2-IIR + 1-DT DFE is less sensitive to coefficient variations since even without coefficient re-adjustment, the bathtub curve is still open.

This work is the first to combine the benefits of 2-IIR DFE taps plus one discrete-time DFE tap. The two IIR DFE taps cancel the long tail of the channel pulse response better than one tap can, and the discrete-time DFE tap makes its performance insensitive to latch timing delays (Fig. 7E). Moreover, unlike past work, the proposed design is implemented in a low-power (LP) process suitable for devices requiring low standby power, but where in general it can be difficult to realize the high gain-bandwidth product required for analog equalization. The proposed DFE implementation relies only upon dynamic logic also contributing to the low power consumption. The entirely dynamic logic DFE allows its power consumption to scale linearly with the bit rate and facilitates porting between CMOS technologies.

III. Proposed Receiver

Fig. 10 shows a block diagram of the proposed half-rate receiver. The front-end comprises a passive equalizer and preamplifier. The passive linear equalizer can be disabled to compare different methods of equalization. Dynamic logic is used throughout. Unlike [2], a current integrating latch is not used which would require a sample and hold to avoid the 3.92dB loss at one-half the bitrate. The 1 discrete-time plus 2-IIR DFE taps all feed directly into latch inputs. A single 2:1 multiplexer, shown in Fig. 13 and followed by cross-coupled buffers, is used to drive both IIR filters. By contrast, [20] used two separate 2:1 multiplexers to minimize the loop delay for the fast IIR filter, while allowing more settling time for the second IIR filter. In this

work, the architecture includes a discrete-time tap making the performance relatively insensitive to small variations in loop delay and obviating the need for the additional multiplexer. The half-rate architecture necessitates the use of a 2:1 multiplexer since the "memory" elements in the analog IIR filters are capacitors which must be exposed to every recovered bit in sequence in order to produce the correct analog feedback waveform. Therefore, the system needs to have a mechanism to multiplex the half-rate data.

A. Input Stage

Fig. 11 shows the CMOS inverter with resistive feedback used as a pre-amp. At the input, C1 and R1 provide attenuation at low-frequencies creating a relative boost at high-frequencies. The boost can be turned off by activating the transmission gate which shorts out C1 and R1. The input resistance to the pre-amp is designed to be more than $10\times$ larger than the required 50Ω termination resistance to minimize its impact on the matching network. The input common-mode is also set by the pre-amp assuming the incoming data is AC coupled.

B. Summing and Latches

The DFE subtraction is directly performed inside the latch to reduce the feedback loop delay. Fig. 12 shows a double-tail latch implementation [21] with three additional differential inputs subtracting the DFE feedback signals: one for the discrete-tap and two for the IIR taps. For each DFE feedback input, three binary-weighted transistor pairs sized $1\times$, $2\times$ and $4\times$ relative to the input pair can be selectively enabled to set the tap gains. In this work, the enable transistors are placed closer to the output to reduce the coupling from the fed-back data in the DFE (D_{ODDp}, D_{ODDn}, IIR_p, IIR_n, etc.) to the latch summing node. The polarity of the subtraction is fixed under the assumption that the channel behavior is low pass and the post-cursor ISI will always

be positive. A pair of transistors are introduced in parallel with the input pair to allow for offset compensation in the latch by adjusting V_{offp} & V_{offn} as shown in Fig. 12. The offset compensation transistor sizes were determined by post-layout monte-carlo simulations and were set to ensure the DC offset can be compensated well beyond 3σ.

C. Data re-multiplexing & IIR Filters

Two single-ended 2:1 multiplexers choose between each of the even and odd inputs and are followed by cross-coupled buffers. The implementation of the 2:1 differential multiplexer is shown in Fig. 13. The clock is placed closer to the output of the multiplexer to provide a shorter clock-to-output delay. The clock edges are aligned midway between data transitions to ensure the data is stable while selected by the multiplexer.

The IIR filter time constants can be adjusted to fit the DFE response to that of the channel as shown in Fig 14. The two IIR filters have time constants an order of magnitude apart; hence, one is intended primarily to cancel the first 6 UI of post-cursor ISI while the other is primarily intended to cancel ISI that persists for more than 6 UI beyond the main-cursor. The higher bandwidth filter, IIR1, can be adjusted between 200MHz to 3.2GHz while the lower bandwidth filter, IIR2, can be adjusted between 20MHz to 320MHz. Fig. 14A shows the IIR filter with a faster time constant (IIR1), which can be adjusted with 3 binary-weighted switched capacitors as well as a varactor. Since the DFE performance is more sensitive to the first few large post-cursor ISI contributors, having the varactor allows for finer tuning of the time constant to better match the pulse response. The tuning range of the varactor was designed to be greater than the 50fF LSB capacitor providing some overlap to cover the entire range 200MHz to 3.2GHz. The filter IIR2, shown in Fig. 14B, has a 4-bit binary-weighted switched capacitor bank for tuning its time constant, but no varactor since the accuracy of this time constant is not as critical. The

time constant of the IIR2 filter only needs to roughly match the long tail of the response to cancel the remaining post-cursor ISI. Any process variations causing a change in the resistance or capacitance values can compensated for by adjusting the filter setting.

D. Clocking and Output Buffers

Two injection locked oscillators (ILOs) are included on-chip to sweep the input half-rate clock phase for BER bathtub curve measurements. Providing two variable clock delays allows for independent control of the clock phases applied to the latches and to the 2:1 multiplexor. A block diagram of the clocking circuits is shown in Fig. 15A. ILO1 is tuned to provide an adjustable phase shift covering 1UI at data rates of 10-12Gb/s [22]. For testing at 7-10Gb/s, additional delay tuning was required. Hence, additional tunable delay cells were included at the input prior to the ILO1 ring. Incorporating the additional delay stages within the ring would not have been practical since that would reduce the frequency lock range of the ILO [23] and thereby limit the achievable phase shifts. Placing the delay stages prior to the ILO ring allows the ring to clean up any duty cycle distortion introduced by the delay stages before the clock is applied to the DFE latches. If the additional delay stages are placed at the output of the ILO they could act as both delay and the clock buffers which would save power.

The second ILO (ILO2) adjusts the clock delay between the multiplexer sampling clock and the latch output. This delay is used to account for the clock-to-Q delay of the latches, and hence requires only fine tuning. Nevertheless, the same wide tuning range ILO was used for ILO1 and ILO2 for simplicity. It is desirable to make the phase shift through ILO2 small, otherwise the IIR tap may not settle prior to the second post-cursor. In that case, the same problem described in Fig. 6 would then apply to canceling the 2nd post-cursor ISI term. The delay stage schematic is shown in Fig. 15B and allows for tuning the delay by varying the voltage across the pull-up

PMOS device [24].

Both ILOs and all clock buffers consume 18.5mW to 35.4mW depending on the ILO control voltages. The power consumption of the clocking was not optimized and hence the ILOs and clock buffers are connected to a separate supply voltage and not included in the receiver's power consumption. This is consistent with the other works cited in Fig. 2 and Fig. 24 except for [9].

IV. Measurement Results

The chip die photo along with an area breakdown is shown in Fig. 16. The measurement setup is shown in Fig. 17. A Centellax TG1B1-A PRBS/BERT unit is used to provide PRBS data to the chip and measure BER. A pair of broadband attenuators are used in conjunction with the swing adjustment available from the source to obtain the desired swing levels. A Centellax TG1C1A provides a half-rate, 5GHz, clock to the DUT. The 10 GHz clock provided for the BERT/PRBS is from an Agilent 83732B Signal Generator. The BERT clock and the 5GHz clock for the DUT are synchronized using 10MHz reference ports in the test equipment. The BERT clock is automatically aligned to the retimed data provided from the DUT. A PC sets the DFE coefficients, latch offset cancellation, and the phase of the clocks using the on-chip ILOs and obtains BER information from the BERT creating a bathtub curve.

To obtain the most accurate information regarding the ILOs' tuning range, the ILOs were characterized in situ using the data path. The configuration for this measurement is shown in Fig. 18A. The input was removed from the system and the digital offset controls shown in Fig. 12 were set to their maximum values. This ensures that the even path in the half-rate receiver always outputs a logic one and the odd path would always output a logic zero. This leads to an oscillating data pattern at the output of the 2:1 multiplexer which is transmitted off chip. The ILO voltage was then set to zero and the output phase was recorded as a baseline. As the ILO

control voltage was increased, the difference in phase was measured as shown in Fig. 18B. Once ILO1 was completely characterized, its control voltage was set to 0 and the second ILO was characterized using the same approach. The measured ILO delay vs. control voltage is shown in Fig. 19 for 10Gb/s and 8Gb/s clocks.

Calibration of the offset in each of the odd/even latches is performed as shown in Fig. 20A. First, the even path digital offset control is set to its maximum value, so that the even path output is always a logic one. The digital offset control in the odd path (V_A) is then adjusted and the output (D_{OUT}) is observed on an oscilloscope. Starting the offset control at a high voltage ensures the odd path output is always a logic one, and therefore $D_{OUT} = 111...11$ as shown in Fig. 20B. The offset control V_A is then decreased one LSB at a time until the output begins to sometimes switch to a logic zero as shown in Fig 20C,D. Finally V_A is decreased until the output completely switches between a logic one and a logic zero leading to the pattern $D_{OUT} = 10101...01$. The offset voltage for the odd path is set to the point where the odd path output is low approximately one-half of the time. The same approach is used to characterize the offset for the even path.

The measured frequency response of the channels used for DFE characterization are shown in Fig. 21A and B: a 6 meter coax channel, and a 34" backplane channel, respectively. The plots also contain the simulated losses of the characterization PCB and the QFN package based on the model shown in Fig. 21E. A 25mm PCB trace is used on the characterization board to connect SMA connectors to the QFN package housing the prototype. An approximately 2.5mm bondwire is used to connect the package pads to the die, modeled as a 2.5nH inductance, and a 70fF pad capacitance is based on post-layout extraction. The losses of the characterization board are ~2.5dB at 5GHz. The pulse response for the coax and backplane channels are shown in Fig.

21C, D, respectively.

Fig. 22 shows an eye diagram at the output of the chip and Fig. 23 C, F show measured eye diagrams at the output of the channel at two different amplitudes. With the passive equalizer disabled, the DFE can successfully equalize a signal launched with a swing of only 150mVpp differential (mVpp-diff) and transmitted over a backplane channel with 24 dB attenuation, or a 19 dB-loss coax cable driven single-endedly with only 75mVpp swing. Finding the DFE coefficients requires iteration since the coefficients are not independent. The discrete-tap is adjusted to lower the BER, then the gain and bandwidth of IIR2, and finally IIR1 are adjusted. The process is repeated a few times to improve the eye-opening on the bathtub curve. Adaptation of the gains in an IIR DFE can be performed using the LMS algorithm, similar to discrete-taps, because as long as the IIR time-constants remain fixed the feedback filter is simply an adaptive linear combiner. If the IIR time constants are also to be adapted, adaptation is more difficult since a multi-modal performance surface arises. In that case, a heuristic or some a priori knowledge may be necessary estimate the IIR time-constants. BER-based adaptation may also be used [25], although they offer slow adaptation times. In [15] and [26] IIR DFEs are presented which include adaptation.

Fig. 23A, B show measured bathtub curves for the two channels with the receiver configured using only the passive equalizer (DFE disabled) for various transmit swing amplitudes. Fig. 23D, E show the bathtub curve for the receiver with the DFE enabled and passive equalizer disabled at a transmit swing of 75mVpp (single-ended), and 150mVpp-diff (shown in Fig. 23F), respectively. For the backplane channel, to obtain similar horizontal eye openings, the passive equalizer requires an input swing which is $8\times$ higher than using the DFE (1.2Vpp-diff shown in Fig. 23C vs. 150mVpp-diff in Fig. 23F). The larger swing is required to compensate for the

continuous-time passive equalizer's low frequency attenuation of the signal. A continuous-time linear equalizer with gain could have been used to improve input sensitivity but the additional power consumption of a continuous-time linear equalizer is expected to be approximately 0.27 mW/Gbps [6].

In comparison, the power overhead for the proposed DFE is only that of the 2:1 CMOS multiplexer, the extra dynamic power of the differential pairs performing subtraction in the DFE, and the pre-amp all totaling only 0.16 mW/Gbps based upon post-layout simulations.

Furthermore, a continuous-time linear equalizer amplifies crosstalk and high frequency noise whereas the proposed DFE-based receiver does not. The improved receiver sensitivity here can be translated into a minimum of 11mW (1.1mW/Gbps) power savings at the transmitter assuming a 150mVpp-diff driver instead of 700mVpp-diff ([2], [20]) over a doubly-terminated 50-Ohm-per-side link.

Fig. 24 shows a power breakdown of the receiver along with a table of comparison to previous work. The DFE power consumption consists of only dynamic power and as a result scales with frequency. Among the compared receivers, this work occupies the least area and can offer the lowest overall link power consumption owing to the greatly reduced transmit swing requirement.

V. Conclusion

Different approaches to equalization of links with smooth pulse responses spanning 10+ UI were presented. The complexity and power consumption of conventional discrete-time DFEs become prohibitive for such channels and IIR DFEs were shown to be a power efficient architecture for these types of channels. A continuous-time equalizer was shown to have the same impact upon received signal ISI as an IIR DFE. Behavioral simulations showed that feedback loop delay has a tremendous impact on the performance of IIR DFEs, but the addition of a

discrete-time tap was shown to make the architecture robust. A circuit implementation of the DFE with two IIR taps and one discrete-time tap was developed in a 28nm-LP process exhibiting only dynamic power consumption. Digital foreground calibration of ILO-based phase shifters and offset cancellation was described. The DFE consumes 4.1 mW at 10Gb/s. The design has a lower input swing requirement and smaller circuit area than all previous designs as well as a lower area. The DFE was able to compensate 24dB of loss with a transmit swing of only 150mVpp-diff, $8\times$ lower than the swing required using the passive equalizer.

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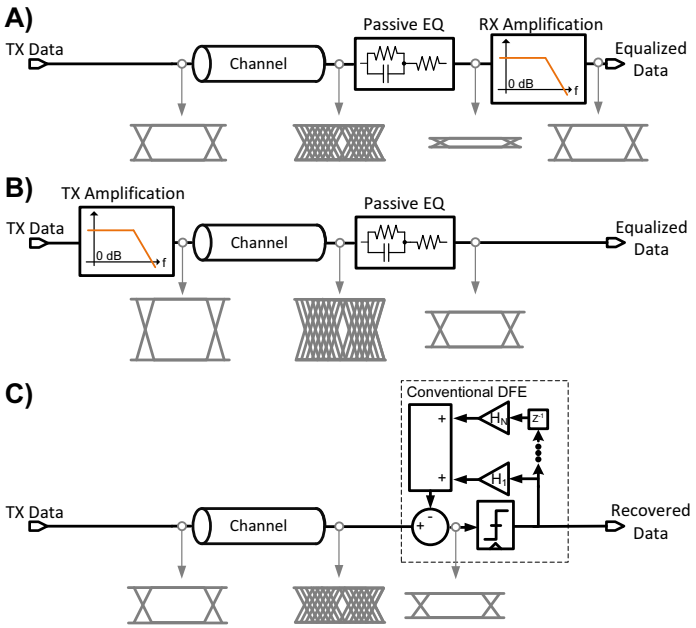
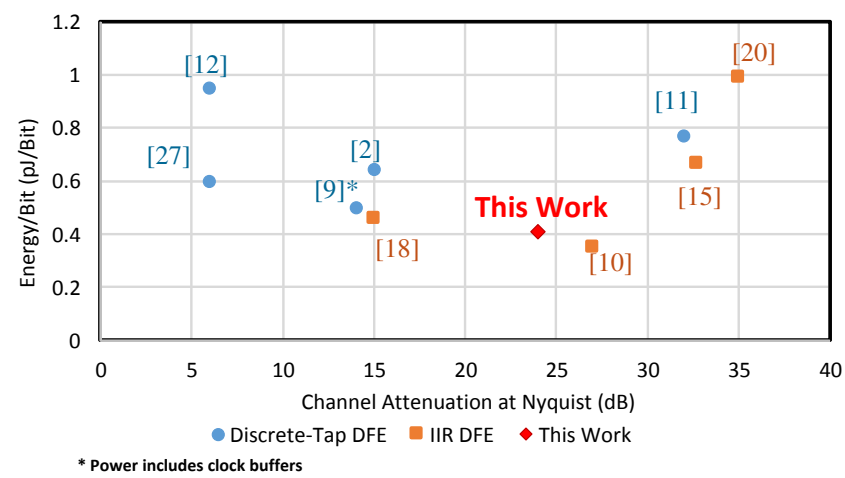


Fig. 1. Various architectures for link equalization: A) A passive equalizer and amplification at the receiver. B) Amplification in the transmitter along with a passive equalizer at the receiver. C) A decision feedback equalizer at the receiver



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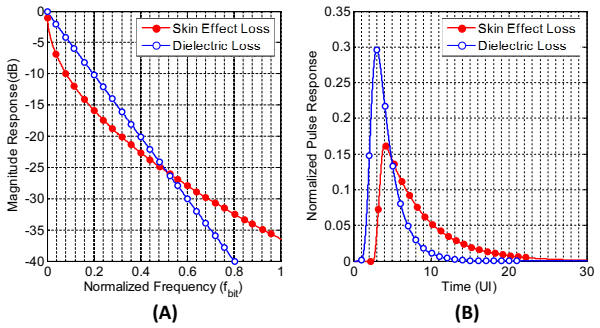

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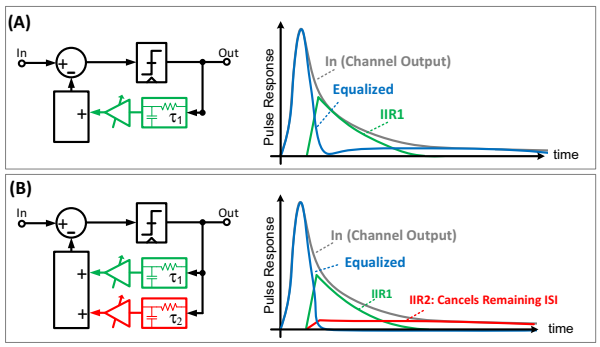

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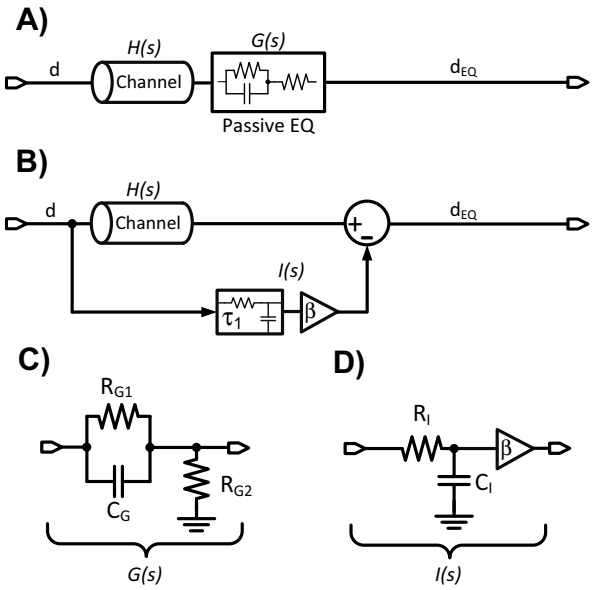

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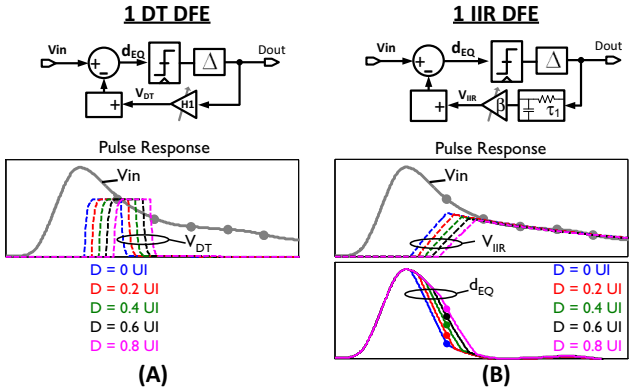

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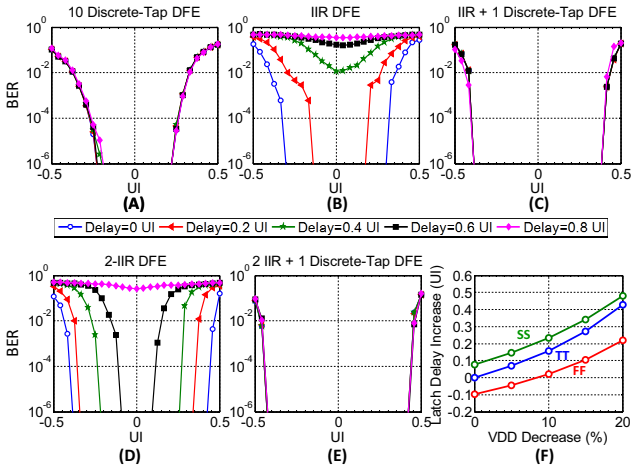

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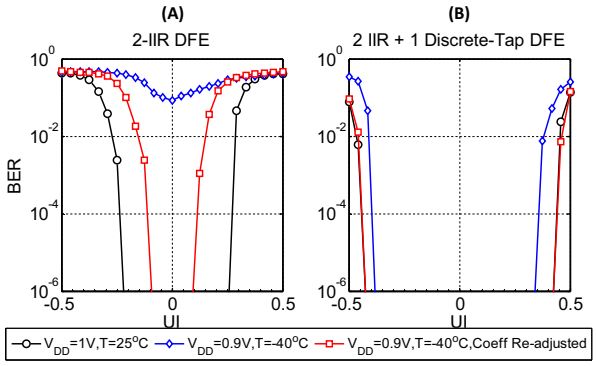

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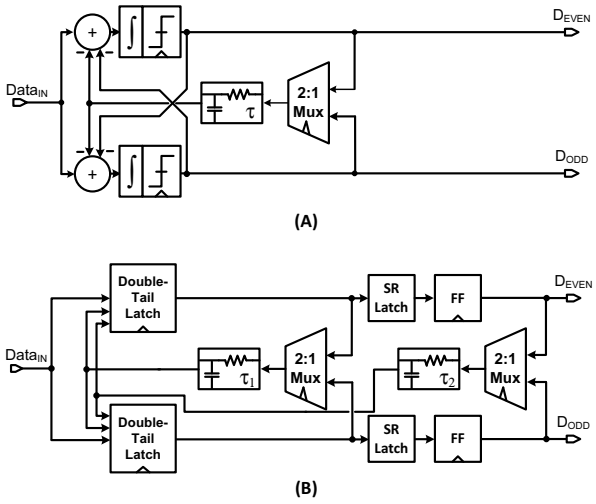


Fig. 9. (A) Block diagram of a 1 IIR + 1 Discrete-tap DFE [2]. (B) Block diagram of a 2 IIR DFE [20]

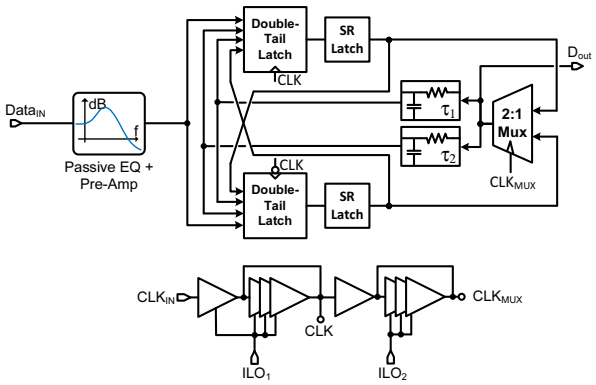


Fig. 10. Block diagram of the receiver

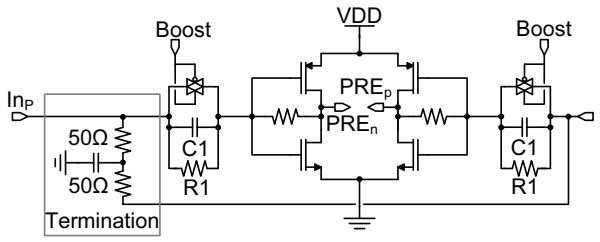


Fig. 11. Input termination, passive equalizer with disable, and preamplifier.

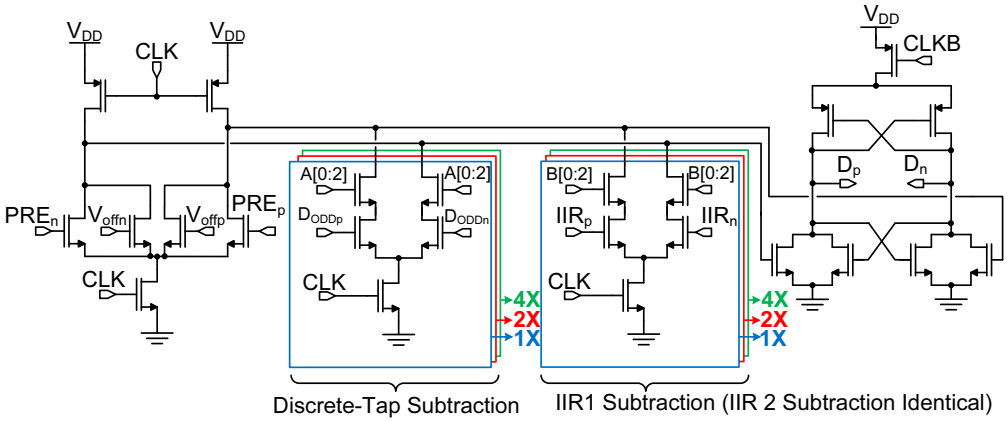


Fig. 12. Double-tail latch with DFE subtraction directly performed inside the latch. The subtraction for IIR2, not shown, is identical to and in parallel with IIR1.

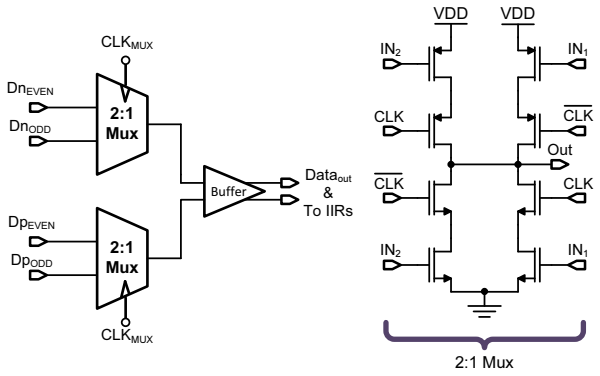


Fig. 13. Two dynamic 2:1 multiplexers are used to create a differential 2:1 multiplexer

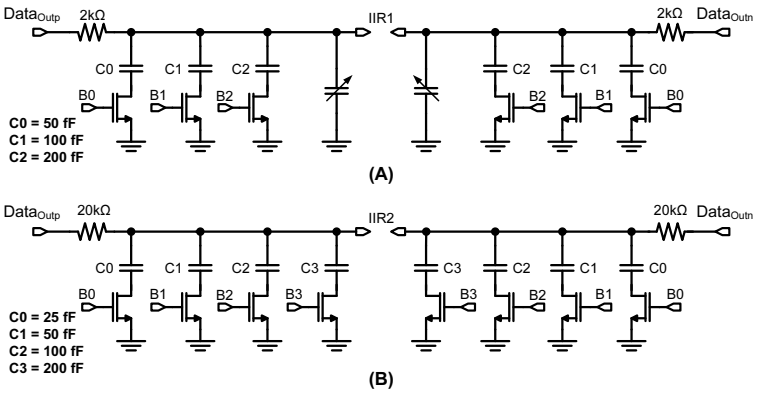


Fig. 14. IIR filters created using a resistor and switched capacitor circuits. The faster time constant IIR1 (A) includes a varactor to allow for finer tuning.

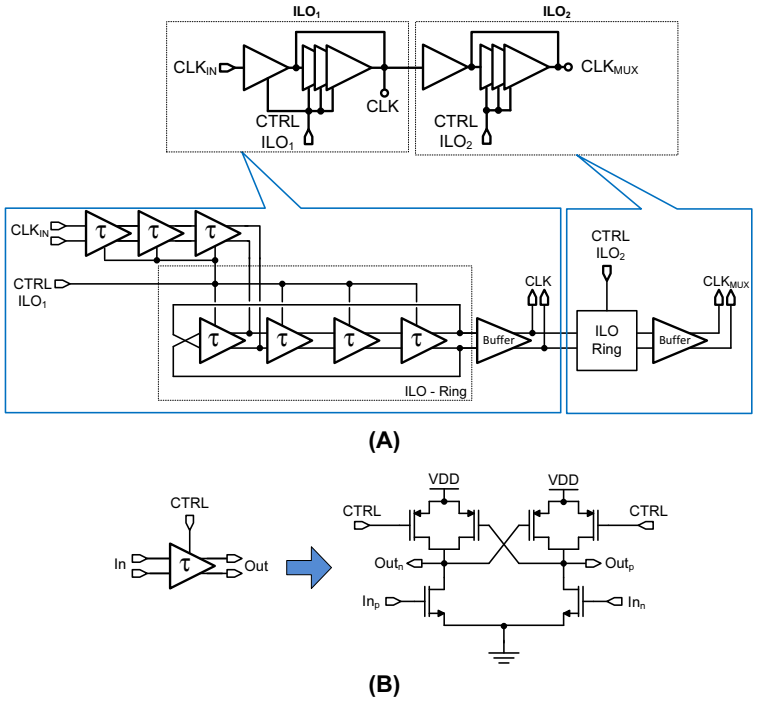
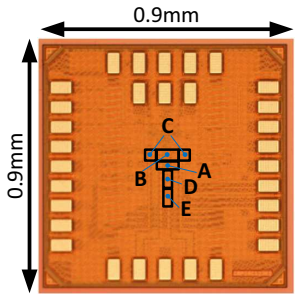


Fig. 15. (A) ILO1 and ILO2 block diagram showing the delay cells and the ring ILO used. (B) ILO delay cell schematic



Block Description		Area (um^2)
A	Pre-Amp	2,030
B	DFE Core	1,620
C	IIR Filters	3,240
D	ILO 1	802
E	ILO 2	1,070
Total		8,762

Fig. 16. Prototype 28nm-LP CMOS Die photo.

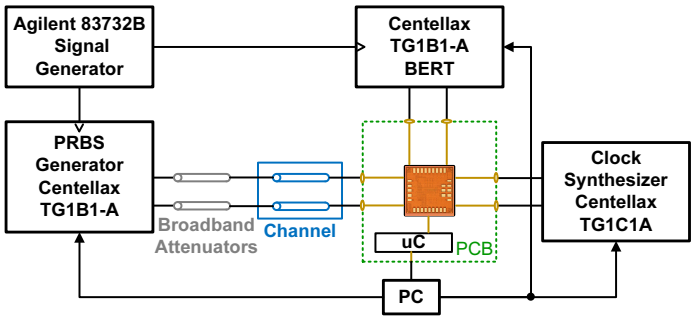


Fig. 17. Measurement setup.

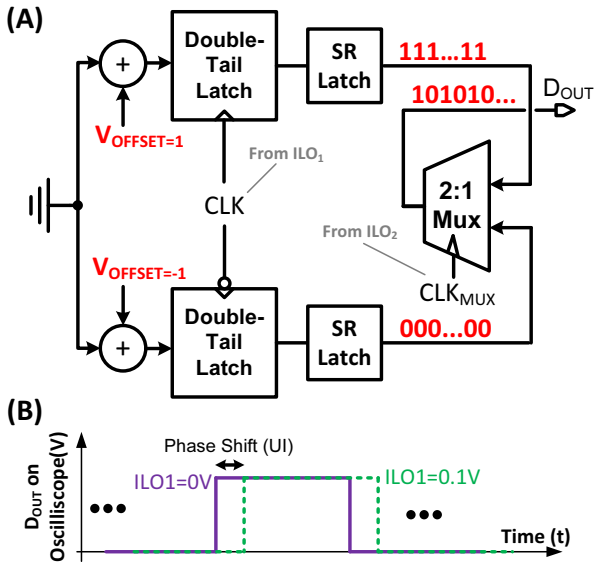


Fig. 18. (A) ILO measurement setup by setting offset voltages to their maximum and minimum values. (B) Clock pattern generated at the output is measured to determine phase shift introduced by the ILOs.

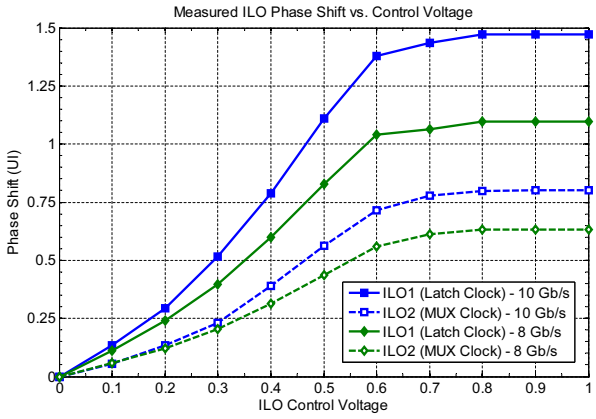


Fig. 19. ILO tuning characteristics for both ILO1 and ILO2 at 10Gb/s and 8Gb/s

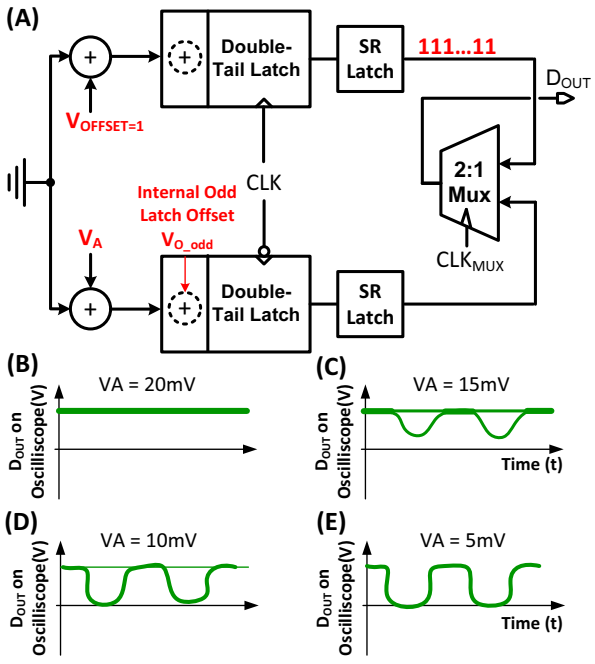


Fig. 20. (A) Latch offset calibration setup to compensate for offset on the odd path (B) Pattern generated at the output is measured to determine amount of offset present in the latch.

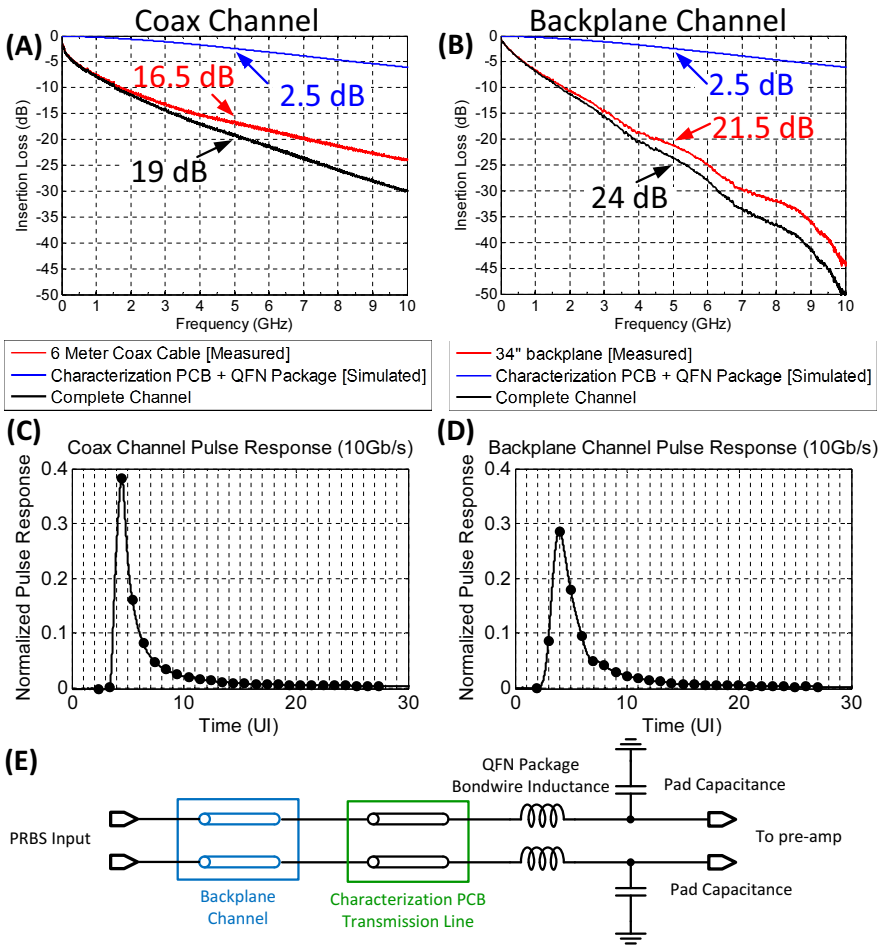


Fig. 21. A, B) Channel insertion loss including the receiver characterization PCB and QFN package loss. The coax and backplane channel losses are dominated by skin effect and dielectric loss, respectively. C,D) Channel pulse response for coax and backplane channels, respectively E) Model for the Characterization PCB + QFN Package.

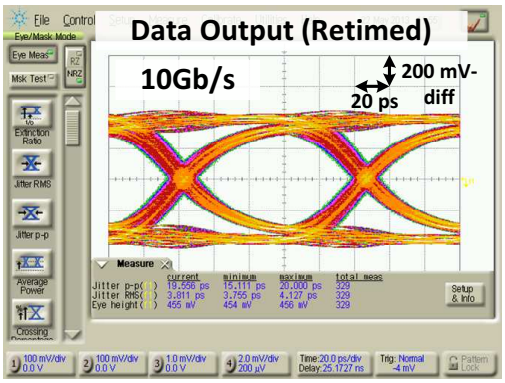


Fig. 22. Full-Rate retimed output from the chip.

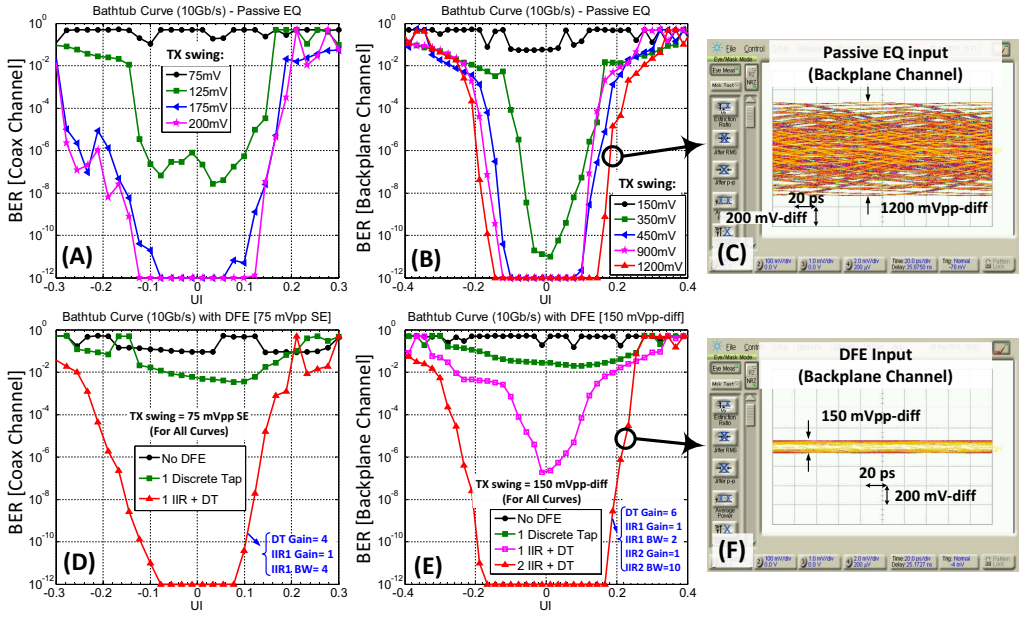
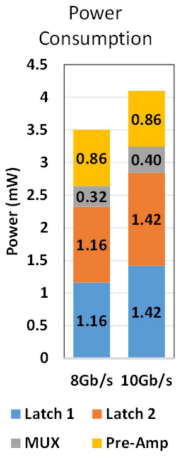


Fig. 23. (A,B) Bathtub curves at 10Gb/s using the passive EQ only for various TX swings. (C) Input to the receiver when the passive equalizer is used to equalize the signal with a swing of 1200 mVpp-diff. (D,E) Bathtub curves at 10 Gb/s for various DFE settings and with the passive EQ disabled. (F) Eye diagram at the channel output and input to the receiver with a swing of 150mVpp-diff when the DFE is used for equalization.



	[2]	[18]	[20]	[6]	[15]	This work
Data Rate (Gb/s)	10	5	10	16	6	10
Architecture	1 IIR + 1 DT DFE	1IIR + 1DT + Pass. EQ	2 IIR DFE	TX EQ & RX CTLE	1 IIR DFE	2 IIR + 1 DT DFE
Transmit Swing (mVpp-diff)	**700**	**NA**	**700**	**360**	**1000[b]**	**150**
Technology	**65nm**	**65nm (LP)**	**65nm**	**32 nm**	**90nm**	**28nm (LP)**
Attenuation @ Nyquist	27 dB	15 dB	35 dB	18 dB	32.7 dB	24 dB
Equalized Eye Width @ BER	28% @ 10^{-9}	66% @ 10^{-9}	31% @ 10^{-12}	40% @ 10^{-9} [b]	NA	33% @ 10^{-12}
PRBS Length	7	7	7	NA	7	7
Supply (V)	1	1.2	1	1.08	NA	1
Power (mW) [Excluding Clock Buffers]	3.5	2.3	9.9	12.64[c]	4	4.1
mW / Gbps	**0.35**	**0.46**	**0.99**	**0.79**	**0.67**	**0.41**
Required TX power (mW)[#] [Calculated into 50Ω load]	14	NA	14	7.78	20	3
Area (μm^2)	17,250	23,321	30,400[a]	20000[d]	89,000	8,760

[a] Area of DFE core only. [b] Calculated from Figure, [c] Includes CTLE & Samplers, [d] per lane
[#] Power consumed in final TX driver stage (doubly-terminated)

Fig. 24. Power breakdown and comparison to previous work