A Methodology for Accurate DFE Characterization

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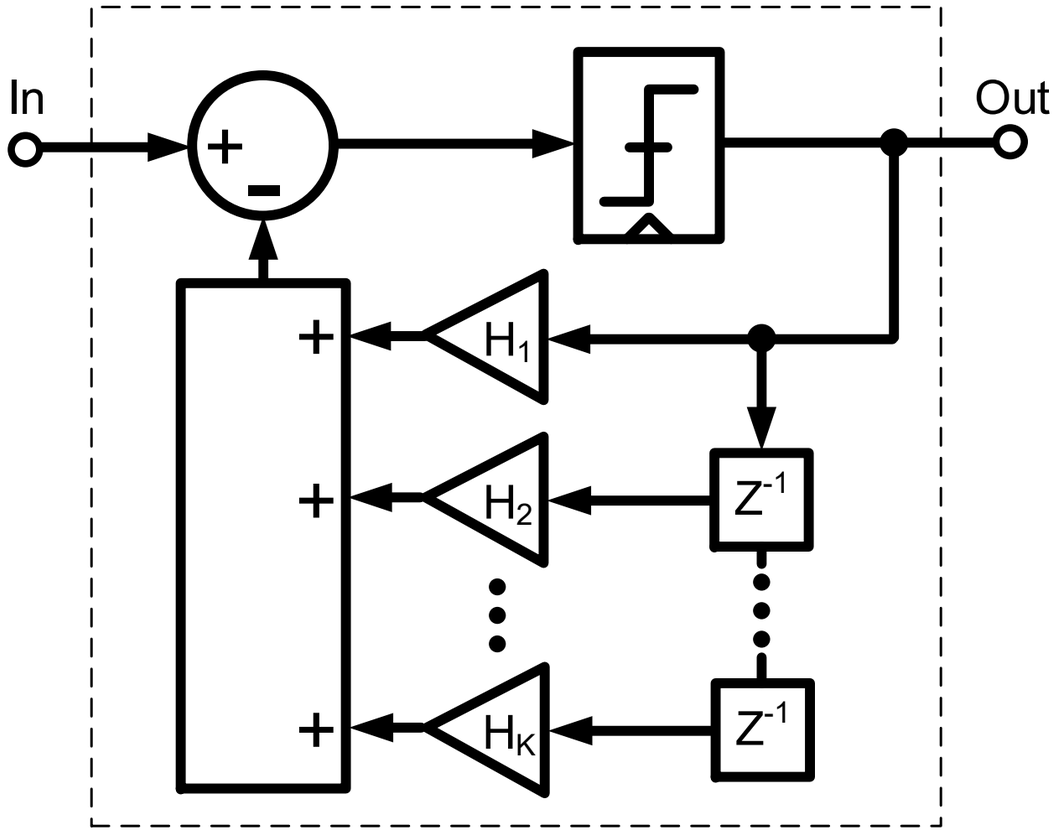
Outline

- Motivation
- Methodology to Characterize and Quantify DFE Performance
- Illustration on Example 1-Tap DFE
- Application to IIR DFE and Comparison with Measurements
- Summary

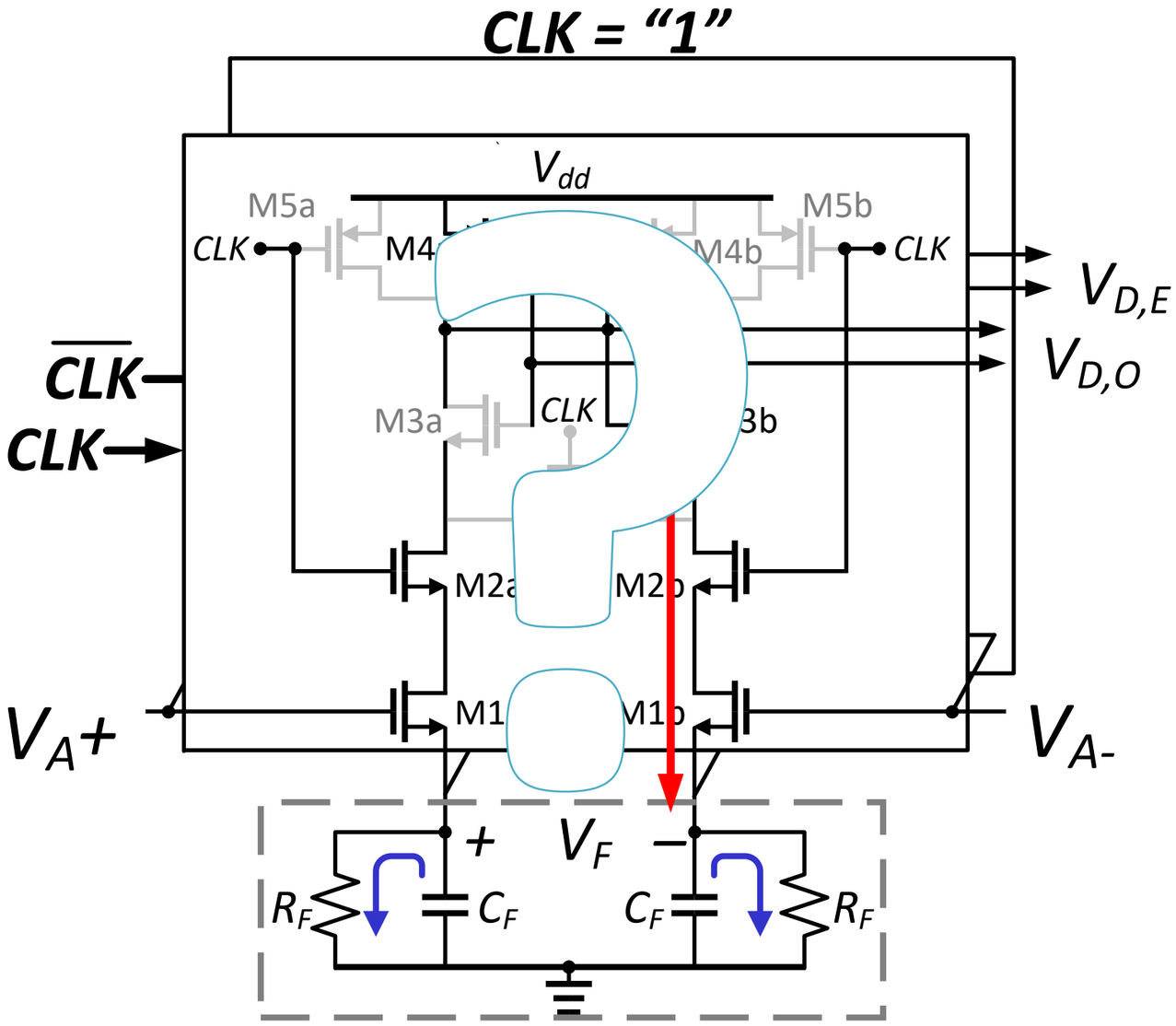
Ideal Model of a DFE

- Tap weights typically assumed to be constant, H_k, independent of:
  - Clock frequency
    - In fact, incomplete settling of the feedback loop may impact the DFE's effect
  - Amplitude at the input to the latch
    - Impacts the delay and hence efficacy of the DFE
  - Each other
    - In fact, increasing one tap weight may impact the effect of another tap weight



Motivation

- Many DFE circuits have unusual responses and timing requirements
  - IIR DFEs (shown on right)
  - Switched capacitor DFEs
  - "Soft" DFEs
- How do we ensure a particular DFE circuit will meet the system specifications?
  - Extensive post layout simulations
    ⇒ costly
  - "By design" (e.g. ratio-based design techniques)
    ⇒ not always possible



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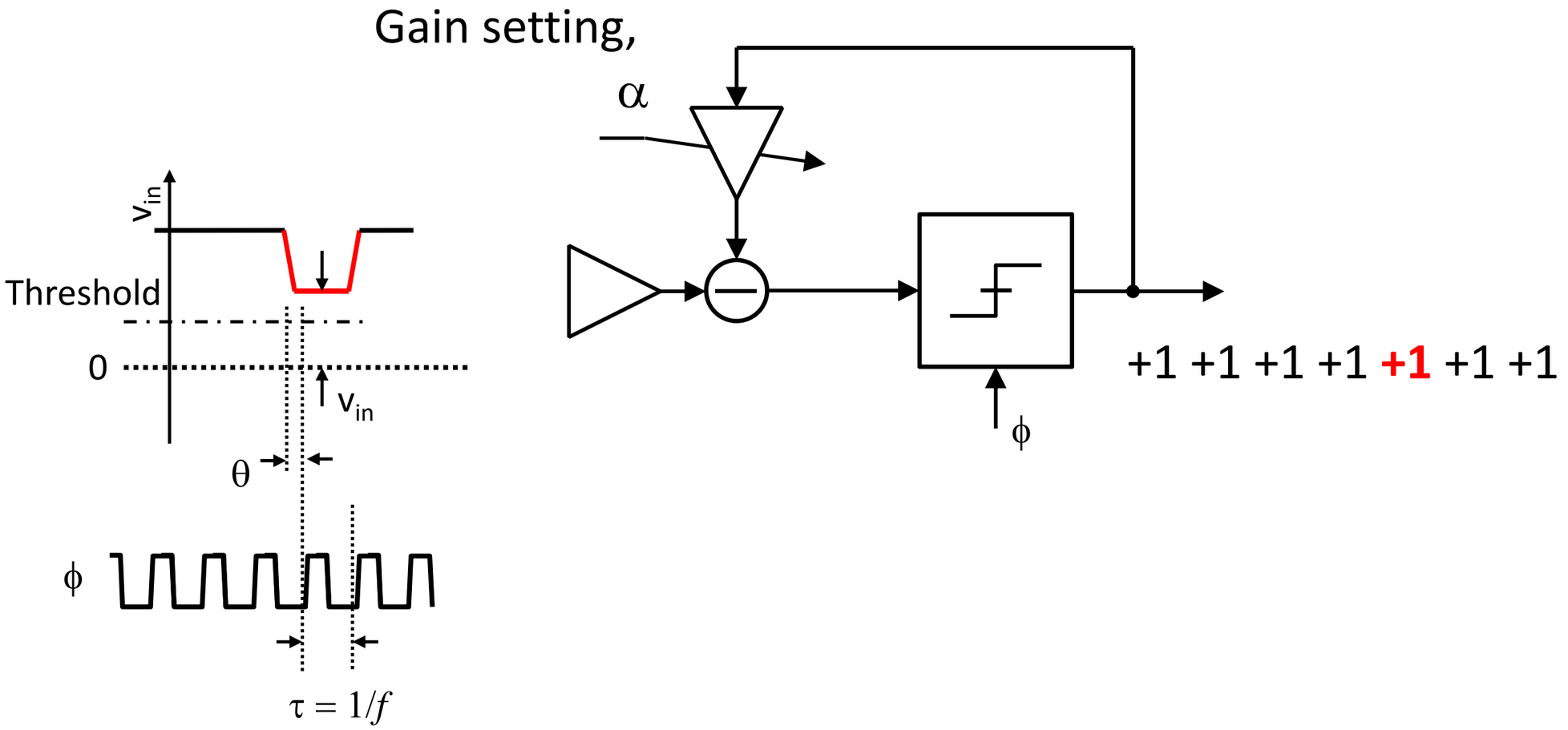
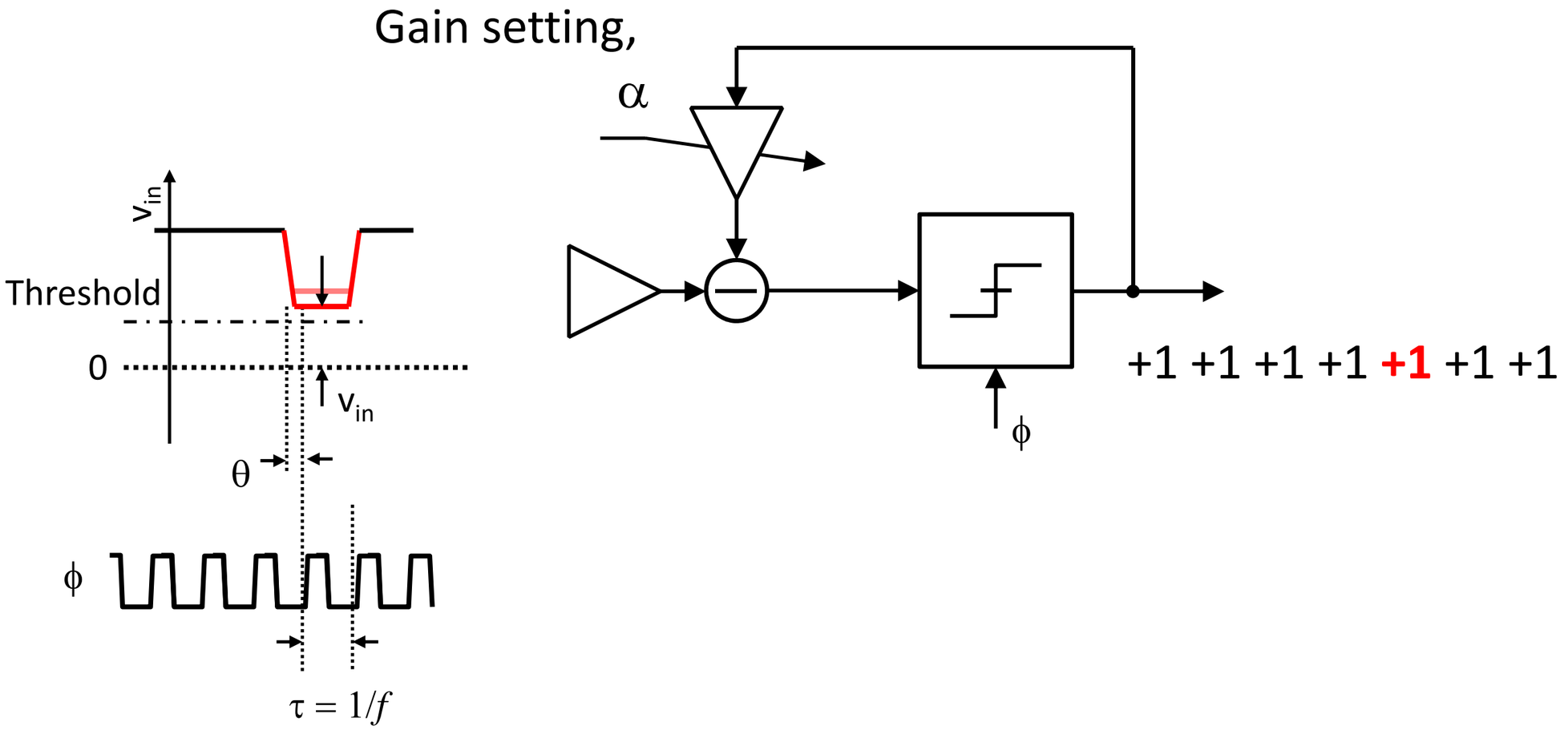
Method to Quantify DFE Tap Weight

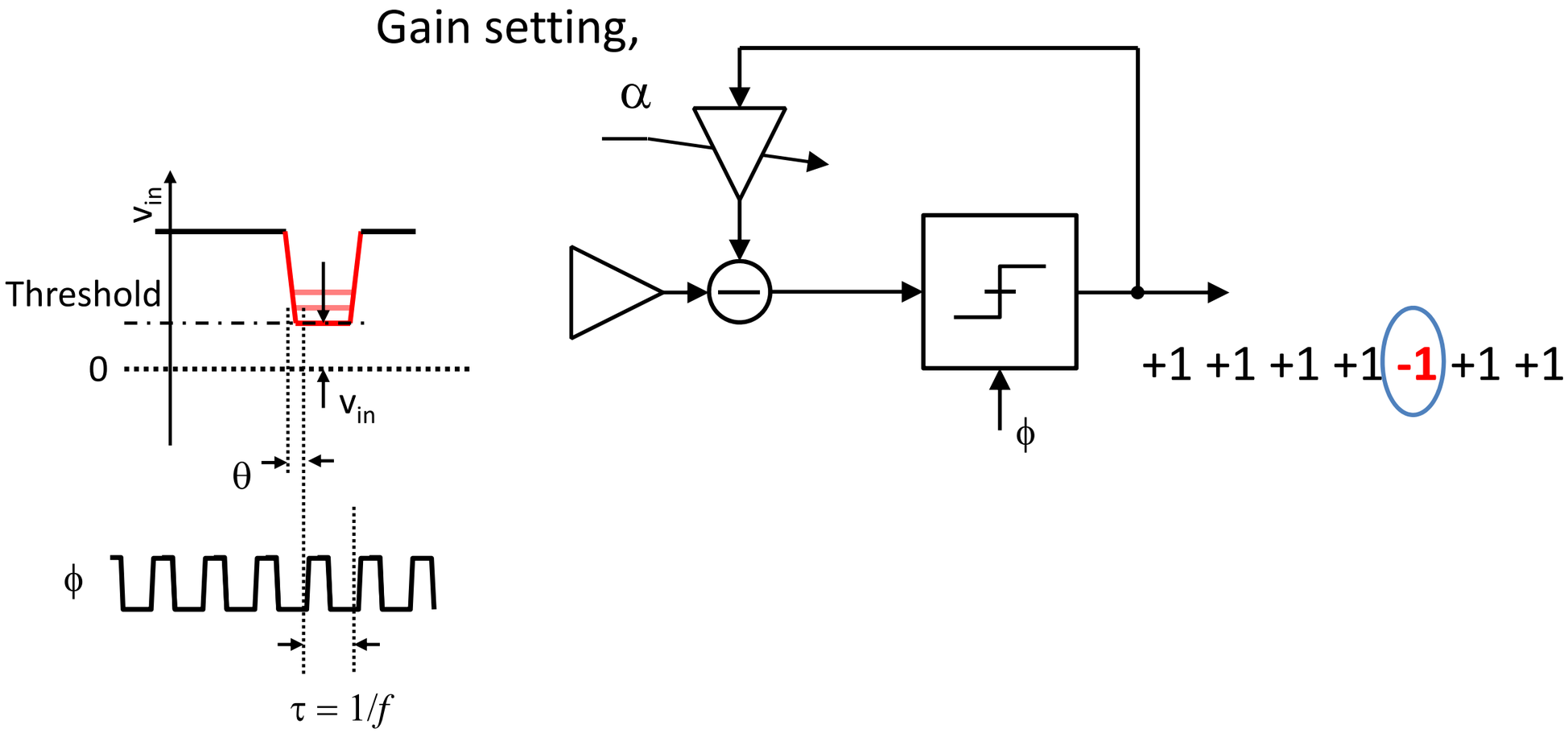
⇒ Example: 1-Tap DFE



Method to Quantify DFE Tap Weight

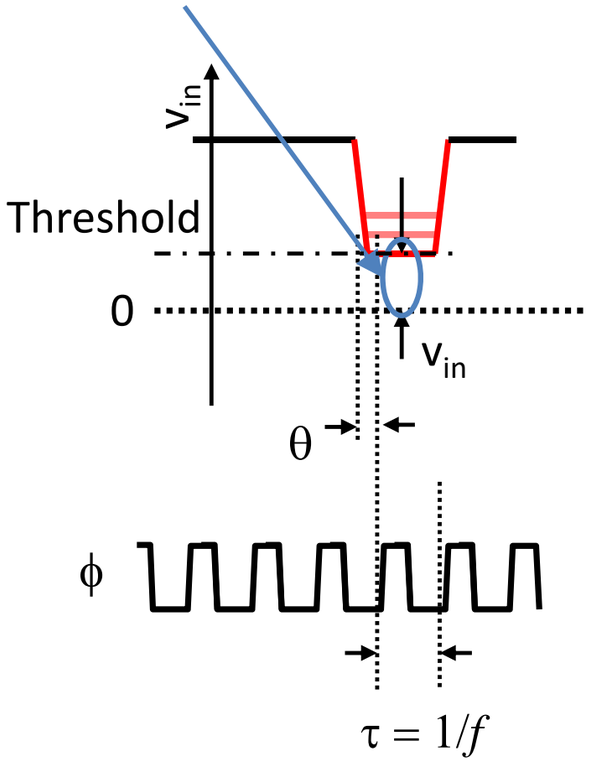


Method to Quantify DFE Tap Weight

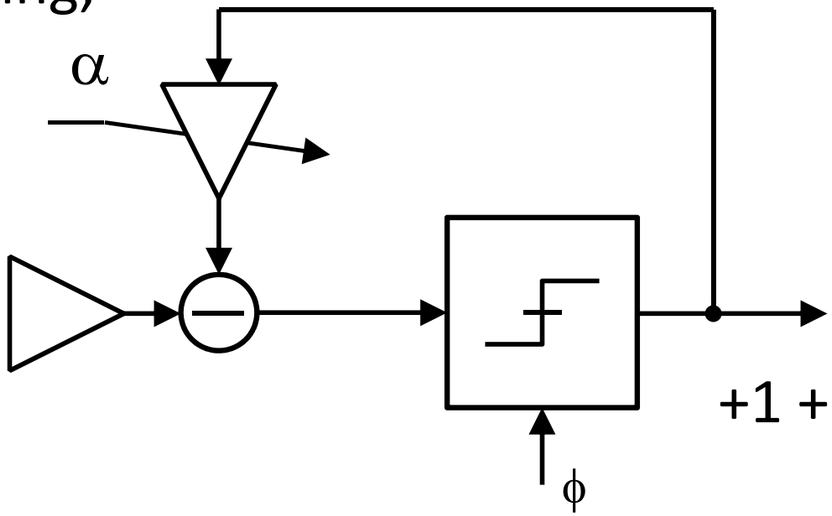


Method to Quantify DFE Tap Weight

Input-referred Effective Tap Weight



Gain setting, α



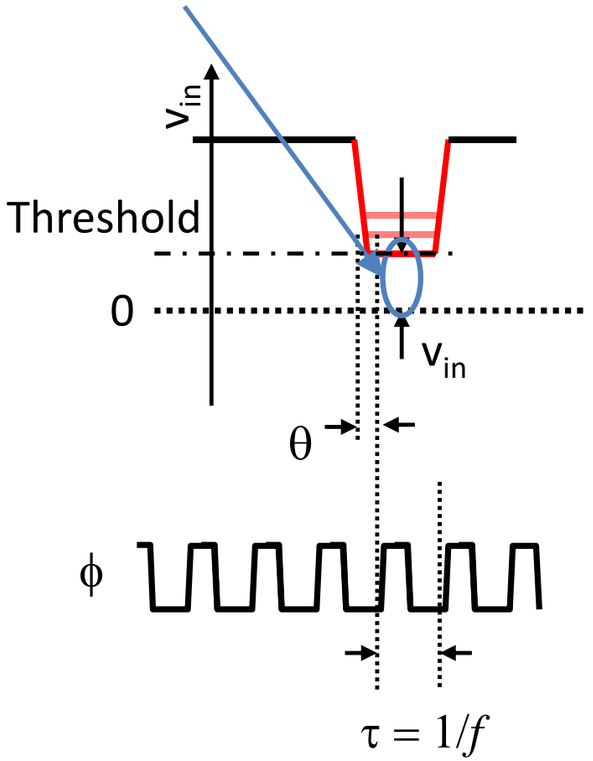
+1 +1 +1 +1 **-1** +1 +1

⇒ **Depends upon α, τ, θ, …**

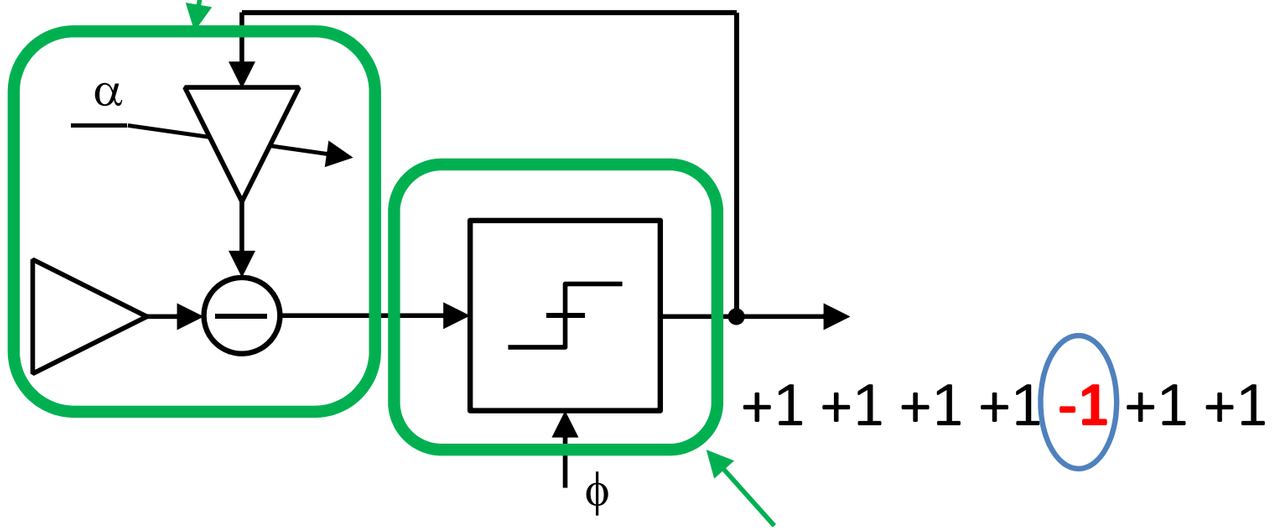
Method to Quantify DFE Tap Weight

- Example simulation in 65-nm CMOS:

Input-referred Effective Tap Weight



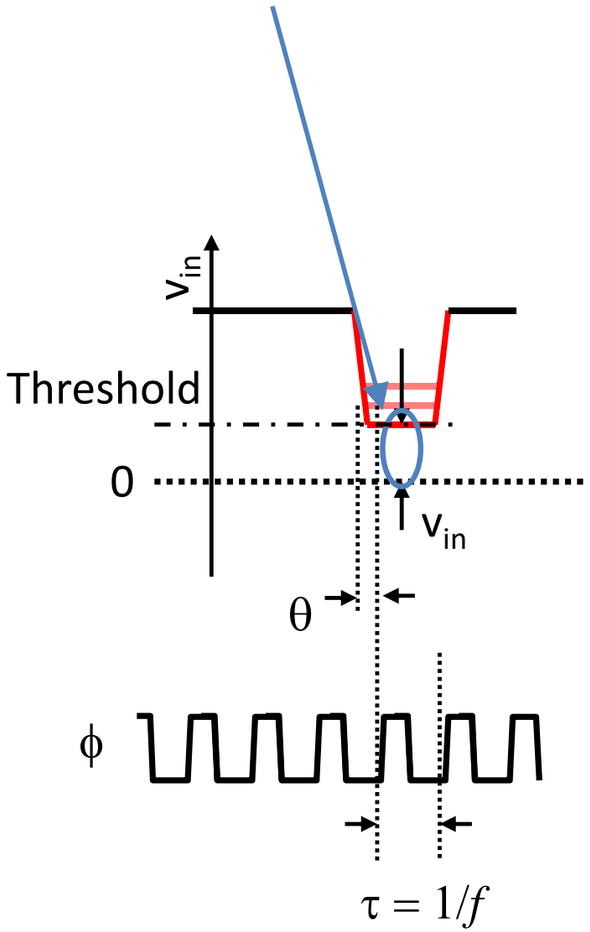
Differential pairs with current-mode summation

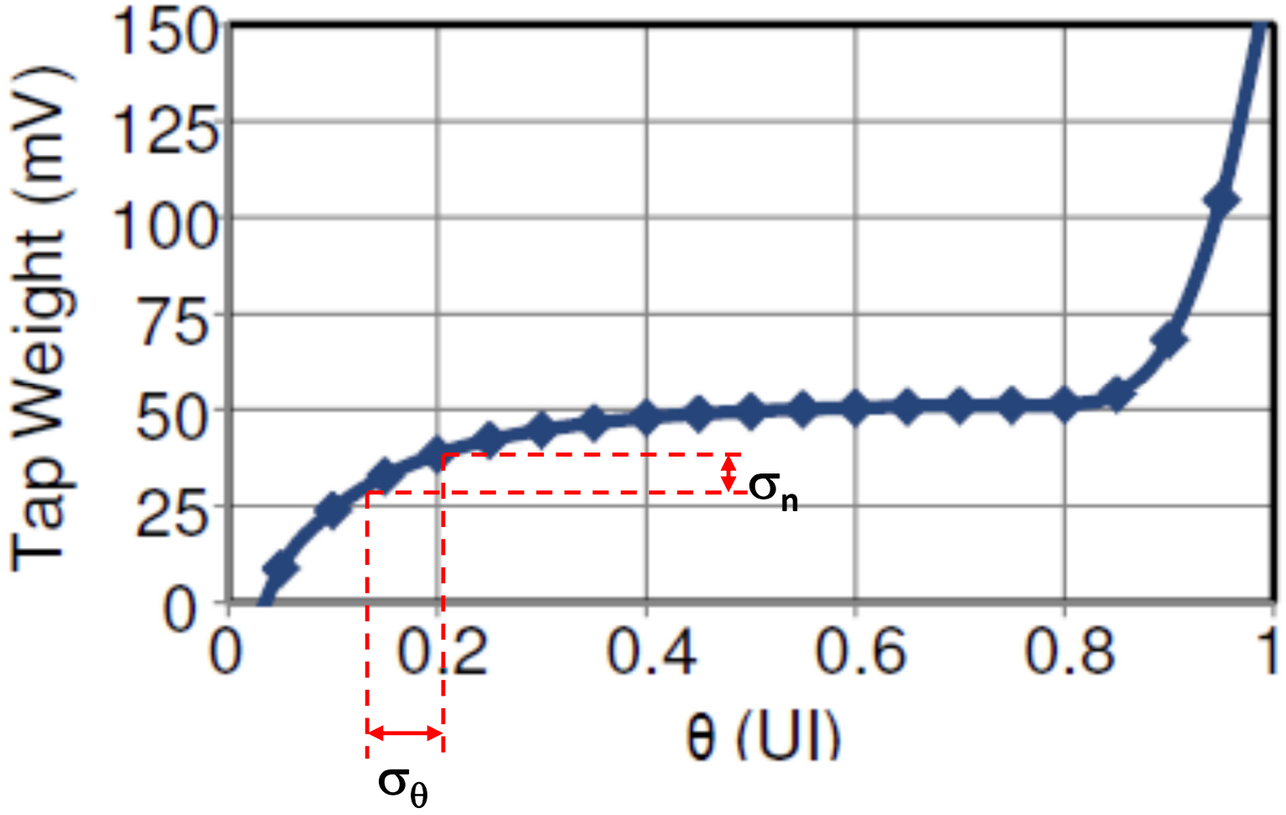


Double-Tail Latch [6] + RS Latch

Example: DFE Tap Weight vs. Clock Phase

- At 10 Gbps: effective tap weight is 50 mV

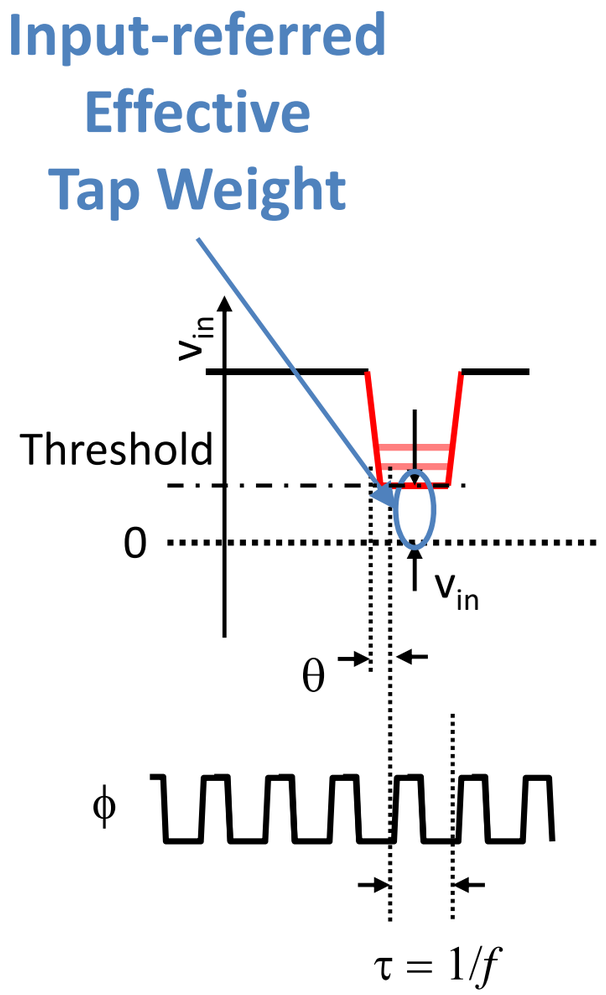


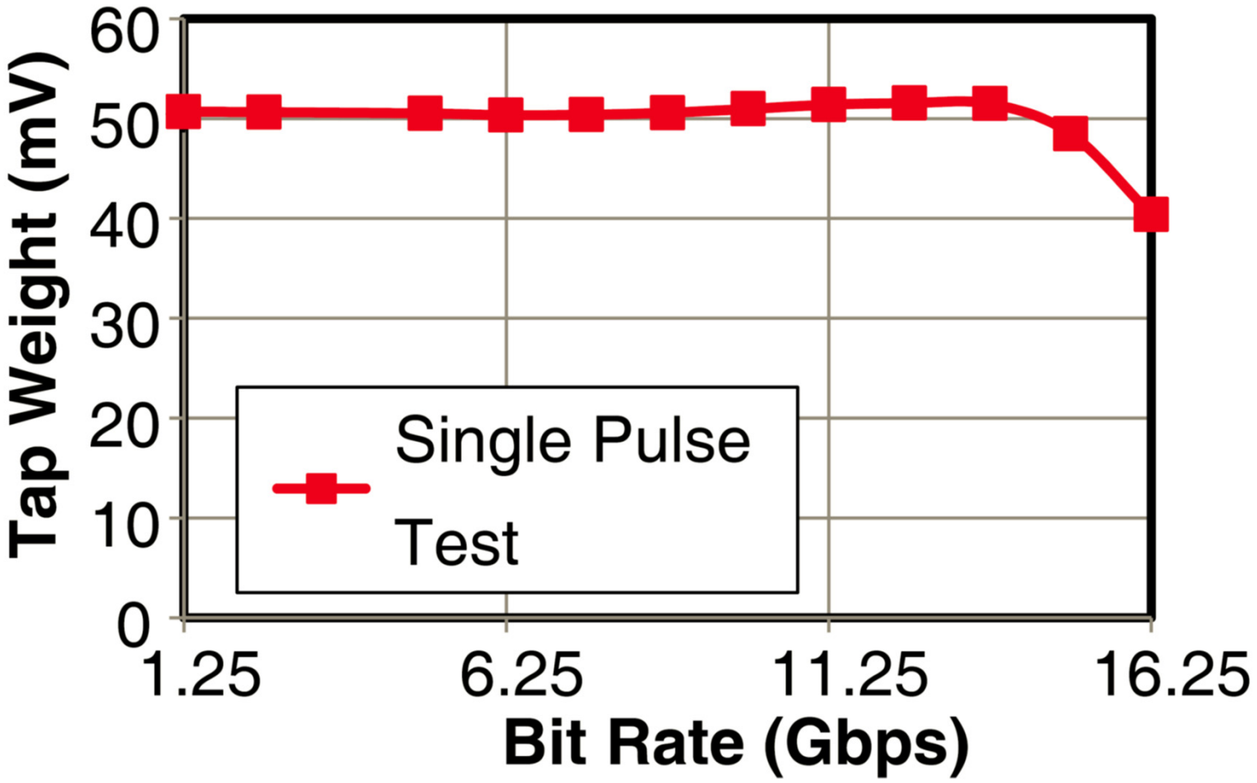


➢ **Jitter can turn into noise due to variations of the effective tap weight with sampling phase**

Maximum DFE Operating Frequency

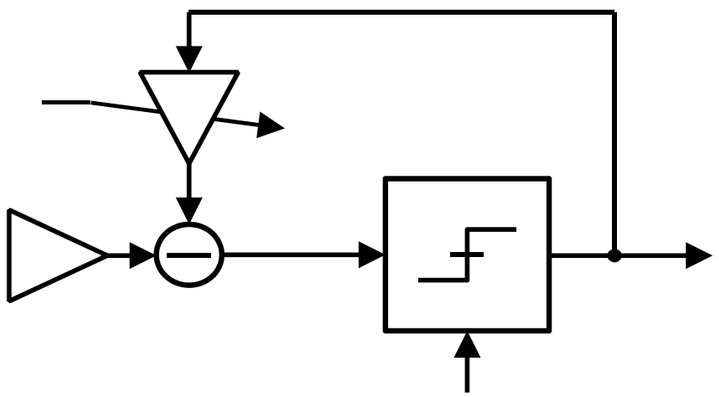
- Versus frequency, $f = 1/\tau$

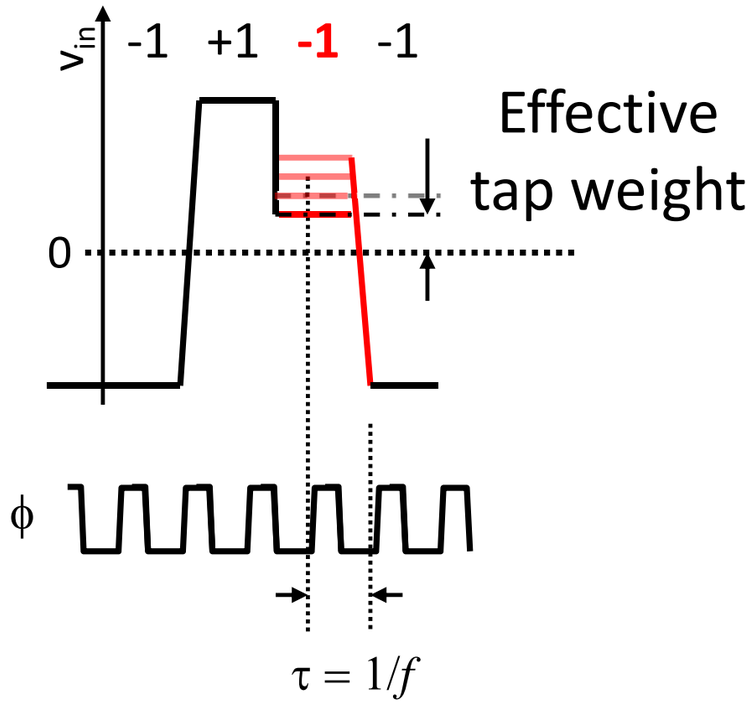


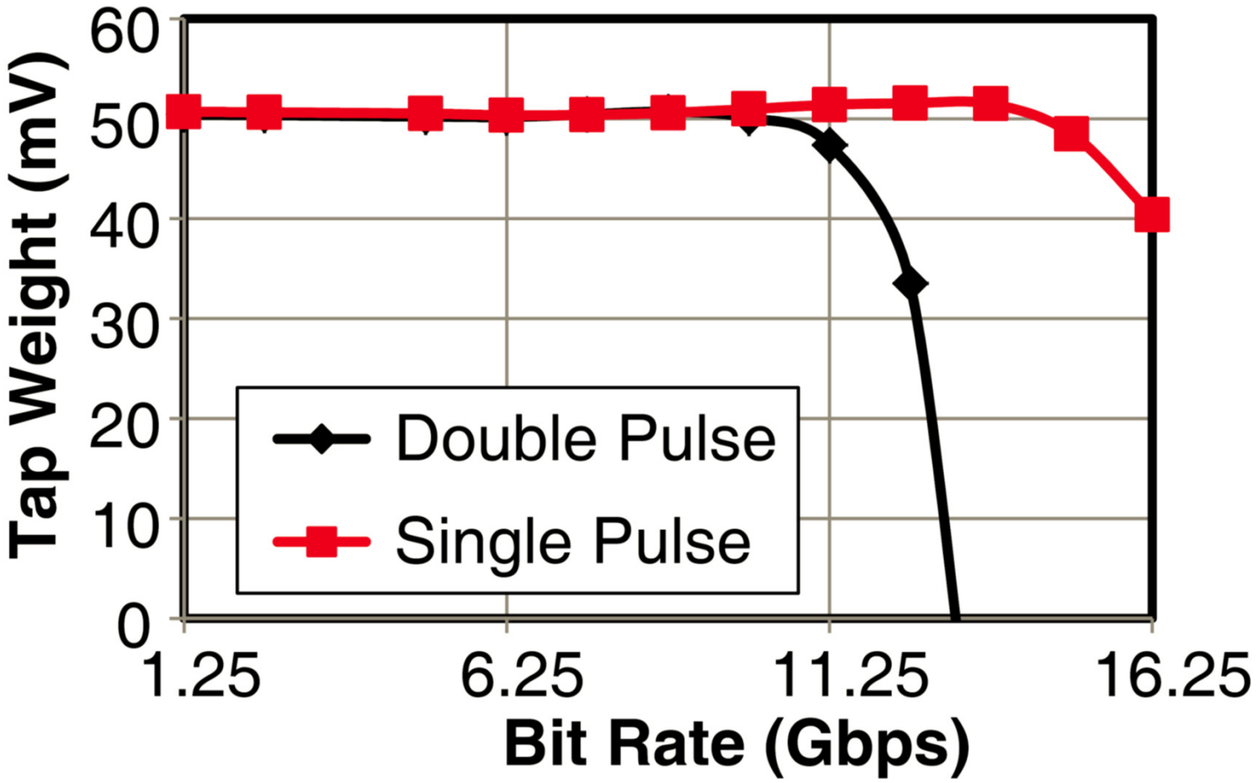


- Beyond some data rate, there is insufficient setup- and hold-time for the latch so a more-negative pulse is required to trip the latch
- However, this does not exercise the feedback loop critical path

Maximum DFE Operating Frequency



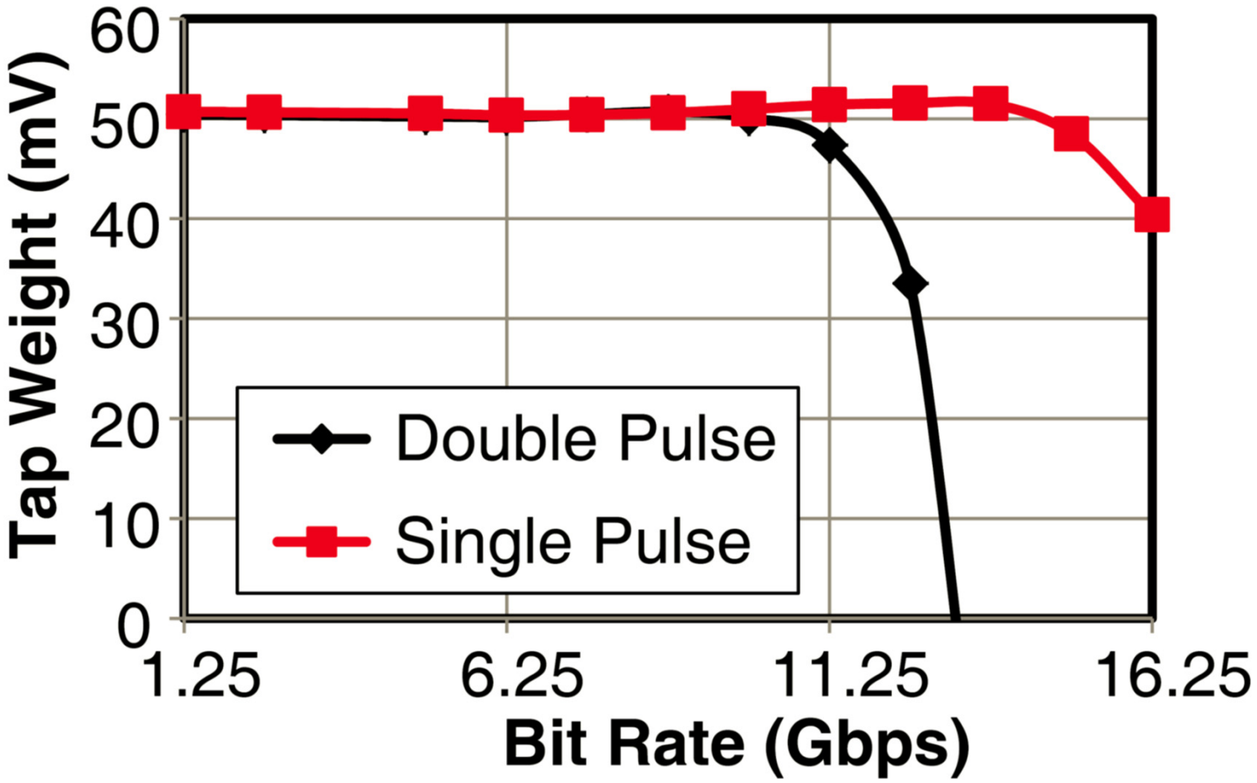


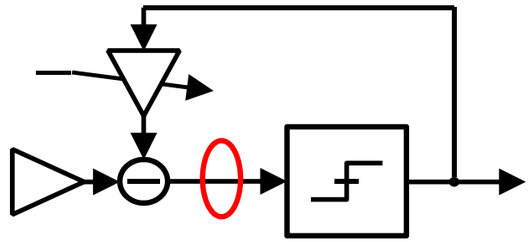


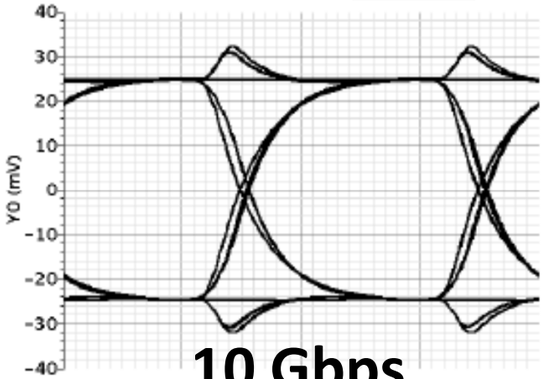
- Providing a lone “+1” bit into the DFE tests the feedback loop critical path settling
- ➢ Effective tap weight above 11Gbps depends upon preceding bits

Maximum DFE Operating Frequency

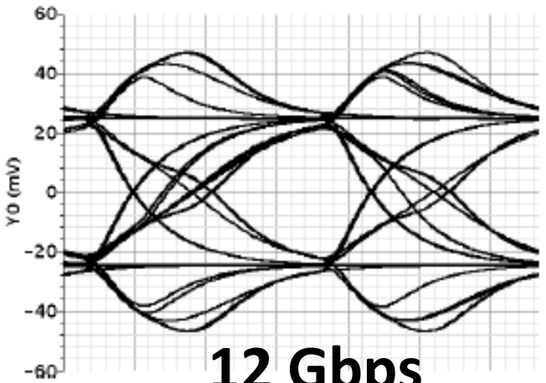
- Transient simulations reveal the problem at the output of the summing node
- Some DFE circuits do not permit direct observation



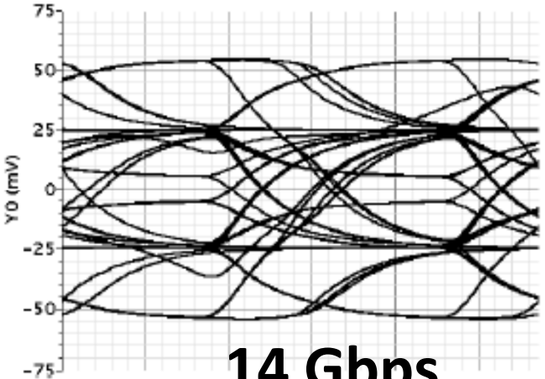




10 Gbps



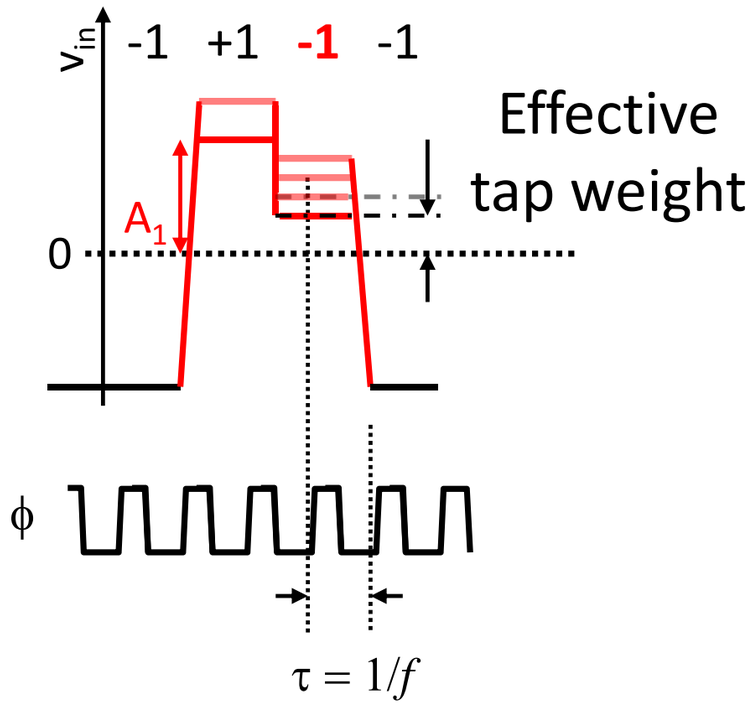
12 Gbps

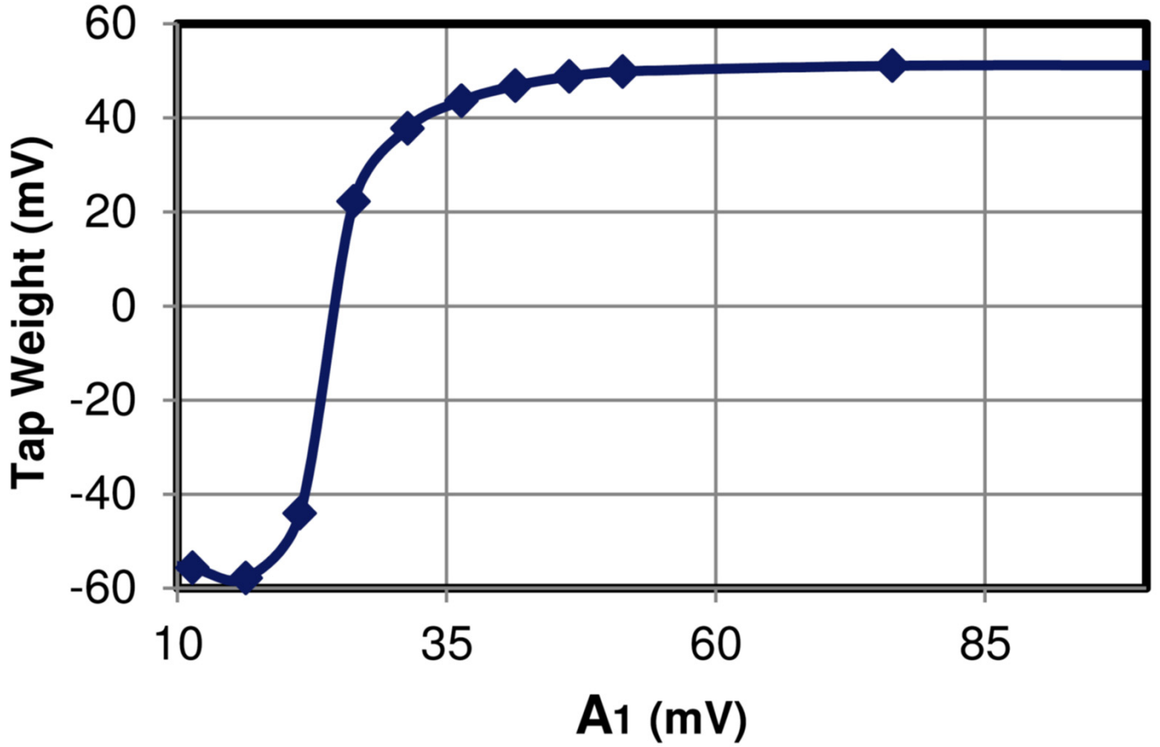


14 Gbps

Sensitivity of the DFE

- Clock-to-Q delay of the DFE depends upon its input amplitude





- e.g. Smaller amplitude A_1
  $\Rightarrow$ slower clock-to-Q delay
  $\Rightarrow$ incomplete settling of DFE feedback path
  $\Rightarrow$ lower effective DFE tap weight
- Hence, this one-tap DFE provides 50 mV effective tap weight as long as the input is at least 50 mV at 11Gbps or lower

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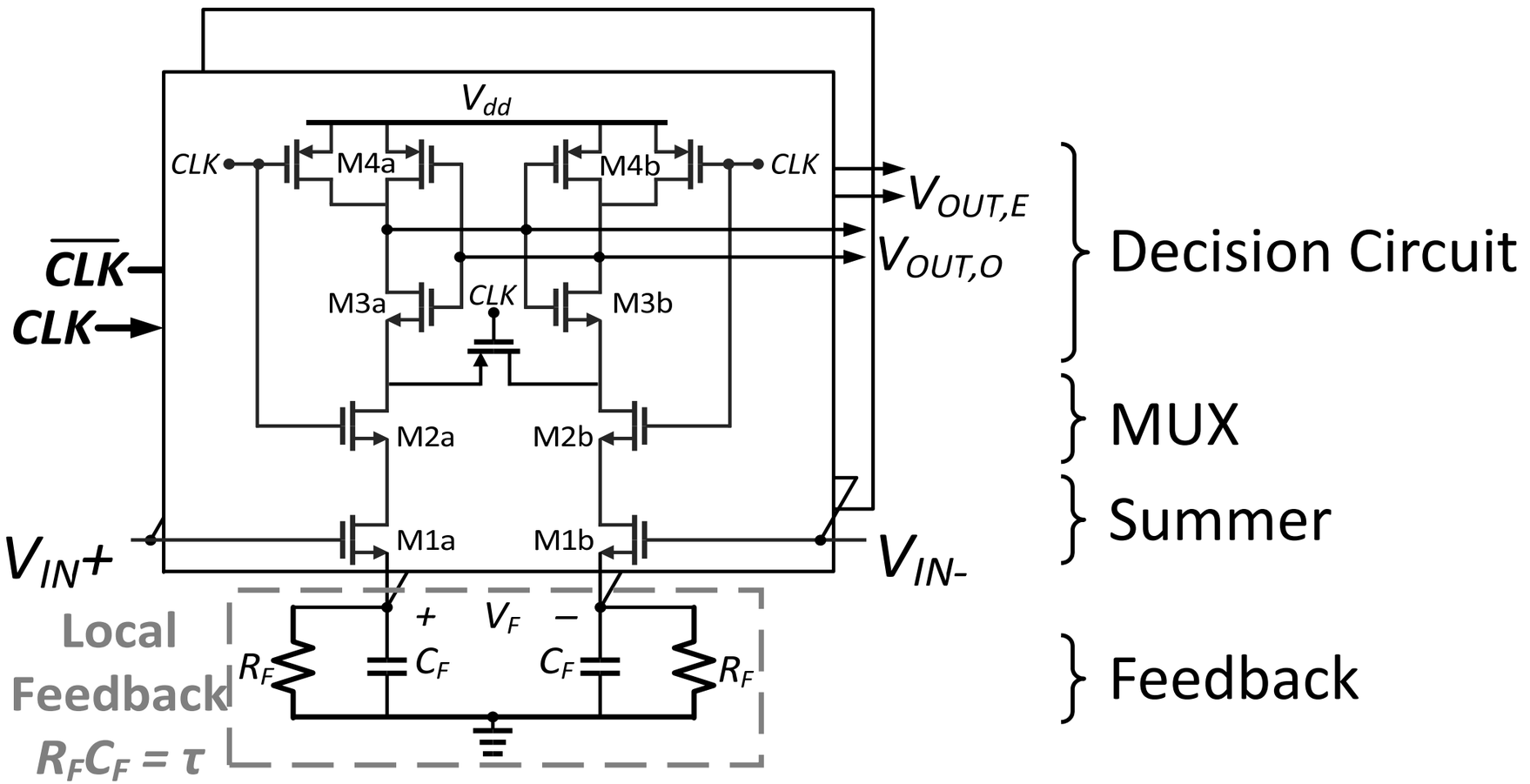
IIR DFE with Local Feedback [5]

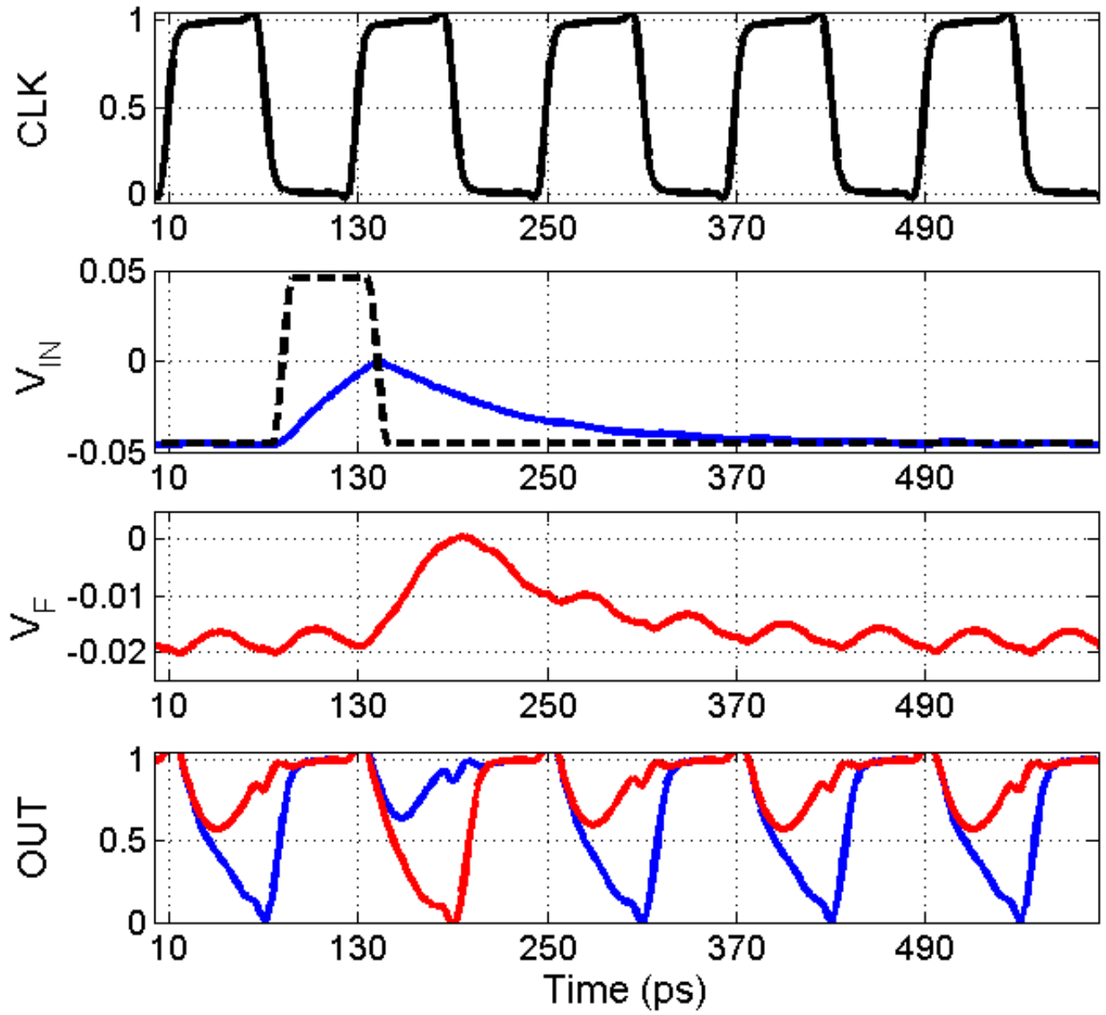
- IIR DFEs can provide many taps of equalization without multiple parallel feedback paths

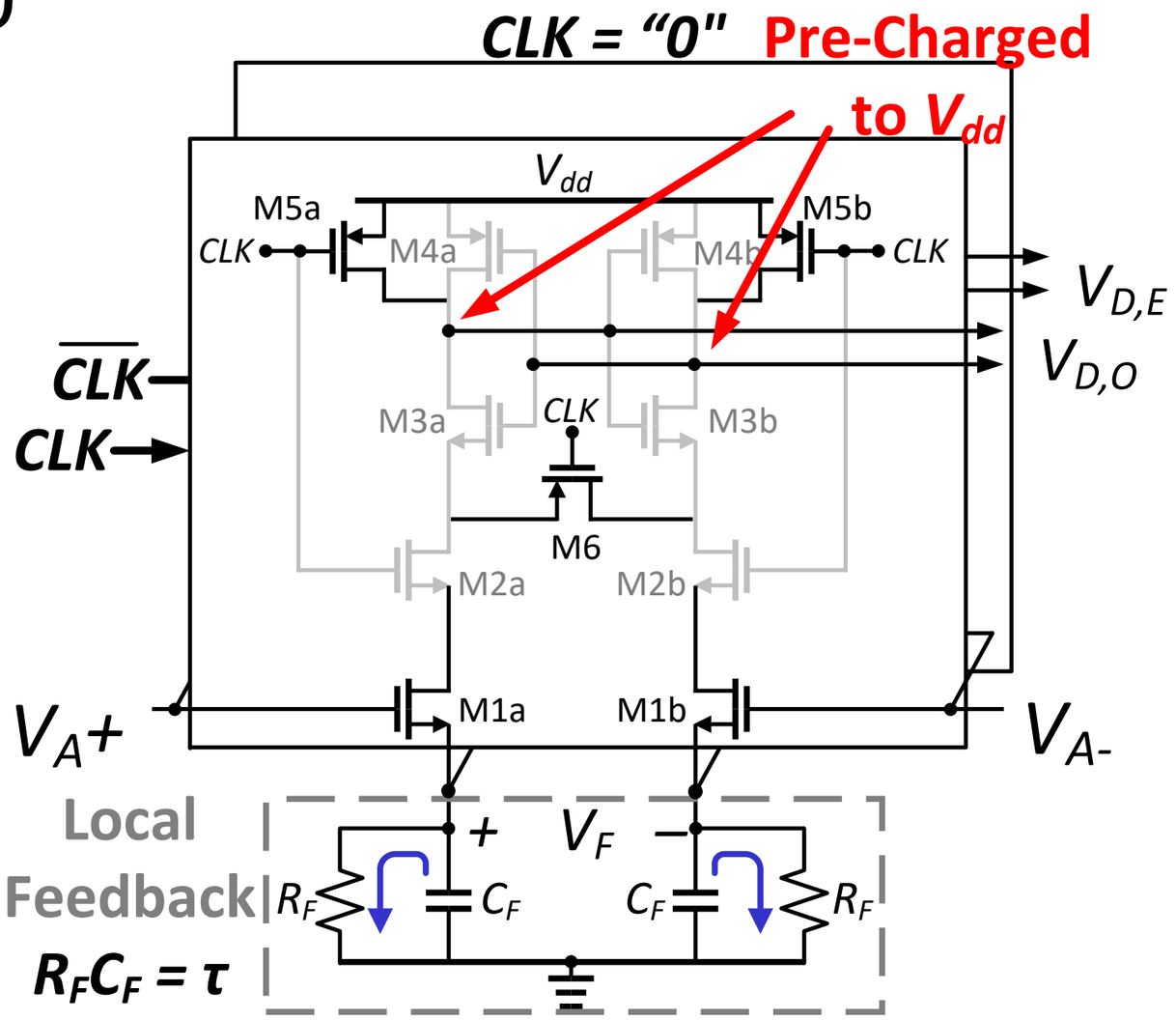


➢ This example incorporated into an optical receiver consuming only 0.7pJ/bit at 20Gb/ps

IIR DFE with Local Feedback [5]

- Example: input = 00..0100..0





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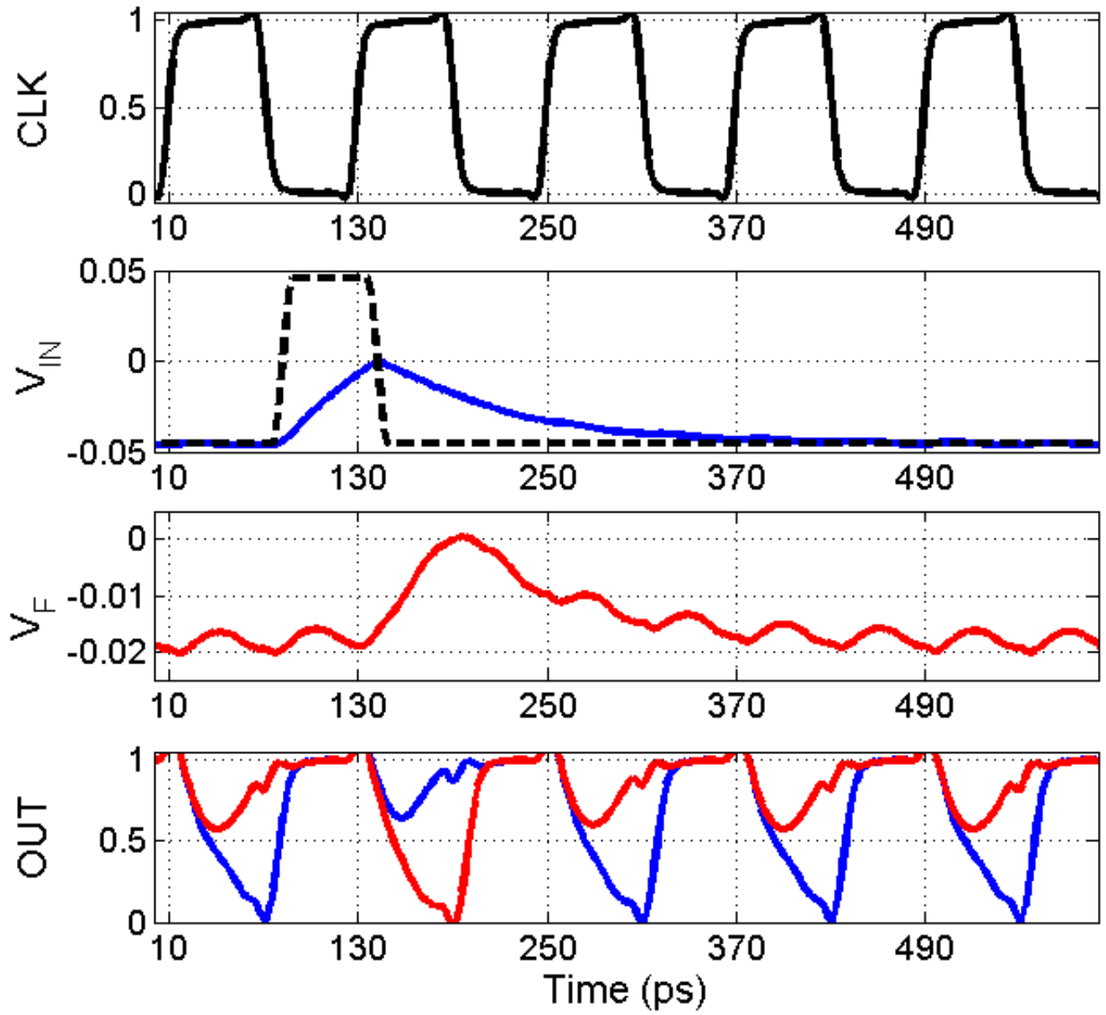
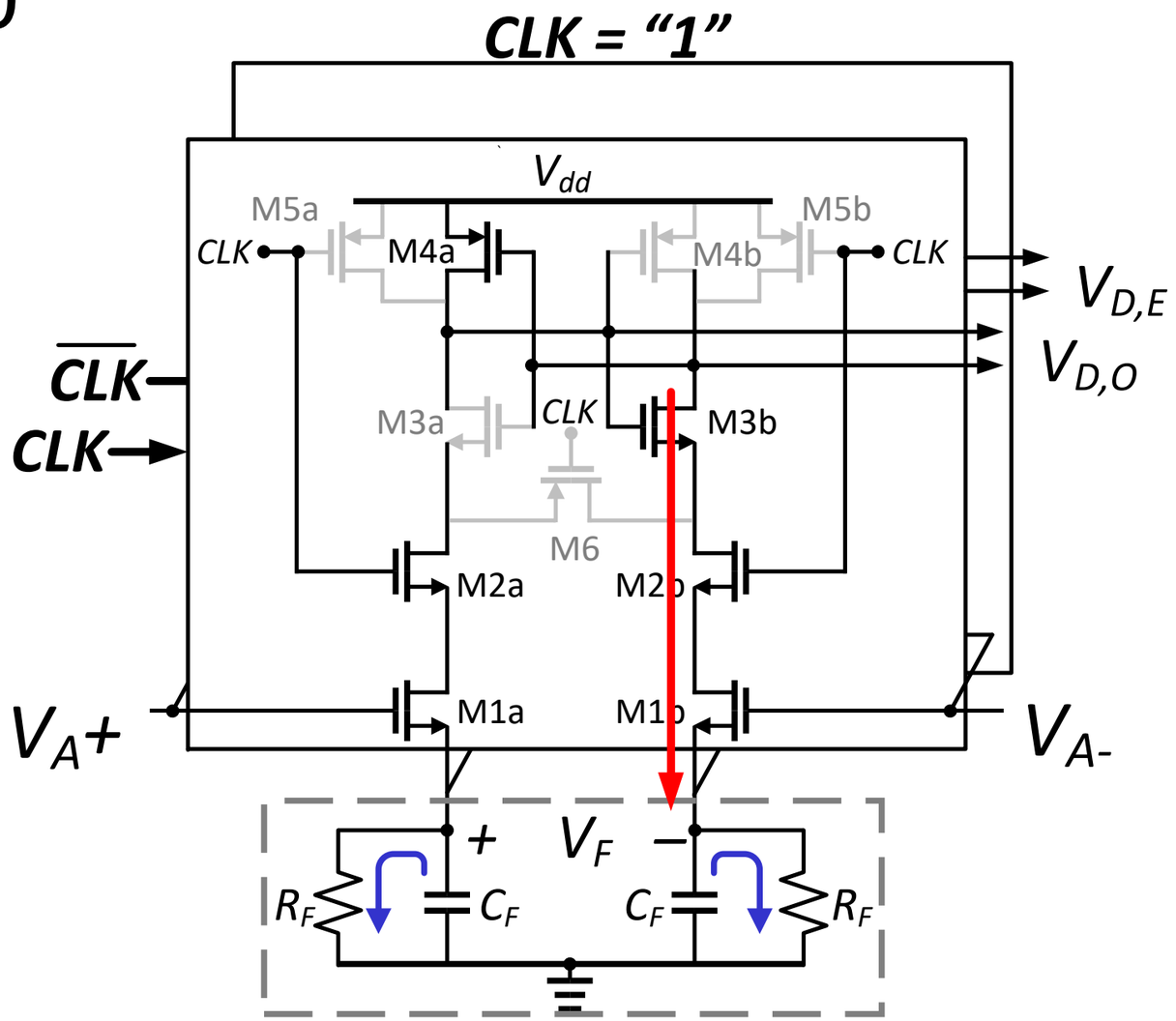
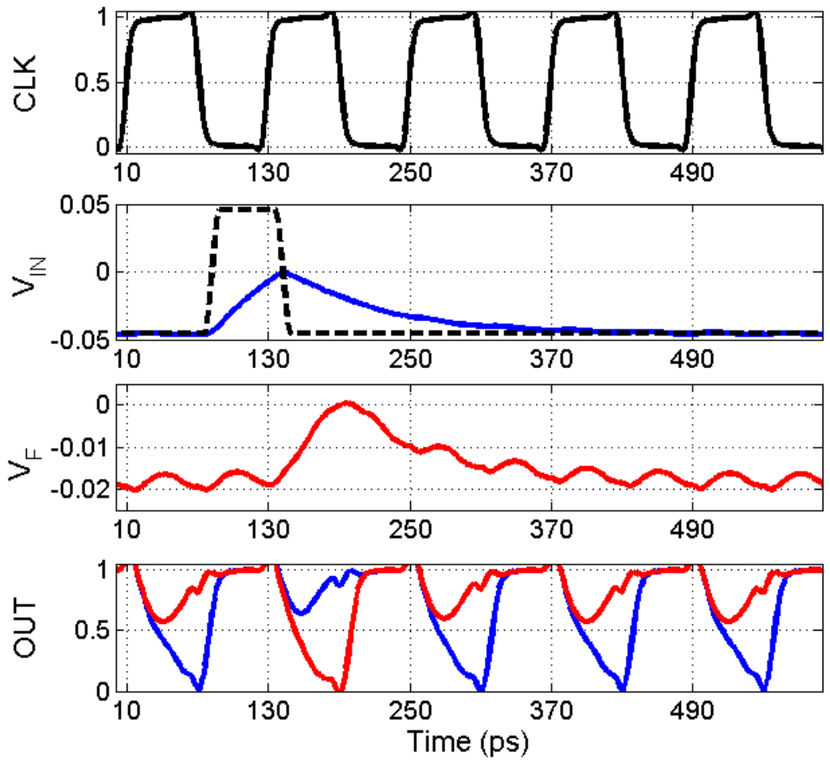
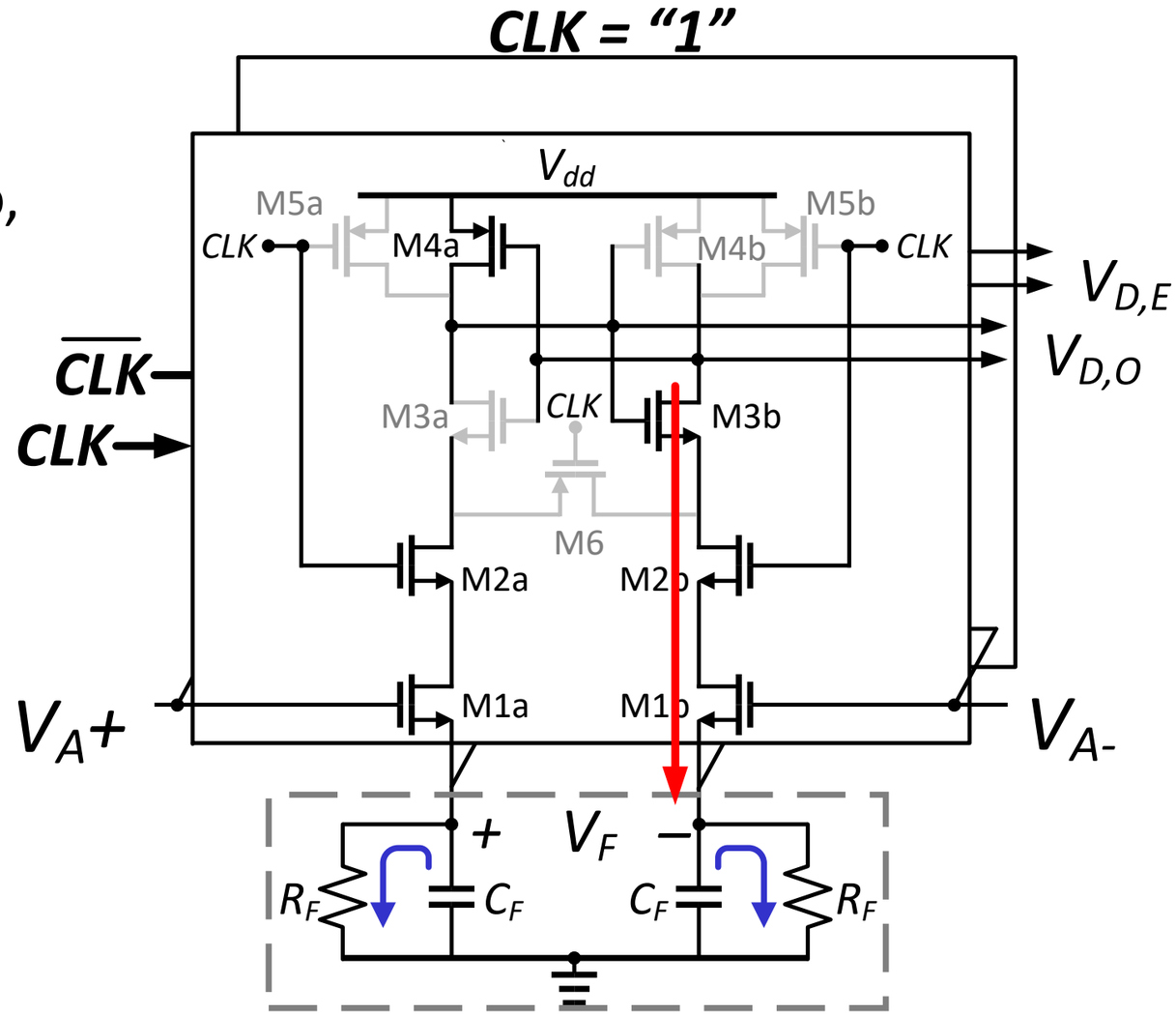




IIR DFE with Local Feedback [5]

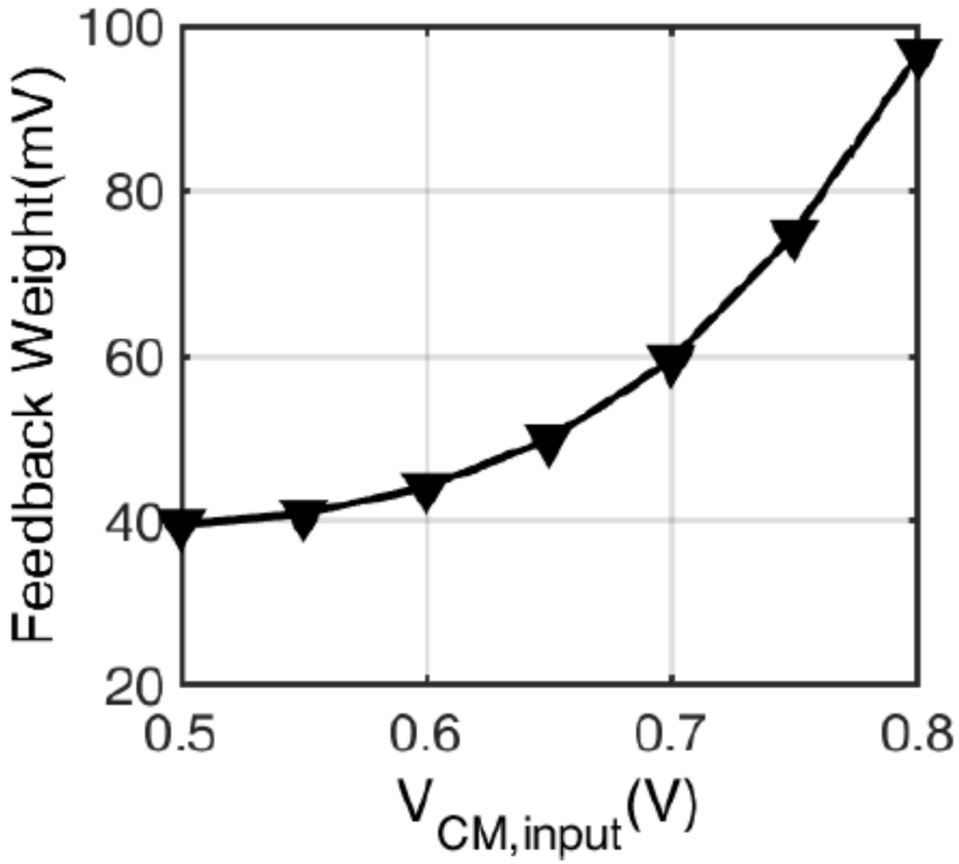
- Wish to characterize this DFE over PVT, for different settings of R_F, C_F, different input common-mode, etc…
- "Tap weight" is not determined by a ratio, and is not directly observable

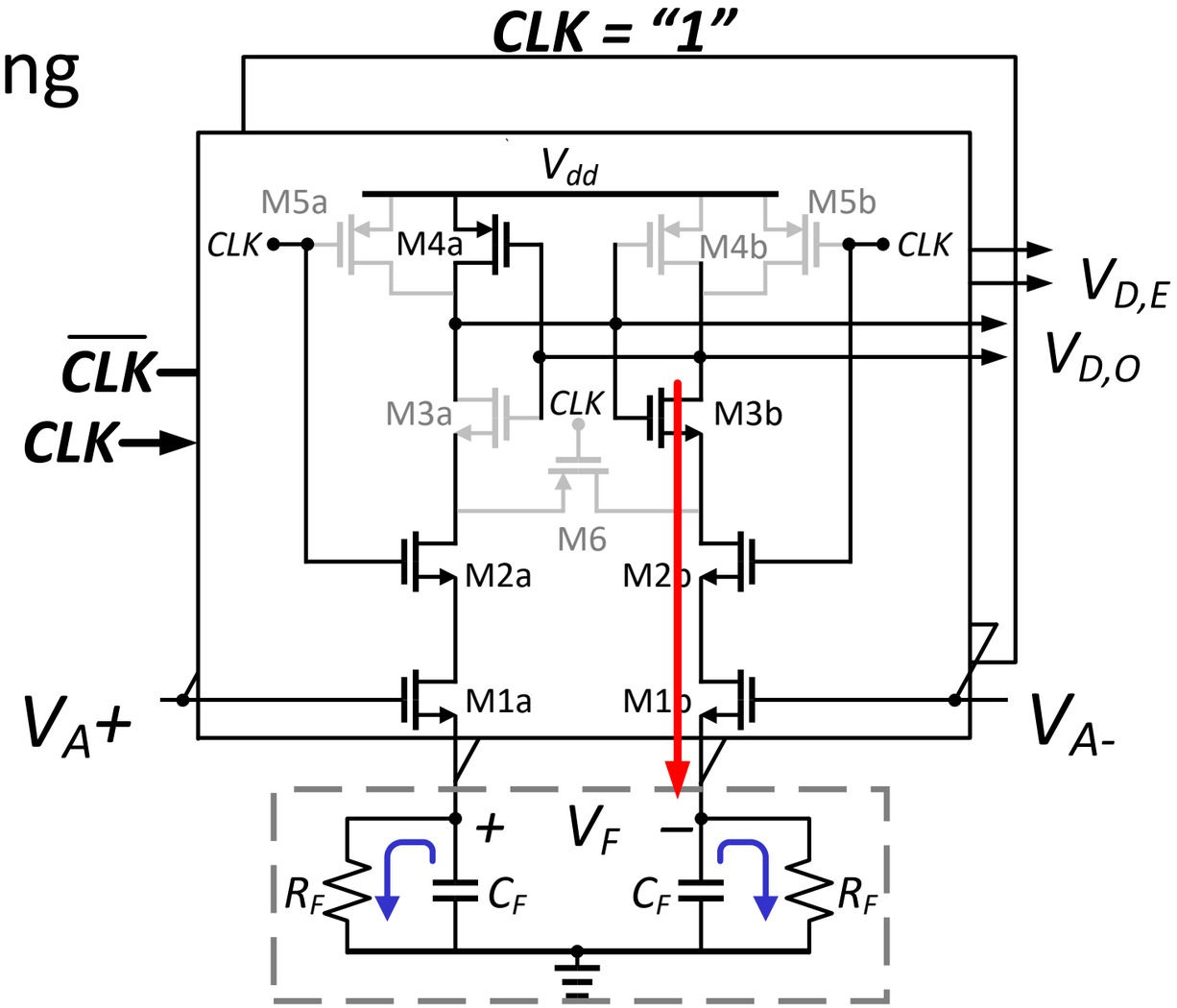




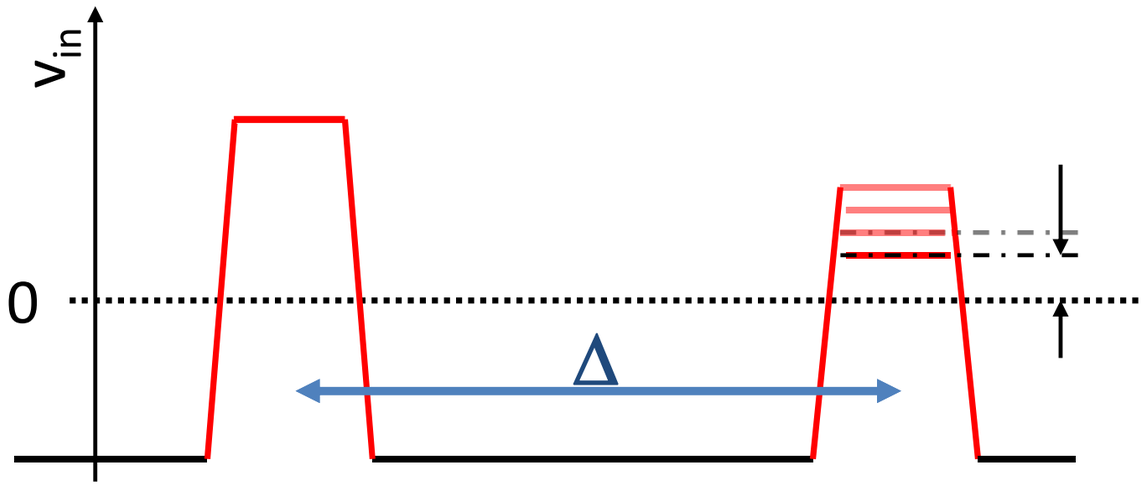
IIR DFE Characterization

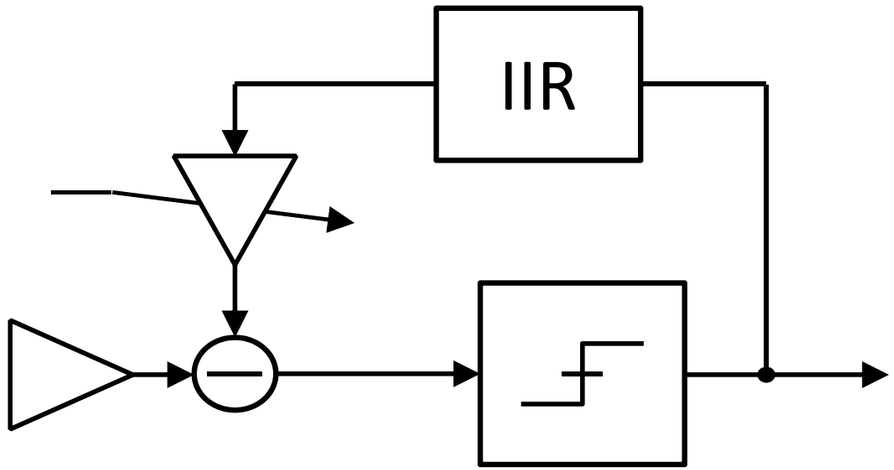
- Single-pulse test used to find effective tap weight while varying input common-mode





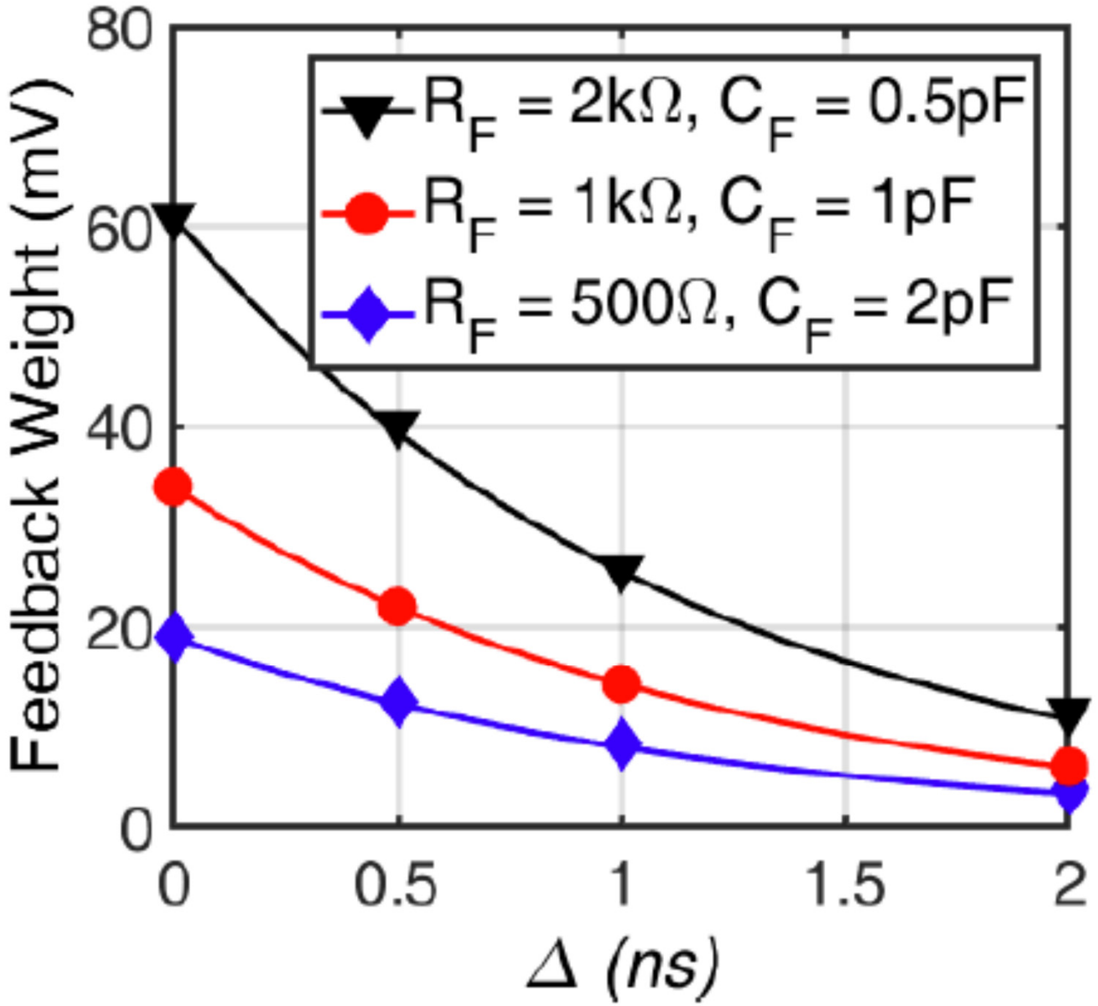
Finding the IIR DFE Response

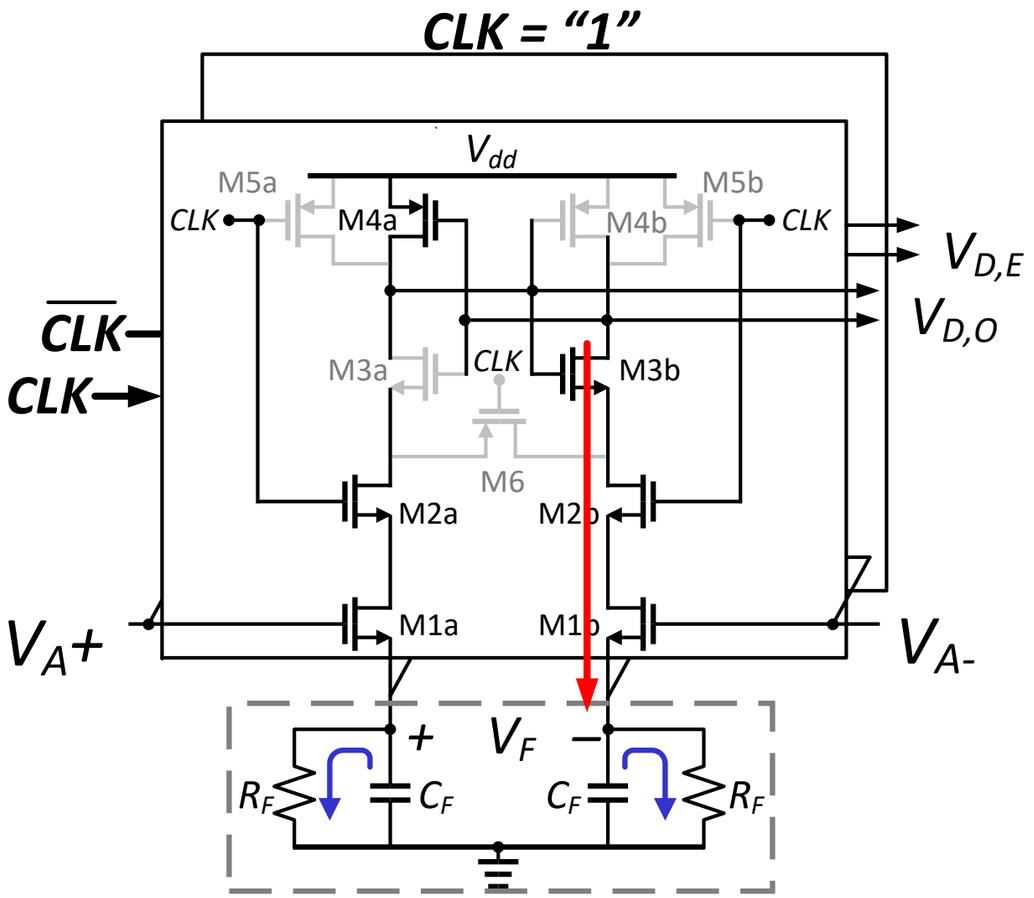




- Performing double-pulse test while varying the delay, D, allows one to observe how the effect of the first pulse upon the DFE threshold decays over time
- Can also be applied to discrete-time multi-tap DFE

Finding the IIR DFE Response

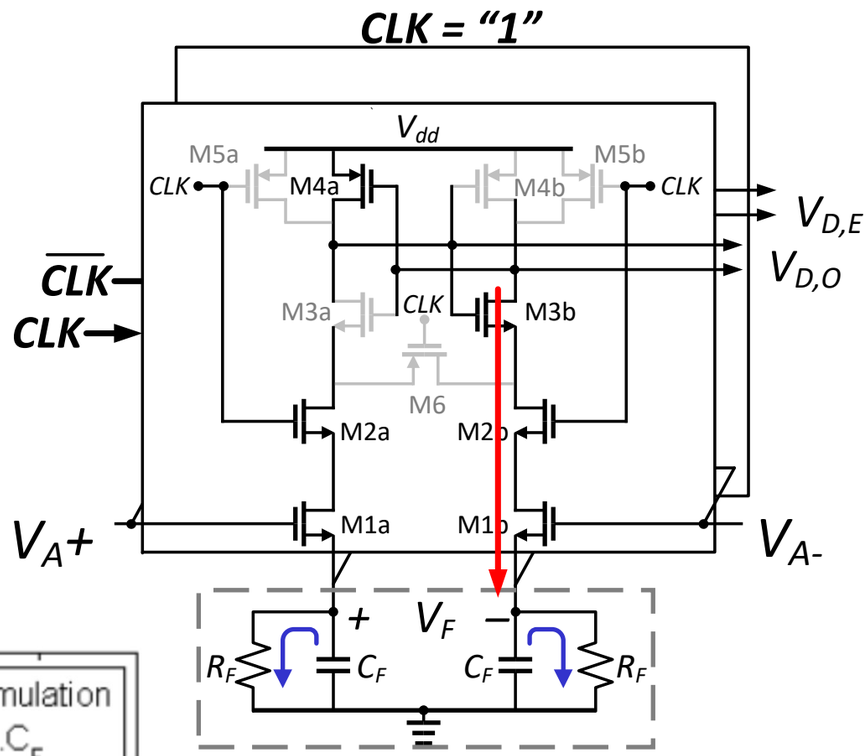


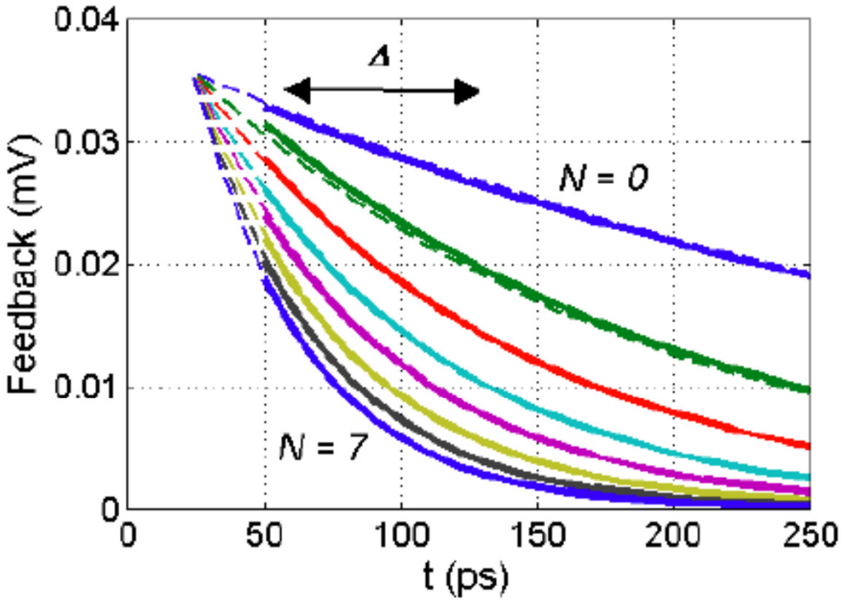


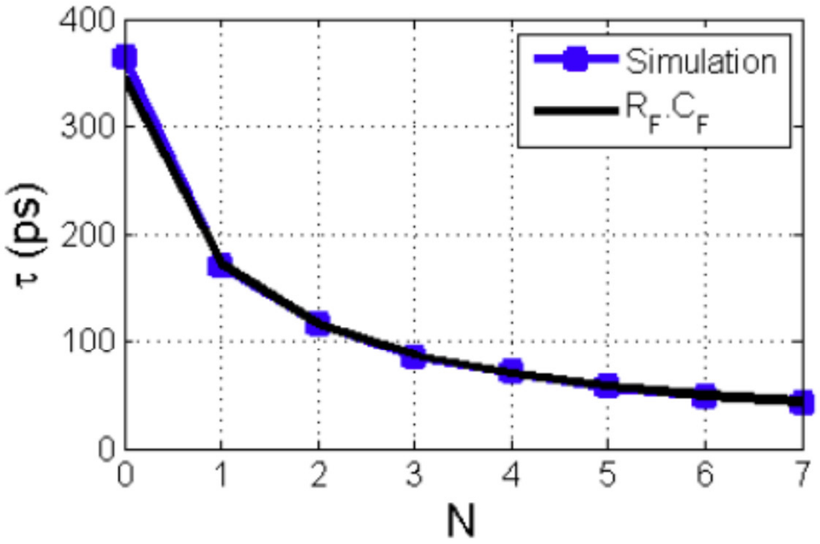
- Results shown for different combinations of R_F and C_F

IIR DFE Characterization

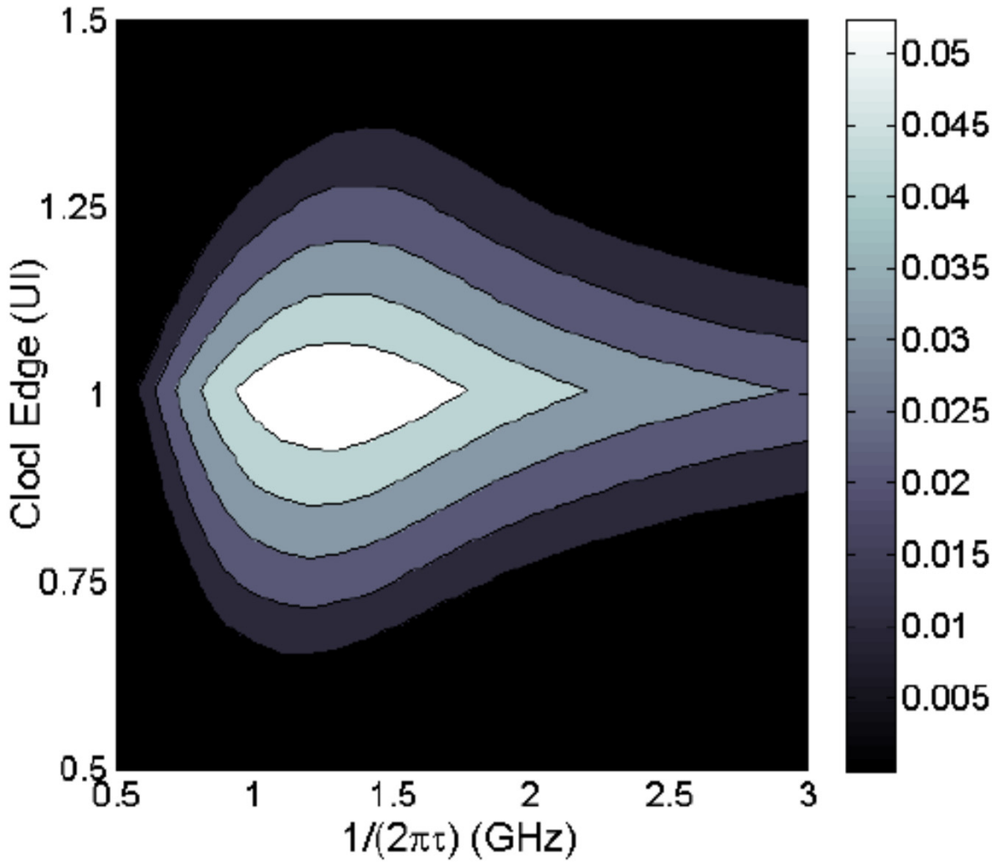
- Resistor R_F implemented with 8 settings, N = 0, 1, … 7
- Post-layout characterization results (bottom left) are fit to single time constant responses (dashed) with time constants τ
- These agree well with the products $R_F C_F$ (bottom right)

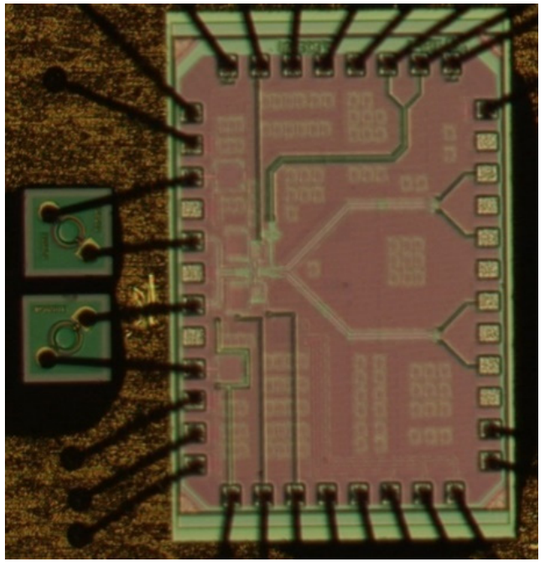


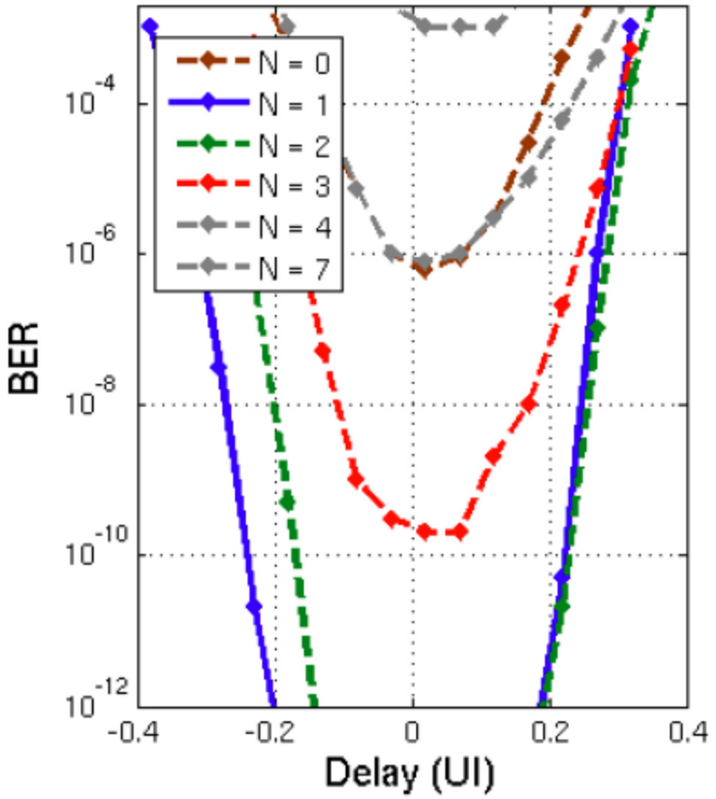




Comparison with System Simulations







- First, a system simulation model is used to predict the best values of τ to find the best

➢ $1/(2\pi\tau) = 1.2$ GHz $\Rightarrow \tau = 132$ ps $\Rightarrow$ between N = 1 and N = 2

➢ Measurement results agree: best results at N = 1, and next-best results at N = 2

Summary

- DFE response is a critically specified part of wireline links
- Verifying a DFE response can be difficult, especially when highly optimized circuit topologies are used
- A methodology to characterize DFEs was presented
  - Relies upon short simulations with contrived input waveforms to extract the DFE's effective response in situ
  - Can capture all nonidealities of a post-layout circuit
- Methodology was validated on a 65nm CMOS prototype IIR-DFE [5]