# Integrated Photodiode Characterization in a SiGe BiCMOS Process

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**Abstract:** Three photodetector structures were simulated, fabricated and characterized at 850nm in a SiGe BiCMOS process. The measurement and simulation results suggest that with modest equalization, multi-Gb/s communication is achievable without any special device fabrication.
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## 1. Introduction

Fiber-optic long reach communication has traditionally been implemented using multiple discrete components. As short-reach connections gain popularity, integrating the entire receiver on one chip is desirable to lower cost. This approach requires the photodiodes to be fabricated within the same process as the receiver circuitry. One approach is to tailor a (Bi)CMOS fabrication process to provide photodiodes with high performance [1] but this in turn increases the fabrication costs. The problem with using a standard process to fabricate photodiodes is the inherent poor bandwidth and responsivity of the resulting silicon photodetectors.

For efficient design of an optical receiver the transfer function of the photodetectors is required, consequently, there have been efforts to fabricate and characterize photodiodes in a standard CMOS process [2] and full optical receivers utilizing them have also been reported [3]. The difficulty is predicting and simulating the photodiode behavior and designing an equalizer that can properly compensate for the inherent poor frequency response. In this work, several photodiode architectures implementable in a standard process are explored, their performance compared, and modeled allowing one to tailor circuits to compensate for their frequency response.

## 2. Photodiode Structures

In this work, three different photodiode structures have been simulated, fabricated, measured and characterized in terms of their bandwidth and responsivity using 850nm wavelength light. The structures chosen can all be implemented in a SiGe BiCMOS process and require no additional manufacturing steps.

The photodetector output current comprises a drift and a diffusion current. The drift current results from the carriers generated in the depletion region of the detector and are swept out by the electric field in the region. The second component consists of the minority carriers which are generated on either side of the depletion region and then pass through the device via diffusion. Although these diffusion currents increase the DC responsivity of the detector, their slow transports increase the inter-symbol interference (ISI) in the detectors and reduce their bandwidths. Figure 1a shows the cross section of a simple n-well/p-substrate diode which can also be fabricated in a standard CMOS process. The low doping levels of the substrate and the n-well result in a relatively wide depletion region. Therefore, a relatively larger drift current is expected in this detector. However, still most of the light is absorbed in the silicon bulk which results in an even larger slow diffusion current and consequently low bandwidth.

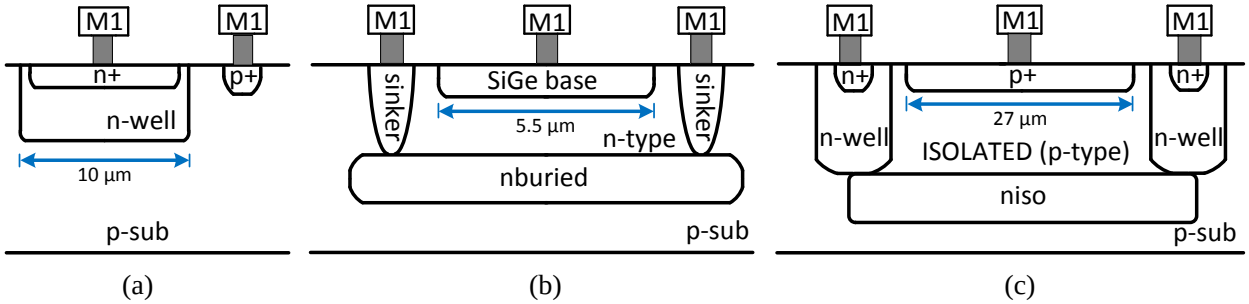



Figure 1 – a) n-well/psub photodiode b) p/nburied photodiode c) p/niso photodiode (thicknesses in the photodiode cross sections are not to scale)

In structures shown in Figure 1(b,c) the slow diffusion current is blocked by the n-type, "nburied" and "niso" layers. Since most of the diffusion current is blocked by these layers these two detectors show smaller responsivities

compared to the n-well detector but wider bandwidths. The detectors shown in Figures 1(b,c) differ in the doping levels of their different regions.

## 3. Circuit Configuration

Figure 2 shows the schematic of the circuits used for characterizing the three photodiode structures. Figure 2a-b shows the circuits used for the DC characterization. This test is used to determine the responsivity of the photodiodes. The p/nburied and p/niso structures require a larger reverse bias voltage as shown in figure 2b to create a larger depletion region to increase the responsivity. Figure 2c shows the block diagram of the electrical path that was used to characterize each of photodiode's frequency response. Two photodiodes are used to provide balanced loading to the transimpedance amplifier (TIA), while one of the photodiodes is covered with metal and does not generate any current. The electrical path provides a flat frequency response up to ~10GHz (including photodiode capacitance), well beyond the bandwidth for all photodiodes. The TIA is followed by emitter follower stages and 50-Ohm buffers to drive the signal off chip. Offset compensation for the system is implemented at the PCB level.

## 4. Measurement Setup & Results

Figure 3a shows a die photo of the fabricated test chip in a BiMOS SiGe process. Figure 3b shows the area occupied by the photodiodes and the electrical path used for testing. Figure 3c shows a simplified measurement setup, where a sinusoidal source is used followed by a laser driver and an optical probe which shines light on one photodiode at a time. The input frequency is varied and the resulting amplitude at the output of the electrical path is recorded using a spectrum analyzer. Since the bandwidth of the electrical path is much larger than the range of interest, this process can be used to characterize the frequency response of the photodiodes. This procedure is repeated for all three photodiodes. The reverse bias voltages used for the photodiodes are 2.3V, 1.7V, and 1.7V for the n-well/psub, p/nburied, and p/niso respectively.

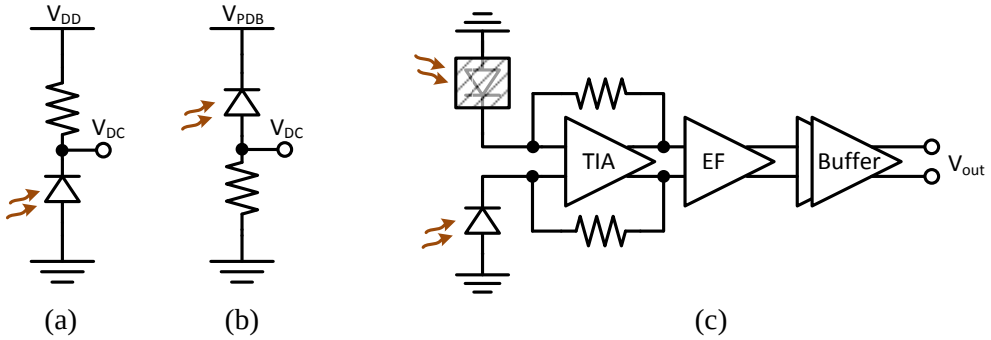
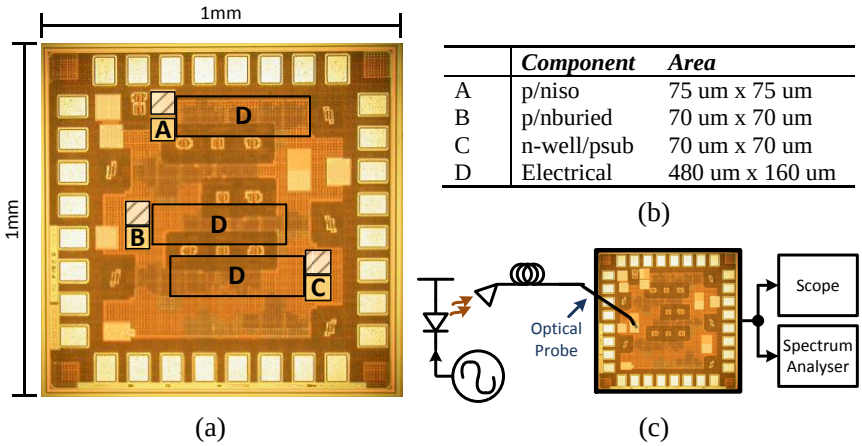



Figure 2 – a) DC test for an n-well photo diode. b) DC test for both PIN & niso photodiodes. c) Electrical block diagram for characterizing the photodiode frequency response



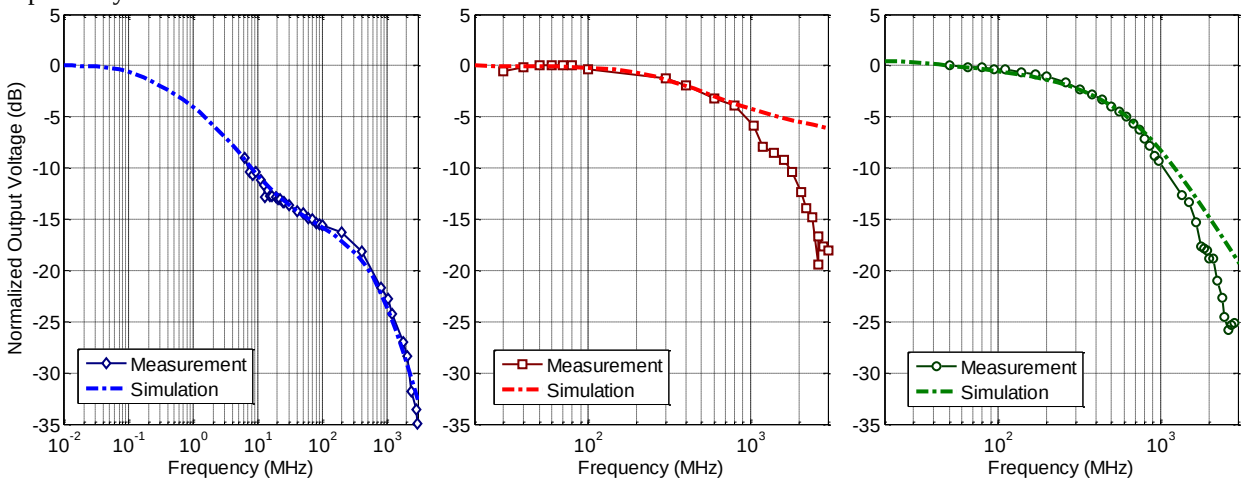

| | *Component* | *Area* |
|---|---|---|
| A | p/niso | 75 um x 75 um |
| B | p/nburied | 70 um x 70 um |
| C | n-well/psub | 70 um x 70 um |
| D | Electrical | 480 um x 160 um |

(b)

Figure 3 - a) Chip die photo b) Area breakdown of different photodiodes and electrical path c) simplified measurement setup

The normalized frequency responses are shown in Figure 4 and can be used as a relative bandwidth comparison for all three photodiodes. The plot also shows device simulation results for the photodiodes obtained using Santaurus software. Table 2 shows the parameters used for simulations.

The n-well/psub photodiode has a 1.5 μm depletion region formed between the n-well and p-substrate. As mentioned earlier, the diffusion current increases the low-frequency responsivity, but limits the bandwidth. In the p/nburied photodiode, due to diffusion of the dopants from the highly doped layers of nburied/SiGe base, there remains only a thin (0.1 um) lightly doped region (1e-17 $cm^{-3}$) between them. An additional thin (0.1 um) depletion region is formed between the nburied layer and the lightly doped region. The small thickness leads to a low responsivity. The strong fields and the isolation provided by the nburied layer, however, improve the bandwidth of the photodiode. Due to the very thin layers in the p/nburied photodiode, small variations cause a large change in the simulated frequency response. The p/niso has a similar structure to the p/nburied photodiode, however, it takes advantage of a thicker lightly doped isolated area which results in a wider depletion region (0.3um). This results in a higher responsivity but a slightly lower bandwidth than the p/nburied photodiode. Table 1 shows the summary of the results for all the characterized photodiodes in terms of responsivity, 3-dB bandwidth, and frequency roll-off. With modest equalization [2], the photodiodes may be suitable for multi-Gb/s communication, particularly the p/niso, whereas more significant equalization is required for the n-well/psub. By assuming that these photodetectors are used in combination with a TIA with input referred noise of $1\mu A_{rms}$ and modest equalization, these responsivity number translate to sensitivities of -14, 1.7, -3.7dBm for the n-well/psub, p/nburied, and p/niso photodiodes respectively.




(a) n-well/psub (b) p/nburied (c) p/niso

Figure 4 – Measurement and simulation results for all three photodiodes for λ = 850nm light

Table 1 - Summary of Photodiode Parameters

| *Photodiode* | *Responsivity (mA/W)* | *3-dB Bandwidth* | *Frequency Roll-off* |
|---|---|---|---|
| n-well/psub | 176 | 580 kHz | -6 dB/dec |
| p/nburied | 4.75 | 600 MHz | -10 dB/dec |
| p/niso | 16.3 | 400 MHz | -16.4 dB/dec |

Table 2 - Simulation parameters

| *Layer* | *Doping ($cm^{-3}$)* | *Thickness (um)* |
|---|---|---|
| n+/p+ | 2e20 | 0.1 |
| SiGe base | 1e20 | 0.1 |
| niso | 1e18 | 0.2 |
| nburied | 3e19 | 0.4 |
| p-sub | 1e15 | 100 |
| ISOLATED | 1e16 | 2 |

## 5. Conclusion

Three photodiodes were simulated, fabricated, and measured under λ = 850nm light in a SiGe BiCMOS process with no additional manufacturing steps, demonstrating that with modest equalization, multi-Gb/s communication is achievable without any special device fabrication. .


## Acknowledgment

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