A 26-Gb/s 1.80-pJ/b CMOS-Driven Transmitter for 850-nm Common-Cathode VCSELs

M. Shibata and A. Chan Carusone
University of Toronto, 10 King's College Road, Toronto, Ontario, M5S 3G4, Canada
masumi.shibata@isl.utoronto.ca and tony.chan.carusone@isl.utoronto.ca

Abstract: A 26-Gb/s, 1.80-pJ/b transmitter composed of a 65-nm bulk-CMOS driver and an 850-nm VCSEL array in a QFN package is demonstrated. The VCSEL's anode is directly modulated without a negative supply voltage at 0.82-dBm OMA.
OCIS codes: (200.4650) Optical interconnects; (060.2360) Fiber optics links and subsystems

1. Introduction

Direct modulation of VCSEL arrays permits parallel optical links with tremendous aggregate bandwidth in a compact footprint at low cost and low power consumption. Direct modulation obviates the need for external optical or silicon photonic modulators which have larger footprints and/or cost. Moreover, VCSEL wafer-level fabrication and testing makes them inexpensive and easy to array. Finally, VCSELs exhibit lower threshold current than edge-emitting lasers [1] permitting lower power consumption.

However, to fully realize the potential benefits of parallel VCSEL-based optical links, CMOS laser drivers are required to permit integration alongside CMOS logic and ultimately lower cost [2]. Unfortunately, most previously-reported CMOS VCSEL drivers are cathode-driving [3–6] making them ill-suited to the least expensive VCSEL arrays which have backside common-cathode terminals. This is because the voltage swings needed to drive the laser diode exceed the core supply voltage of nanoscale CMOS process technologies.

In this paper, we present an inexpensive, 26-Gb/s and 1.80-pJ/b transmitter, comprising a VCSEL driver in a standard 65-nm bulk CMOS technology and a commercially available common-cathode 20-Gb/s VCSEL array assembled into a standard QFN package. All methods used to implement this transmitter module are mass production technologies, including a standard bulk CMOS process without any additional options, a commercially available VCSEL, a standard QFN (Quad Flat No lead) package, a standard FR-4 PCB, and assembly by wire-bonding. The driver IC sources current to the laser diode's anode without a negative power supply.

2. CMOS-driven Optical transmitter

The proposed transmitter is made up of a CMOS driver and a VCSEL array, and the CMOS driver consists of a pre-driver with pre-emphasis, a main driver and a pad shield driver as shown in Fig. 1 (a). A cross-section of the

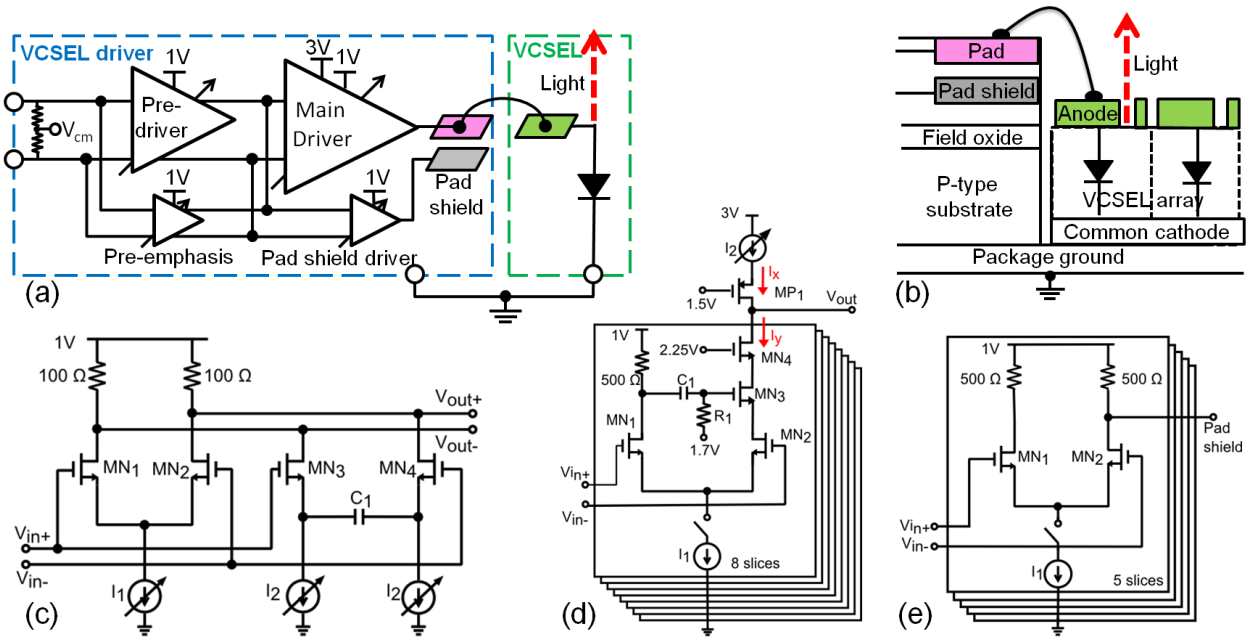


Fig. 1 (a) Block diagram, (b) cross-section of the packaging, (c) pre-driver, (d) main driver and (e) pad shield driver.

packaging interconnect with the pad shield is shown in Fig. 1 (b). The pre-driver has an analog pre-emphasis circuit as shown in Fig. 1 (c), which comprises two paths: a gain path and a high-pass path. The main driver is shown in Fig. 1 (d). The main input signal pair is MN_1, MN_2. When, MN_2 is off, all of the current I_x flows from the 3-V supply to the output pad into the VCSEL. When MN_2 is on, the current $I_y < I_x$ is shunted to ground on-chip, reducing the VCSEL current to $I_x - I_y$. Unlike [4–6], no dummy VCSEL or resistor modeled VCSEL is used for balancing, which facilitates integration of many parallel VCSEL drivers, and reduces the current drawn from the 3-V supply and hence the power consumption of the driver IC.

To drive the anode of a VCSEL directly, the driver output voltage must exceed the VCSEL's threshold voltage, typically more than 1.5 V. If thick-oxide devices are used in the signal path, they will increase parasitic capacitances and limit the driver bandwidth. Hence, in this work, core thin-oxide 65-nm devices are used in the signal path. The gate voltages applied to the cascoded transistors MN_3, MN_4 and MP_1 are chosen to ensure none of the devices' terminal-to-terminal voltages exceeds 1V, as in [7]. Nevertheless, the combination of the parasitic capacitances of MP_1, MN_4, and the output pad along with the bondwire and VCSEL parasitic capacitances limit the driver's bandwidth. To mitigate the output pad capacitance, a metal shield is introduced under the pad to shield it from ground and driven by a fully differential replica driver as shown in Fig. 1 (e). The pad shield is fabricated on the CMOS driver's metal-5 layer, under the output bond pad on the metal-8 and -9 layers. Since the pad shield voltage follows the output pad voltage, the parasitic capacitance between the pad and the pad shield holds a relatively constant voltage and therefore presents little load to the output stage. Although the pad shield driver is now driving the pad capacitance instead, its design is much simpler than that of the output stage as it does not require high output impedance, can use smaller core transistors, and consumes relatively little power from the low 1-V supply. The power consumption of the pad shield driver is tunable up to 5 mW to optimize the transmitter's performance.

In addition, a bootstrap technique was used to reduce the input capacitance of the main driver, hence improving the bandwidth of the pre-driver. Specifically, MN_3, is bootstrapped by the drain voltage of MN_1, through the capacitance, C_1, in Fig. 1 (d). This minimizes the input capacitance of MN_2, by holding the charge on the parasitic capacitance between the drain and the gate of MN_2 approximately constant.

3. Measurement Results

The custom VCSEL driver was fabricated in a standard bulk 65-nm CMOS technology. The photo of the transmitter is shown in Fig. 2 (a), of which the driver core area occupies 0.15 mm × 0.16 mm = 0.024 mm^2 as shown in Fig. (b). The photo and the diagram of the optical test setups are shown in Fig. 2 (c) and (d). The commercially-available 850-nm 20-Gb/s multimode VCSELs have a typical modulation bandwidth of 16 GHz according to the data sheet. The CMOS driver chip and VCSEL array, which has four topside anode contacts and a backside common-cathode contact, are wire-bonded in the same open-cavity QFN package and soldered onto a standard FR-4 PCB. The output pad of a CMOS driver chip and the topside anode pad of a VCSEL chip were connected by a 25-µm diameter gold wire bond and the backside cathode pad is directly connected to a package-common ground by using a conductive epoxy. The assembly methods we used are all standard inexpensive methods. A Keysight 86100C oscilloscope was used to capture single-ended optical eye diagrams using a Keysight 86105D 20-GHz optical module. An input pattern (NRZ 2^7-1 PRBS pattern) was provided from a combination of a Keysight N4960A Serial BERT controller and a N4951B pattern generator remote head to the driver through a pair of 15 cm cables, DC blocking capacitors, SMA connectors, transmission lines on FR-4 PCB and the QFN package. The amplitude of the input signals was 458 mV peak to peak per side and the input rms jitter was 1.86 ps at 26 Gb/s.

The output optical eye diagrams are shown in Fig. 3 (a), (b) and (c). No damage was observed to any of the output stage transistors including three 1-V devices, MN_3, MN_4 and MP_1 in Fig. 1 (d), in spite of output terminal voltages changes in the range from 1.6 V to 2.3 V in our measurements. Even with a 20-Gb/s VCSEL, a clear eye opening was obtained up to 26-Gb/s operation with a 6-mA bias current and a 8-mA modulation current amplitude, resulting in an average output power of 1.4 dBm (1.38 mW), optical modulation amplitude (OMA) of 0.82 dBm (1.21 mW), ER of 3.8 dB and 2.95 ps-rms jitter. As shown in Fig. 3 (b) and (c), the combination of the pre-emphasis

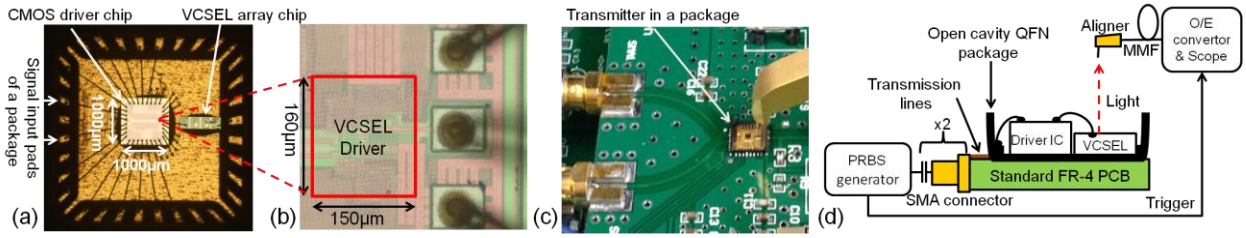


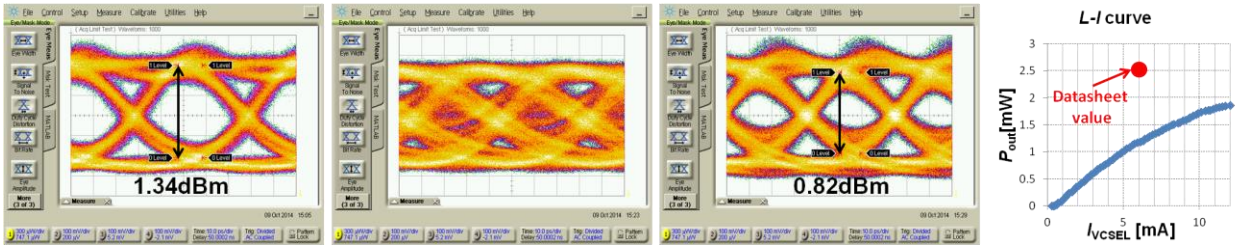
Fig. 2 (a) Transmitter photo, (b) a driver core area, (c) setups photo and (d) setup diagram.

(PE) and the pad shield driving (PS) techniques was needed to enable 26-Gb/s operation. The pad shield driving alone increased the OMA by 17% at 26 Gb/s. In addition, opens eyes were measured at 28 Gb/s with OMA of 0.46 dBm, exceeding the typical requirements of low-power optical links (e.g. -4dBm in [8]).

The light emitting from the VCSEL was coupled by a 3-m pigtail of 50/125 µm multimode fiber (OM2), which was aligned manually. The measured VCSEL's *L-I* characteristics at room temperature is shown in Fig. 3 (d). According to our measurements, our setup has 53 % coupling loss which we believe is attributable to the difficulty of manual aligning the fiber to the VCSEL.

4. Conclusions

A 26-Gb/s and 1.80-pJ/b bulk-CMOS transmitter with an 850-nm common-cathode VCSEL array has been demonstrated. The driver was fabricated in a standard 65-nm bulk CMOS technology, with pre-emphasis and a novel pad shield driving technique to enhance bandwidth. All methods used for fabrication and assembly of this transmitter module are mass production technologies. This VCSEL driver is compared with other reported drivers in Table 1. To authors' knowledge, this transmitter has the smallest area and the best power efficiency amongst anode-driving circuits in any process technology, which are preferred to drive low-cost VCSELs in a 2-D array structure.



(a) 20Gb/s w PE and PS (b) 26Gb/s w/o PE and PS (c) 26Gb/s w PE and PS (d) L-I characteristics

Fig.3 (a) – (c) Optical eye diagrams. Scales: 0.3 mW/div and 10 ps/div, (d) measured *L-I* characteristics at room temperature.

Table 1. Performance comparison of VCSEL drivers. The power efficiency of [4-6] include a dummy VCSEL's power.

	This work	[9]	[10]	[3]	[4]	[5]			[6]	
Process	CMOS 65nm	CMOS 65nm	SiGe 0.13µm	CMOS 65nm	SiGe 0.13µm	CMOS 90nm			SOI CMOS 32nm	
Data rate [Gb/s]	26	10	40	25	64	15	25	28.5	25	35
Supply voltage [V]	1.0/3.0	1.2/3.3	2.5/3.3	1.2/3.6	N/A	1.2/2.18	0.7/0.6/2.35	1.2/0.7/2.5	0.63/0.4/2.25	1.1/3.09
Power efficiency [pJ/b]	**1.80**	6.95	7.8	3.96	14.7	1.01	1.37	2.47	0.93	2.1
OMA [dBm]	0.82	6.4	2.3	0.78	–0.70	–1.1	–0.41	–0.76	–2.0	1.5
Area [mm^2]	**0.024**	0.13	0.5	0.5	N/A	0.014	0.056		0.0021	
Year	2015	2014	2014	2013	2014	2012			2013	
Driver type	**Anode-driving**			Cathode-driving						

5. References

[1] F. Koyama, "Recent Advances of VCSEL photonics," IEEE *J. Lightwave Technology*, vol. 24, no. 12, pp.4502–4513, Dec. 2006.

[2] J. A. Tatum, "The Evolution of 850nm VCSELs from 10Gb/s to 25 and 56Gb/s," in *Proc. Optical Fiber Communications Conf. (OFC),* paper Th3C1, Mar. 2014.

[3] J. Jiang, et al., "100Gb/s Ethernet Chipsets in 65nm CMOS Technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 120–122, Feb. 2013.

[4] D. M. Kuchta, et al., "64Gb/s Transmission over 57m MMF using an NRZ Modulated 850nm VCSEL," in *Proc. Optical Fiber Communications Conf. (OFC)*, paper Th3C2, Mar. 2014.

[5] J. E. Proesel, et al., " Ultra-Low-Power 10 to 28.5 Gb/s CMOS-Driven VCSEL-Based Optical Links," *J. Opt. Commun. Netw.*,Vol.4, no.11, pp. B114–B123, Nov. 2012.

[6] J. E. Proesel, et al., "35-Gb/s VCSEL-Based Optical Link using 32-nm SOI CMOS Circuits," in *Proc. Optical Fiber Communications Conf. (OFC)*, paper OM2H2, Mar. 2013.

[7] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[8] J. B. Heroux, et al., "Optical Transmitter with 1060 nm VCSEL for Low Power Interconnect," in *Proc. Optical Fiber Communications Conf. (OFC)*, paper JThA45, Mar. 2011.

[9] H. Morita, et al., "A 12×5 Two-Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 140–142, Feb. 2014.

[10] Y. Tsunoda, et al., "A 40Gb/s VCSEL Over-Driving IC with Group-Delay-Tunable Pre-Emphasis for Optical Interconnection," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 154–156, Feb. 2014.