A 5-Gbps Optical Receiver with Monolithically Integrated Photodetector in 0.18-μm CMOS

by

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Abstract

An optical receiver with monolithically integrated photodetector in 0.18-μm CMOS technology was investigated. Using a combination of spatially modulated light detection and an analog equalizer, a maximum data rate of 5 Gbps was achieved. A transimpedance amplifier employing negative Miller capacitance is introduced to increase its bandwidth without causing gain peaking. Occupying a total area of 4.2 mm^2 and a core area of 0.72 mm^2, the fully integrated optical receiver achieves 4.25 Gbps and 5 Gbps with a power consumption of 144 mW and 183 mW respectively.

Acknowledgments

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Great appreciation for the constant support from my family.

To my sweetie Christy, thanks for everything else.

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List of Acronyms

AC Alternating Current

BER Bit Error Rate

BERT Bit-Error-Rate Tester

BiCMOS Bipolar Complementary Metal Oxide Semiconductor

CD-ROM Compact Disc Read-Only Memory

CID Consecutive Identical Digits

CMOS Complimentary Metal-Oxide Semiconductor

DC Direct Current

DVD Digital Versatile Disc

EMI Electromagnetic Interference

ESD Electrostatic Discharge

FTTH Fiber-to-the-Home

GBW Gain Bandwidth Product

HS High Speed

IC Integrated Circuit

ISI Inter-symbol Interference

LA Limiting-Amplifier

LAN Local Area Network

LP Low Power

MIM Metal-Insulator-Metal

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NFET N-Channel Field Effect Transistor

NMOS N-Channel MOSFET

NRZ Nonreturn-to-zero

PA Post-Amplifier

PCB Printed Circuit Board

PFET P-Channel Field Effect Transistor

PM Phase Margin

PN P-type and N-type

PRBS Pseudorandom Binary Sequence

QFN Quad Flat No leads

RGC Regulated Cascode

RMS Root Mean Square

SML Spatially Modulated Light

SOI Silicon on Insulator

TIA Transimpedance Amplifier

VCSEL Vertical-Cavity Surface Emitting Laser

Chapter 1

Introduction

1.1. Motivation

Optical receivers with monolithically integrated photodetectors are attractive as they can be used in short-distance communication systems such as local-area networks (LANs), fiber-to-the-home (FTTH), automotive interconnects, board-to-board links, and chip-to-chip interconnects. Optical interfaces are also required in optical storage systems such as Compact Disc Read-Only Memory (CD-ROM), Digital Versatile Disc (DVD), and Blue-ray Disc. In all these applications, a photodetector is necessary to establish the conversion from light to electrical signal for further processing.

Optical receivers built in standard Complimentary Metal-Oxide Semiconductor (CMOS) technology have been an active area of research. Commercially, high-speed photodetectors have mainly been implemented in III-V technologies such as GaAs [1] and InP-InGaAs [2] for long-haul optical communication. Although the cost of the entire system is high due to the use of these expensive technologies, the cost per user remains low thanks to the large number of users per channel. However, for short-distance communication, a low-cost solution must be investigated as the communication channels are usually not shared by a large number of users. This motivates the use of 850-nm low-cost vertical-cavity surface-emitting lasers (VCSELs) at the transmitter side as the source. To further reduce the cost, the entire optical receiver must be implemented in standard CMOS technology. This not only can save the extra overhead and cost during assembly for multi-chip solutions, but ground-bounce issues, electrostatic discharge (ESD) problems, and parasitics associated with bond pads and bond wires can also be eliminated.

1.2. State of the Art

In general, light detection in CMOS technology is achieved by a reverse biased PN junction which creates a depletion region to collect the electron-hole pairs generated by the incident photons. However, the penetration depth of 850-nm light is much larger than where the depletion region occurs in standard CMOS technology. Consequently, many carriers generated deep in the silicon substrate must diffuse all the way up to the depletion region. The slow diffusion mechanism limits the data rate to only a few hundreds of Mbps [3, 4].

Several methods have been provided to eliminate the slow diffusive carriers in order to improve the speed of monolithically integrated photodetectors in CMOS. In many cases, this can be achieved by using a buried oxide layer [5] or silicon on insulator (SOI) [6, 7] process, but this requires modification to the standard CMOS process which leads to an increase in cost. Similarly, many photodetectors are built in Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) due to its superior performance for optical receivers [8, 9], but this approach disallows monolithic integration in large scaled CMOS ICs. In purely standard CMOS technology, speed can be improved by applying a high reverse biased voltage, often higher than the power supply, to generate a very thick depletion region [10, 11, 12]. This approach however seriously impacts the reliability of the photodetector. A spatially modulated light (SML) detector topology which consists of alternatively covered and exposed diodes has been used to eliminate the slow diffusive carriers [13, 14]. The SML detection improves at the expense of a relatively smaller responsivity. Equalization has also been applied to solve this problem. In [4], a high-pass analog equalizer is used to improve the low intrinsic bandwidth of the photodiode.

In addition, the highest reported responsivity of CMOS photodetectors is only 0.07 A/W with standard power supplies [15]; whereas the responsivity of the photodetectors built in dedicated technology such as BiCMOS can be as high as 0.4 A/W [9].

1.3. Objective

The highest data rate previously reported for a fully integrated CMOS optical receiver is limited to 3.125 Gbps at a sensitivity of -4.2 dBm with a BER of 10^{-12} [15]. The objective of this thesis is to extend the state-of-the-art data rate to 4 Gbps by using a combination of SML detection and an analog equalizer. In addition, a low-noise optical receiver is also investigated to improve sensitivity in order to compensate for the typically low responsivity of the CMOS photodetectors.

1.4. Outline

The remaining chapters are organized as follows. Chapter 2 provides the necessary background information on monolithically integrated photodetectors and the system-level simulations of the photodetector with equalization. Chapter 3 details the transistor-level design and simulations of various circuit blocks of the optical receiver. Chapter 4 presents measurement results. Chapter 5 concludes the thesis and provides suggestions for further work.

Chapter 2

Background and System Design

This chapter begins with background information on the photodetector and equalizer in section 2.1 and section 2.2 respectively. It concludes with system-level simulation results in section 2.3.

2.1. Photodetector

A photodetector converts the incident optical power into a current. The principles of light detection in the photodetector along with its model are presented as follows. A system-level simulation based on the model is performed to show the bandwidth limitation of the photodetector.

2.1.1. Light Detection

Light comprises a stream of photons. Each photon can be characterized by its energy, E_{ph},

$$E_{ph} = \frac{hc}{\lambda}. \tag{2.1}$$

where $h = 6.63 \cdot 10^{-34}$ J$\cdot$s, $c = 3 \cdot 10^{8}$ m/s, and λ is the corresponding wavelength. Light detection may be performed by a reverse biased PN junction. The bandgap energy of the semiconductor material used to create the PN junction is denoted as E_g. For each photon with $E_{ph} \geq E_g$, an electron-hole pair is created; hence, current is generated. The electron-hole pairs created in the depletion region of the PN junction are separated by a large electric field corresponding to the drift current. The carriers generated outside the depletion region in both P-type and N-type material correspond

Table 2.1: α as a function of the wavelength.

Wavelength (nm)	α **(um^{-1})**
850	0.06
780	0.12
680	0.24
635	0.38
430	5.7

to the diffusion current as they must diffuse towards the depletion region before they can be collected, provided they reach the junction before recombination occurs. The absorption coefficient, α, determines how deep the light penetrates into a material and is a function of the wavelength as shown in Table 2.1 [16].

According to Lambert-Beer's law, the intensity of light penetrating into a medium decreases exponentially with depth [17]:

$$\Phi(x) = \Phi_0 \cdot e^{-\alpha x}. \tag{2.2}$$

where $\Phi(x)$ is the light flux at depth x into the semiconductor material, and Φ_0 is the initial flux.

As shown in equation (2.2), the smaller α is, the deeper the light can penetrate down. Since the penetration depth of 850-nm light is much larger than where the depletion region occurs in standard CMOS technology, it is therefore desirable to have a wide depletion region so that the diffusive carriers can arrive at the junction as quickly as possible. The depletion width, W, is [17]

$$W = \sqrt{\frac{2\epsilon_{Si}}{q}\frac{N_A + N_D}{N_A N_D}(V_{bi} - V_R)}. \tag{2.3}$$

where N_A is the doping concentration of acceptors in the P-type material, N_D is the doping concentration of donors in the N-type material, ϵ_{Si} is the permittivity of Si, q is the charge of an election, V_{bi} is the built-in voltage which is technology dependent, and V_R is the reverse-bias voltage and is a negative number. Hence, a wider depletion region can be achieved with lower doping concentrations and higher reverse biased voltage. In a standard CMOS process, the n-well has a lower dopant concentration than the n+ region and the p-substrate has a lower dopant concentration than the p+ region. Hence, the PN junction of the photodetector was built between a n-well

and p-substrate to increase the depletion width.

The total current density, J_{total}, is the sum of the drift component in the depletion region together with the diffusive components in both p-substrate, $J_{diff,\ p-substrate}$ and n-well, $J_{diff,\ n-well}$:

$$J_{total} = J_{drift} + J_{diff,\ p-substrate} + J_{diff,\ n-well}. \tag{2.4}$$

The overall bandwidth is mainly limited by $J_{diff,\ p-substrate}$ and has been reported to be only 70 MHz [18]. To obtain a higher speed, the slow diffusive carriers must be eliminated. This can be achieved by using a spatially modulated light (SML) detector. A simplified cross section of the SML detector is shown in Figure 2.1. It consists of an exposed and a covered photodiode with a light-blocking metal. When the light is incident on the surface of the detector, carriers generated in the depletion region are immediately collected by the exposed photodiode. Carriers generated in the deep substrate will diffuse towards the depletion region and have equal probability of reaching either the exposed or the covered photodiode. Hence, when the signal currents collected by these two photodiodes are subtracted, the slow diffusive currents are cancelled and a faster response is obtained. The cancellation however reduces the responsivity of the photodetector, and a low-noise receiver is necessary to amplify differential currents in the range of a few microamperes from the SML detector without degrading the sensitivity.

2.1.2. Photodetector Model

The frequency response of J_{drift}, $J_{diff,\ p-substrate}$, and $J_{diff,\ n-well}$ are discussed individually as follows based on the simplified cross section of the SML detector shown in Figure 2.1.

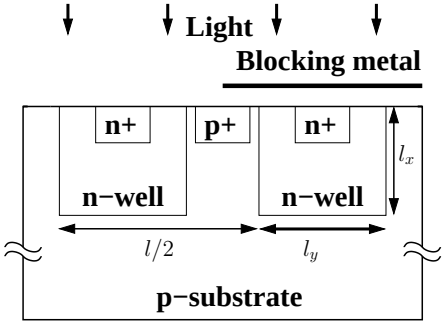


Figure 2.1: Simplified cross section of the SML detector.

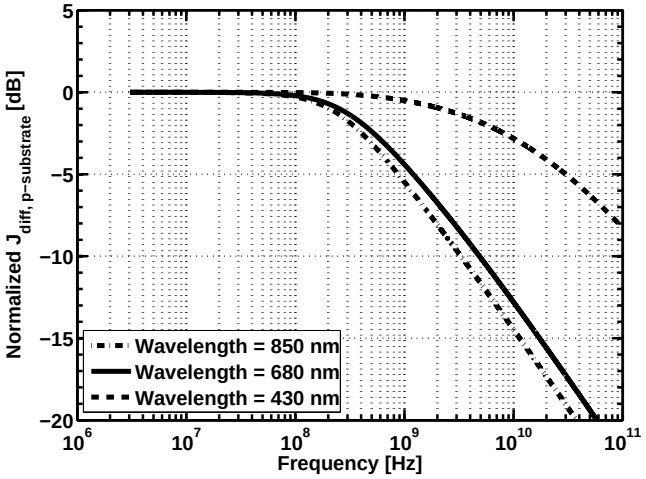


Figure 2.2: Normalized $J_{diff,\ p-substrate}$ for different wavelengths.

J_{drift}

Due to the large electric field in the depletion region, the bandwidth of J_{drift} will always be much larger than that of $J_{diff,\ p-substrate}$ and $J_{diff,\ n-well}$. Therefore, J_{drift} is assumed to be frequency independent, and its magnitude is directly proportional to the width of the depletion region.

$J_{diff,\ p-substrate}$

The current response of $J_{diff,\ p-substrate}$ is shown in equation (2.5) [19].

$$J_{diff,\ p-substrate} = q\alpha L_n e^{-\alpha l_x} \sum_{n=1}^{\infty} \frac{4}{\pi^2(2n-1)^2} \frac{1}{\sqrt{(\frac{(2n-1)2\pi L_n}{l})^2 + 1 + j\omega\tau_n} + \alpha L_n}. \quad (2.5)$$

where L_n is the diffusion length of electrons, l_x is the distance between the surface and the PN junction, τ_n is the lifetime of electrons, and l is the periodicity of the structure. Since α is related to the wavelength, normalized $J_{diff,\ p-substrate}$ for different wavelengths is shown in Figure 2.2. The result confirms that smaller α results to a lower bandwidth as light penetrates deeper into the substrate and carriers generated further down must slowly diffusive up to the junction.

$J_{diff,\ n-well}$

The current response of $J_{diff,\ n-well}$ is shown in equation (2.6) [19].

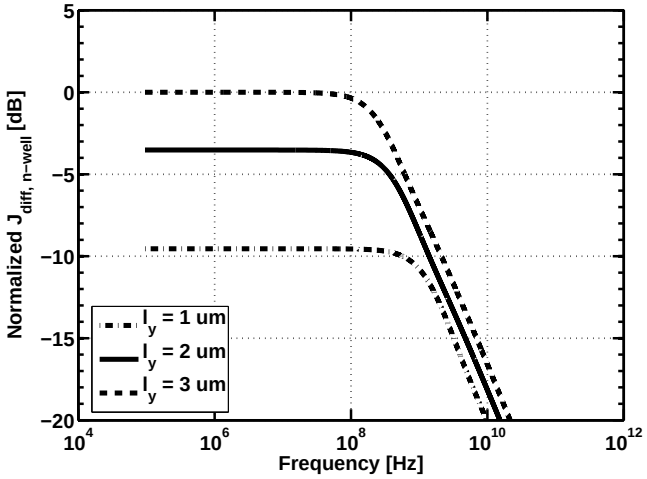


Figure 2.3: Normalized $J_{diff,\ n-well}$ for different l_y.

$$J_{diff,\ n-well} = q\frac{L_p^2}{l}\frac{32}{\pi^2}\frac{(1-e^{-\alpha l_x})}{l_x}\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{\frac{2l_x}{l_y}(\frac{1}{2n-1})^2+\frac{l_y}{2l_x}(\frac{1}{2m-1})^2}{(\frac{(2n-1)\pi L_p}{2l_x})^2+(\frac{(2m-1)\pi L_p}{l_y})^2+1+j\omega\tau_p}. \quad (2.6)$$

where l_y is the width of the n-well, L_p is the diffusion length of holes, and τ_p is the lifetime of holes. As l_y reduces, holes arrives at the junction more quickly and results in a higher bandwidth. Normalized $J_{diff,\ n-well}$ is shown in Figure 2.3. It can also be observed that although $l_y = 1$ um results in the highest bandwidth, but it also leads to a lower responsivity and has less effect on the overall bandwidth.

2.1.3. Photodetector Simulation in Matlab

The final dimension of $l_y = 2.6$ um was chosen as a compromise between bandwidth and responsivity. The spacing between neighboring n-wells was the minimum allowable distance set by the design rules, 1.4 um. Hence, this results $l = 8$ um. The photodetector occupies a total area of 75 um $\times$ 75 um. The normalized total current response, J_{total}, is shown in Figure 2.4. The slow roll-off at high frequencies is due to the summation of the different current responses. The bandwidth of the SML detector has been improved to 700 MHz. An eye diagram of the SML detector at 4 Gbps is shown in Figure 2.5 simulated using the presented model. The tail seen in the eye diagram is the result of the slow-roll off of J_{total} and can be removed by an equalizer.

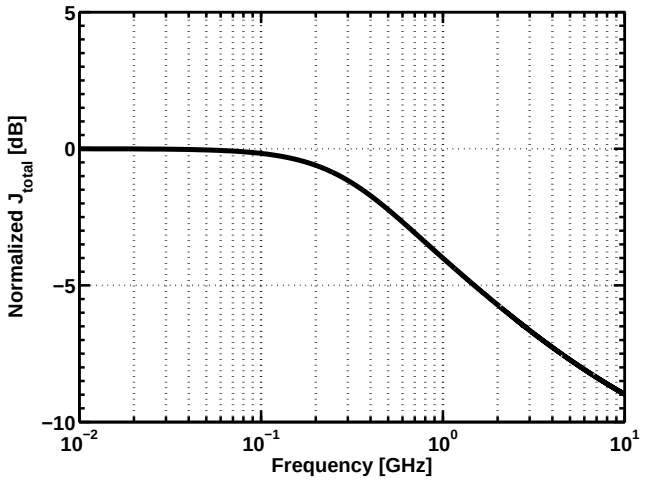


Figure 2.4: Normalized J_{total}.

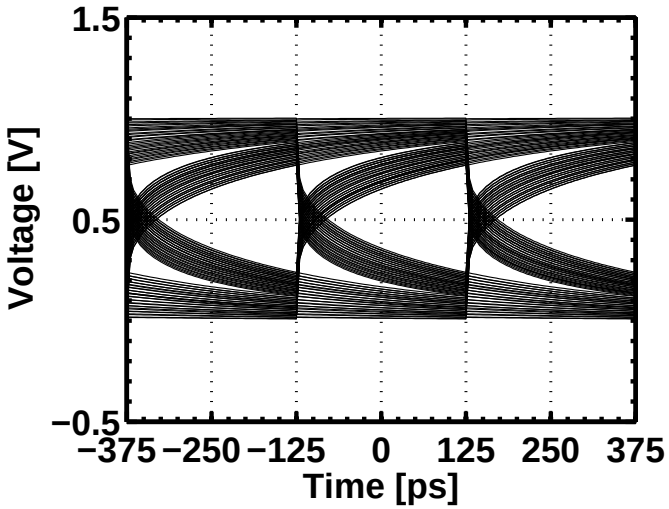


Figure 2.5: Behavioral simulation eye diagram of the SML detector at 4 Gbps.

2.2. Equalizer

The SML detector acts as a built-in equalizer to eliminate the slow diffusive carriers; nevertheless, the resulting intrinsic bandwidth of the photodetector is not sufficient for the targeted 4 Gbps operation. Hence, an additional equalizer is used to compensate the frequency roll-off of the SML detector.

2.2.1. Equalizer Model

Peaking equalizers have commonly been used to provide a simple implementation to compensate notch-free and low-pass channels. The zero provided by the peaking equalizers may be implemented using a weighted sum of low-pass and high-pass paths [20] or capacitive degeneration [21, 22]. In this work, the peaking equalizer was implemented with capacitive degeneration. The peaking in the equalizer is modeled with a zero and two poles in its transfer function, H_{eq},

$$H_{eq}(s) = \frac{1 + \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}. \tag{2.7}$$

where ω_z, ω_{p1}, and ω_{p2} denote the zero and the two poles of H_{eq} respectively [22]. The second pole of the equalizer is used to model the output parasitic capacitance of the equalizer which arises during circuit design.

2.3. System Simulation

The frequency response of the SML detector, the equalizer, and the equalized SML detector is shown in Figure 2.6. A boosting of 4 dB extends the bandwidth of the SML detector to 3 GHz. The eye diagram of the equalized SML detector at 4 Gbps is shown in Figure 2.7. The ISI shown in Figure 2.5 has been significantly removed by the proposed equalizer. With the combination of the SML detector and an analog equalizer, a higher speed of operation is achievable.

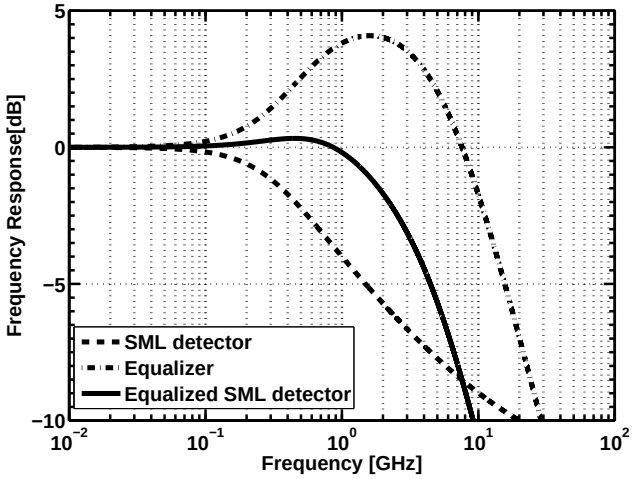


Figure 2.6: Frequency response of the SML detector, the equalizer, and the equalized SML detector.

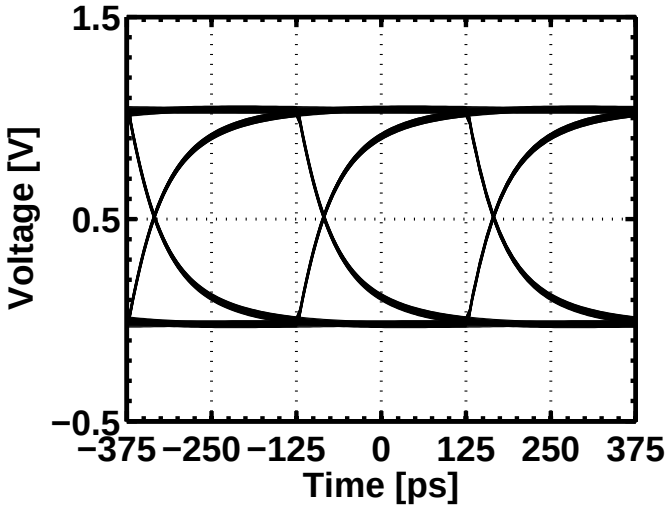


Figure 2.7: Behavioral simulation eye diagram of the equalized SML detector at 4 Gbps.

Chapter 3

Circuit Design and Simulation

This chapter discusses the circuit design of the optical receiver front-end whose architecture is shown in Figure 3.1. Section 3.1 provides a top-level description of the design. Sections 3.2 to 3.6 detail the design and simulation results of each circuit block. The remaining two sections verify the design by showing simulation results of the entire receiver and concluding the chapter respectively.

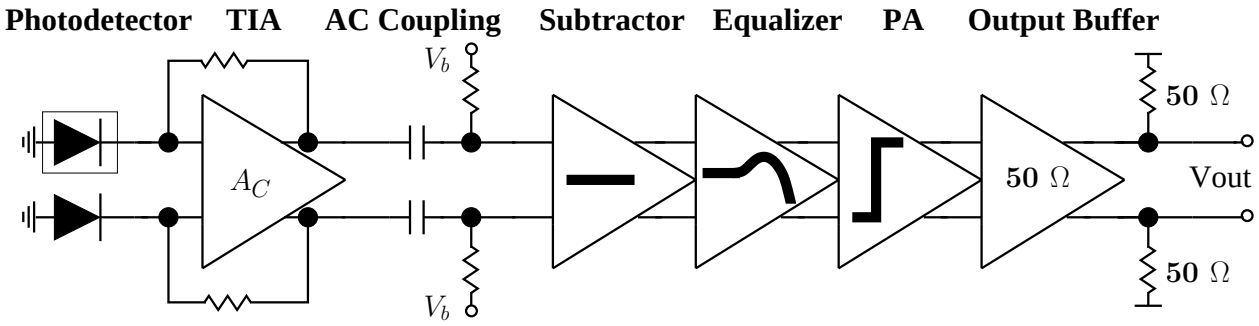


Figure 3.1: Optical receiver block diagram.

3.1. General Information

3.1.1. Circuit Description

As shown in Figure 3.1, the entire optical receiver front-end begins with the SML detector which converts the incident optical power into two currents. When the subtraction of these two signals is performed, the signal due to slow diffusive carriers from the substrate can be removed and the bandwidth of the photodetector can be improved

to 1 GHz [14]. A differential TIA converts the two currents from the photodiodes into two voltages. The supply of the TIA was 3.3 V in order to provide a high reverse bias voltage for the photodiodes so that a large photodetector bandwidth and responsivity can be achieved simultaneously. AC coupling with a cutoff frequency of 100 kHz was used to connect the TIA to the rest of the circuit blocks which operate from a 1.8 V supply. Since the current from the exposed photodiode is always larger than that from the covered photodiode, the AC coupling link has the added benefit of eliminating any difference between the common-mode levels of the two signals. A subtracter follows to further improve common-mode rejection and cancel the slow diffusive carriers generated by photon absorption deep in the substrate. The resulting signal after the subtracter is completely differential. An equalizer and a post-amplifier (PA) follow to further remove inter-symbol interference (ISI) and increase the signal swing respectively. For testing purposes, an output buffer was used to drive the signal to the oscilloscope.

3.1.2. Technology

The design was implemented in 0.18-µm CMOS technology with $f_T \approx 48$ GHz which offers 1 poly and 6 metal layers.

3.1.3. Simulation Corners

The entire design was optimized for TT/60°C. However, simulation corners at SS/100°C and FF/20°C were also performed in order to ensure robustness with process variation. Current densities were maintained across corners by adjusting control voltages associated with the bias circuitry.

3.2. Transimpedance Amplifier

Among all the building blocks in the whole receiver, the TIA is the most critical one in this design. Since the current signals from the photodetector are only tens of micro amperes, the performance of the TIA often limits the overall performance of the entire receiver. Hence, trade-offs between transimpedance gain, bandwidth, noise, and stability will hence be discussed in this section.

3.2.1. Specifications

Noise

Since the TIA is placed right at the input, its noise contribution often dominates over that from other blocks. The total integrated input-referred noise current, $I_{n,in,tot}$, is determined by dividing the total integrated output noise voltage, $V_{n,out,tot}$, by the TIA's low-frequency transimpedance gain, R_T, as expressed by

$$I_{n,in,tot} = \frac{V_{n,out,tot}}{R_T}. \tag{3.1}$$

While a low-noise TIA is desirable, the main focus of this optical receiver is to extend the state-of-the-art data rate for integrated CMOS photodetectors to at least 4 Gbps with standard voltage supplies.

Transimpedance Gain

A large transimpedance gain is desirable for two reasons. First, it relaxes the gain requirement in the PA. Second, increasing R_T reduces the input-referred noise as noise contributions from later stages will be divided by a large transimpedance gain as shown from equation (3.1). A minimum transimpedance gain of 5 kΩ (74 dBΩ) was targeted for R_T.

Bandwidth

The bandwidth of the TIA must be chosen carefully. A small bandwidth causes ISI and reduces the eye-opening; a large bandwidth increases the total integrated noise and reduces the input sensitivity. As a compromise between ISI and noise, the bandwidth of the TIA is often targeted to be $0.7 \cdot R_b$ [23], where R_b represents the data rate of the NRZ signal. For 4-Gbps operation, the bandwidth was aimed to be about 2.8 GHz. Since the bandwidth of the photodetector is only 1 GHz, a TIA bandwidth of 2.8 GHz is large enough to carry the signal to the equalizer. In addition, the selected bandwidth also ensures peaking at $0.5 \cdot R_b$ from the equalizer is not attenuated.

Stability

As TIAs generally employ feedback, stability must be examined. A minimum phase margin of 60 degrees was targeted to minimize overshoot and hence ensure the quality of the eye diagram.

3.2.2. Design

The shunt-shunt feedback TIA has been frequently used in optical receiver front-ends. Its general architecture is shown in Figure 3.2. Denoting the low-frequency voltage gain of the core amplifier as A_C, the DC transimpedance gain, R_T, of the TIA can be approximated as

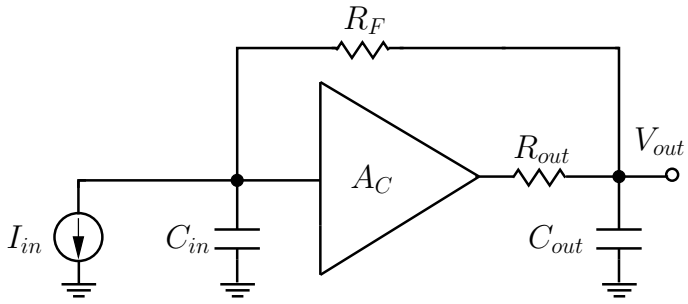


Figure 3.2: Shunt-shunt feedback TIA.

$$R_T \approx \frac{R_F A_C}{A_C + 1}. \tag{3.2}$$

Hence, R_T is approximately equal to R_F for large A_C. The input current source, I_{in}, models the current of the photodetector. The total input capacitance, C_{in}, at the input of the TIA includes the input capacitance of the core amplifier and the parasitic capacitance of the photodetector. The total output capacitance, C_{out}, at the output of the TIA includes the output capacitance of the core amplifier and the input capacitance of the next stage. The core amplifier has an output resistance R_{out}. Making the following approximations:

$$A_C + 1 \approx A_C, \tag{3.3}$$

$$R_{out} \ll R_F, \tag{3.4}$$

$$R_{out} C_{out} \ll R_F C_{in}, \tag{3.5}$$

the bandwidth of the TIA, BW_{TIA}, can be approximated as [17]

$$BW_{TIA} = \frac{A_C}{2\pi R_F C_{in}} \tag{3.6}$$

where R_F and C_{in} form the dominant pole of the closed-loop system.

A regulated cascode (RGC) stage has often been employed to alleviate bandwidth reduction of the TIA due the large parasitic capacitance of photodetectors [11], [15]. This topology however increases the noise contribution from the TIA due to the added components directly at its input. In addition, the RGC stage often leads to a lower reverse bias voltage for the photodetector which further degrades its responsivity. Since the sensitivity degrades with an increase of noise in the TIA and a decrease of responsivity in the photodetector, the RGC stage is not considered for the implementation of the TIA.

As C_{in} is mainly dominated by the capacitance of the photodetector which is fixed for a given dimension to comply with the diameter of the multimode fiber, the only two ways to increase the bandwidth is to either reduce R_F or increase A_C. Reducing R_F is undesirable as it leads into a higher input-referred noise current due to the decrease of the transimpedance gain as seen from equation (3.1). Therefore, a high A_C is targeted during the design of the TIA to achieve both high transimpedance gain and high bandwidth.

By assuming that the core amplifier has only one dominant pole, the close-loop response of the TIA forms a two-pole system and peaking might occur if the two poles were complex conjugate pair close to the $j\omega$ axis. It can be shown that for $A_C \gg 1$, the condition to guarantee a flat frequency response is [24]

$$BW_{CA} \geq \frac{2A_C}{2\ \pi R_F C_{in}} \tag{3.7}$$

Equation (3.7) shows that A_C cannot be maximized indefinitely to achieve a high bandwidth without causing too much overshoot in the time domain due to the peaking in the frequency response. Although it is derived based on a two-pole system, in the case of a multiple-pole system, it is still important to note that the bandwidth of the core amplifier must be high enough in order to ensure a flat frequency response thus a good stability.

In summary, to achieve a high transimpedance gain, a large R_F must be chosen. Since the bandwidth of the TIA varies inversely proportional to R_F, the gain of the core amplifier, A_C, must be made large to keep the bandwidth high. As A_C increases, the bandwidth of the core amplifier also needs to be extended in order to ensure a flat frequency response so that the amount of the overshoot in the time domain can be minimized.

The schematic of the TIA is shown in Figure 3.3. The transistor size is specified as N_f x W_f / L, where N_f, W_f, and L denote the number of fingers, the finger width, and

the finger length. A supply of 3.3 V was used to provide a large reverse-bias voltage for both the exposed and covered photodiodes so that bandwidth and responsivity of the photodetector can be improved together. The gate-source and gate-drain voltages of all transistors are kept within 1.8 V to guarantee reliability of the operation. To increase A_C, two identical differential-pair amplifiers were cascaded to implement the core amplifier. The number of stages was limited to two as a compromise between gain and stability. A capacitor can be added in parallel with R_F to eliminate possible gain peaking but at the expense of a reduce TIA bandwidth [16]. Instead, the topology used in this work employs a negative Miller capacitance in the core amplifier, which extends the dominant pole of this stage and leads to an increase in the overall TIA bandwidth. In addition, the improvement in the phase margin created by this shift of the core-amplifier pole allows A_C to be increased without sacrificing stability. This further increases the bandwidth of the TIA as shown in equation (3.6). In conclusion, the use of the negative Miller capacitance achieves a higher bandwidth without sacrificing the transimpedance gain and stability.

3.2.3. Simulation Results

The frequency response of the TIA is shown in Figure 3.4 with different values of C_m. The value of C_m was optimized in order to achieve a maximally flat response. The performance comparison of different values of C_m is summarized in Table 3.1. While a larger core-amplifier gain could be implemented to achieve a higher TIA bandwidth, it often sacrifices the PM. The result of Table 3.1 shows that with the appropriate value of C_m, PM is improved due to a higher bandwidth of the core amplifier. The output noise spectrum density of the TIA is shown in Figure 3.5. A summary of the simulation results in different corners with $C_m = 90$ fF is shown in Table 3.2. The eye diagrams at both positive and negative output terminals of the TIA are shown Figure 3.6(a) and Figure 3.6(b). A portion of a $2^{31} - 1$ PRBS pattern including 31 CID was used for the input. It can be observed that the output common-modes at both output terminals of the TIA are different since the current converted by the exposed photodiode is always higher than that by the covered photodiode. Furthermore, since the eye diagrams of the signals at both terminals look different, the common-mode rejection must be improved in order to effectively remove the slow diffusive carriers.

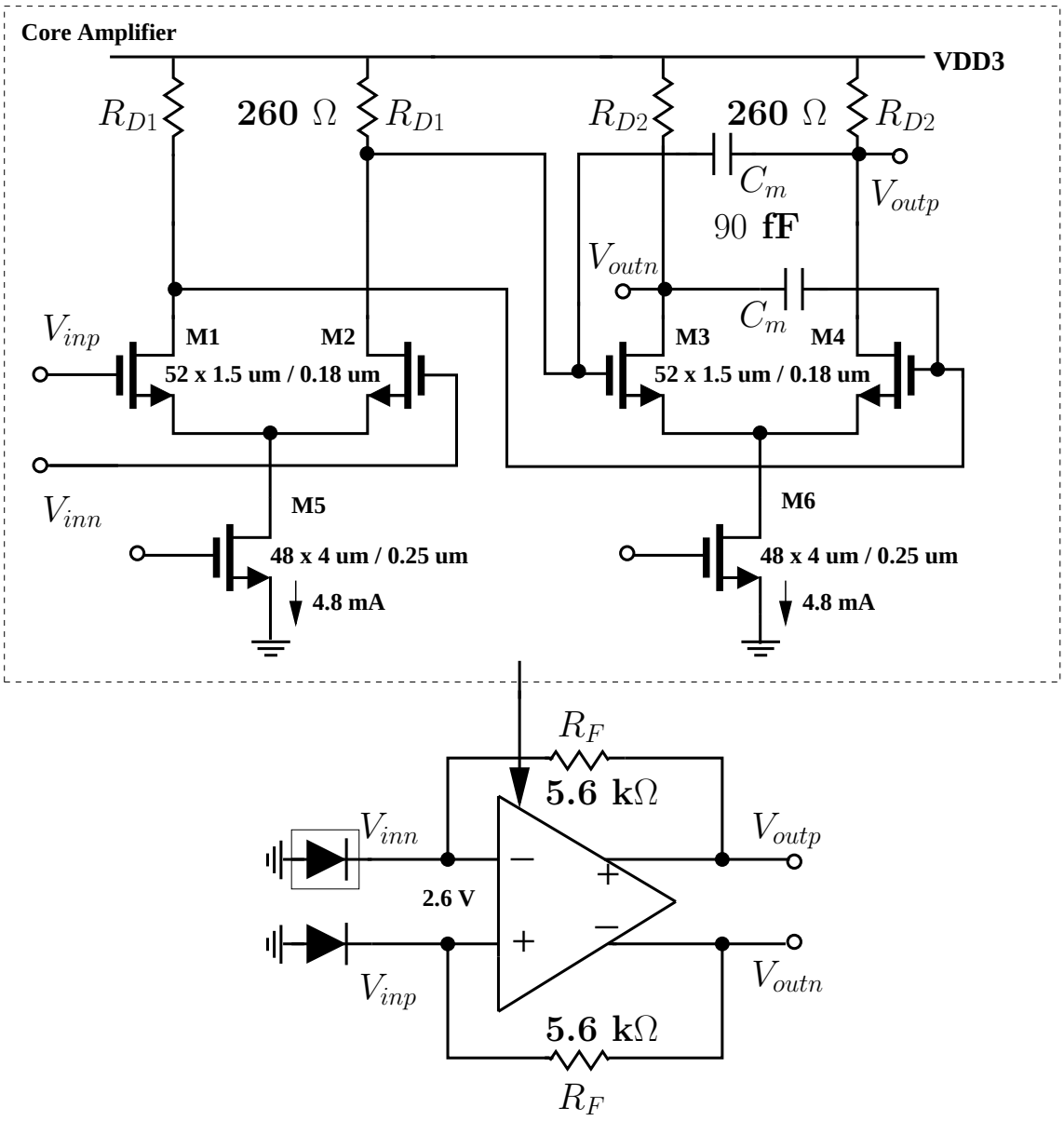


Figure 3.3: TIA: Schematic.

Table 3.1: Performance comparison of different values of C_m.

C_m **(fF)**	**0**	**90**	**150**
DC gain (dB)	74.6	74.6	74.6
Bandwdith (GHz)	2.0	2.9	3.3
Peaking (dB)	0.48	0.18	10.38
PM (degrees)	59	64	34

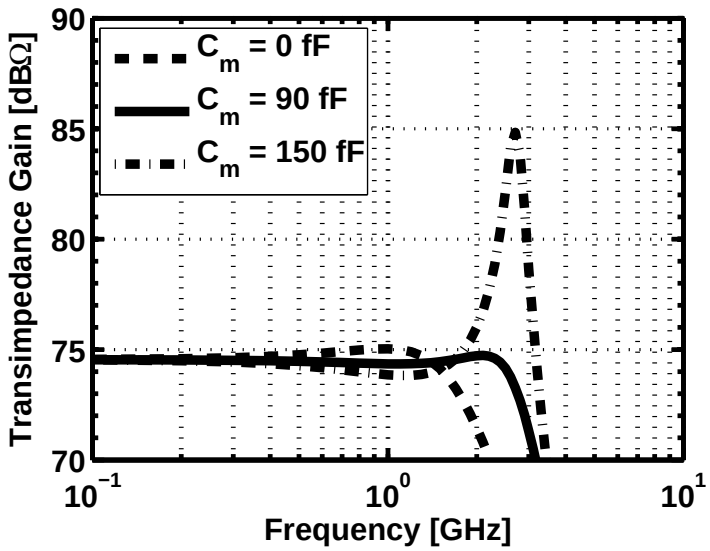


Figure 3.4: TIA: Frequency response with different values of C_m.

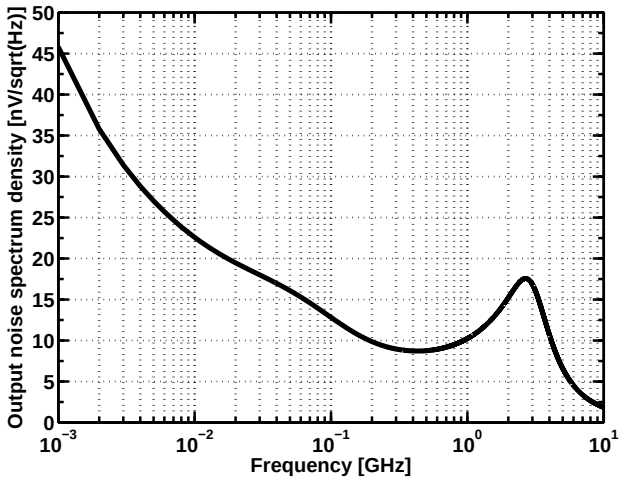
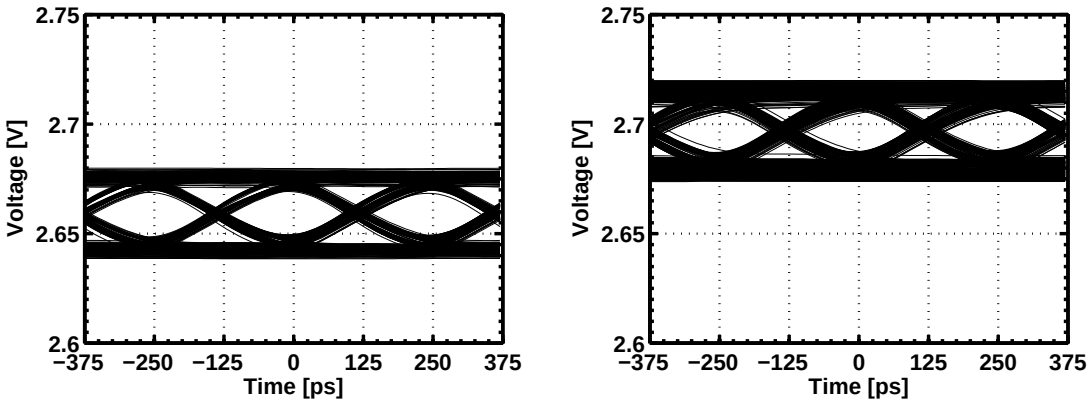


Figure 3.5: TIA: Output noise spectrum density.

Table 3.2: TIA simulation summary.

Corner	**TT/60°C**	**SS/100°C**	**FF/20°C**
DC gain (dBΩ)	74.6	74.5	74.6
Bandwidth (GHz)	2.9	2.5	3.5
Peaking (dB)	0.18	0	0.76
PM (degree)	64	68	62
Input-referred noise current (uA_{rms})	0.19	0.17	0.20



(a) (b)

Figure 3.6: TIA: Eye diagram at 4 Gbps at the (a) positive output terminal and (b) negative output terminal.

3.3. Subtracter

A subtracter was added to ensure the proper cancellation of the slow diffusive carriers by improving the common-mode rejection since that from the TIA is insufficient. AC coupling was used so that a new input common-mode could be set to comply with the 1.8 V supply. The different output common-modes at both terminals are also re-aligned through an external bias, V_b. Lastly, the subtracter provides DC gain which is particularly important since some DC gain is lost by the equalizer; consequently, the input-referred noise of all subsequent stages is kept small compared to that of the TIA.

3.3.1. Specifications

Bandwidth

The bandwidth of the subtracter was targeted to be greater than 10 GHz so that it does not limit overall bandwidth.

3.3.2. Design

The schematic of subtracter is shown in Figure 3.7. In order to achieve a higher GBW, the implementation of the gain cell is based on the Cherry-Hooper amplifier with active feedback. The transfer function of this amplifier is [25]:

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_{vo}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{3.8}$$

where

$$A_{vo} = \frac{g_{m1}g_{m3}R_{D1}R_{D2}}{1 + g_{m3}g_{m5}R_{D1}R_{D2}}, \tag{3.9}$$

$$\zeta = \frac{1}{2}\frac{R_{D1}C_{L1} + R_{D2}C_{L2}}{\sqrt[2]{R_{D1}R_{D2}C_{L1}C_{L2}(1 + g_{m5}g_{m3}R_{D1}R_{D2})}}, \tag{3.10}$$

$$\omega_n^2 = \frac{1 + g_{m5}g_{m3}R_{D1}R_{D2}}{R_{D1}R_{D2}C_{L1}C_{L2}}. \tag{3.11}$$

In the above equations, C_{L1} and C_{L2} represent the load capacitance at the internal and output node respectively, while g_{m1}, g_{m3}, and g_{m5} denote the small-signal transconductance of $M1$, $M3$, and $M5$ respectively. As seen from equation (3.9), to achieve high gain, g_{m5} must be small and g_{m1} must be large. g_{m3} must also be large to sup-

port a high bandwidth according to equation (3.11). These goals were achieved with appropriate bias currents and device sizes. A nominal value of $\zeta \leq \sqrt{2}/2$ was chosen so that a high bandwidth could be achieved without causing peaking.

The schematic of the AC coupling channel is shown in Figure 3.8. The values of R_{AC} and C_{AC} were chosen so that the cutoff frequency is small enough to pass the lower frequency content in the $2^{31} - 1$ pattern. To reduce the load on TIA, a combination of lower C_{AC} and higher R_{AC} were used.

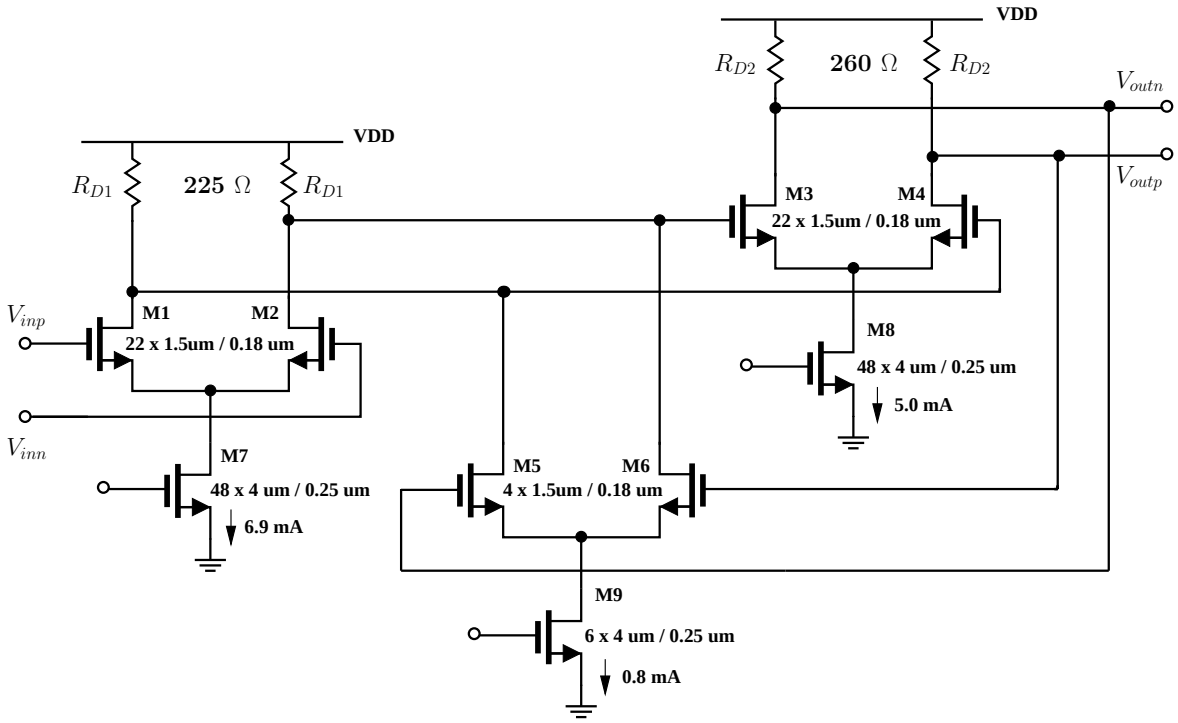


Figure 3.7: Subtracter: Schematic.

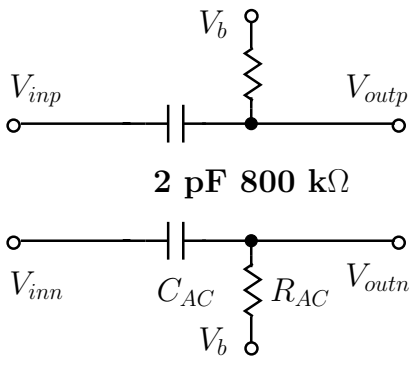


Figure 3.8: AC coupling: Schematic.

Table 3.3: Subtracter simulation summary.

Corner	**TT/60°C**	**SS/100°C**	**FF/20°C**
DC gain (dB)	10.0	8.4	11.0
Bandwdith (GHz)	12.4	10.3	14.7
GBW (GHz)	39	27	52

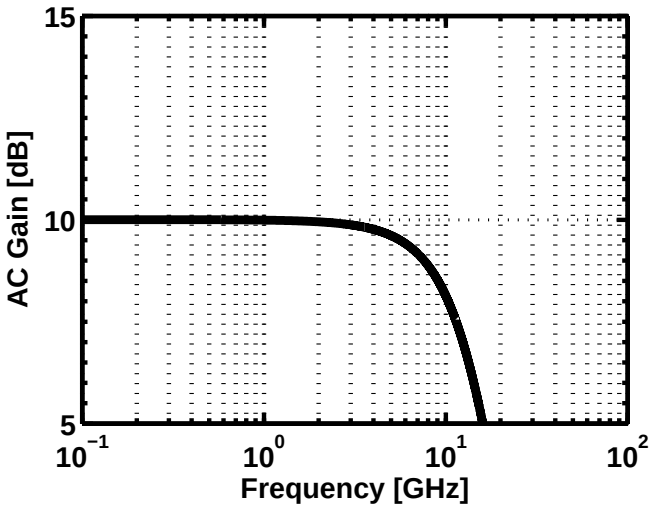


Figure 3.9: Subtracter: Frequency response.

3.3.3. Simulation Results

The frequency response of the subtracter is shown in Figure 3.9. A DC gain of 10 dB and a bandwidth of 12.4 GHz were achieved. A summary of the simulation results at different corners is shown in Table 3.3.

The frequency response of the AC coupling channel is also shown in Figure 3.10 and the cutoff frequency is 100 kHz.

3.4. Equalizer

While the SML topology acts as a built-in equalizer within the monolithically integrated photodetector, the data rate using this approach done has been limited to only 2 Gbps [14]. The purpose of the equalizer was to further remove the remaining ISI so that a higher data rate could be achieved.

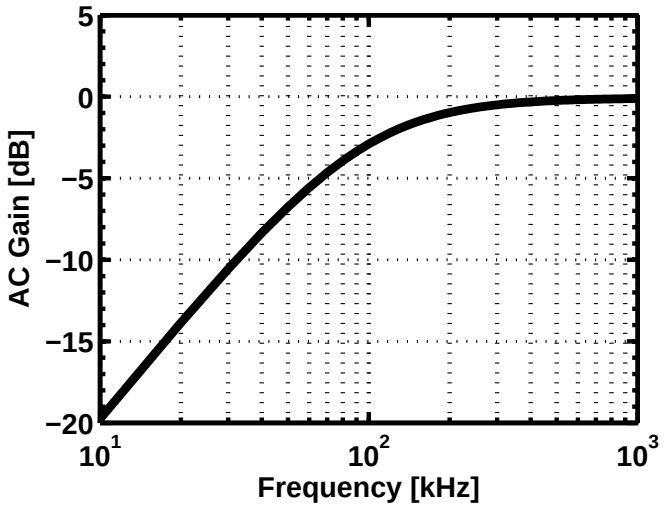


Figure 3.10: AC coupling: Frequency response.

3.4.1. Specifications

Peaking

Based on the results of the system-level simulations in Section 2.3, 4 dB was required from the equalizer. Although intended as a fixed (not adaptive) equalizer, in this prototype some tunable boost was designed to account for any inaccuracy in the modeling of the photodetector or preceding circuits.

DC gain

As the minimum DC gain of the subtracter was 8 dB, a minimum DC gain of -8 dB was sought from the equalizer so that the contribution of the two maintains at least the same signal level at the TIA output.

3.4.2. Design

The schematic of the equalizer is shown in Figure 3.11. It consists of a capacitive degeneration to provide a zero in the small-signal transfer function. Triode device, M3, and the MOS varactors, M4 and M5, were used to adjust the values of the degeneration resistance and capacitance respectively in order to provide fine-tuning. The transfer function can be expressed as [22].

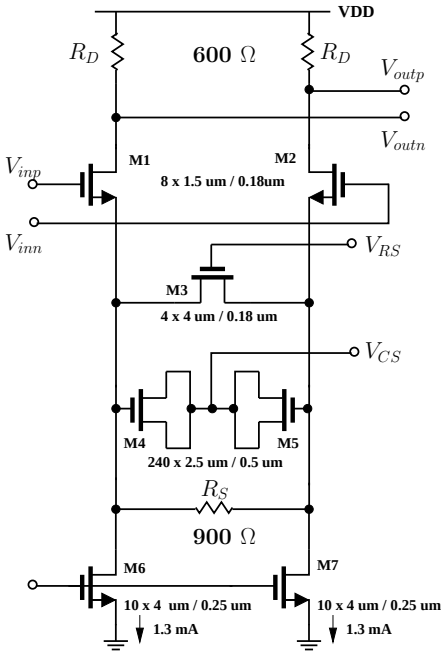


Figure 3.11: Equalizer: Schematic.

$$\frac{V_{out}}{V_{in}}(s) = E_0 \cdot \frac{1 + \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}. \tag{3.12}$$

where E_0, ω_z, ω_{p1}, and ω_{p2} denote the DC gain, the zero, and the two poles of the equalizer which can be expressed as follows:

$$E_0 = \frac{g_{m1} R_D}{1 + \frac{g_{m1} R_S}{2}}, \tag{3.13}$$

where g_{m1} is the transconductance of $M1$,

$$\omega_z = \frac{1}{R_S C_S}, \tag{3.14}$$

$$\omega_{p1} = \frac{1 + \frac{g_{m1} R_S}{2}}{R_S C_S}, \tag{3.15}$$

$$\omega_{p2} = \frac{1}{R_D C_L}. \tag{3.16}$$

The maximum amount of boost is provided when M3 is turned off. As M3 turns on, the amount of boost compared to the DC gain is reduced as the effective source resistance is lower which in turn leads to a higher DC gain. The MOS varactors were implemented in the accumulation mode by placing NMOS transistors inside an n-well.

Table 3.4: Equalizer simulation summary.

Corner	**TT/60°C**	**SS/100°C**	**FF/20°C**
DC gain (dB)	-0.2 to 7.1	-0.1 to 5.0	-0.4 to 8.5
Peaking range (GHz)	2.0 to 3.3	2.1 to 3.2	2.2 to 3.4

A wider tuning range can be achieved by tuning the gate-source voltage of the varactors.

3.4.3. Simulation Results

The frequency response while varying V_{RS} and V_{CS} are shown in Figure 3.12(a) and Figure 3.12(b) respectively. Transient simulation was used to verify the performance of the equalizer by comparing the eye diagrams before and after the equalizer at 4 Gbps as shown in Figure 3.13(a) and Figure 3.13(b) respectively. A portion of a $2^{31}-1$ PRBS pattern including 31 CID was used, and the qualizer was tuned to its optimal setting with $V_{CS} = 1.2$ V and $V_{RS} = 0.8$ V. The pattern dependent jitter was reduced from 36.6 ps to 9.9 ps. A summary of the simulation results in different corners is shown in Table 3.4.

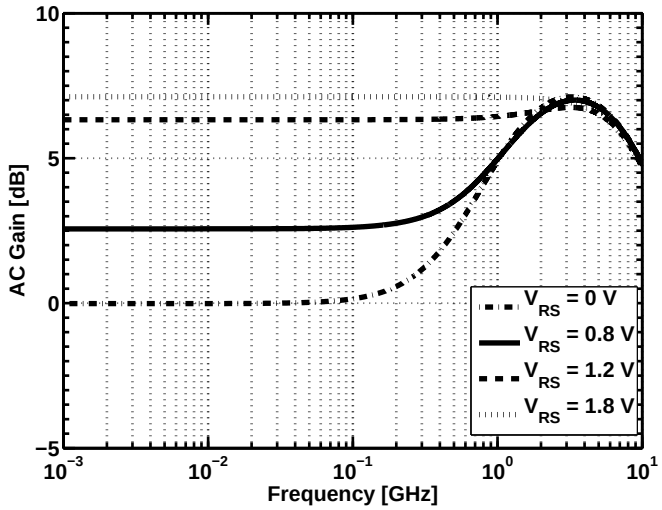
3.5. Post Amplifier

The purpose of the PA is to enlarge the signal swing to ensure the correction functionality of subsequent blocks. As linearity is only important up to the equalizer, an LA was used to amplify the signal without a gain-control mechanism.

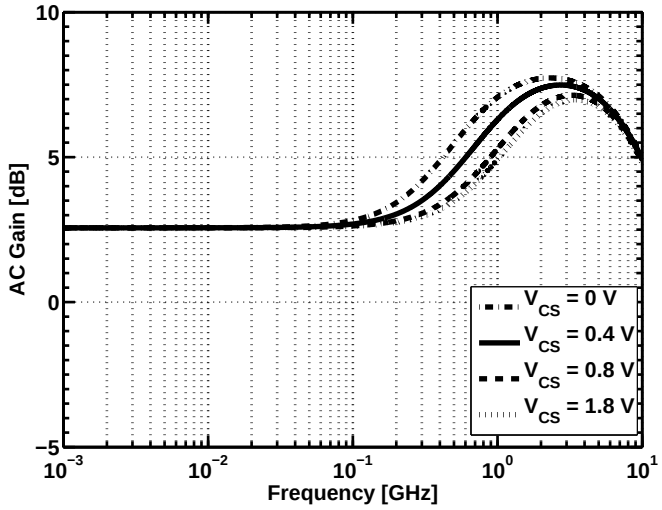
3.5.1. Specifications

Gain

With a minimum expected received average optical power of -12 dBm from the VCSEL source, a large extinction ratio, a photodiode responsivity of 0.03 A/W, and a combined gain of approximately 80 dBΩ from TIA to the equalizer, LA would sense an input signal of 38 mV. The gain of the LA was targeted to be at least 30 dB to provide enough swing.



(a)



(b)

Figure 3.12: Equalizer: Frequency response while (a) varying V_{RS} for $V_{CS} = 1.2\ V$ and (b) varying V_{CS} for $V_{RS} = 0.8\ V$.

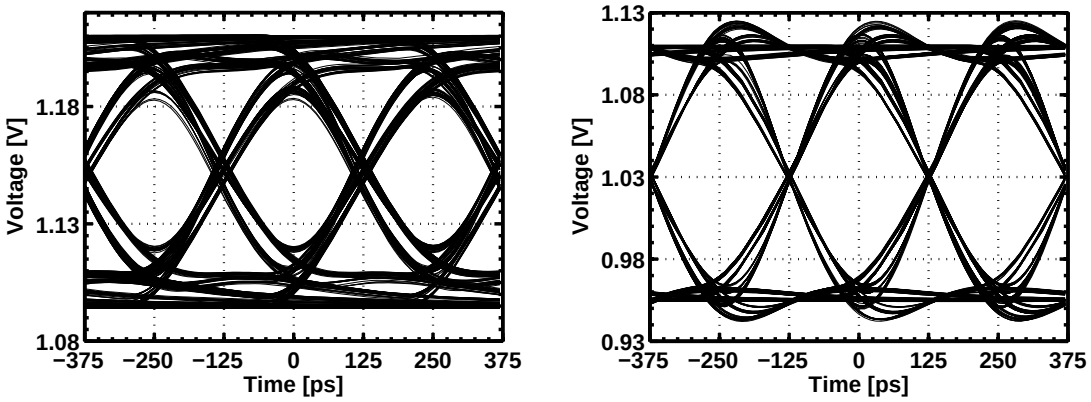


Figure 3.13: Equalizer: Eye diagram at 4 Gbps (a) before and (b) after the equalizer with $V_{CS} = 1.2$ V and $V_{RS} = 0.8$ V.

Bandwidth

The bandwidth of the LA is designed to be larger than the TIA bandwidth such that it does not limit the overall performance. A common approach is to target a bandwidth equal to the data rate [23]. However, this is based on a small-signal approximation which becomes less valid as the amplitude increases. Hence, while the bandwidth of the first few stages must be close to the data rate, the bandwidth of the entire LA can be slightly relaxed.

Noise

The majority of the noise in the receiver is attributed to the TIA; however, the noise generated by the LA also adds to the total noise and degrades the overall sensitivity of the receiver. As the number of stages reduces, the gain per stage becomes large which makes the noise contributed by all of the stages less significant. As a result, the number of stages for a high-gain LA is usually limited to less than 5 stages [23].

Offset Voltage

Due to the large gain of the LA, even a small input offset voltage may saturate the latter stages. Thus, offset cancellation must be incorporated into the LA.

3.5.2. Design

The block digram of the LA is shown in Figure 3.14. It consists of 4 identical gain cells to provide the necessary gain, an input stage that performs offset cancellation, and an offset cancellation network to low-pass filter the output and sense any DC offset. Each gain cell was implemented using the same topology as the one in the subtracter but with different biasing as shown in Figure 3.15.

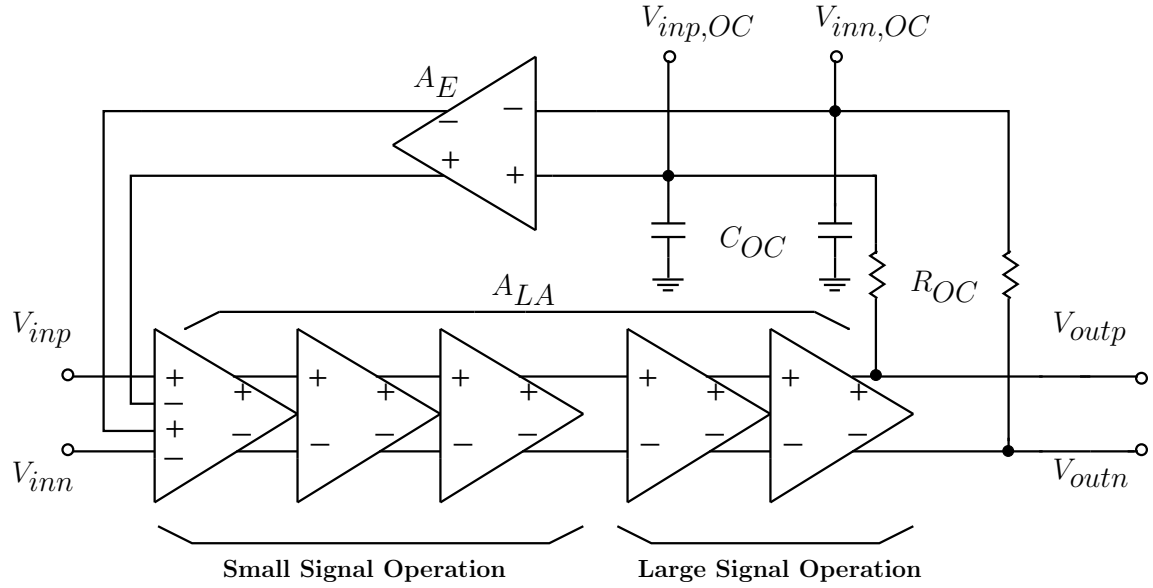


Figure 3.14: LA: Block diagram.

Although a greater overall GBW can be achieved with a higher number of stages, power increases and noise performance degrades as the gain per stage drops. Since the bandwidth requirement is less than one tenth of the nMOS devices' peak f_T, 4 stages were sufficient.

The schematic of the input stage of the LA is shown in Figure 3.16 which consists of two differential inputs. one input passes the data through the chain of gain cells with a total gain of A_{LA}, and the other input takes the DC signal fed back from the offset cancellation network through an error amplifier with voltage gain, A_E.

The cutoff frequency, f_C, of the offset cancellation network is given as

$$f_C = \frac{A_{LA}A_E + 1}{2\pi \cdot R_{OC}C_{OC}}. \tag{3.17}$$

f_C must be low enough to reduce baseline wander and data-dependent jitter. Since $A_{LA}A_E$ is large, $R_{OC}C_{OC}$ must also be large, and were implemented using high-ohmic resistors and MOS capacitors to achieve 11 MΩ and 70 pF respectively.

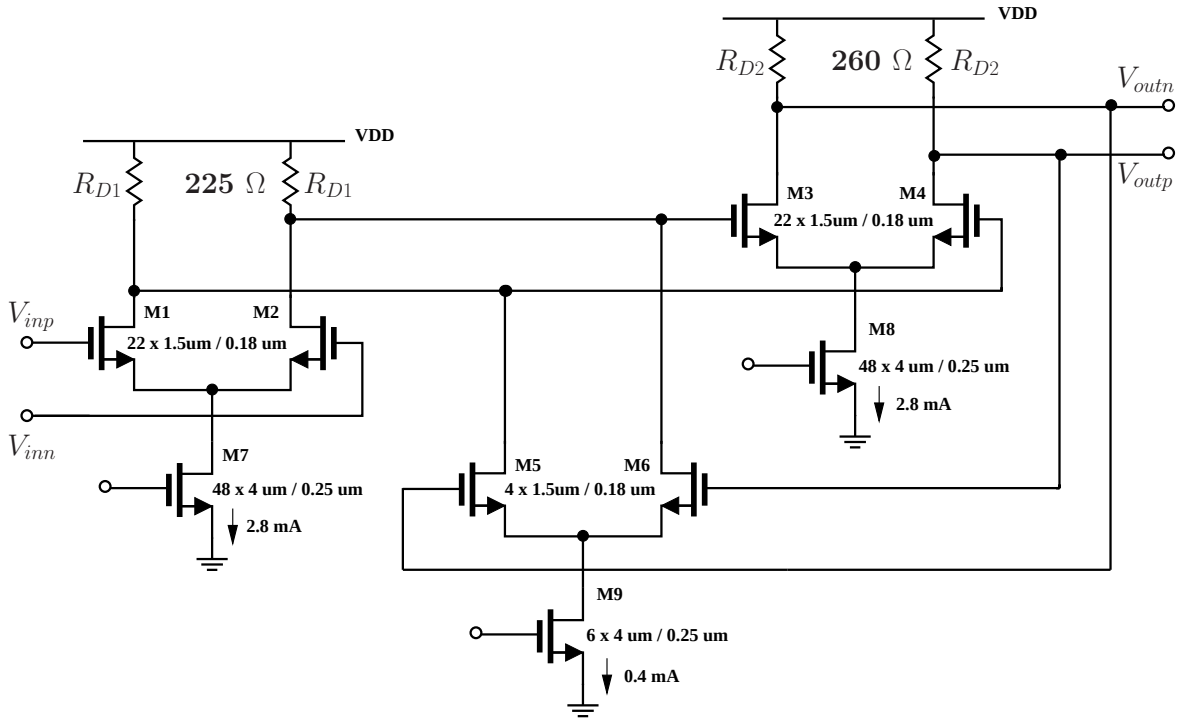


Figure 3.15: LA: Gain cell schematic.

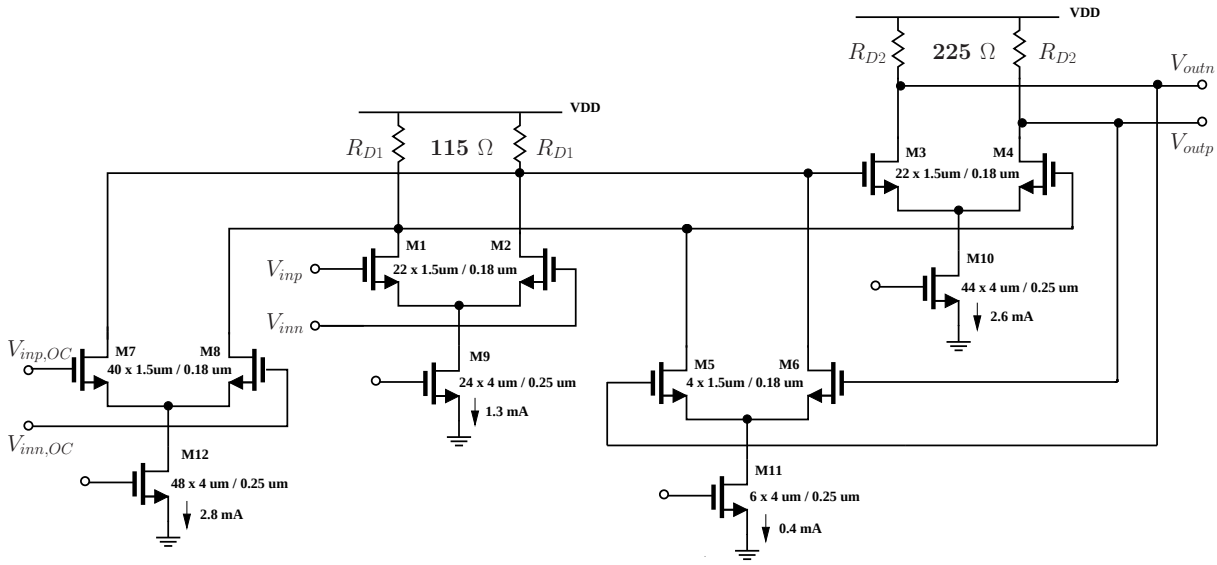


Figure 3.16: LA: Input stage schematic.

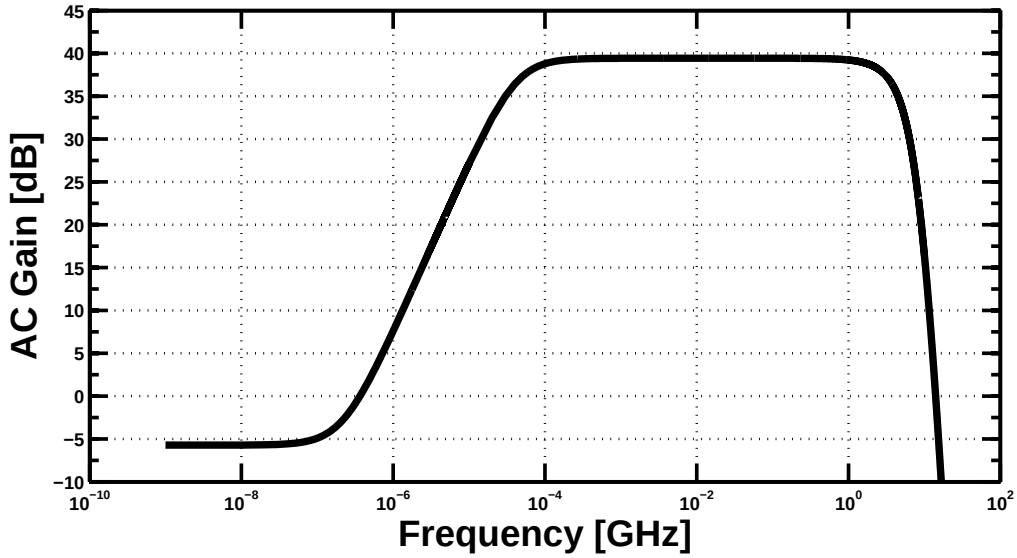


Figure 3.17: LA: Frequency response.

Table 3.5: LA simulation summary.

Corner	**TT/60°C**	**SS/100°C**	**FF/20°C**
DC gain (dB)	39	31	46
Small signal Bandwdith (GHz)	4.7	4.0	6.0
Overall Bandwdith (GHz)	3.7	3.2	4.5
GBW (GHz)	352	110	862

3.5.3. Simulation Results

The frequency response of the LA is shown in Figure 3.17. A DC gain of 39 dB was achieved. The small signal bandwidth simulated from the input stage of the LA up to end of the second gain cell and was at 4.7 GHz beyond which the signal will normally saturate the remaining stages. A summary of the simulation results in different corners is shown in Table 3.5. The cutoff frequency, f_C, was 40 kHz.

3.6. Output Buffer

In order to facilitate the measurement in the 50 Ω testing environment, an output buffer with 50 Ω on chip termination was used to provide matching while delivering an appropriate signal swing to the oscilloscope.

3.6.1. Specifications

Bandwidth

As the signal goes through the PA, it has such a high amplitude at the input of the output buffer that the small-signal bandwidth becomes inapplicable. However, the small-signal bandwidth can be used as a conservative lower limit, and a target of 5 GHz was established assuming a 400 fF output load which models the pad and package parasitic capacitances.

Swing

A swing of 200 mV_{pp} per side is targeted for the doubly-terminated 50 Ω (25 Ω effective) output load.

3.6.2. Design

To deliver a swing of 200 mV_{pp} per side to an effective load of 25 Ω, the buffer must steer a total current of 8 mA. Hence, the transistors need to be sized large enough to ensure the driving capability. As a result, the input capacitance of the differential pair presents a significant load to the last stage of the LA and can reduce its overall bandwidth. A f_T doubler was used to halve the effective input capacitance [23]. The schematic of the output buffer is shown in Figure 3.18. A differential pair with half of the transistor width (20 x 1.5 um / 0.18 um) also achieves the same input capacitance to the first order; however, this would lead to a lower voltage head room for the tail transistor compared to M5 and M6 if the same total current (8.4 mA) were supplied. Therefore, the differential pair was not used to implement the output buffer.

3.6.3. Simulation Results

A small-signal bandwidth of 5.4 GHz was achieved as shown by the frequency response of the output buffer in Figure 3.19. A summary of the simulation results in different corners is shown in Table 3.6.

3.7. Complete Optical Receiver

The complete optical receiver operated under two power supplies. The supply of the TIA was 3.3 V in order to provide a large reverse-bias voltage for the photodetector while the supply of the remaining blocks was 1.8 V. The overall frequency response is

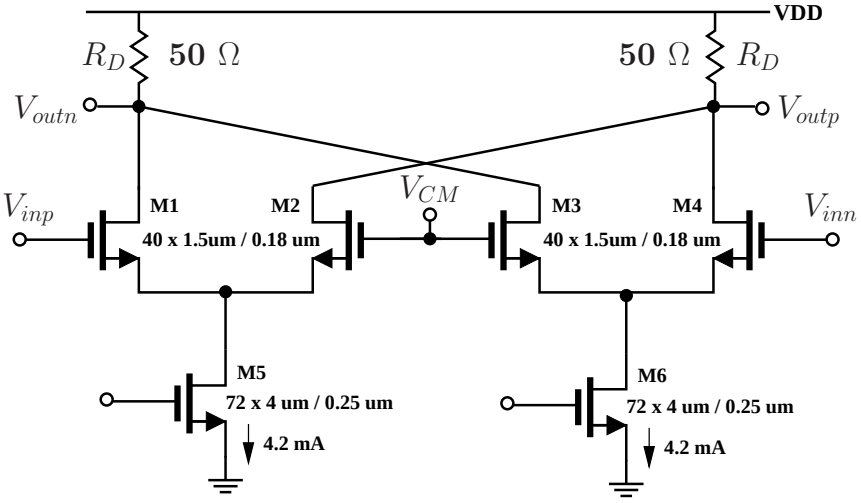


Figure 3.18: Output buffer: Schematic.

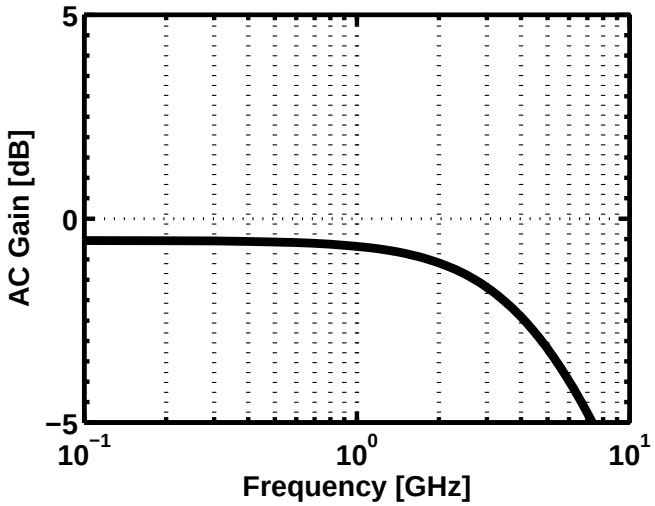


Figure 3.19: Output buffer: Frequency response.

Table 3.6: Output buffer simulation summary.

Corner	**TT/60°C**	**SS/100°C**	**FF/20°C**
Bandwdith (GHz)	5.4	5.3	5.6
Swing (mV)	200	200	200

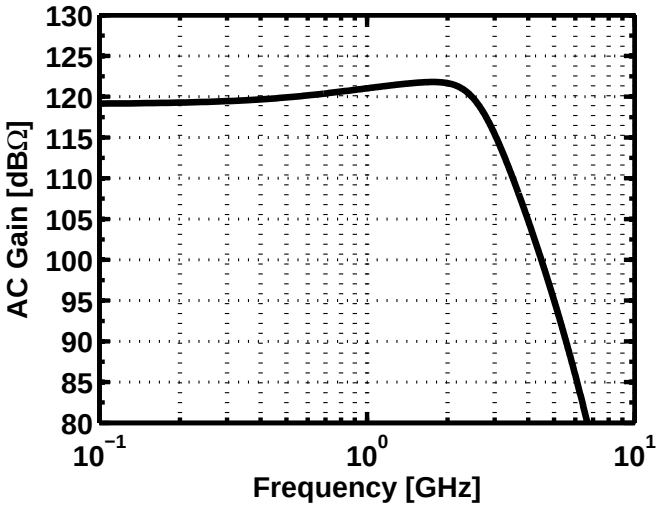


Figure 3.20: Complete optical receiver: Frequency response.

Table 3.7: Simulated power consumption break down.

Block	**Power (mW)**
TIA	32
Subtracter	23
Equalizer	5
LA	55
Output buffer	14
Biasing circuit	16
Total	**145**

shown in Figure 3.20 with the optimal equalizer setting at $V_{CS} = 1.2$ V and $V_{RS} = 0.8$ V. The overall small-signal transimpedance gain from TIA to output buffer was 119 dBΩ with an effective load of 25 Ω. The amount of boost at 2 GHz is 2.7 dB. The output buffer delivered a swing of 200 $\mathrm{mV_{pp}}$ per side to an effective load of 25 Ω at the output. The power consumption break down is summarized in Table 3.7. All targeted specifications of each block have been met in SS/100°C, TT/60°C, and FF/20°C corners. Measurement results will be presented in Chapter 4.

Chapter 4

Layout and Measurements

This chapter presents the circuit layout and measurement results of the optical receiver front-end. The test-chip was fabricated in 0.18-μm CMOS technology with 6 metal layers and deep n-well option. Section 4.1 describes the circuit layout and section 4.2 addresses the measurement results.

4.1. Circuit Layout

The die was packaged with Quad Flat No leads (QFN). The total chip area is 2.8 x 1.5 = 4.2 mm^2 as shown in Figure 4.1. Shown in Figure 4.2 is the core area of the chip which occupies 0.86 x 0.84 = 0.72 mm^2, and consists of the photodetector described in section 2.1 attached to the optical receiver front-end presented in chapter 3. The die includes a duplicate of the electrical receiver with the photodetector removed so that an electrical test can be performed to verify the functionality of the electrical circuit blocks. A stand-alone photodetector (including both the exposed and covered photodiodes) with the same dimension as the one attached to the TIA of the optical receiver front-end was also included as a test feature for DC responsivity measurements.

4.2. Measurements

The packaged chip was mounted on a Printed Circuit Board (PCB) for testing as shown in Figure 4.3. Commercial voltage regulators and potentiometers were used to generate the supply voltages and provide proper biasing for the transistors on chip. This section describes the test setup and experimental results for an electrical test, a photodetector responsivity test, and an optical test with BER measurements.

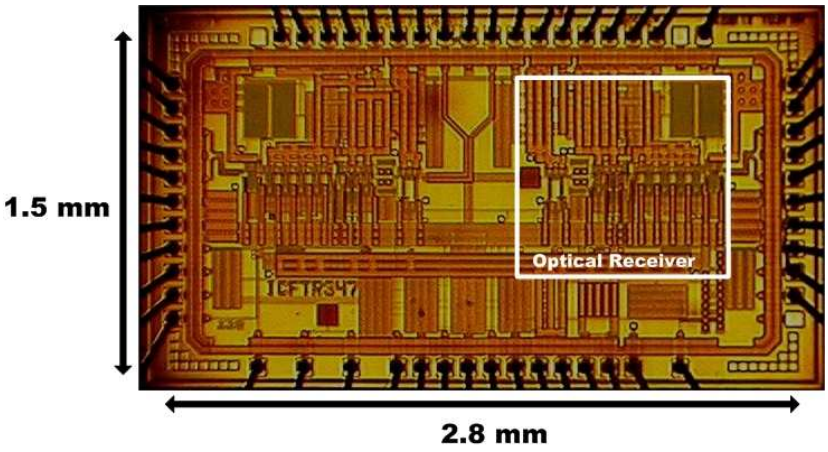


Figure 4.1: Die photo of the chip with the optical receiver highlighted.

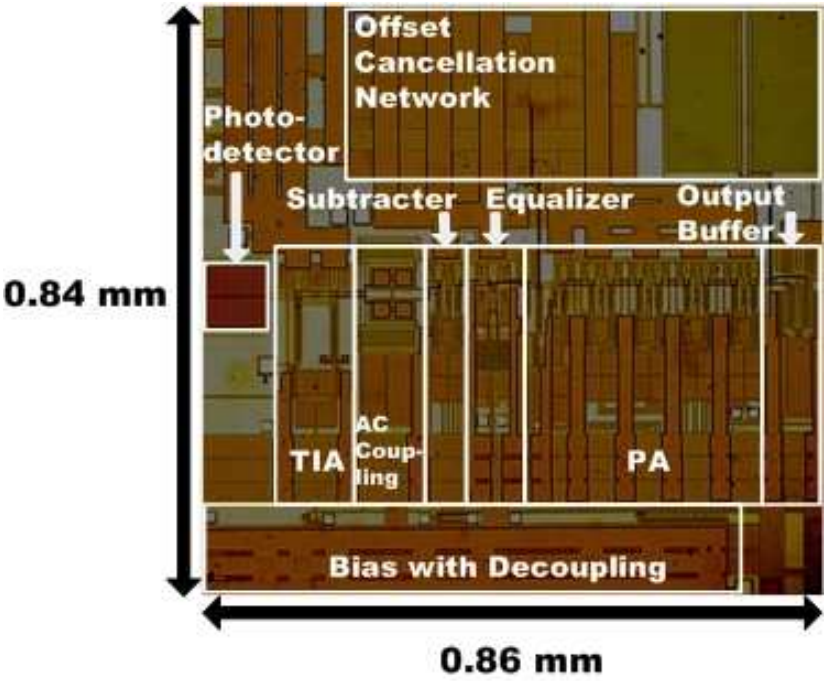


Figure 4.2: Die photo of the optical receiver.

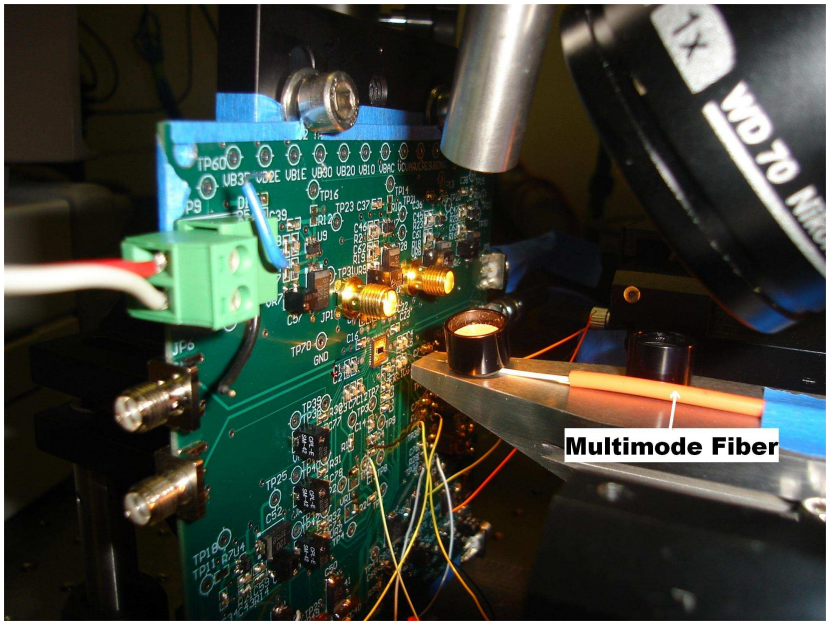


Figure 4.3: PCB.

4.2.1. Electrical Test

The electrical test setup is shown in Figure 4.4. A pattern generator (MP1701A) was used to generate the PRBS signal to the input of the TIA to verify the functionality of the electrical circuit blocks. The measured output eye diagram at 5 Gbps using $2^{31}-1$ PRBS pattern with an input swing of 8 mV_{pp} is shown in Figure 4.5. As the data rate exceeds 5 Gbps, both the horizontal and vertical eye opening reduce sharply even with a larger input amplitude. As a result, 5-Gbps represents an upper limit on the achievable data rate in a complete optical test including the photodetector.

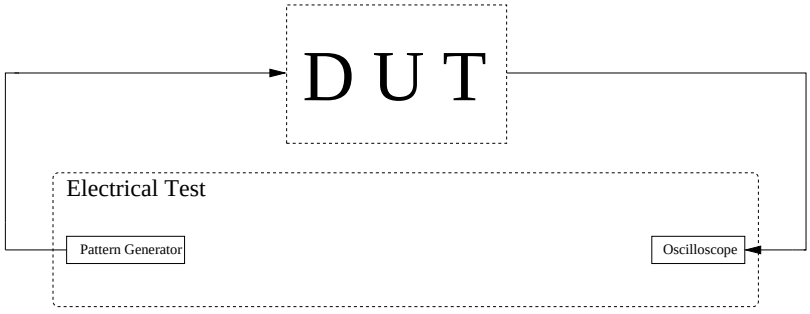


Figure 4.4: Electrical test setup.

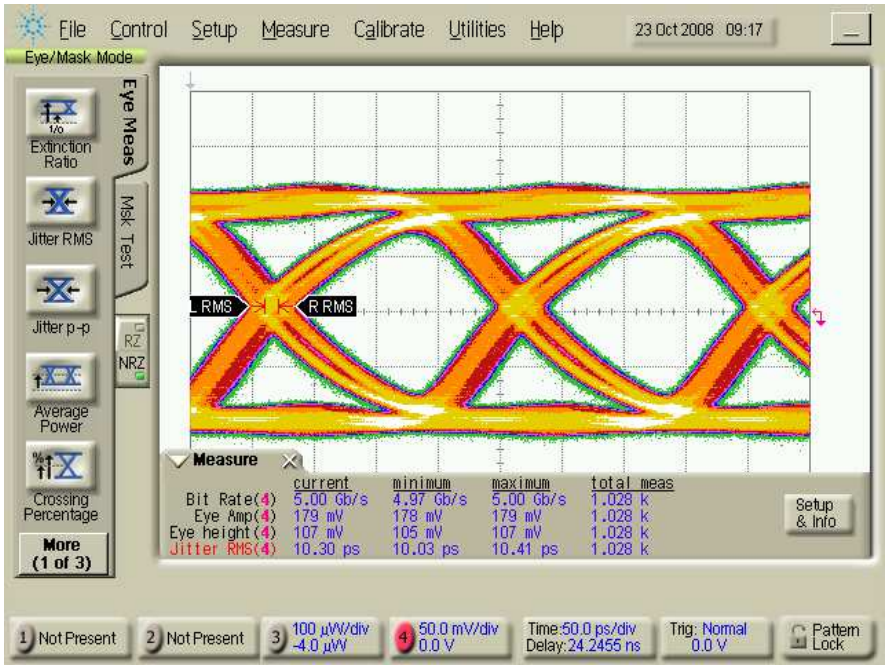


Figure 4.5: Measured eye diagram at 5 Gbps using $2^{31}-1$ PRBS pattern with an input swing of 8 mV_{pp}.

4.2.2. Photodetector Responsivity Test

The photodetector responsivity test setup is shown in Figure 4.6. The photodetector occupies a total area of 75 um × 75 um. A 50/125um multi-mode fiber was used to couple the optical power emitted from a 850-nm VCSEL source (HFE4192-582) to the on-chip photodetector. A power meter (Noyes OPM4) and a multimeter (Keithley 2400) were used to measure the input optical power and the output current in order to determine the DC responsivity of the photodetector. With an input power of -3 dBm or equivalently 500 uW, the currents coming from both exposed and covered photodiodes were 68.4 uA and 42.5 uA respectively when the reverse-bias voltage was set to 2 V. This leads to a net responsivity of 0.052 A/W. The net responsivity of the photodetector was also measured at other reverse-bias voltages, and the result is plotted in Figure 4.7.

4.2.3. Optical Test

The optical test setup is shown in Figure 4.8. The same pattern generator was used to modulate the VCSEL source through a high-speed VCSEL driver (MAX3795). A wideband oscilloscope (Agilent 86100B) was used to capture eye diagrams. In addition,

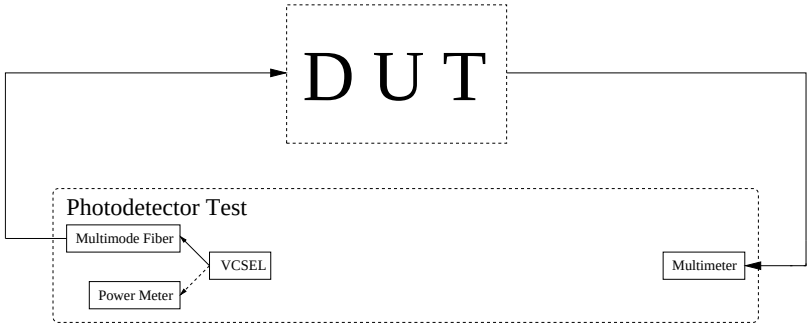


Figure 4.6: Photodetector responsivity test setup.

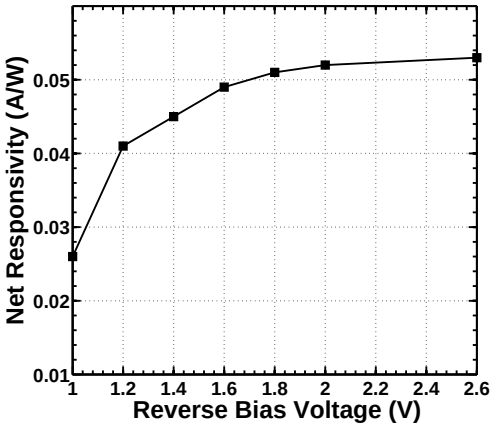


Figure 4.7: Net responsivity of the photodetector at different reverse bias voltages.

BER measurements were performed to determine the sensitivity of the optical receiver front-end. The BER measurement setup is shown in Figure 4.9. A BER tester (Anritsu MP1800A) was used to send patterns to modulate the VCSEL source.

The optical receiver front-end was operated in two modes which differ by the current consumption in the TIA. Hence, two sets of measurements were obtained. The first set of measurements corresponds to biasing the TIA with a total current consumption of 9 mA. This is referred to as the low-power (LP) mode. The second set of measurements corresponds to biasing the TIA with a higher total current consumption of 20 mA in order to increase its bandwidth so that a higher data rate can be achieved. This is referred to as the high-speed (HS) mode. A $2^{31}-1$ PRBS pattern was used to modulate the 850-nm VCSEL source for all eye diagram measurements. The equalizer shown in Figure 3.11 was fixed with $V_{RS} = 0\ V$ and $V_{CS} = 1.2\ V$ for all measurement points in both modes.

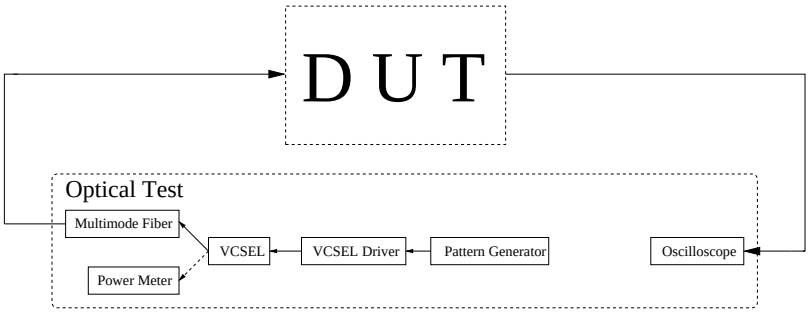


Figure 4.8: Optical test setup.

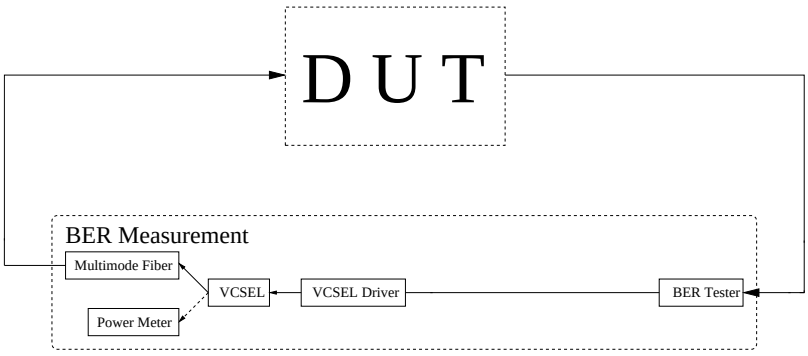
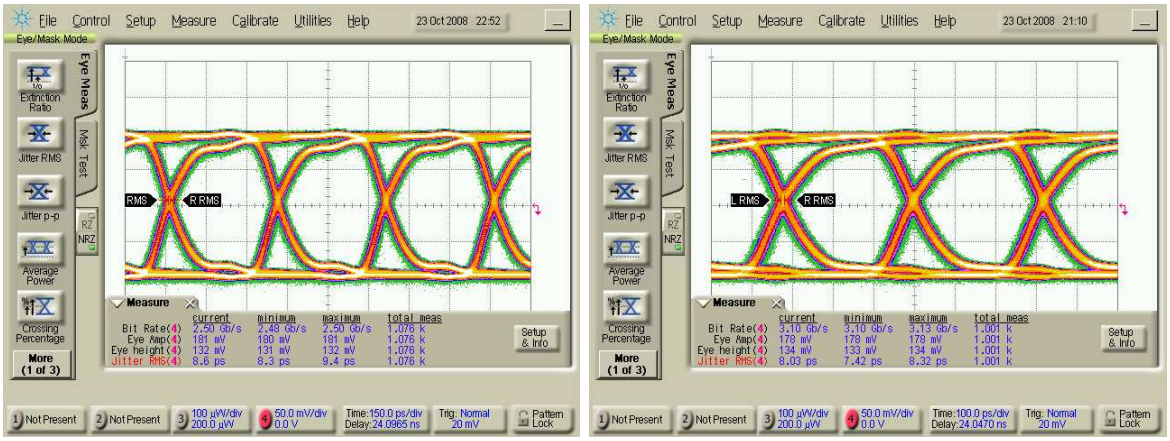


Figure 4.9: BER measurement setup.

Low Power Mode

Eye diagrams at 2.5 Gbps and 3.125 Gbps are shown in Figure 4.10(a) and Figure 4.10(b) for an average optical input power of -3 dBm. The highest data rate



(a) (b)

Figure 4.10: Measured eye diagrams for a $2^{31}-1$ PRBS pattern with an average optical input power of -3 dBm at (a) 2.5 Gbps and (b) 3.125 Gbps.

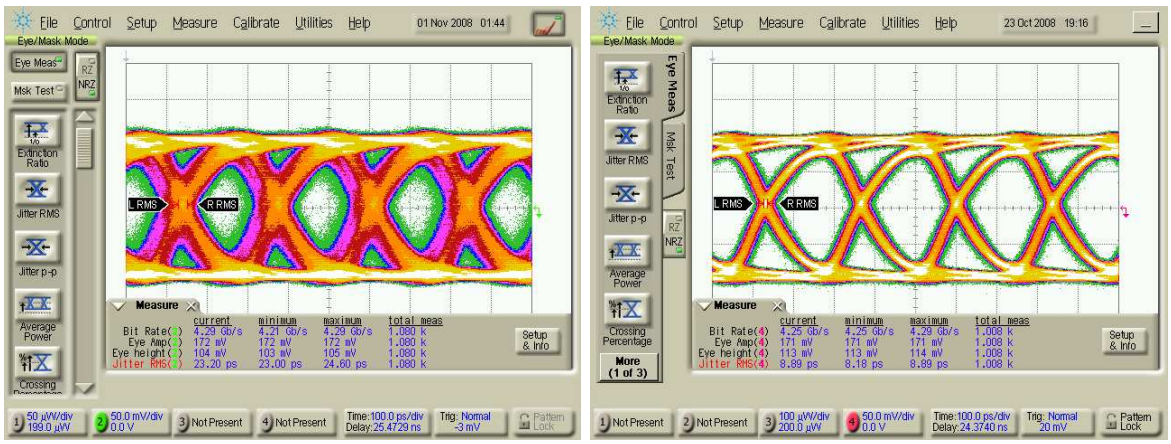
that can be achieved at a BER less than 10^{-12} with an average optical input power of -3 dBm in the LP mode is 4.25 Gbps. In order to verify the performance improvement provided by the equalizer, the boosting must be eliminated. This was achieved by pulling both V_{RS} and V_{CS} to 1.8 V. The eye diagrams with equalizer off and equalizer on are shown in Figure 4.11(a) and Figure 4.11(b) respectively. The measured BER as a function of average optical input power at different data rates is shown in Figure 4.12.

High-Speed Mode

With a higher current consumption in the TIA, the data rate was extended to 5 Gbps attributed to a larger TIA bandwidth. Shown in Figure 4.13(a) and Figure 4.13(b) are the eye diagrams with equalizer off and equalizer on for an average optical input power of -3 dBm. The boosting of the equalizer was deactivated using the same approach done in the LP mode. The measured BER as a function of average optical input power at different data rates is shown in Figure 4.14.

Comparison

The main measurement results of both LP mode and HS mode are summarized in Table 4.1. As shown in Figure 4.12, the highest date rate with BER less than 10^{-12} is 4.25 Gbps for the LP mode. It can also be observed that at 5 Gbps, the BER improves very little as average optical input power increases. Therefore, the BER at 5 Gbps is mainly limited by the bandwidth of the receiver rather than noise in the LP mode.



(a) (b)

Figure 4.11: Measured eye diagrams for at 4.25 Gbps for a $2^{31} - 1$ PRBS pattern with an average optical input power of -3 dBm with (a) equalization off and with (b) equalization on.

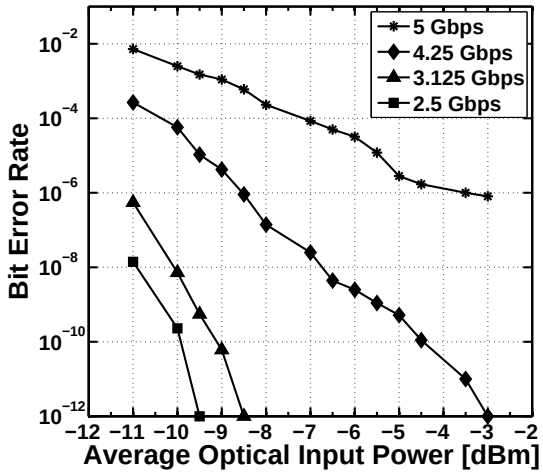
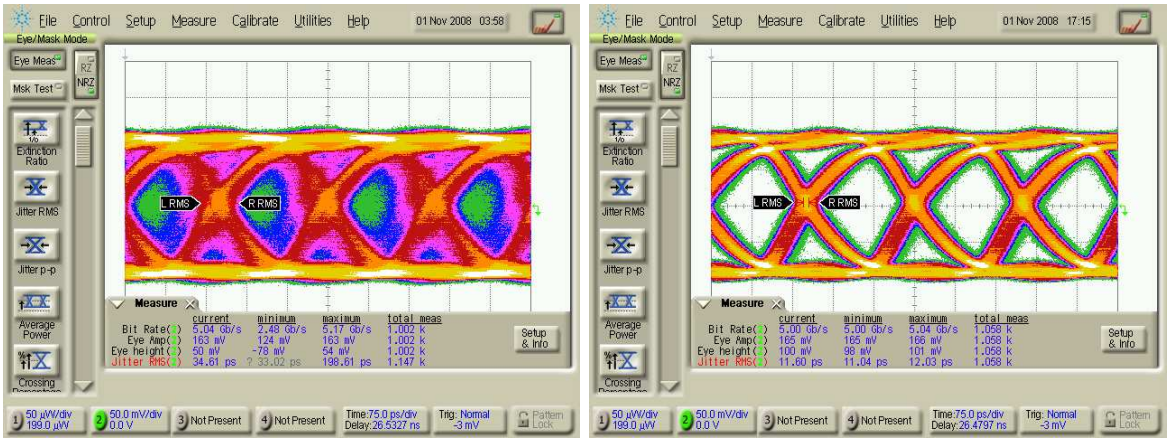


Figure 4.12: Measured BER as a function of average optical input power at different data rates under low power setting.



(a) (b)

Figure 4.13: Measured eye diagrams for at 5 Gbps for a $2^{31} - 1$ PRBS pattern with an average optical input power of -3 dBm with (a) equalization off and with (b) equalization on.

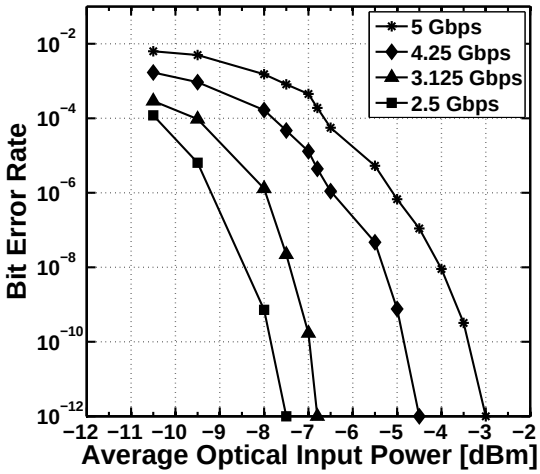


Figure 4.14: Measured BER as a function of average optical input power at different data rates under high speed setting.

Table 4.1: Main measurement results in low power mode and high speed mode.

	LP	**HS**
Technology	0.18-µm CMOS	
Supply voltages	3.3 V, 1.8 V	
Total chip area	1.5 x 2.8 = 4.2 mm^2	
Core area of optical receiver front-end	0.86 x 0.84 = 0.72 mm^2	
Optical wavelength	850 nm	
Average input power	-3 dBm	
Current Consumption in the TIA	9 mA	20 mA
Highest data rate with BER less than 10^{-12}	4.25 Gbps	5 Gbps
RMS jitter	8.89 ps	11.6 ps
Total power consumption with output buffer	144 mW	183 mW
Power consumption without output buffer	129 mW	168 mW

To alleviate the bandwidth problem, the current consumption of TIA is increased in the HS mode. As shown in Figure 4.14, at 5 Gbps significant improvement of BER is observed as average optical input power increases in the HS mode. Consequently, 5 Gbps operation was achieved with a BER of 10^{-12} at an average optical input power of -3 dBm. One can note that the sensitivity level for a BER less than 10^{-12} has become worse when switching to the HS mode for the lower data rates. This is because an increase in the TIA bandwidth leads to a higher total integrated noise. Therefore, while the HS mode is able to operate at higher data rates, the LP mode is preferred for data rates below 4.25 Gbps from both power consumption and sensitivity perspectives.

Chapter 5

Conclusion

5.1. Conclusion

The design of an optical receiver with monolithically integrated photodetector was investigated. Due to the low intrinsic bandwidth of the CMOS photodetector, a combination of a SML detector followed by an analog equalizer was used to extend the state-of-the-art data rate to 5 Gbps. To the authors' knowledge, it is the fastest photodetector integrated in a standard CMOS technology using standard supplies below 3.3 V. A low-noise TIA with high bandwidth and high transimpedance gain was also proposed. By employing negative Miller capacitance, the bandwidth of the TIA can be extended while keeping a flat frequency response. The measurement results of the optical receiver operating in two modes are compared with recently published photodetectors built in standard CMOS technology and operated with 850-nm optical light source in Table 5.1. The areas of all these photodetectors are approximately equal to 50 um $\times$ 50 um to comply with the core diameter of the multimode fiber. Among the references mentioned in Table 5.1, [11], [15], and [26] are the only ones that have an integrated TIA and PA together with the photodetector on chip. A more detailed comparison between these fully integrated optical receivers with this work is summarized in Table 5.2. Although 5 Gbps was reported in [12], it used a very high supply at 13.9 V to reverse-bias its photodiode through a bias-T. In addition, the authors failed to report the sensitivity at 5 Gbps. Moreover, since TIA and PA were not integrated on chip with the photodetector, an external TIA was used for testing. In conclusion, the optical receiver achieves a better sensitivity at 2.5 Gbps and 3.125 Gbps at a BER less than 10^{-12} compared to [11] and [15] in both LP and HS modes. When operating in the LP mode, the optical receiver accomplishes so with 4.3 dB improvement in sen-

Table 5.1: Photodetectors in standard CMOS technology

	Technology	Responsivity	Highest Supply	Data Rate
[4]	0.18-µm CMOS	-	1.8 V	3 Gbps
[11]	0.18-µm CMOS	-	6 V	2.5 Gbps
[12]	0.18-µm CMOS	0.38 A/W	13.9 V	5 Gbps
[13]	0.6-µm CMOS	0.1 A/W	5 V	250 Mbps
[15]	0.18-µm CMOS	0.07 A/W	3.3 V	3.125 Gbps
[26]	0.18-µm CMOS	0.03 A/W	1.8 V	1.2 Gbps
This work (LP)	0.18-µm CMOS	0.05 A/W	3.3 V	4.25 Gbps
This work (HS)	0.18-µm CMOS	0.05 A/W	3.3 V	5 Gbps

Table 5.2: Detailed comparison of fully integrated optical receivers including photodetector, TIA, and PA

	Power	Data Rate	Sensitivity	Area
[11]	138 mW	2.5 Gbps	-4.5 dBm	0.53 mm^2
[15]	175 mW	3.125 Gbps	-4.2 dBm	0.7 mm^2
[26]	250 mW	1.2 Gbps	-8 dBm	4.5 mm^2
This work (LP)	144 mW	2.5 Gbps	-9.5 dBm	0.72 mm^2
		3.125 Gbps	-8.5 dBm	
		4.25 Gbps	-3 dBm	
This work (HS)	183 mW	2.5 Gbps	-7.5 dBm	0.72 mm^2
		3.125 Gbps	-6.8 dBm	
		4.25 Gbps	-4.5 dBm	
		5 Gbps	-3 dBm	

sitivity and 18 % power reduction compared to [15]. The improvement in sensitivity justifies the design of the proposed low-noise TIA compared to the RGC stage used in [11] and [15]. With a maximum data rate of 5 Gbps, it is the only fully integrated optical receiver operating at speeds exceeding 3.125 Gbps.

5.2. Future Work

This thesis has demonstrated that equalization can be used to extend the data rate of monolithically integrated CMOS photodetectors. Due to the bandwidth limitation from the TIA, the highest data rate achieved was 5 Gbps under the HS mode. In terms

of future work, a high-bandwidth and low-noise TIA should be investigated so that the data rate can be further extended with reasonable power penalty.

Furthermore, the influence of technology scaling must be studied. As higher doping levels and lower supply voltages are used in newer technologies, the depletion region unavoidably decreases. This in turn leads to a simultaneous reduction of responsivity and intrinsic bandwidth of photodetectors; consequently, it poses serious design challenges.

Upon successful integration of a high bandwidth and high responsivity photodetector in standard CMOS technology, a low-cost fully integrated optical receiver can be realized.

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