All-Digital Calibration of Timing Mismatch Error in Time-Interleaved Analog-to-Digital Converters

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Outline

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Motivation

• For a time-interleaved ADC, timing skew mismatch degrades SNDR significantly at high frequencies.
Motivation

- Estimation & correction using mixed-signal approaches or purely digital approaches
- Digital Cal. is immune to PVT variations and doesn’t introduce additional jitter: analog variable delay line (VDL) is not required
- DSP cost (power, area) also decreases as technology scaling continues
Derivative-based Correction

- The amplitude error due to skew in $i^{th}$ subADC ($\Delta T_i$) can be expressed as a Taylor series expansion around the ideal sampling point.
- 1st term suggests correction can be done using a derivative estimate.

\[
\tilde{x}[n] = \sum_{k=1}^{\infty} \frac{1}{k!} \left(\frac{\Delta T_i}{T_s}\right)^k x^{(k)}[n]
\]

**Sampling in the $i^{th}$ Sub-ADC**
Derivative-based Correction

- Consider a 4-way TI-ADC, take sub-ADC1 as the reference channel and normalize timing mismatches to 

\[ r_{2-4} = (\Delta T_{2-4} - \Delta T_1)/T_s \]

- The SNDR with timing mismatches can be shown to be

\[
SNDR = \frac{1}{\frac{1}{6} \left( \frac{2}{2^B} \right)^2 + \frac{1}{4} \pi^2 \left[ (r_2 - r_3 + r_4)^2 + 2(r_2 - r_4)^2 + 2r_3^2 \right] \left( \frac{f_{in}}{f_s} \right)^2} \tag{9}
\]

- If skew is bounded by \([\Delta T_{\text{min}}, \Delta T_{\text{max}}]\), the worst SNDR in (9) arises when \(r_2 = r_4 = \pm r_{\text{max}}\) and \(r_3 = 0\), where \(r_{\text{max}} = (\Delta T_{\text{max}} - \Delta T_{\text{min}})/T_s\).

\[
SNDR_{\text{worst}} = \frac{1}{\frac{1}{6} \left( \frac{2}{2^B} \right)^2 + \pi^2 r_{\text{max}}^2 \left( \frac{f_{in}}{f_s} \right)^2} \tag{10}
\]
Derivative-based Correction

- With derivative-based skew correction, we can derive a similar expression

\[
SNR_{cal} = \begin{cases} 
\frac{1}{6\left(\frac{2}{2^B}\right)^2} + |A_1|^2 + |A_2|^2 + |A_3|^2, & f_{in} < \frac{f_s}{4} \\
\frac{1}{6\left(\frac{2}{2^B}\right)^2} + |B_1|^2 + |B_2|^2 + |B_3|^2, & f_{in} > \frac{f_s}{4}
\end{cases}
\]

\[
SNR_{cal, worst} = \frac{1}{\frac{1}{6\left(\frac{2}{2^B}\right)^2} + \frac{11}{16} \pi^4 r_{max}^4 \left(\frac{f_{in}}{f_s}\right)^4}
\]
Derivative-based Correction

• Comparison of worst-case expressions

\[ SNDR_{\text{worst}} = \frac{1}{\frac{1}{6} \left( \frac{2}{2^B} \right)^2 + \pi^2 r^2_{\text{max}} \left( \frac{f_{\text{in}}}{f_s} \right)^2} \]  

(10)

\[ SNDR_{\text{cal,worst}} = \frac{1}{\frac{1}{6} \left( \frac{2}{2^B} \right)^2 + \frac{11}{16} \pi^4 r^4_{\text{max}} \left( \frac{f_{\text{in}}}{f_s} \right)^4} \]  

(16)
If we budget 3dB degradation in SNDR at Nyquist frequency, the timing skew tolerance improves $\sim 76x$ for a 12-bit 4-way TI-ADC after correction.

1% of period
Difference-based Skew Estimation

- In order to estimate the skew $\Delta T_i$, difference-based approach is used [Wang, ESSCIRC 2014][Wei, JSSC 2014]
Difference-based Skew Estimation

• This **Timing Mismatch Estimator** is shown here in block diagram form, where the estimate can be updated via LMS

\[
\hat{e}_i = \left| \frac{1}{N} \sum_{k=1}^{N} (|\hat{x}_i[k] - \hat{x}_{ref1}[k]| - |\hat{x}_i[k] - \hat{x}_{ref2}[k]|) \right| \quad (17)
\]

\[
\hat{r}_i(n+1) = \hat{r}_i(n) - \mu \cdot \hat{e}_i[n] \cdot \frac{\text{sign}(\hat{e}_i[n] - \hat{e}_i[n-1])}{\text{sign}(\hat{r}_i[n] - \hat{r}_i[n-1])} \quad (24)
\]
Proposed All-Digital Calibration

- Estimation and correction can thus be done both in the digital domain.
- Filter is full-rate type III 33 tap FIR with cut-off frequency of $0.42f_s$. 

\[
\begin{align*}
\tilde{x}_i[n] & \quad Z^{-1} \\
\tilde{x}_M[n] & \quad Z^{-1} \\
\vdots & \quad \vdots \\
\tilde{x}_i'[n] & \quad Z^{-1} \\
\tilde{x}_M'[n] & \quad Z^{-1} \\
\end{align*}
\]
Proposed All-Digital Calibration

- Estimation strategy can also be extended to 4 channels by changing the channel in calibration & “reference channels” $x_{ref1}$ and $x_{ref2}$ iteratively.
Proposed All-Digital Calibration

- Overall 4 channel block diagram
Simulation Results

- Simulation for 4xTI 12b 2GS/s ADC, $\Delta T_{1-4} = [1\text{ps}, 4\text{ps}, 3\text{ps}, 2\text{ps}]$, $f_{in} = 0.41f_s$
- The estimator can accurately converge to $\Delta T_{2-4} - \Delta T_1$ with < 0.1% error
- Every iteration collects 4000 points and the timing estimation loop converges in about 20 iterations
Simulation Results

- Simulation for 4xTl 12b 2GS/s ADC, $\Delta T_{1-4} = [1\text{ps}, 4\text{ps}, 3\text{ps}, 2\text{ps}]$, $f_{in} = 0.41f_s$
- Behaviour matches theoretical expression over frequency until FIR bandwidth of $0.42f_s$
Simulation Results

- Calibration also verified with QPSK and multi-tone signal
- Background calibration is possible without restricting input to single tone

Before

After
Simulation Results

- Worst-case SNDR expressions are verified using 1000 Monte-Carlo simulations, where $\Delta T_{1\sim4}$ are iid Guassian with $\sigma = 1\text{ps}$
- Theoretical limit shown here for $[\Delta T_{\text{min}}, \Delta T_{\text{max}}] = [-3\sigma, 3\sigma]$
Measurement Results

- A commercial 12bit 3.6GS/s 2 channel TI-ADC [21] was also used to verify this work.
- An on-chip manual timing skew adjustment code (analog delay) is available to compare with this work.
Measurement Results

- Using the on-chip delay code, we see the estimation does not vary with input frequency as expected for a single-tone input at 1400MHz and 780MHz.
Measurement Results

• By varying the on-chip delay code, we converge the calibration for a single-tone input at 1400MHz, which improves SNDR for all delay range
Measurement Results

- The calibration is also verified for other input frequencies

\[ F_s = 3.6 \text{GS/s} \]
Comparison to Other Works

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<td>32K</td>
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\(^1\) for per sub-ADC channel  
\(^2\) for the correction and estimation of timing mismatch  
\(^3\) for the 12bit 3.6GS/s two-channel TI-ADC with a single-tone input at 1065MHz
Conclusion

- Derivative-based digital correction and digital adaptive timing mismatch estimation are combined to achieve accurate closed-loop timing mismatch estimation and effective distortion tone suppression.
- Explicit formulas (9), (10), (13) and (16) are also obtained accurately predicting SNDR and providing the bounds on the tolerable timing mismatch for four-channel TI-ADCs both before and after derivative-based digital correction, serving as useful guidelines for designers.
Acknowledgement

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References


[21] 12-Bit, Dual 1.6/1.8 GSPS or Single 3.2/3.6 GSPS ADC12D1800 Reference Board, Link: http://www.ti.com/tool/adc12d1800rb