Filtering ADCs for Wireless Receivers: A Survey

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***Abstract*—Analog to digital converters (ADC) are used in wireless receivers to process signals in the presence of blockers. These blockers, usually much larger than the signal itself, necessitate the use of a filter upfront to reduce the dynamic range requirement of the ADC. A filtering ADC can be created by placing both the filter and the ADC in a global feedback loop, with improvement in noise and power efficiency. This paper reviews and analyzes two design methodologies for analog filtering ADCs, where the filter response is defined by analog circuits. Then, a digital filtering ADC architecture is discussed that takes advantage of the programmability of digital circuits.**

I. Introduction

Low supply voltages and analog gain in nanoscale CMOS make the design of a wireless receiver (RX) very challenging. One of the most difficult requirements is to reject signals in adjacent bands (blockers) whose amplitude is much larger than the inband signal. Typically, the biggest blocker comes from a local transmitter (TX). For example, in the LTE standard TX leakage can be as high as -30dBm at the receiver front-end assuming a TX-RX isolation of 57dB and TX-antenna insertion loss of 2dB [1]. Additionally, one other blocker (or two in an IMD test) may be present as shown in Fig. 1.

Traditionally, an analog low pass filter (LPF) is used before the ADC to filter the blocker. Alternatively, to improve noise shaping and power efficiency a global feedback loop can be built around the filter and the ADC thus creating an analog filtering ADC [2]–[7]. To utilize the advantages of digital circuits in reconfigurability and technology scaling, a digital filter in feedback around the ADC can be used to create a digital filtering ADC [8]–[10].

II. Analog Filtering ADC

There are two approaches to designing an analog filtering ADC. The first embeds the filter inside the feedback loop of the ADC, thus relaxing the filter's noise and distortion requirements [2], [3]. The second approach moves the ADC inside the feedback loop of the filter, relaxing the ADC thermal and quantization noise requirements [4]–[7].

A. ADC with Embedded Filter

The conventional baseband implementation shown in Fig. 2(a), takes the mixer output X, which could be either voltage or current depending on the mixer architecture, goes into a LPF with a transfer function $H_{LPF}(s)$, followed by a continuous-time delta-sigma modulator (CTDSM). The first integrator of the modulator has a gain of ω_{ADC}/s. The subsequent stages are combined inside the block $L_{ADC}(s)$ such that the transfer function from V_1 to the quantizer input is $L_{ADC}(s)$. The feedback signal Y is injected into zero, one, or multiple integrators inside the block $L_{ADC}(s)$ depending on the ADC architecture, and its transfer function to the quantizer input is not $L_{ADC}(s)$.

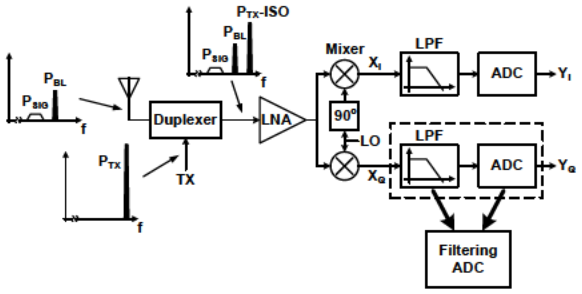

Fig. 1: The front-end block diagram of a typical wireless receiver, with TX and duplexer to illustrate the blocker profile.

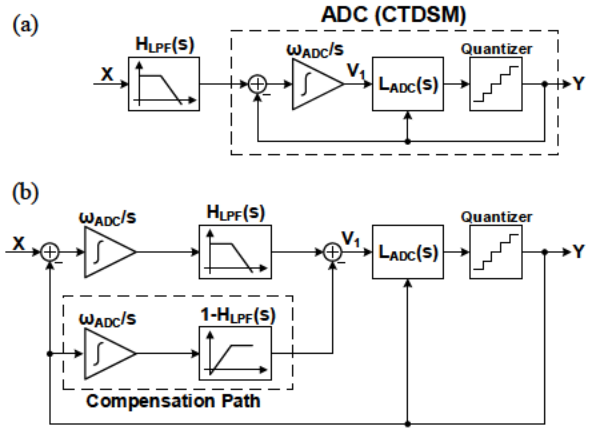

Fig. 2: The block diagram of (a) the cascade of filter and ADC, and (b) ADC with embedded filter [2]. The integrator gain ω_{ADC}/s in (a) and (b) after dynamic range scaling are not necessarily the same.

The filter can be moved into the $\Delta\Sigma$ loop of the ADC, after the first integrator. A compensation path is introduced as shown in Fig. 2(b) to restore the noise transfer function (NTF) and ensure loop stability [2]. With the assumption that $H_{LPF}(s)$ has a DC gain of unity, the compensation path consists of an integrator with the same gain ω_{ADC}/s and a highpass filter with transfer function $1\text{-}H_{LPF}(s)$. It is easy to see that the transfer function from X to Y as well as NTF are the same for Fig. 2(a)

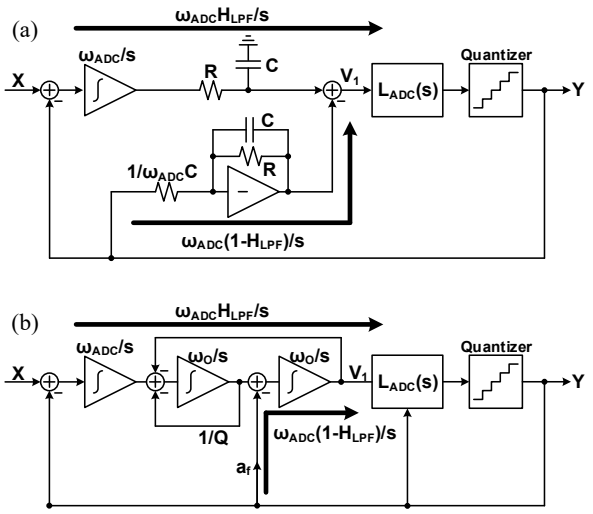

Fig. 3: The filtering ADC implementation with embedded (a) first order passive filter [2], and (b) second order active filter [3].

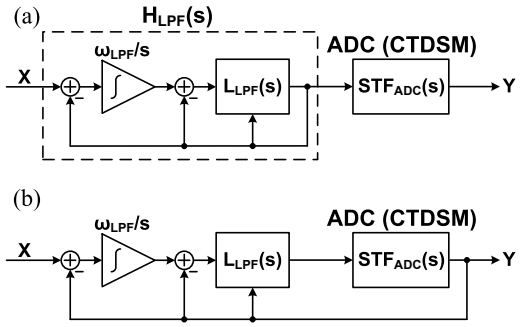

Fig. 4: The block diagram of (a) the cascade of filter and ADC, and (b) filter with embedded ADC.

and (b). Specifically, the voltage V_1 at the input of $L_{ADC}(s)$ are the same in both cases.

By embedding the filter inside of the ADC, the filter noise is divided by the gain of the first integrator when referred to the input. To maximize the benefit of this technique, the gain of the first integrator ω_{ADC}/s should be as high as possible, without saturation at the integrator output. If the modulator uses a feedforward architecture, the DC component at V_1 in Fig. 2(a) is zero, since it directly connects to subsequent integrators [11]. With the first integrator only processing shaped quantization noise, its gain can be very high after proper dynamic range scaling.

When the filter is embedded into the $\Delta\Sigma$ loop (Fig. 2(b)) however, the gain of the first integrator needs to be lower compared to the the cascade of filter and ADC (Fig. 2(a)) for two reasons. First, the signal at the output node Y goes through the compensation path and appears at the summing node in front of the node V_1. Since V_1 contains only quantization noise, the same signal must come from the output of $H_{LPF}(s)$, and thus the output of the first integrator will have a signal component. Second, if a strong out of band blocker appears at the input X, almost all the blocker power goes through the first integrator because the feedback Y already has the blocker attenuated by the filter. Therefore the output swing of the first integrator would be dominated either by the signal or out of band blockers, not quantization noise. As a result, even though by embedding the filter inside the $\Delta\Sigma$ loop, the filter noise is reduced, the subsequent integrators in the modulator ($L_{ADC}(s)$) will contribute more noise due to the reduction in the gain of the first integrator.

The first analog filtering ADC with embedded filter is proposed in [2] where a single bit fourth order CTDSM is used in a cascade of integrators with feedforward (CIFF) topology and no feedback path to $L_{ADC}(s)$, as shown in Fig. 3(a). The low pass filter $H_{LPF}(s)$ is realized with a first order passive RC filter. Since the DC gain of $H_{LPF}(s)$ is unity, 1-$H_{LPF}(s)$ has a zero at DC, which cancels the integrator pole; therefore only one opamp is required in the compensation path. The first order filter combined with a CIFF architecture which has peaking and slow roll-off in the signal transfer function (STF), offers very limited blocker filtering. Also due to the single-bit DAC, the modulator is sensitive to clock jitter and the first integrator needs to consume extra power to achieve the required linearity.

An improved filtering ADC has a second order Butterworth low pass filter embedded into a single bit fourth order CTDSM [3], as shown in Fig. 3(b). The filter has a transfer function $1/[1 + (s/w_oQ) + (s^2/w_o^2)]$ and is implemented with two integrators. Similar to [2], the zero in 1-$H_{LPF}(s)$ cancels the integrator pole. As a result, the response of the compensation path and the filter have identical polynomials in the denominator, and can be realized with the same network with appropriate choice of feedback factor a_f. In this design, the gain of the first integrator ω_{ADC}/s attenuates the total in-band filter noise power by 8.3dB. To compromise between power efficiency and STF roll-off, the cascade of integrators with feedforward-feedback (CIFF-B) modulator topology is used. The jitter sensitivity and linearity requirements of the first integrator are relaxed by the use of 4 bit FIR feedback DAC.

B. Filter with Embedded ADC

The conventional cascade of filter and ADC is again used as a starting point as shown in Fig. 4(a), where the filter is expressed as a feedback loop comprising a first integrator with gain ω_{LPF}/s and subsequent stages with transfer function $L_{LPF}(s)$. The ADC is modeled by the transfer function $STF_{ADC}(s)$. The modulator can be embedded into the filter, as shown in Fig. 4(b). The transfer function from X to Y remains the same as the case in Fig. 4(a) if $STF_{ADC}(s)$ is unity within the frequency range of interest. By embedding the ADC inside the filter, the thermal and quantization noise of the ADC is

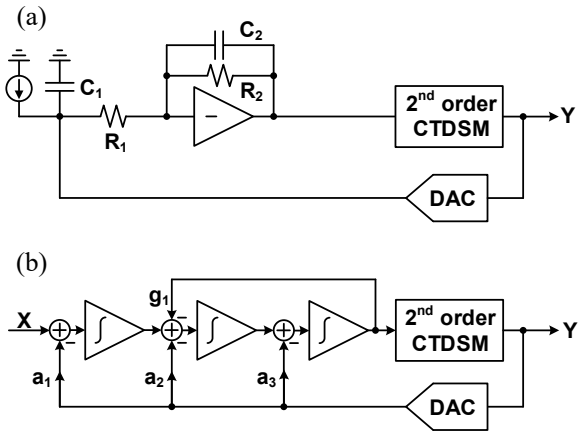

Fig. 5: The filtering ADC implementation with second order modulator embedded in (a) second order Rauch biquad [4], [5], and (b) third order Chebyshev filter [6]

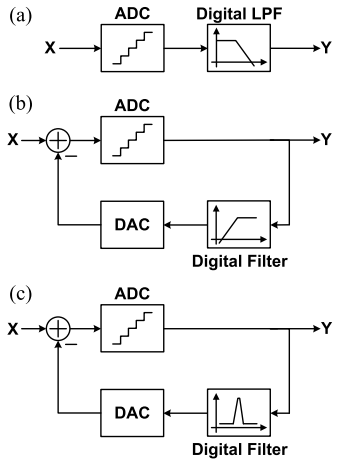

Fig. 7: Block diagram of digital filtering ADC with (a) low pass filter after the ADC, (b) highpass filter in feedback, and (c) bandpass filter in feedback.

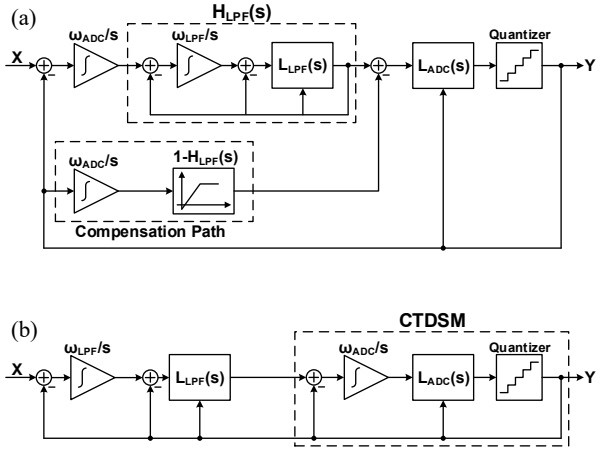

Fig. 6: The block diagram of (a) ADC with embedded filter, and (b) filter with embedded ADC

reduced compared with the the cascade of filter and ADC, because the filter open loop gain $\omega_{LPF}L_{LPF}(s)/s$ is larger than the closed-loop filter response $H_{LPF}(s)$ in the signal band.

The first filter with embedded ADC is proposed in [4], [5] as shown in Fig. 5(a). The design takes a current input, and a second order modulator is embedded in a second order Rauch biquad. The noise advantage compared to a filter-ADC cascade for this work is 7.5dB for the integrated quantization noise and 2dB for the total integrated analog noise. The extra phase shift contributed by the ADC STF and the DAC delay do not alter the filter closed loop transfer function significantly because of the high oversampling ratio and low filter order.

The filter with embedded ADC was further developed in [6] where a second order CTDSM is embedded in a third order Chebyshev filter (Fig. 5(b)). A large open loop gain is developed by the three integrators inside the filter, thus attenuating the ADC in-band quantization and thermal noise by 19.8dB compared with the conventional filter-ADC cascade. The extra phase shift contributed by the ADC STF and the DAC delay is compensated by adjusting the filter coefficients a_1-a_3 with techniques presented in the same work [6]. The same research group published a wireless receiver with a first order modulator embedded in a fourth order Butterworth filter [7]. The ADC quantization noise is improved by 23.6dB compared with the cascade of a filter and ADC.

C. Comparison of Analog Filtering ADCs

The block diagram of the two types of analog filtering ADCs is shown in Fig. 6, with all stages in the filter and the ADC shown. In the presence of large blockers, the gain of the first integrators for the two implementations will have the same maximum gain to prevent saturation at the integrator output. Therefore the second integrator ω_{LPF}/s and $L_{LPF}(s)$ in Fig. 6(a) will have similar noise requirements as $L_{LPF}(s)$ and ω_{ADC}/s in Fig. 6(b). The main difference between the two approaches is the gain seen by $L_{ADC}(s)$ and the quantizer. In the case of Fig. 6(a), $L_{ADC}(s)$ and the quantizer are preceded by $H_{LPF}(s)$ which is unity inside the signal band and the first integrator. In the case of Fig. 6(b), $L_{ADC}(s)$ and the quantizer are preceded by $L_{LPF}(s)$ and ω_{ADC}/s in addition to the first integrator, therefore the design requirements of $L_{ADC}(s)$ and the quantizer will be relaxed by the extra gain compared to Fig. 6(a).

III. Digital Filtering ADC

Several recent works have moved the filtering into the digital domain [8]–[10]. A starting point is shown in Fig. 7(a), where a digital low pass filter is placed after the ADC to attenuate the blockers, however the ADC needs to have a high dynamic

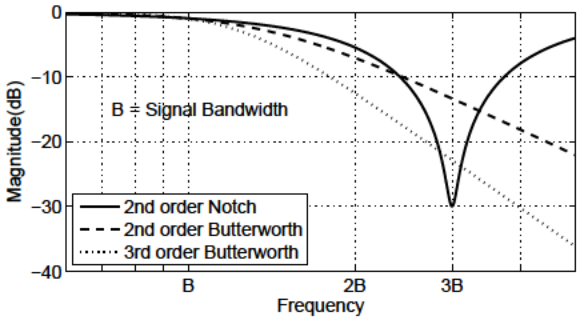

Fig. 8: Comparison between different filters in in the amount of blocker attenuation. The second order notch filter has a Q factor of 24.

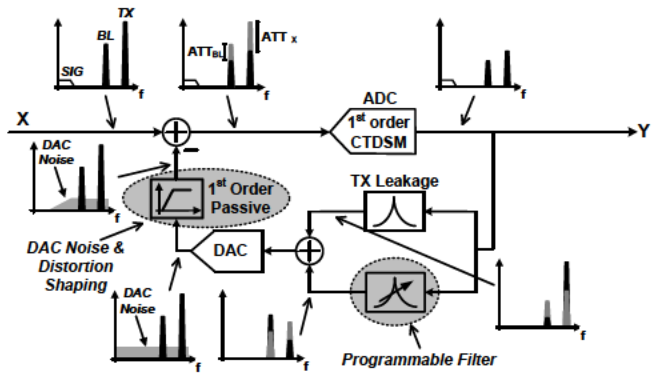

Fig. 9: Signal flow for the digital filtering ADC

range to handle the blocker. A digital high pass filter in feedback can be used to cancel the blocker at the summing node before the ADC (Fig. 7(b)), however with the gain in the digital filter never rolling off, the feedback loop will become unstable at high frequency when the phase shift contributed by the ADC and digital filter becomes significant. Instead, a digital bandpass filter (Fig. 7(c)) can be used to cancel blockers in a frequency range, without the loop stability problem.

A second order digital bandpass filter can be implemented to achieve a closed loop response of a second order notch filter. The resulting closed-loop magnitude response is compared with second and third order Butterworth filters in Fig. 8. All three filters have 1dB attenuation at the signal bandwidth B. The notch filter with Q = 24 achieves higher attenuation at 3B than a third order Butterworth filter for a narrowband blocker, or similar average attenuation than a second order Butterworth filter for a modulated blocker with bandwidth B centred around 3B.

The digital feedback filter was first used in [8], [9] to digitally assist the STF roll off of a third order CTDSM, providing an additional 6dB suppression. A complete digital filtering ADC was then proposed in [10] where the filter transfer function is completely defined in the digital domain. The detailed signal flow for the digital filtering ADC is shown in Fig. 9. The baseband receives a current-mode signal comprised of the inband signal (SIG), TX leakage and an additional blocker (BL). A digital bandpass filter extracts the TX leakage at its known frequency offset, while a programmable digital bandpass filter can be used to track another blocker. The programmable filter can be set to reject blockers at any frequency offset in the range 17.5MHz–107.5MHz under the control of an adaptive algorithm. The DAC converts the summed digital filter outputs to an analog current.

The DAC requires sufficient DR to cancel full-scale TX leakage and blockers while contributing minimal noise in the signal band. Recognizing that the DAC is used to replicate blockers and does not have any signal content in the band of interest, a 1st order passive highpass filter is placed at the DAC output to reduce in-band thermal noise, quantization noise and distortion from the DAC. Only a 1st order CTDSM ADC is needed in the main signal path because most of the blocker power is already absorbed by the digital path and DAC.

IV. Conclusion

Different architectures of filtering ADC have been investigated and compared in this paper. In the case of an analog filtering ADC, if the blocker power is comparable to the signal power, an ADC with embedded filter is preferred due to its large possible gain in the first integrator. If the blocker defines the dynamic range requirement of the ADC, a filter with embedded ADC should be used to fully take advantage of the large open loop gain of the filter. With technology scaling, easily reconfigurable digital filtering ADC shows potential to replace the analog counterpart.

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