A Multi-bit Delta-Sigma Modulator with a Passband Tunable from DC to Half the Sampling Frequency

by

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Abstract

The analysis and design of a discrete-time fully-tunable multi-bit delta-sigma modulator are presented in this thesis. The fourth-order CRFF (Cascade of resonators with feedforward) structure is employed with a four-bit quantizer whose nonlinearity is compensated using digital correction. The design of a tunable delta-sigma modulator for an integrated-circuit (IC) implementation involves some challenges such as coefficient quantization and the realization of coefficient programmability. The tunable modulator was designed and fabricated in the 0.18-μm CMOS technology. A peak SNDR of 96 dB was achieved at an OSR of 96 (270-kHz bandwidth) with a sampling frequency of 50 MHz and 108-mW power consumption was achieved for configurations from the lowpass configuration to the highpass configuration through the bandpass configuration based on the simulation results. These simulated results suggest that the tunable modulator is competitive with conventional bandpass delta-sigma modulators with a fixed passband in terms of the figure of merit (FOM).

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List of Acronyms

ADC Analog to Digital Converter

CMFB Common Mode Feedback

CRFB Cascade of Resonators with Feedback

CRFF Cascade of Resonators with Feedforward

DAC Digital to Analog Converter

DEM Dynamic Element Matching

DWA Data Weighted Averaging

FOM Figure of Merit

IC Integrated Circuit

IF Intermediate Frequency

LSB Least Significant Bit

NTF Noise Transfer Function

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

RF Radio Frequency

SC Switched Capacitor

SNR Signal to Noise Ratio

SNDR Signal to Noise plus Distortion Ratio

SQNR Signal to Quantization Noise Ratio

STF Signal Transfer Function

Chapter 1

Introduction

Analog-to-digital converters (ADCs) play important roles in many applications in electronics. Their importance has grown due to the rapid improvements of the CMOS technologies, which allow more signal processing to be performed in the digital domain instead of the analog domain. In other words, the current trend in signal processing systems is to replace as many analog components as possible with digital circuits, necessitating high-performance ADCs and digital-to-analog converters (DACs).

For years, delta-sigma modulators have been one of the most active research areas in data converters. Their noise shaping capability, which allows us to have a high dynamic range over a narrow frequency band, introduces a notch or notches into the quantization noise power spectrum. Conventional delta-sigma modulators have a fixed narrow passband usually centered around DC (lowpass delta-sigma modulator) or occasionally around some frequency between DC and half the sampling frequency (bandpass delta-sigma modulator). These modulators require the signal band of interest to coincide with the band of low noise spectral density, called the passband of the modulator.

1.1 Thesis Motivation

In some applications such as intermediate frequency (IF) digitization for radio communication, it is necessary to tune the channel (band) of interest to the passband of the delta-sigma modulator. This is typically done by tuning the frequency of a local oscillator at the mixer in the analog domain. If the passband (notch) of the delta-sigma modulator is movable, then it is possible to fix the local oscillator frequency, so tuning

can be done by moving the passband of the modulator as desired. If the passband is digitally programmable, it allows digital tuning of the channel. The rest of the processing, such as downconversion and filtering, is performed in the digital domain, whose IC implementation has grown increasingly less expensive due to the rapid evolution of the CMOS technologies.

For spectral analysis applications, such as harmonic distortion measurement of AC power lines, it is necessary to measure spectra in a wide frequency range with a very low noise floor and high linearity. Such an application usually does not require simultaneous sampling of the entire frequency band, so a delta-sigma modulator with a variable passband location can be used to cover a wide range of frequencies separately. This saves analog components compared with conventional implementations, which employ an analog mixer and a filter, by relying on digital signal processing, which is inexpensive these days.

So far, no IC implementation of a delta-sigma modulator with full tunability has been reported although several IC implementations of delta-sigma modulators with some center-frequency programmability have been reported. For example, IC implementations of bandpass delta-sigma modulators only with a narrow tuning range have been reported in [2] and [3].

There have been reports such as [4] and [5], of discrete-time fully-tunable delta-sigma modulators simulated at the system level without an IC implementation. However, they do not consider important parameters for an IC implementation such as thermal noise, integrator output swing, circuit nonidealities, and/or methods in coefficient programmability.

Therefore, further research into a fully tunable delta-sigma modulator for an IC implementation may enable new applications of delta-sigma modulators.

1.2 Thesis Objective

In this thesis, the analysis and design of a fully-tunable multi-bit delta-sigma modulator, whose passband center frequency can be tuned from DC to half the sampling frequency ($f_s/2$) with a competitive figure of merit (FOM) with conventional bandpass delta-sigma modulators, are presented. The figure of merit is a quantitative measure of the tradeoff between the resolution, the bandwidth, and the power consumption of ADCs, and it is

Table 1.1: Recently published discrete-time band-pass delta-sigma modulators.

	Technology (CMOS)	CT/DT	f_s (MHz)	SNDR (dB)	SNR (dB)	Power (mW)	BW (MHz)	Center f (MHz)	FOM (dB)
[6]	0.18-μm	DT	37	-	72	88	0.2	10.7	136
[7]	0.35-μm	DT	80	78	80	24	0.27	20	146
			80	75	75	37	1.25	20	150
			80	69	70	37	1.76	20	146
			80	48	48	38	3.84	20	128
[8]	0.18-μm	DT	120	69	72	150	2.5	40	141
[9]	0.35-μm	DT	240	72	-	37	0.2	60	139
			55		-		1		129
			52		-		1.25		127
[2]	HBT	CT	4000	72.5	-	3500	1	140-210	127
				47.7	-		60		120
[3]	2-μm	DT	2.358	-	47	-	0.012	0.47-0.70	-
				-	59	-	0.00625	0.25-0.38	-
Target	0.18-μm	DT	50	90	-	100	0.26	0-25	154

expressed as

$$\text{FOM (dB)} \equiv \text{SNDR (dB)} + 10\log_{10}\frac{\text{BW (Hz)}}{\text{P (W)}}, \tag{1.1}$$

where SNDR is the signal-to-noise and distortion ratio, BW is the bandwidth, and P is the power consumption. In order to achieve FOMs competitive with conventional bandpass deltasigma modulators, 90-dB SNDR over a 260-kHz bandwidth (OSR=96) at a 50-MHz sampling frequency with 100-mW power consumption for any center frequency was chosen considering the specifications of the recently published bandpass delta-sigma modulators shown in Table 1.1. The target technology for implementation is 0.18-μm CMOS process.

It is difficult for the tunable delta-sigma modulator in this thesis to compete with state-of-art lowpass delta-sigma modulators in terms of the FOM because of the hardware overhead (as will be explained later in this thesis).

This thesis covers the design from the system level to IC implementation in detail. Features, procedures, and analyses specific to the design of a tunable delta-sigma modulator are emphasized throughout the thesis.

1.3 Thesis Outline

This thesis consists of three body chapters. Chapter 2 introduces fundamental ideas of delta-sigma modulation including single-bit first and second-order delta-sigma modulation, high-order delta-sigma modulation, multi-bit delta-sigma modulation, band-pass delta-sigma modulation, and tunable delta-sigma modulation.

Chapter 3 covers the system-level design of a tunable delta-sigma modulator with an emphasis on features and challenges that are specific to design of a tunable delta-sigma modulator including the determination of the modulator architecture, coefficient quantization, digital correction of DAC nonlinearity, thermal noise analysis, and integrator nonidealities.

In Chapter 4, the transistor-level design of the tunable delta-sigma modulator is described. It is shown that the digital correction feature is easily accommodated by the modulator with minimal changes to the circuit due to its programmability. An efficient implementation of the programmable switched-capacitors is shown as well. Results from full circuit simulations are presented to verify the performance of the modulator at the transistor level.

In Chapter 5, the reasons for having no experimental results are briefly explained, and the prepared test setup is described.

Chapter 2

Delta-Sigma Modulation Background

2.1 Overview

This chapter briefly introduces the basic theories of delta-sigma modulation. The simplest delta-sigma modulators such as the first and the second-order lowpass modulators, which offer low quantization noise near DC, are presented first. Subsequently, the benefits, the disadvantage, and the solutions to the disadvantage of the multi-bit delta-sigma modulator follow. In the end, the bandpass delta-sigma modulator with high quantization-noise attenuation around some frequency other than DC, and the tunable delta-sigma modulator with programmable quantization-noise shaping are briefly reviewed.

2.2 Delta-Sigma Modulation

2.2.1 First-order Low-pass Delta-Sigma Modulation

Figure 2.1 shows a block diagram of the discrete-time first-order single-bit delta-sigma modulator for A-to-D conversion, which is one of the simplest delta-sigma modulators. It consists of an integrator, a single-bit ADC, and a single-bit DAC. The modulator can be modeled with a quantizer as shown in Figure 2.2. For linear analysis of the modulator, the quantization error of the quantizer can be taken as an input to the system as shown in Figure 2.3. However, the modulator in Figure 2.3 is not a pure linear system since the relationship between Y and e is nonlinear. Nevertheless, this linearized model is useful for analysis to find the relationship between the output V and the quantization noise e.

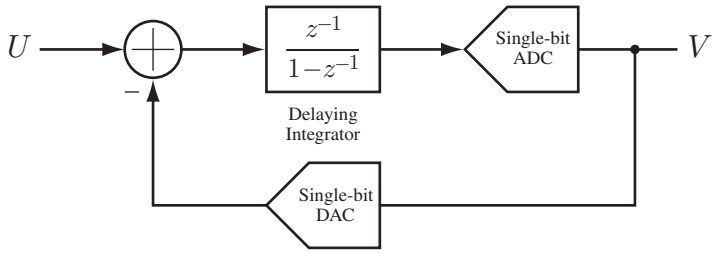

Figure 2.1: First-order delta-sigma modulator.

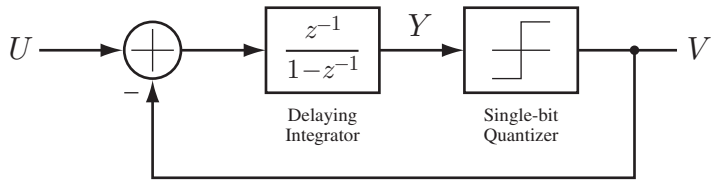

Figure 2.2: Equivalent model with a quantizer.

One important aspect of the linear analysis of the single-bit delta-sigma modulator is that the gain of the single-bit quantizer is not well defined unlike multi-bit ones [10, Ch.2] as shown in 2.4. In order to maximize the accuracy of the linear analysis, the gain must be obtained from a statistical analysis of the quantizer input Y which requires a time-domain analysis of the modulator [10, Ch.2]. In this section, the output level of the single-bit quantizers is set to be +1 and -1, and the gain is assumed to be 1 for simplicity. This condition is not optimal for accurate linear analysis. However, it has been confirmed that this condition leads to results that do not deviate too much from the results obtained using the accurate quantizer gain.

Our main interest is how the input U and the quantization noise e are transferred to

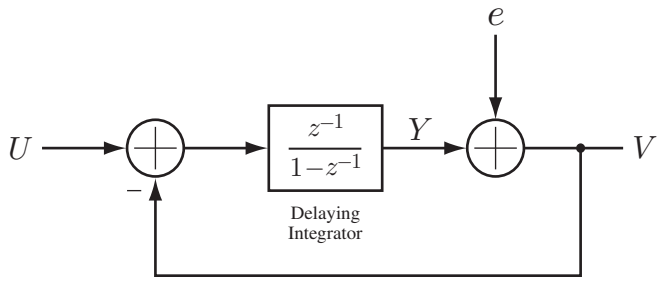

Figure 2.3: Linearized model of first-order delta-sigma modulator.

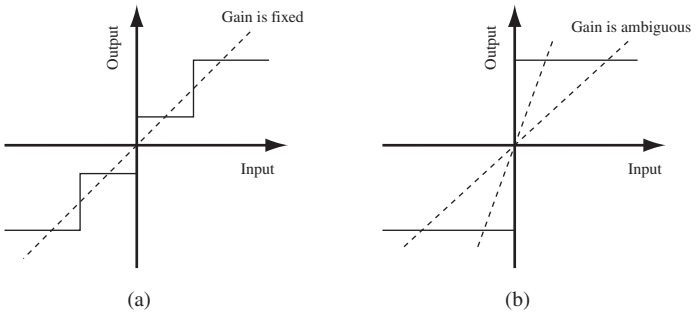

Figure 2.4: Transfer curves of (a) multi-bit quantizer and (b) single-bit quantizer.

the output V. Therefore, we express the output V as

$$V(z) = \mathrm{STF}(z)U(z) + \mathrm{NTF}(z)e(z) \tag{2.1}$$

where $\mathrm{STF}(z)$ is called a Signal Transfer Function, and $\mathrm{NTF}(z)$ is called a Noise Transfer Function. For the modulator of Figure 2.3,

$$V(z) = z^{-1}U(z) + (1 - z^{-1})e(z). \tag{2.2}$$

Therefore, the STF and the NTF are

$$\mathrm{STF}(z) = z^{-1} \tag{2.3}$$

$$\mathrm{NTF}(z) = 1 - z^{-1}. \tag{2.4}$$

The STF is a simple unit delay function, which preserves the amplitude of the input $U(z)$. The NTF is a first-order highpass transfer function whose transfer characteristic is shown in Figure 2.5. The power of the quantization noise is strongly attenuated for the low-frequency band around DC. Therefore, a high signal-to-quantization noise ratio (SQNR) is obtained if the frequency band of interest is limited to a value much lower than half the sampling frequency. For this reason, data converters based on delta-sigma modulation are always used as oversampling converters with some kind of filter to eliminate the quantization noise outside the frequency band of interest. The ratio of $\frac{f_s}{2}$, to the band of interest, f_b, is called the oversampling ratio (OSR),

$$\mathrm{OSR} = \frac{f_s}{2f_b}. \tag{2.5}$$

where f_s is the sampling frequency, and f_b is the band of interest (bandwidth).

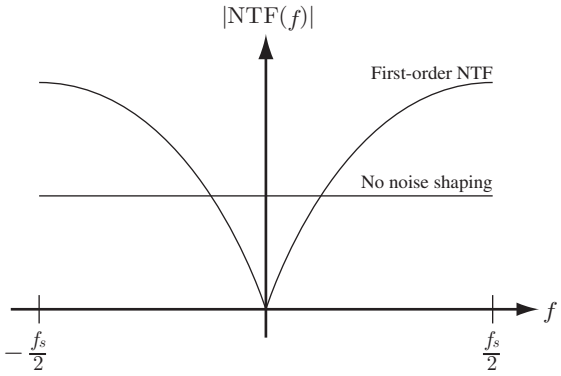

Figure 2.5: First-order NTF.

The simulated modulator output for a single-tone input is shown in Figure 2.6. It exhibits the expected first order (20 dB per decade) attenuation of the quantization noise. Hann windowing is used for Discrete Fourier Transform (DFT) to prevent excessive leakage of the strong out-of-band quantization noise to the band of interest.

2.2.2 Second-order Delta-sigma Modulation

The order of the NTF can be increased to two by adding a second integrator to the modulator. Figure 2.7 shows one of the possible configurations for a single-bit second-order delta-sigma modulator. For this modulator,

$$\mathrm{STF}(z) = 1 \tag{2.6}$$

$$\mathrm{NTF}(z) = (1 - z^{-1})^2. \tag{2.7}$$

This NTF exhibits second-order noise shaping, which results in higher SQNR than the first-order noise shaping for a given bandwidth (or OSR). Figure 2.8 briefly compares NTFs of different orders.

Figure 2.9 shows the simulated output of the modulator. It clearly shows the second-order (40 dB/decade) attenuation of the quantization noise. The SQNR is increased by 20 dB for the same OSR.

Since a delta-sigma modulator is linear except for the quantizer, the input of the quantizer can be expressed by a linear combination of the input U and output V [10, Ch.4]. Therefore, the schematic representation of single-loop modulators can be generalized as

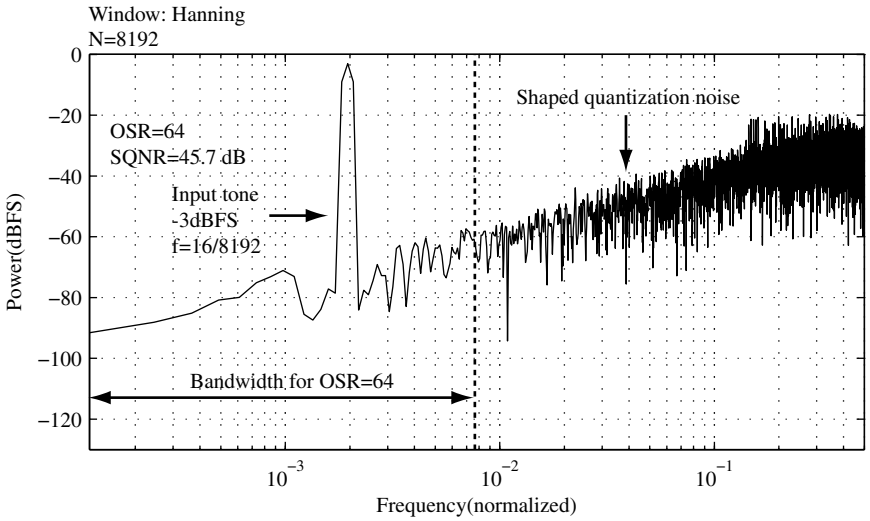

Figure 2.6: Output spectrum of the first-order delta-sigma modulator with a single-sinusoid input.

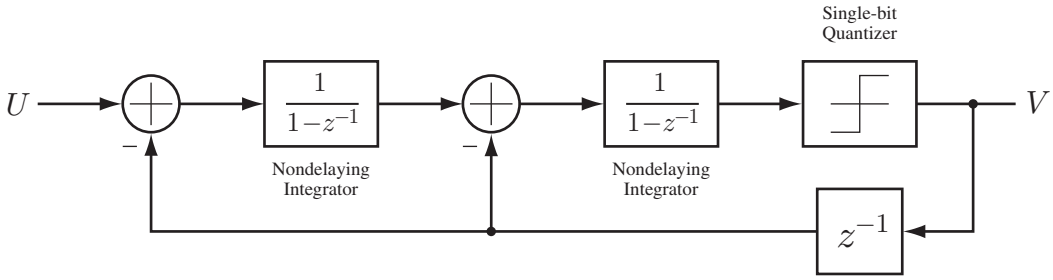

Figure 2.7: Second-order delta-sigma modulator.

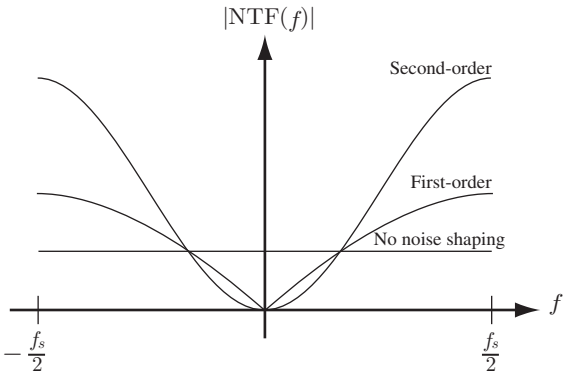

Figure 2.8: Comparison of NTFs.

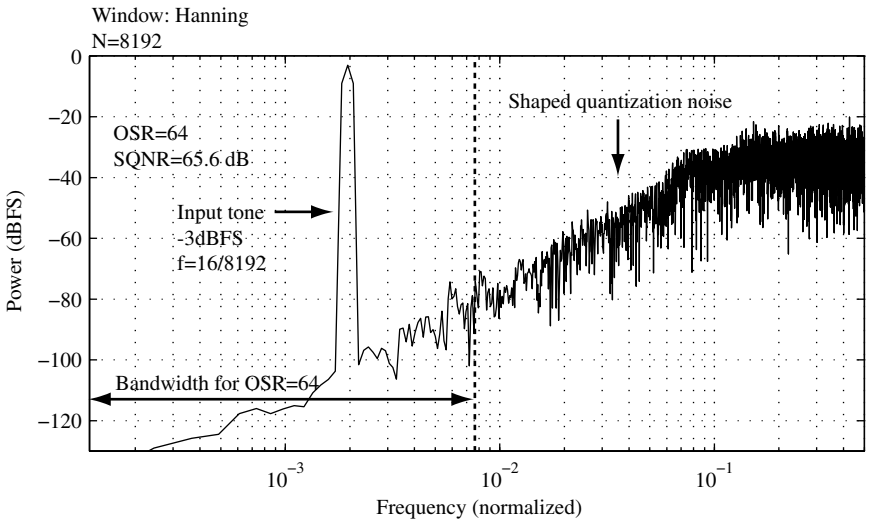

Figure 2.9: Output spectrum of the second-order delta-sigma modulator with a single-sinusoid input.

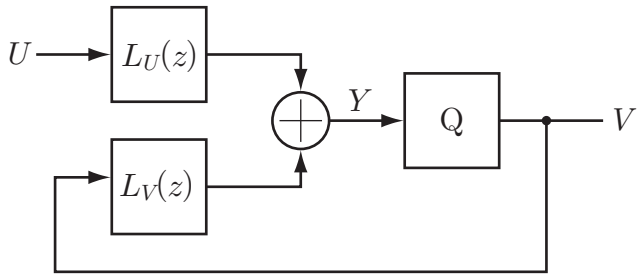

Figure 2.10: General model of a delta-sigma modulator.

shown in Figure 2.10 where L_U and L_V are the transfer functions of U and V to the quantizer input Y, respectively. Therefore,

$$Y(z) = L_U(z)U(z) + L_V(z)V(z) \tag{2.8}$$

$$\mathrm{STF}(z) = \frac{L_U(z)}{1 - L_V(z)} \tag{2.9}$$

$$\mathrm{NTF}(z) = \frac{1}{1 - L_V(z)}. \tag{2.10}$$

The quantizer, which could be single-bit or multi-bit, is expressed as Q in Figure 2.10.

2.2.3 Higher-order Delta-Sigma Modulation

Even higher SQNR can be achieved by linking more integrators to increase the order of the NTF. However, high-order single-loop modulators are more susceptible to instability[1] than low-order ones. The reason is that the quantizer input Y is expressed as

$$Y = \mathrm{STF}(z)U(z) + [\mathrm{NTF}(z) - 1]\, e(z), \tag{2.11}$$

and for high-order lowpass delta-sigma modulators $|\mathrm{NTF}(z)|$ tends to be very high for high frequencies (high out-of-band gain of NTF) as shown in Figure 2.8. When $|Y|$ is too large, it overloads the quantizer causing the modulator loop to go unstable. In order to prevent overloading, the out-of-band gain of the NTF can be limited by adding poles to the NTF. Unfortunately, limiting the out-of-band gain reduces the achievable SQNR for a given order of the modulator, and the effort required to limit the out-of-band gain increases for an increasing order of the modulator [10, Ch.4]. Therefore, the achievable SQNR saturates as the order of the single-loop modulator increases.

The cascaded-modulator structure known as MASH (Multi-Stage Noise Shaping) shown in Figure 2.11 is an alternative topology for high-order noise shaping [10, Ch.4]. The second modulator subtracts the quantization noise of the first stage, and the order of the NTF of the entire system is sum of the orders of the two modulators. Since cascading modulators does not change the stability of each modulator loop, this topology is more stable than the single-loop modulators for the same order of NTF. The drawback of this topology is its strict requirement of matching between NTF of the first modulator and the post filter of the second modulator [10, Ch.4]. Poor matching causes the quantization noise of the first stage not to be canceled well, and it decreases the SQNR. NTF of the discrete-time delta-sigma modulator for A-to-D conversion is affected by the matching of capacitors in switched-capacitor circuits and the finite DC gain of operational transconductance amplifiers (OTAs).

[1] A widely-recognized clear definition of instability of a delta-sigma modulator has not been established. However, [11, Ch.4] states that

> By "not stable" we mean that the modulator exhibits large, although not necessarily unbounded, states and a poor SNR compared with that predicted by linear models.

"More stable" in this thesis means that the modulator less unlikely goes into instability and more likely recovers from such a state, and "less stable" means the modulator more likely goes into instability and less likely recovers from such a state.

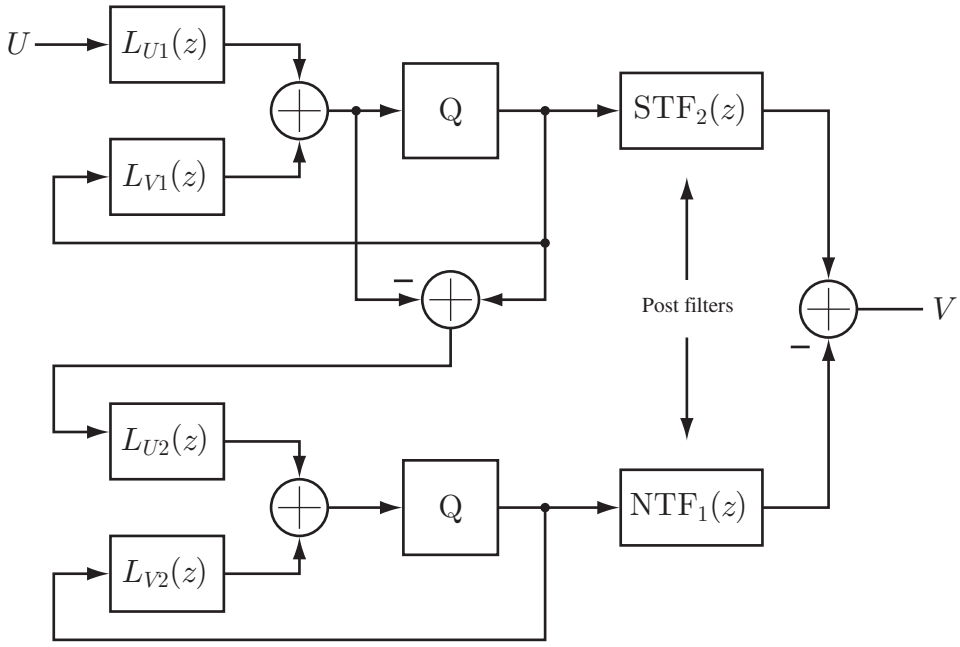

Figure 2.11: Cascaded-modulator structure.

2.3 Multi-bit Delta-Sigma Modulation

Increasing the order of the NTF is one way to increase SQNR. Another way to improve SQNR is to increase the number of levels of the quantizer with a multi-bit quantizer. The direct benefit of the multi-bit quantizer is the smaller quantization noise to be shaped by the NTF. Increasing the resolution of the quantizer by one bit decreases the power of the quantization noise to be shaped by 6 dB. Therefore, the SQNR is improved by 6 dB as well. More importantly, however, modulators with a multi-bit quantizer enjoy more significant indirect benefits due to the smaller quantization noise and improved linearity of the quantizer. The following description summarizes the benefits [10, Ch.6]:

Robust stability At a system level, the only nonlinear component in a delta-sigma modulator is the quantizer. Since a multi-bit quantizer behaves more linearly than single-bit ones, a multi-bit modulator becomes more like a linear system, and it enhances the stability of the system.

Predictable stability Nonlinearity of the quantizer makes linear analysis of the system more unreliable, and extensive time-domain simulations are required for evaluation of stability. The use of a multi-bit quantizer improves the linearity of the quantizer,

and the stability can be determined more reliably with linear analysis. In addition, the gain of the quantizer is fixed unlike the single-bit quantizer.

Improved NTF For high-order modulators with a single-bit quantizer, the out-of-band gain of the NTF has to be limited in order to prevent overloading of the quantizer. However, for multi-bit modulators, the out-of-band gain limit is relaxed due to the smaller value of e. Consequently some improvement in the SQNR is achieved in addition to the 6 dB/bit advantage.

Relaxed slew-rate requirements The feedback signal from a single-bit DAC in a single-bit modulator always swings between the smallest value and the largest value. This causes the output of the integrators to change by a large amount for each sample. Therefore, high slew rate is required for the integrators for sufficient settling of the output, and high slew rate requires high bias current of OTAs resulting in high power consumption. Multi-bit modulators, however, have smoother feedback signals due to the multiple steps between the largest and smallest output of the DAC. This makes the output of the integrators smoother, and the slew rate requirement is relaxed.

2.3.1 Effects of the Multi-bit DAC Non-idealities

In reality, neither single-bit DACs nor multi-bit DACs are perfect. Their output levels deviate from the ideal values due to imperfections in the circuit elements. However, there is one major difference in the nature of the output of a single-bit DAC and a multi-bit DAC. As shown in Figure 2.12, both the single-bit DAC and the multi-bit DAC may have a DC offset and a gain error. The output of the multi-bit DAC, however, may be nonlinear whereas the single-bit DAC is inherently linear. Unfortunately, none of these errors (DC offset, gain error, and nonlinearity) are corrected by the modulator loop because the DAC output error directly affects the output of the modulator for the following reasons.

In order to analyze contribution of the DAC output error to the output of a multi-bit delta-sigma modulator, we can model the modulator as shown in Figure 2.13, where e_Q is the quantization noise of the multi-bit ADC, and e_{DAC} is the DAC output error, which is a function of the DAC input V. Solving for V yields

$$V(z) = \frac{L_U(z)}{1 - L_V(z)}U(z) + \frac{1}{1 - L_V(z)}e_Q(z) + \frac{L_V(z)}{1 - L_V(z)}e_{DAC}(V) \qquad (2.12)$$

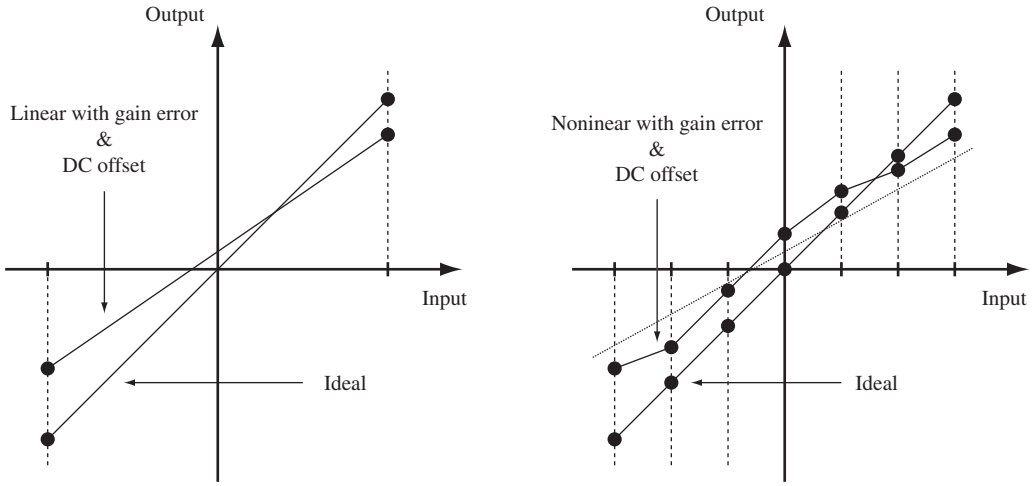

Figure 2.12: Comparison of non-ideal single-bit and multi-bit DACs.

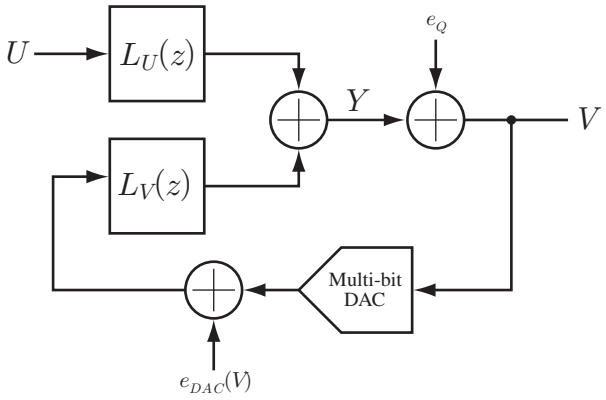

Figure 2.13: Multi-bit delta-sigma modulator with a nonlinear DAC.

$$= \text{STF}(z)U(z) + \text{NTF(z)}e_Q(z) + \frac{L_V(z)}{1 - L_V(z)}e_{DAC}(V). \tag{2.13}$$

For the band of interest, $|L_V(z)| \gg 1$. Therefore,

$$V(z) \approx \text{STF}(z)U(z) + \text{NTF}(z)e_Q(z) - e_{DAC}(V) \tag{2.14}$$

for the band of interest. Thus, DAC output error is not attenuated by the modulator loop, and it directly affects the output of the modulator.

Out of the DAC non-idealities (DC offset, gain error, and nonlinearity), nonlinearity causes severe reduction of the SNDR. The effect of each non-ideality is described below:

DC offset A DC offset of the DAC output simply adds the offset to the modulator

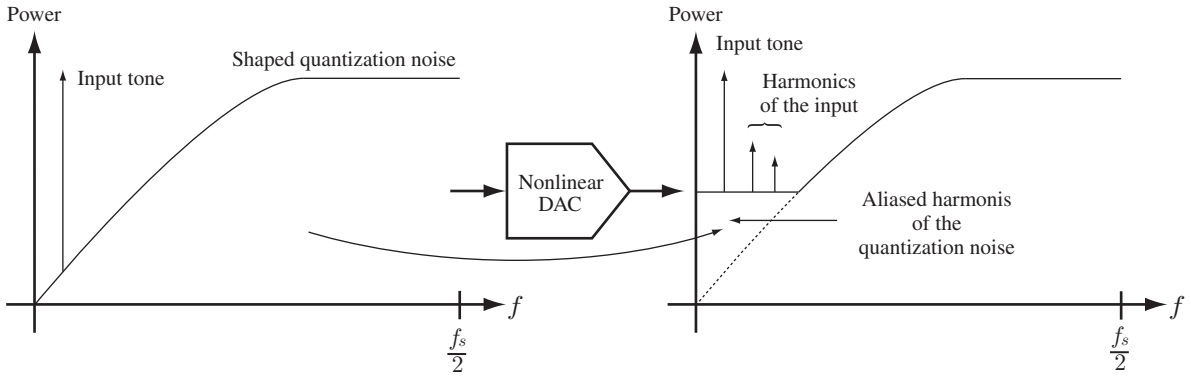

Figure 2.14: The effect of a nonlinear DAC.

output. In applications sensitive to DC offset such as instrumentation applications, this offset is not acceptable.

Gain error A gain error effectively multiplies $L_V(z)$ with some factor. This alters the STF and the NTF. However, for a reasonable gain error, the they do not change significantly, and it does not affect the SNDR or stability of the modulator. This can be verified by extensive simulations for the expected gain variance.

Nonlinearity The nonlinearity of the DAC generates harmonics of the feedback signal V, which is $\mathrm{STF}(z)U(z) + \mathrm{NTF}(z)e(z)$. Therefore, harmonics of the input signal U and the harmonics of the out-of-band noise aliased back to the band of interest are directly added to the output of the modulator. Even a small nonlinearity can raise the noise floor significantly because the out-of-band noise is much larger (by tens of dBs) than the noise floor in band. Hence, the nonlinearity severely deteriorates the SNDR of the modulator, and it is usually the limiting factor of the accuracy of multi-bit delta-sigma modulators without any DAC non-ideality compensation technique.

Multi-bit D-to-A conversion is done by activating the specified number of unit circuit elements such as capacitors or transistors as shown in Figure 2.15. Therefore, linearity of the DAC usually depends on the matching of the unit elements. For high-resolution modulators, it is impossible to achieve sufficient linearity of the DAC with reasonable size of the DAC unit elements unless expensive techniques such as trimming are employed. Nevertheless, the benefits of the multi-bit modulators are still very attractive, and for-

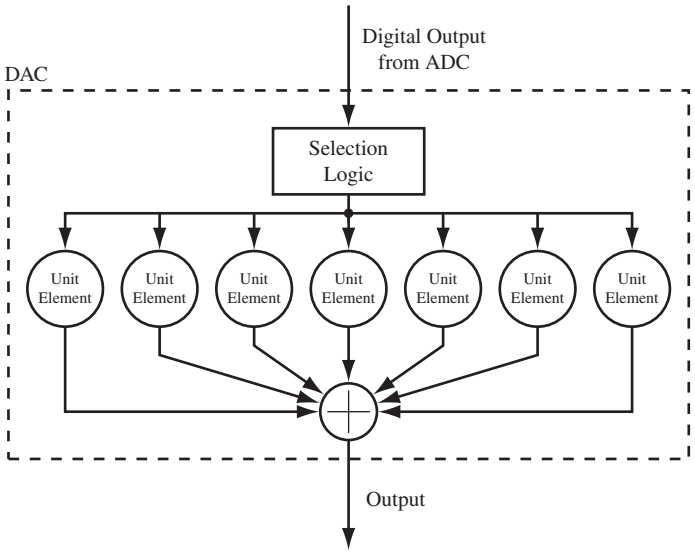

Figure 2.15: An 8-level DAC with unit elements.

tunately there exist some techniques such as dynamic element matching (DEM), digital correction to reduce the impact of the DAC nonlinearity.

2.3.2 Dynamic Element Matching

A multi-bit DAC is formed by a set of unit elements such as capacitors and transistors. For an n-level DAC with the input code $k \in \{0, 1, \cdots, n-1\}$, k elements out of $n-1$ elements are activated for D-to-A conversion. In a straightforward implementation of a multi-bit DAC without any dynamic element matching (DEM) technique, the same unit elements are always selected for the same input code. There are actually multiple ways to select k elements out of $n-1$ elements for $0 < k < n-1$. This redundancy enables us to filter the nonlinearity of the multi-bit DAC. Different algorithms for utilizing the redundancy have been studied. In [12, Ch.2], many different algorithms including the data weighted averaging (DWA), the tree structure, and the vector-quantization structure are compared with extensive simulation results. Most of the algorithms filter (shape) the output error of the DAC with a highpass transfer function to recover the low noise floor and the low distortion for the band of interest, but none of the algorithms actually cancel the DAC output errors.

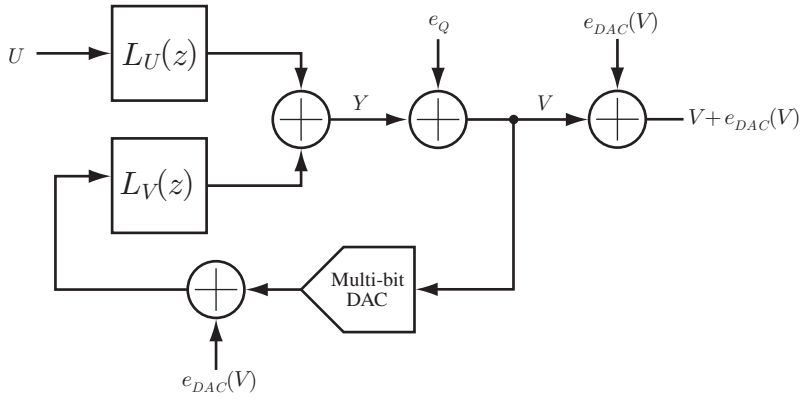

Figure 2.16: Digital Correction of the DAC Non-idealities.

2.3.3 Digital Correction

As explained in Section 2.3, output of a multi-bit delta-sigma modulator is expressed as $V(z) \approx \mathrm{STF(z)}U(z) + \mathrm{NTF(z)}e_Q(z) - e_{DAC}(V)$ for the band of interest. This equation suggests that if values of $e_{DAC}(V)$ are known for all possible V, we can cancel the effect of the DAC output errors by adding $e_{DAC}(V)$ to the output V as shown in Figure 2.16. This is equivalent to replacing V with $V + e_{DAC}(V)$ in digital domain. This technique is called digital correction of DAC nonidealities [13]. Since this technique requires precise digital representation of $V + e_{DAC}(V)$, analog-to-digital conversion of the DAC output in high precision is required. This can be done by transforming the multi-bit delta-sigma modulator to a single-bit modulator, whose DAC is inherently linear, for measurement of the DAC output. A successful implementation was reported by [14].

2.4 Bandpass Delta-Sigma Modulation

The delta-sigma modulators described so far are lowpass modulators which are useful only for digitization of narrow frequency bands near DC. In applications such as communication and instrumentation, the frequency band of interest may be narrow and far away from DC. Obviously, a high SQNR cannot be achieved with a lowpass delta-sigma modulators for these applications. The lowpass nature of the lowpass delta-sigma modulators is due to the high gain of the integrators at low frequency which results in NTF zeros at low frequency. A low quantization noise frequency band away from DC, as shown in Figure 2.17, can be achieved with resonators, whose gain is very high around a certain frequency,

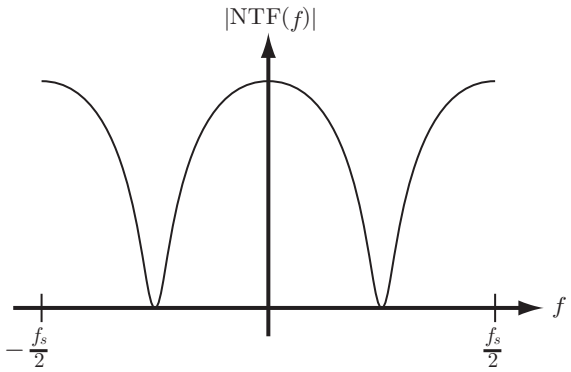

Figure 2.17: NTF of a bandpass delta-sigma modulator.

instead of integrators. Delta-sigma modulators with such a response are called bandpass delta-sigma modulators. Bandpass delta-sigma ADCs allow us to efficiently digitize a narrow frequency band away from DC without downconversion in the analog domain. With typical ADC architectures, the bandwidth of the ADC has to be more than the center frequency. For example, if the signal band of 1 MHz is located around 50 MHz, typical ADCs have to have a bandwidth of more than 50.5 MHz wasting the frequency band between 0 Hz to 49.5 MHz unless the signal band is downconverted. On the other hand, the bandpass ADCs only need to have a bandwidth of 1 MHz with a center frequency of 50 MHz.

For the discrete-time implementation, an nth-order lowpass delta-sigma modulator can be easily converted to a $2n$th-order bandpass one whose center frequency is $f_s/4$ with the same stability characteristic and SQNR by replacing z with $-z^2$ [10, Ch.5]. Figure 2.18 shows an example of a fourth-order bandpass delta-sigma modulator converted from the second-order modulator in Figure 2.7 with this transformation technique. As shown in Figure 2.19, this modulator achieves almost the same SQNR as the second-order modulator for the same OSR.

Although many bandpass delta-sigma modulators with a cetner frequency of $f_s/4$ have been reported due to easy downconversion and implementation of the resonators, the center frequency is not limited to $f_s/4$. Since the center frequency of a bandpass modulator coincides with the resonant frequency of the resonators, the center frequency can be freely selected within $f_s/2$.

Many of the design considerations described so far in this chapter for lowpass delta-sigma modulators apply to bandpass modulators as well. High-order bandpass modulators

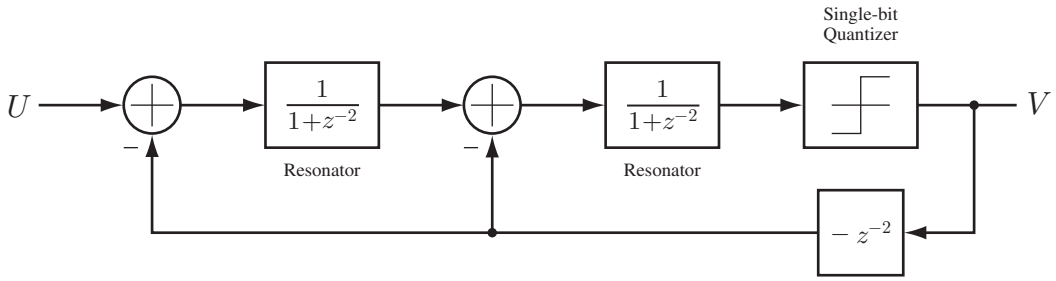

Figure 2.18: Fourth-order Bandpass Delta-Sigma Modulator.

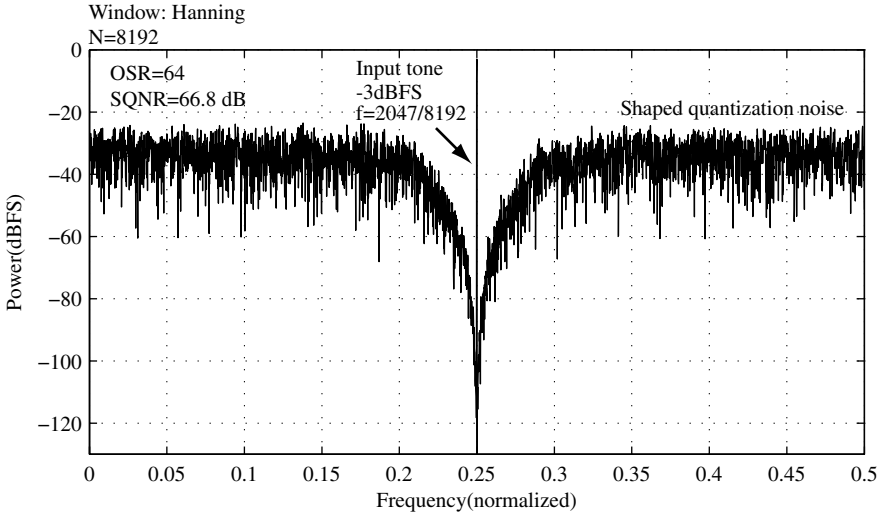

Figure 2.19: Output spectrum of the fourth-order delta-sigma modulator.

tend to be unstable although the achievable SQNR is higher. A multi-bit quantizer enhances the SQNR and stabilize the modulator loop while significantly affecting the SNDR due to its linearity by generating intermodulation products as well as a high noise floor. The DAC nonlinearity digital correction technique is applicable to bandpass delta-sigma modulators as well.

However, there are some expceptions. For example, most of the DEM algorithms for multi-bit DAC nonlinearity compensation such as DWA are not useful for bandpass delta-sigma modulators at all. In order to apply a DEM technique, a different algorithm such as [15] is required for a bandpass delta-sigma modulator. In addition, due to the proximity of the frequency band of interest to $f_s/2$, the requirement for the anti-aliasing filter is tighter, so a high-order filter is required. Due to the fast-changing nature of the input signal, the sampling clock jitter requirement is much tighter as well [10, Ch.5]. Furthermore, for a modulator architecture whose loop filter processes the modulator signal input components, slew-rate requirements of the loop-filter components are more strict because of the fast-changing input signal.

2.5 Tunable Delta-Sigma Modulation

Locations of NTF zeros are determined by the resonant frequency of the resonators. Therefore, NTF zeros can be moved to the desired frequencies by making the resonant frequency of the resonators tunable as shown in Figure 2.20. Tunability is quite useful for some applications where the center frequency of interest varies. For example, tunability allows full digital tuning in communication systems. Tunability is also useful for spectral analysis over a wide frequency range with a very low noise floor where simultaneous measurement of the low frequency to high frequency range is not required.

For discrete-time modulators with switched-capacitor circuits, the tunability can be achieved by utilizing programmable switched-capacitors which change the resonant frequency of the resonator. NTF zeros of the modulator coincide with the resonant frequency. Much extra care must be taken in the design of a tunable delta-sigma modulator compared to the conventional single-NTF delta-sigma modulators. Changing the resonant frequency moves the NTF zeros, so NTF poles have to be moved accordingly to maximize the SQNR and to ensure robust stability. In addition, the output swing of the resonators must be examined and controlled for different center frequencies to maintain reasonable

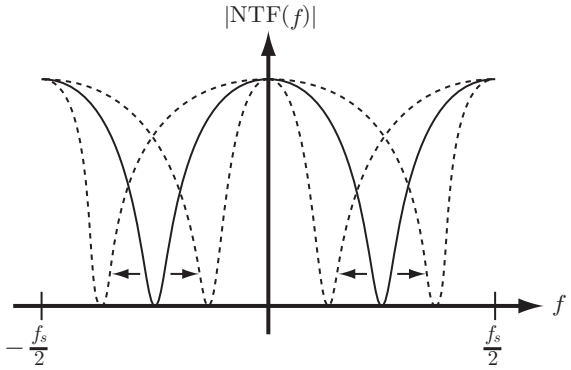

Figure 2.20: NTF of a Tunable Bandpass Delta-Sigma Modulator.

dynamic range of the resonator outputs while preventing clipping at the output. Furthermore, the effect of the programmable switched-capacitor circuits on the thermal noise and the settling time of the resonator output have to be carefully examined. Moreover, the resolution of each capacitor bank in the programmable switched-capacitor must be chosen to compromise between accuracy in setting the NTF zeros and poles, and saving the silicon area and power.

2.6 Summary

In this chapter, very basic ideas of delta-sigma modulation including multi-bit delta-sigma modulation, bandpass modulation, and tunable modulation were briefly described. High-order delta-sigma modulators have a potential for a high SQNR for a given OSR with an expense of stability. Multi-bit delta-sigma modulators improve SQNR,and stability, but their performance is limited by linearity of the multi-bit DAC unless a DAC-mismatch compensation technique, such as DEM and digital correction, is employed. Bandpass delta-sigma modulation allows the user to digitize a narrow frequency band away from DC, and tunable delta-sigma modulation has a capability to move the band of interest as desired.

Chapter 3

Tunable Modulator System Design

3.1 Overview

This chapter describes the system-level design and analysis of a tunable delta-sigma modulator, from determination of the modulator architecture to simulations of some of the expected circuit nonidealities such as thermal noise, limited settling capability and finite DC gain of the OTAs.

Since the tunable modulator has numerous configurations to cover all of the frequency bands between DC and $f_s/2$, all of the analyses have one extra dimension compared to typical delta-sigma modulators with a single configuration. For example, dynamic range scaling of the integrator outputs and thermal noise analysis have to be repeated for all possible configurations of the modulator. This complicates the analysis and design of the tunable modulator.

In addition, a distinctive feature of the digitally tunable modulator is quantization of the modulator coefficients. In a normal delta-sigma modulator, the capacitors can be ratioed to accurately realize just one set of modulator coefficients. For the tunable modulator, however, this is not the case because the coefficients are realized with programmable capacitor banks, and the coefficients change widely for different configurations. It is very costly to achieve high accuracy and resolution of the modulator coefficients that vary in a wide range because a large number of unit capacitors (to be explained later in this chapter) are required. However, these costs can be reduced significantly by making compromises in the dynamic range scaling of the integrator output and the location of the NTF zeros.

The design starts with the selection of the modulator architecture. Once the architecture is determined, the NTFs and the STF are determined with a help of a computer program, and the corresponding ideal modulator coefficients are obtained. Then, the modulator coefficients are quantized for an eventual implementation with digitally-programmable capacitor banks. Consequently, the effectiveness of the digital correction of DAC nonlinearities is verified with simulations. Finally, circuit non-idealities such as thermal noise and imperfections of the OTAs inside the integrators are analyzed and simulated in order to determine the required specifications of the OTAs.

3.2 Target Modulator Specifications

As explained in Chapter 1, the target specification of the modulator is 50-MHz sampling frequency at an OSR of 96 (260 kHz) with 90-dB SNDR with a four-bit quantizer for any center frequency between DC to $f_s/2$. Since the bandwidth is 260 kHz, and the sampling frequency is 50 MHz, 96 configurations are required in order to be able to cover all frequency bands from DC to $f_s/2$. According to [10, Ch.9], it is reasonable to add a margin of 10 to 20 dB in the SQNR when designing the architecture in order to allow for degradation of the SNDR by thermal noise and other circuit non-idealities. Since the tunable modulator has an extra nonideality in its deign (i.e. quantization of the modulator coefficients), a 20-dB margin is selected. Therefore, the initial system design should be done for a 110-dB SQNR at an OSR of 96.

3.3 Order of the Modulator and Resolution of the Quantizer

Since a tunable delta-sigma modulator acts as a lowpass, bandpass, or highpass modulator depending on the configuration, it is very important that the specification exceeds the required one for any configuration while ensuring stability by selecting the proper order and resolution of the quantizer.

The choice of either a single-loop architecture or a cascaded-modulator architecture has to be made first since this choice changes all of the following analysis and design. Once this decision is made, the order of the modulator and the resolution of the quantizer

is chosen to satisfy the design specification.

As explained in Section 2.2.3, the major differences between the single-loop architecture and the cascaded-modulator architecture are the stability and the need for transfer function matching. The latter prohibits the choice of the cascaded-modulator structure for a tunable delta-sigma modulator.

Since the NTF of the tunable modulator varies with the desired center frequency, the digital post filter has to track the change of NTF accurately for the cascaded-modulator structure in order to prevent leakage of the quantization noise. Therefore, a large hardware overhead will be incurred for the digital post filter in order to achieve matching to all possible NTFs. On the other hand, the single-loop architecture does not require any transfer function matching. Hence, the single-loop architecture is more appropriate for a tunable delta-sigma modulator.

As shown in Section 2.4, a $2n$-th-order tunable bandpass modulator achieves the minimum peak SQNR at the center frequency of $f_s/4$, and this SQNR coincides with that of an equivalent k-th-order lowpass modulator. Therefore, a lowpass modulator is evaluated as a prototype in order to determine the required order of the modulator and the number of bits of the quantizer.

According to [16, Ch.14], the maximum achievable SQNR (in dB) for the first-order and the second-order lowpass delta-sigma modulators with an N-bit quantizer are expressed as

$$\mathrm{SQNR} = 6.02\mathrm{N} + 1.76 - 5.17 + 30\log_{10}\mathrm{OSR} \tag{3.1}$$

$$\mathrm{SQNR} = 6.02\mathrm{N} + 1.76 - 12.9 + 50\log_{10}\mathrm{OSR}, \tag{3.2}$$

respectively. Therefore, in order to achieve an SQNR of 110 dB at an OSR of 96, N has to be at least 9 and 4 for a first-order modulator and a second-order modulator, respectively. Use of a 9-bit quantizer in a delta-sigma modulator is highly impractical due to the large required silicon area ($2^9 - 1 = 511$ comparators have to be placed), high power consumption, and the very stringent offset requirements on the comparators required to guarantee sufficient resolution. On the other hand, a 4-bit quantizer requires only fifteen comparators with relaxed offset requirements. In fact, many successful modulator implementations such as [6] and [17] with a quantizer of 4-bit resolution or more in the 0.18-μm CMOS technology have been reported.

A third-order lowpass prototype can also satisfy the specification with fewer bits in

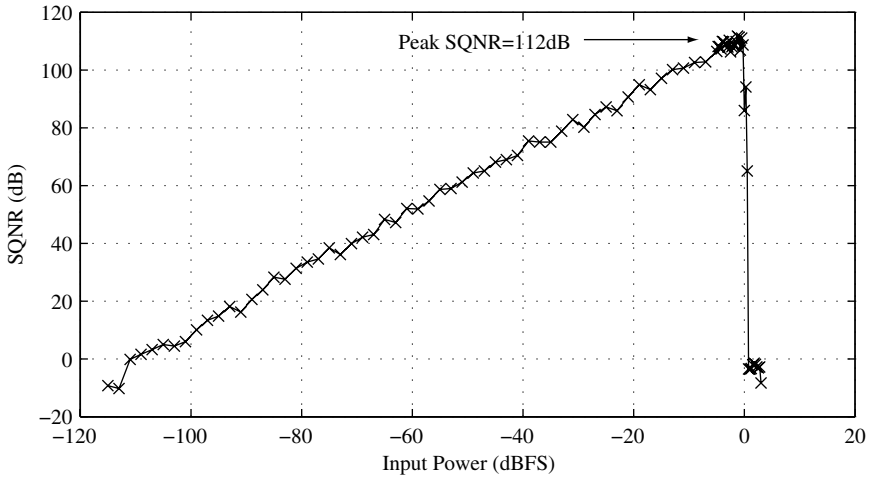

Figure 3.1: SQNR versus input level of the second-order modulator with a 4-bit quantizer.

the quantizer. However, the third-order lowpass prototype corresponds to a sixth-order tunable delta-sigma modulator. When such a tunable modulator is configured for a very low center frequency, it simply becomes a sixth-order lowpass delta-sigma modulator, which is difficult to stabilize without compromising the NTF and increasing the number of bits of the quantizer. Increasing the resolution of the quantizer will be an over-design for the bandpass configuration.

For these reasons, the second-order lowpass prototype with a 4-bit quantizer for the fourth-order tunable modulator with a 4-bit quantizer was chosen for the target specification.

In order to verify the achievable SQNR of the second-order modulator prototype, a simple 4-bit second-order modulator was simulated. Figure 3.1 shows the peak SQNR of 112 dB at -1.5 dBFS input power. This exceeds the target peak SQNR of 110 dB. Therefore, it can be concluded that a fourth-order tunable delta-sigma modulator with a 4-bit quantizer should also satisfy the same specification of 110 dB SQNR with an OSR of 96 for any center frequency from 0 to $f_s/2$.

3.4 Modulator Topology

Choice of a modulator topology is very important for a tunable delta-sigma modulator because required programmability of the switched-capacitor circuits is significantly reduced with a proper choice as shown in this section.

There are two general structures for a delta-sigma modulator with resonators. One is called a Cascade of Resonators with Feedback (CRFB) structure and the other is called a Cascade of Resonators with Feed-forward (CRFF) structure [10, Ch.5]. Fourth-order modulators with these structures are shown in Figures 3.2 (a) and 3.2 (b). Appendix A.1 and Appendix A.2 analyze these structures in detail.

As explained in Appendix A.1, for the CRFF structure, the NTF is a function of a_k, c_k, and g_k, and the STF is a function of a_k, b_k, c_k, and g_k. Interestingly, STF = 1 if $b_1 = c_1$, $b_2 = b_3 = b_4 = 0$, and $b_5 = 1$. STF = 1 is preferred for stability because such an STF does not amplify the input of any frequency. Amplification of the input signal by the STF is highly undesirable because it may overload the internal states of the modulator driving the modulator into instability. This condition for STF = 1 is very easy to achieve even in an actual implementation, and it does not affect the NTF at all because the NTF is independent of b_k. In other words, a change of the NTF for tunability does not bother the condition for STF = 1.

On the other hand for the CRFB structure, the required conditions for STF = 1 are $a_1 = b_1$, $a_2 = b_2$, $a_3 = b_3$, $b_4 = a_4$, and $b_5 = 1$. Since the NTF is a function of a_k, all of the a_k's and b_k's must be programmable in order to obtain different NTFs while satisfying the condition for STF = 1. This complicates the implementation of the modulator. In addition, existence of multiple DACs in the CRFB structure requires any DAC nonlinearity alleviation technique to be applied to multiple DACs (although not necessarily to all of the DACs because the nonlinearity of DACs close to the ADC are strongly attenuated by the modulator loop). As explained later, DEM is not preferable for a tunable modulator, and digital correction of multiple DACs is very cumbersome.

Thus, the CRFF structure, whose NTF can be varied freely without affecting STF, with a single DAC is the preferred structure for a tunable delta-sigma modulator.

3.5 Noise Transfer Functions (NTF) and Signal Transfer Functions (STF)

In order to achieve noise shaping for arbitrary center frequencies, the NTF must be programmable so that the NTF zero locations can be moved as desired. This requires synthesis of the NTFs for all possible center frequencies.

As explained in the previous section, STF is set to 1 for all of the center frequen-

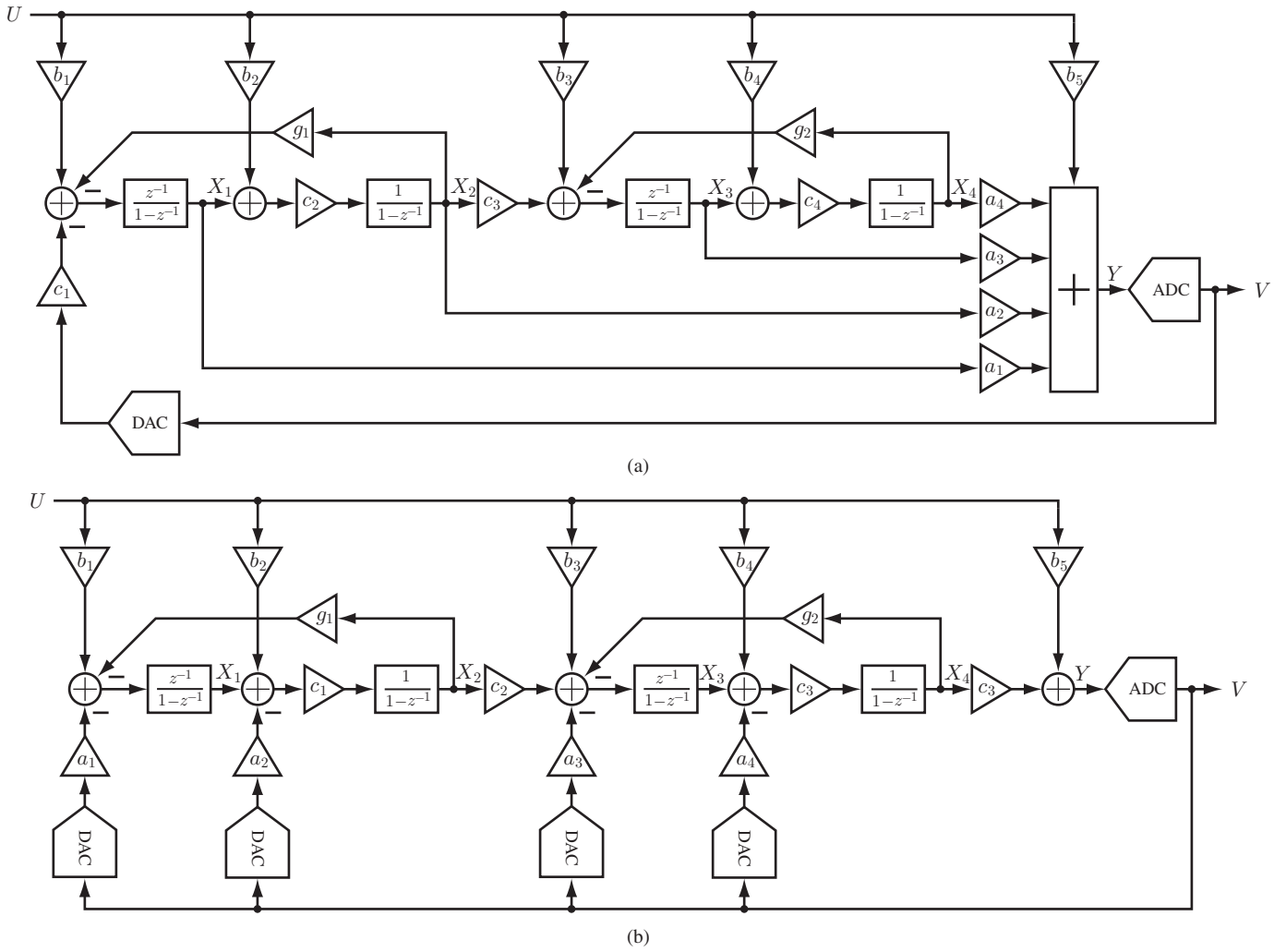

Figure 3.2: (a)Fourth-order CRFF Structure (b)Fourth-order CRFB structure.

cies. NTFs are synthesized with a computer program called *synthesizeNTF* in [18]. This computer program computes the optimal NTF for a given order, the center frequency, the OSR, and the out-of-band gain of a single-loop delta-sigma modulator. The obtained NTFs are passed to another computer program named *realizeNTF* in [18] in order to obtain the corresponding modulator coefficients such as a_k, b_k, c_k, and g_k in Figure 3.2.

Ideally, different out-of-band gains should be set for a specified center for the following reasons. For low (near DC) or high (near $f_s/2$) center frequencies, achievable SQNR is high due to proximity of the NTF zeros, but the modulator tends to be more unstable. Therefore, lower out-of-band noise gain is required. On the other hand, for the center frequencies near $f_s/4$, where the modulator operates as a bandpass modulator, the modulator is more stable but the achievable SQNR is not as good as it is at low and high center frequencies. Therefore, the out-of-band noise gain should be maximized in order to achieve the required SQNR for the bandpass region.

However, it takes excessive computation efforts to find the optimal out-of-band noise gain for each center frequency because the optimal out-of-band NTF gain must be found by extensive time-domain simulations, and there are three variables to sweep for the optimization: the input amplitude, the center frequency, and the out-of-band noise gain. Therefore, instead of optimizing the out-of-band NTF gain for each center frequency, it is kept constant over the center frequencies. It was found that an out-of-band noise gain of 2.8 results in an SQNR higher than 104 dB for any center frequency with two -7.5 dBFS input tones spaced 8.1 kHz apart [1] (total power of -4.5 dBFS) as shown in Figure 3.3. This SQNR is 8 dB lower than that of the second-order lowpass prototype because there is a 3-dB loss due to the use of a two-tone test instead of a single-tone test, plus additional loss due to the less aggressive out-of-band noise gain.

3.6 Modulator Coefficients and Dynamic Range Scaling

Now that the required NTFs and STFs have been established, the corresponding modulator coefficients can be found. For a tunable delta-sigma modulator there are multiple

[1] Two-tone input is required for a bandpass system in order to observe the effect of the nonlinearity [19, Ch.2]. With a single-tone input, harmonics due to the nonlinearity are out of band, and it does not affect the SNDR.

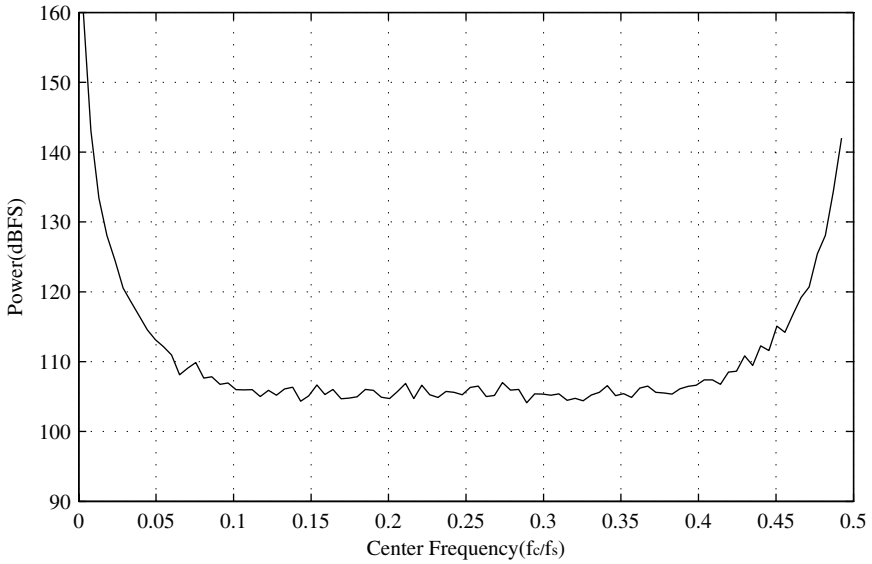

Figure 3.3: SQNR for different center frequencies for the tunable modulator at an OSR of 96 with two-tone input.

NTFs for different center frequencies. Therefore, multiple sets of the modulator coefficients must be found to realize the NTFs. In addition, output swing of the integrator is not constant for different configurations, so dynamic range scaling of the integrator output has to be performed for each configuration.

Figure 3.4 shows the values of the modulator coefficients a_k, b_k, c_k, g_k obtained with [18] for different center frequencies. For the simulations, the feedback DAC reference was set to 3.6 V_{pp} (differential, maximum possible for V_{DD}=1.8 V) to minimize the thermal noise contribution of the DAC (to be explained later in this chapter), and the ADC reference was set to 0.6 V_{pp} (differential) due to the limited acceptable input swing of the ADC (to be explained in the next chapter). Coefficients c_k are set to 1. They will later be used for dynamic range scaling of the integrator outputs. The simulated distribution of the output swing of each integrator is shown in Figure 3.5. Obviously, dynamic range scaling is needed to normalize the output swings across all center frequencies.

The maximum allowable output swing of the integrators depends on the OTA structure and their supply voltage because the output of an integrator is driven by the OTA in it. For this project, the gain-boosted fully-differential single-stage folded-cascode structure is selected (to be explained in the next chapter). This structure with a 1.8-V supply, which is the standard V_{DD} for the 0.18-μm CMOS technology, can achieve 1.6-V_{pp} differential

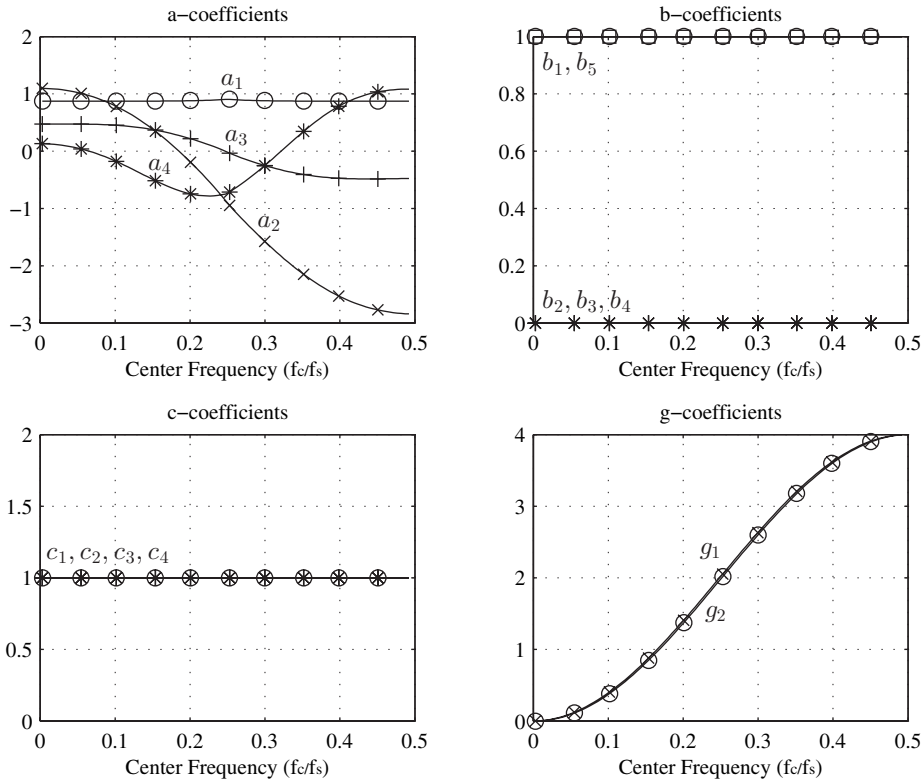

Figure 3.4: Modulator coefficients before dynamic range scaling.

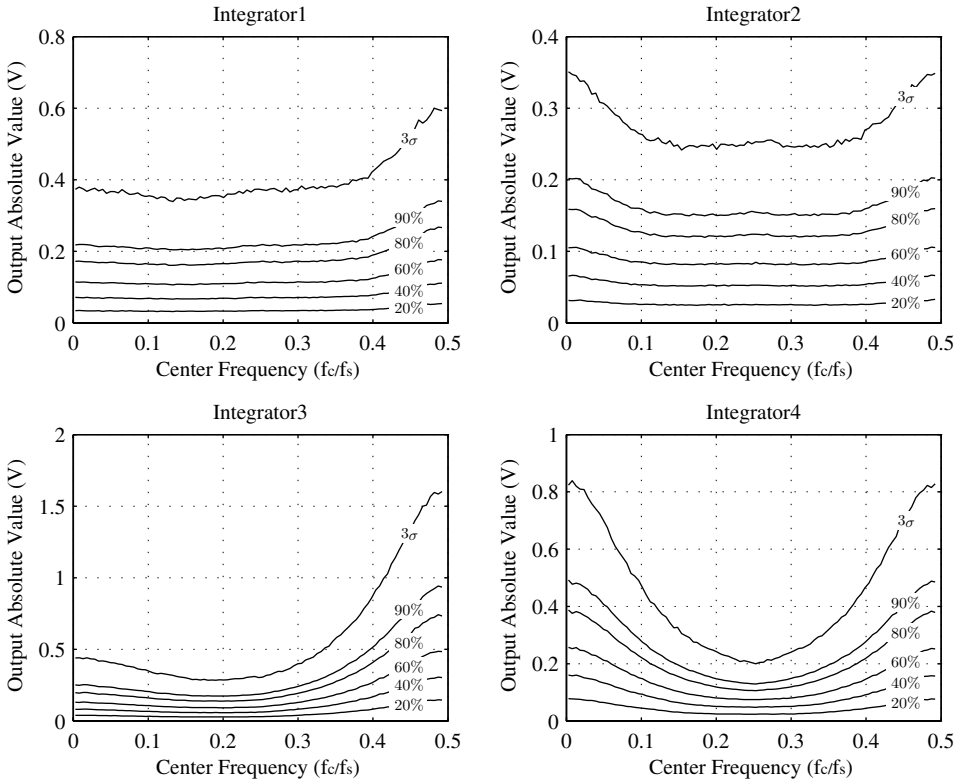

Figure 3.5: Integrator output swing for different center frequencies before dynamic range scaling.

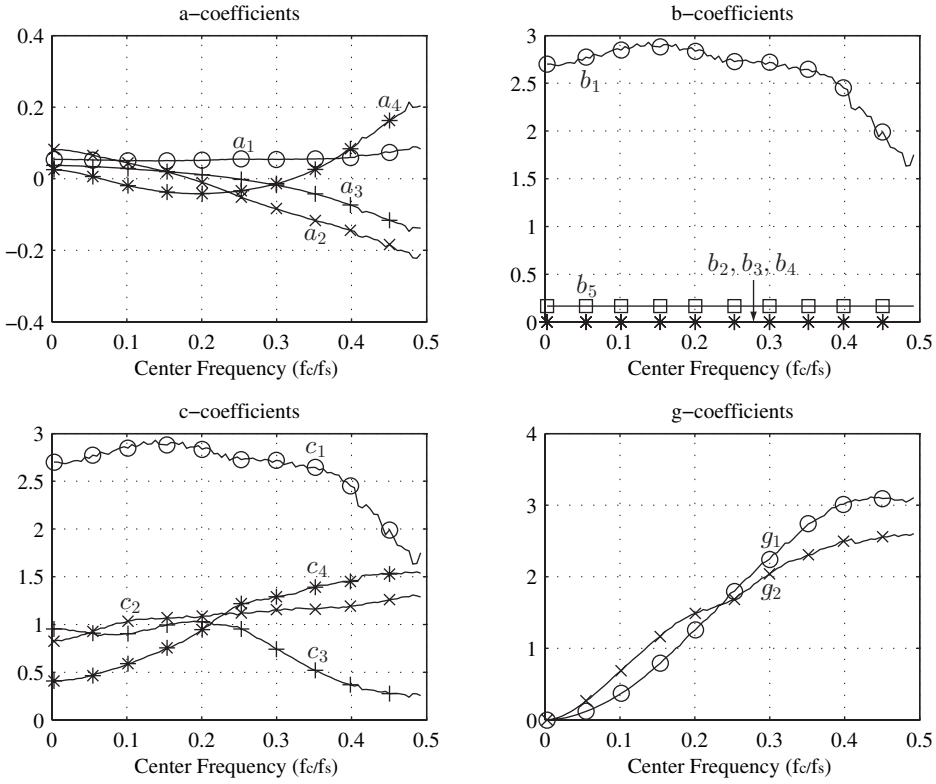

Figure 3.6: Modulator coefficients after dynamic range scaling.

output swing without too much drop of the DC gain. Therefore, the dynamic range scaling was performed in such a way that the 3σ-value (99.73%) of the output swing is 1.3 V_{pp} instead of 1.6 V_{pp} in order to accommodate any changes in the output swings resulting from quantization of the modulator coefficients (to be explained in the next section). It was assumed that overloading of the integrator will occur rarely enough to ensure that the modulator does not go into instability if the output swing is kept within the 3-σ range. This assumption can be verified in simulations.

Dynamic range scaling of the integrators by a factor of k was done by multiplying all of the input coefficients to the integrator by k, and dividing all of the output coefficients of the integrator by k. This way, output swing of the integrators can be controlled without affecting the NTF and the STF at all. For example, for the first integrator of the CRFF structure shown in Figure 3.2 (a), b_1, c_1, and g_1 are multiplied by k, and b_2, c_2 and a_2 are divided by k. Figures 3.6 and 3.7 show the modulator coefficients and the output swing of the integrators after the dynamic range scaling.

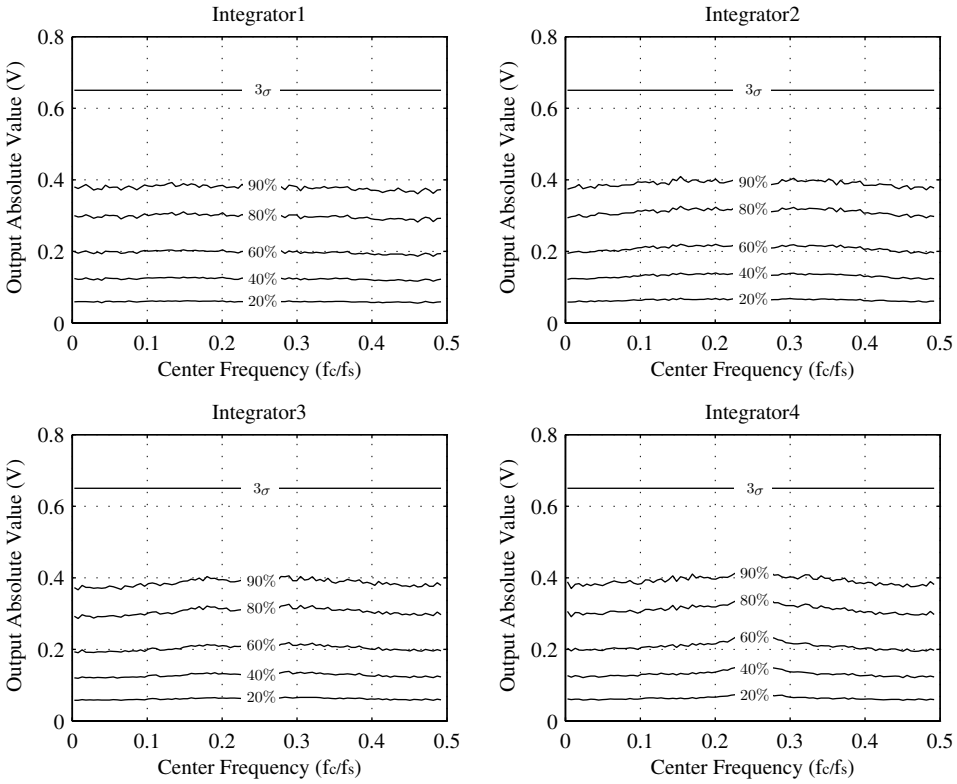

Figure 3.7: Integrator output after dynamic range scaling.

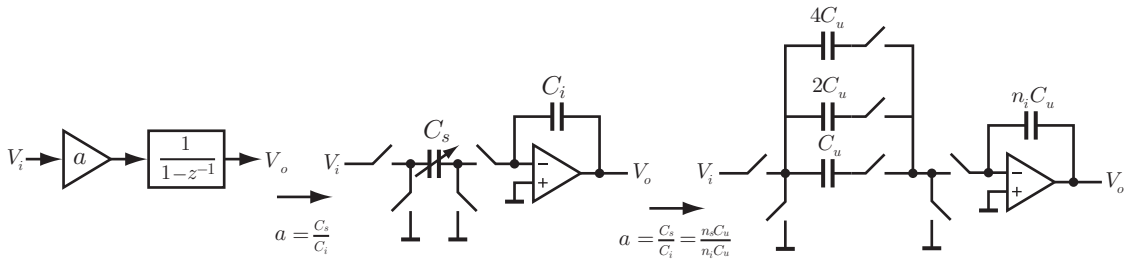

Figure 3.8: Conceptual implementation of a programmable coefficient.

3.7 Quantization of the Modulator Coefficients

In the previous section, full control of the modulator coefficients with an infinite resolution was assumed. In an actual implementation of the modulator, this is not the case because the modulator coefficients are determined by capacitor ratios. Programmability of the ratios is achieved by changing the number of active capacitors in programmable capacitor banks. That is, we have discrete control of the modulator coefficients, which requires quantization of the coefficients. Figure 3.8 shows the conceptual implementation of a quantized coefficient with 3-bit resolution. Quantization of the coefficients affects the following:

- NTF zero location
- NTF pole location
- Dynamic range scaling

Among these, a slight change in the NTF poles and dynamic range scaling is acceptable as long as stability is assured. On the other hand, shift of the NTF zero locations greatly affects the SQNR because it moves the notches of the NTFs away from the desired locations. Since the NTF zero locations coincide with the resonant frequencies, it is very important to maintain accuracy of the pole locations of the resonators. A block diagram of the resonator used in the modulator is shown in Figure 3.9. The transfer function of the resonator is

$$H_r(z) = \frac{Y}{X} = \frac{cz^{-1}}{z^{-2} + (cg - 2)z^{-1} + 1}. \tag{3.3}$$

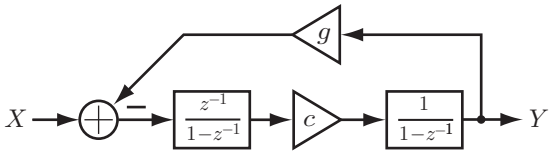

Figure 3.9: Discrete-time resonator.

Since the absolute values of the pole locations are 1 for $0 \leq cg \leq 4$, poles are always located on the z-domain unit circle. The resonant frequency of the resonator is given as

$$f_r = \frac{\tan^{-1} \frac{\sqrt{4cg - c^2g^2}}{2-cg}}{2\pi}. \tag{3.4}$$

That is, the NTF notch frequencies are a function of the product cg . Multiplication of two quantized variables may generate a large error because

$$(c + \Delta c)(g + \Delta g) = cg + c\Delta g + g\Delta c + \Delta c\Delta g. \tag{3.5}$$

This equation suggests that Δg and Δc must be very small for a small error of the product. A proper approach is, rather than quantizing the two variables simultaneously, to first quantize one of the variables with moderate resolution and quantize the other variable with high resolution in such a way that the error of cg is minimized. To describe the approach mathematically, let $c_q \equiv c + \Delta c$. If one can make the new value of g: $g' = \frac{cg}{c_q}$, there will be no change in the NTF zeros. After quantization of g', $g'_q = g' + \Delta g'$, and

$$g'_q c_q = c_q(g' + \Delta g') = c_q g' + c_q \Delta g'. \tag{3.6}$$

Since $c_q g' = cg$, the error due to the quantization of c and g is only $c_q \Delta g'$ instead of $c\Delta g + g\Delta c + \Delta c\Delta g$.. Therefore, high resolution of g (for small Δg) yields small errors in the NTF notch frequencies.

The modulator coefficients are realized by the ratio of a sampling capacitor and an integrating capacitor. A simplified single-ended version of the modulator schematic is shown in Figure 3.10. The first four OTAs are for the four integrators, and OTA5 is for the last stage, which sums the feed-forward signals. All of the variable capacitors are realized with programmable capacitor banks like that shown in Figure 3.8 except for the first integrator. The relationship between the modulator coefficients and the capacitor sizes is shown in Table 3.1. For the first integrator, C_{i1} is made programmable instead of its sampling capacitors C_{sb_1} and ΣC_D because ΣC_D cannot be changed for digital correction

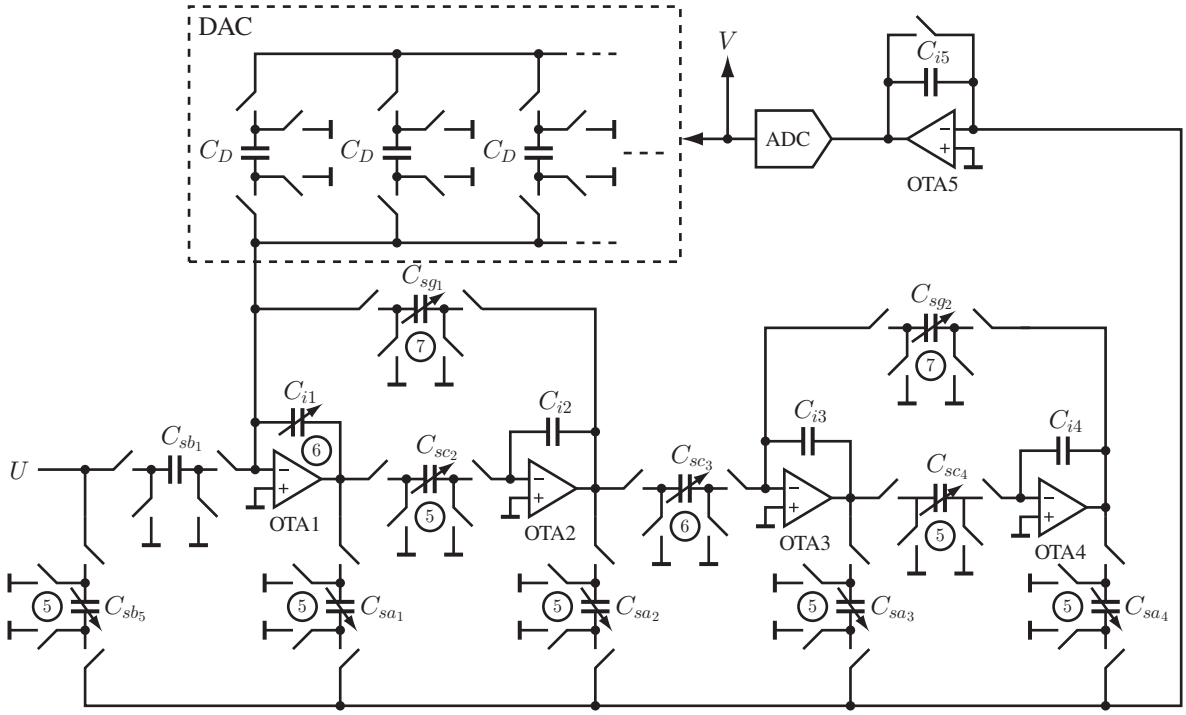

Figure 3.10: Simplified single-ended version of the modulator.

Table 3.1: Expressions for the modulator coefficients.

a_1	a_2	a_3	a_4	b_1	b_5	c_1	c_2	c_3	c_4	g_1	g_2
$\frac{C_{sa_1}}{C_{i5}}$	$\frac{C_{sa_2}}{C_{i5}}$	$\frac{C_{sa_3}}{C_{i5}}$	$\frac{C_{sa_4}}{C_{i5}}$	$\frac{C_{sb_1}}{C_{i1}}$	$\frac{C_{sb_5}}{C_{i5}}$	$\frac{\sum C_D}{C_{i1}}$	$\frac{C_{sc_2}}{C_{i2}}$	$\frac{C_{sc_3}}{C_{i3}}$	$\frac{C_{sc_4}}{C_{i4}}$	$\frac{C_{sg_1}}{C_{i1}}$	$\frac{C_{sg_2}}{C_{i3}}$

purposes. This causes b_1 and c_1 to vary together, but this is not a problem because $b_1 = c_1$ is the required condition for STF $= 1$. For the other integrators, the sampling capacitors are made programmable for individual control of the modulator coefficients. The resolutions of the programmable capacitor banks were minimized to save silicon area. They were determined by trying to reduce the resolution of the coefficients until the loss of SQNR becomes unacceptable. The circled numbers in Figure 3.10 are the resolutions in bits of the programmable capacitor banks. Table 3.2 shows the programmability of the capacitor banks.

Figure 3.11 shows the modulator coefficients after proper quantization. The output swing of the modulator is disturbed by the quantization as expected as shown in Figure 3.12. However, the fluctuation is still within the acceptable range. Figure 3.13 compares the SQNR before and after proper and improper quantization. The SQNR is obviously

Table 3.2: Programmability of the capacitors banks.

Sampling capacitor	C_{sb_1}	$\sum C_D$	C_{sg_1}	C_{sc_2}	C_{sc_3}	C_{sg_2}	C_{sc_4}	C_{sb_5}	C_{sa_k}
Number of unit capacitors	45	45	0-127	0-31	0-63	0-127	0-31	0-31	0-31
Integrating capacitor	C_i1			C_{i2}	C_{i3}		C_{i4}	C_i5	
Number of unit capacitors	0-63			16	48		16	90	
Unit capacitor	C_{u1}			C_{u2}	C_{u3}		C_{u4}	C_{u5}	

degraded due to quantization of the modulator coefficients. This is mainly due to shifts of the NTF zero locations caused by coefficient quantization. Improper quantization leads to much more significant loss of the SQNR especially at center frequencies beyond $f_s/4$ compared to the proper quantization. As explained later, thermal noise limits the maximum SNR. Therefore, the loss of SQNR due to proper coefficient quantization will eventually be almost negligible. This is not the case for the improper quantization because the SQNR is far below 90 dB for high center frequencies above $f_s/4$ as shown in Figure 3.13.

3.8 Digital Correction for DAC Nonlinearity

Any high-resolution multi-bit delta-sigma modulator requires compensation of DAC nonlinearity as explained in the previous chapter. For a multi-bit tunable delta-sigma modulator, not all of the techniques are preferable because of its programmable NTF zero locations, and in fact, the digital correction technique is the preferred technique. In order to measure the DAC output for digital correction, the tunable modulator can be easily transformed to a lowpass delta-sigma modulator with the multi-bit DAC as the input. Effectiveness of the technique is verified with simulations, and its robustness against gain error and offset in the digital representation of the DAC output is investigated.

As explained in the previous chapter, nonlinearity of the DAC is unfortunately not shaped by the modulator loop, and the in-band error component of the DAC can be directly referred to the output of the modulator. Since the DAC input contains signal components $\mathrm{STF}(z)U(z)$ as well as the shaped quantization noise $\mathrm{NTF}(z)e_Q(z)$, the nonlinearity of the DAC generates harmonics of the input signal and raises the in-band noise floor due to the aliasing of the shaped quantization noise. Therefore, if uncompensated, the DAC nonlinearity limits the modulator's SNDR.

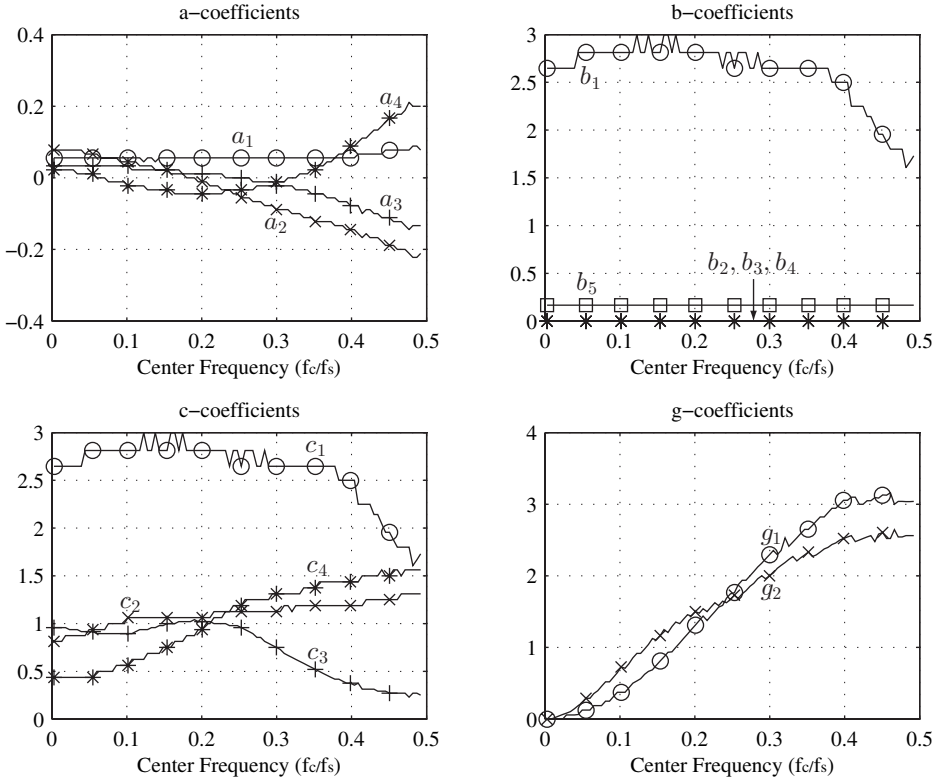

Figure 3.11: Quantized modulator coefficients.

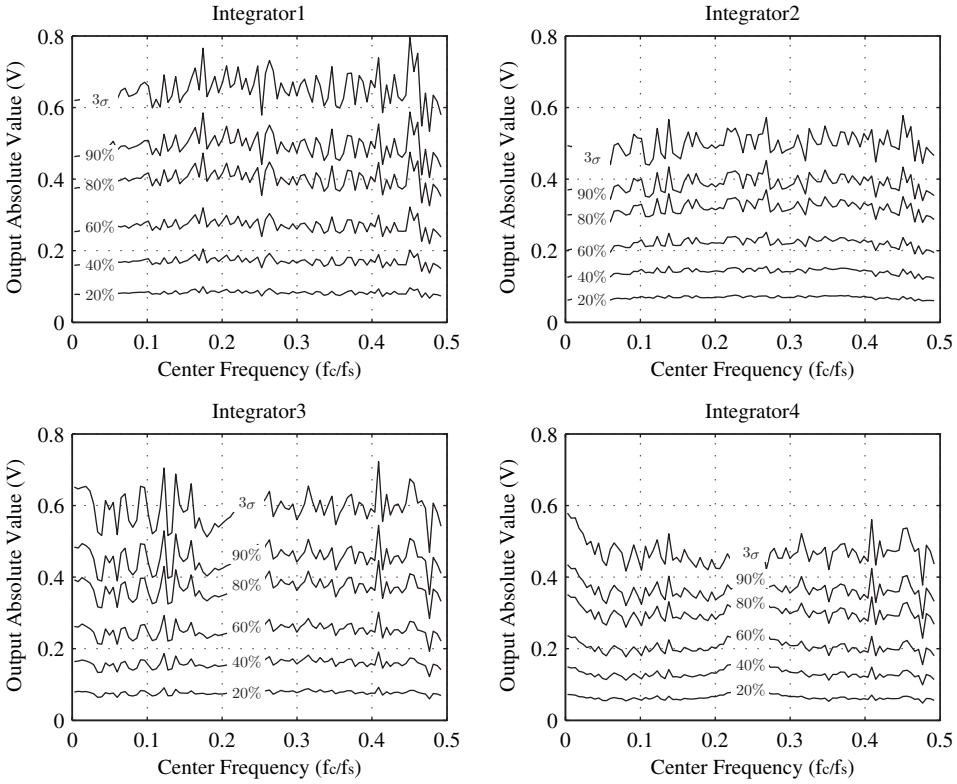

Figure 3.12: Integrator output after coefficient quantization.

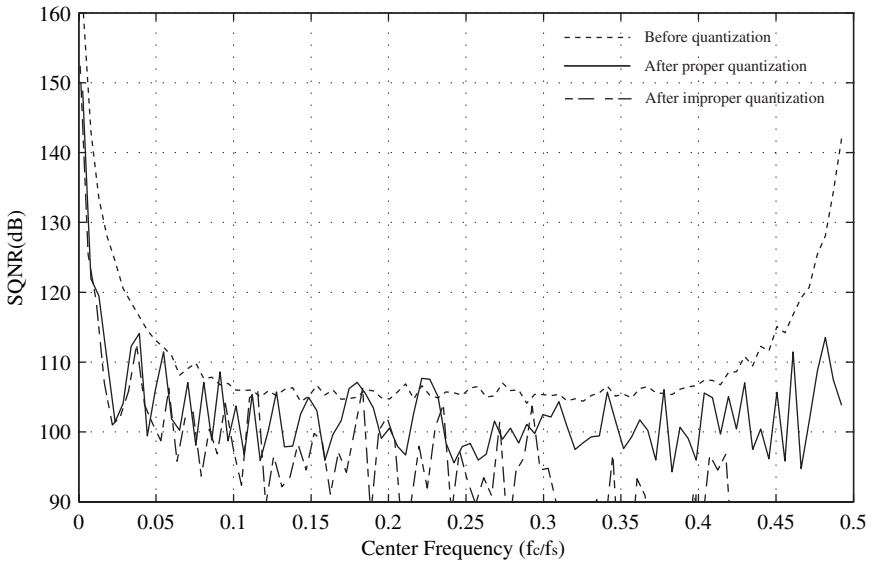

Figure 3.13: SQNR after modulator coefficient quantization.

There are two major methods (DEM and digital correction) for DAC nonlinearity mitigation as shown in Section 2.3. However, applying established DEM techniques to the tunable modulator is not preferred because most of DEM techniques are only appicalble to lowpass delta-sigma modulators, and even with a DEM technique compatible with a tunable modulator, a large hardware overhead is expected since the unit-element selection algorithm has to be able to cover all possible center frequencies. The digital correction technique is preferred because the same and simple algorithm can be applied to any center frequency of the tunable modulator because it cancels the in-band DAC nonlinearity based on the fact that

$$V \approx \mathrm{STF}(z) \cdot U + \mathrm{NTF}(z) - e_{DAC}(V) \tag{3.7}$$

for the band of interest due to a high loop gain of the modulator.

3.8.1 Measurement of DAC Output

The idea of digital correction is to measure all possible outputs of the DAC, $V(z) + e_{DAC}(V)$, very accurately before operating the modulator. Then, the effects of DAC output errors are digitally canceled during normal operation at the modulator output by replacing the modulator digital output V with $V + e_{DAC}(V)$.

One possibility is to build an independent ADC outside the modulator just to measure the DAC output. Alternately, due to its required programmability, it is very easy to reconfigure the tunable modulator with minor modifications to perform the DAC output measurements.

The approach is to reconfigure the tunable modulator as a single-bit second-order lowpass modulator as shown in Figure 3.14. The central comparator of the multi-bit ADC can be used as a single-bit ADC since the number of quantization levels is even. This output is fed back to a single-bit DAC, which is inherently linear. Since a single-bit quantizer is used in the modulator loop, the last two integrators are disabled to form a second-order modulator for robust stability. The single-bit delta-sigma modulated DAC output appears at the output of the ADC, and the DAC output for each input code can be measured by averaging the output of the modulator since the DAC output under measurement is DC.

For $b_1 = 1, a_1 = 1, a_2 = 1, c_2 = 1$, the STF and the NTF are given as

$$\mathrm{STF}(z) = c_1 z^{-1} \left(2 - z^{-1}\right) \tag{3.8}$$

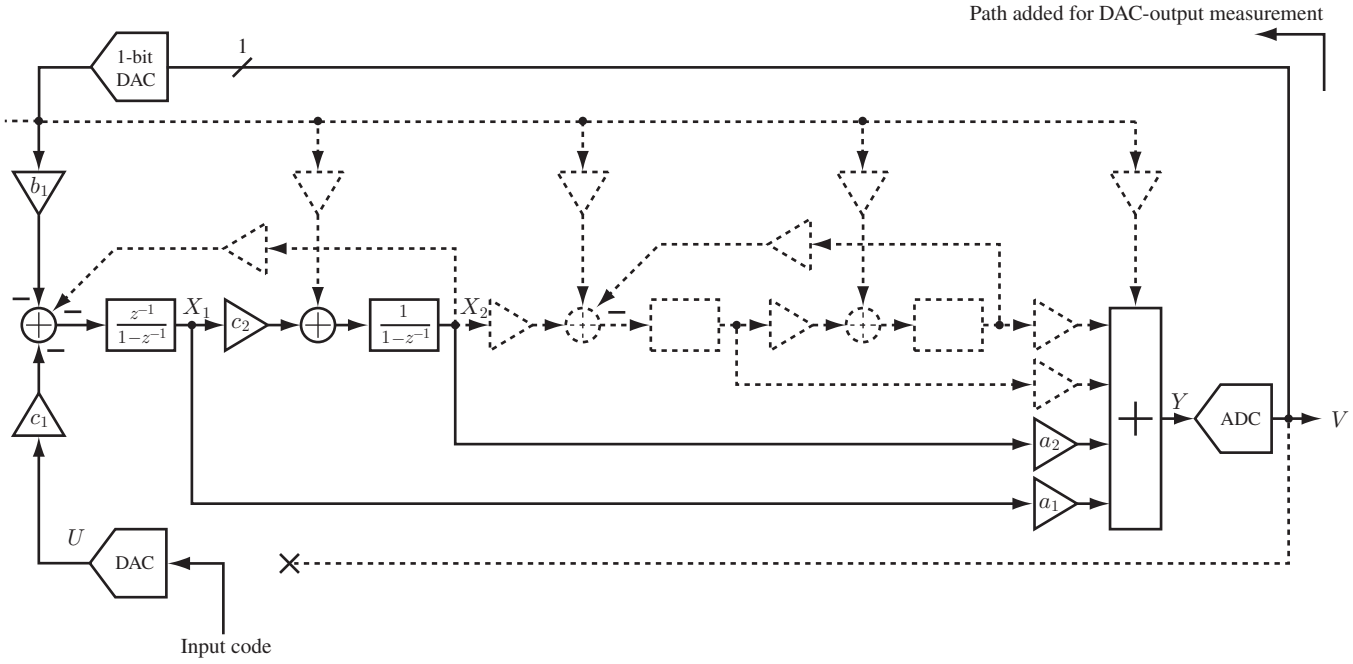

Figure 3.14: Modulator configuration to measure the DAC nonlinearity for digital correction.

$$\mathrm{NTF}(z) = \left(1 - z^{-1}\right)^2 \tag{3.9}$$

Unlike the normal operation of the tunable modulator, the STF in this configuration is not unity. It actually has a maximum gain of $3c_1$ at $f_s/2$. This is due to the lack of a feed-forward path from the input to the ADC. However, this is not a problem because the input to the modulator is DC. The DC gain of STF is $\frac{c_1}{b_1}$. It is very important to keep c_1 less than b_1 since the DAC output swings at full scale relative to the reference level of the single-bit feedback DAC. In this case, c_1 was made $\frac{3}{4}b_1$ This can be done by adding 15 unit capacitors to C_{sb_1}. The attenuation of the DAC output due to this condition can be corrected digitally.

Dynamic range scaling of the integrator outputs and quantization of the coefficients were done in the same manner described in the previous section. It was difficult to limit the swing at the integrator outputs within the acceptable range when a 3.6-V_{pp} reference was used for both the multi-bit DAC under measurement and the single-bit DAC for feedback with the available programmability of the integrator. This is due to lack of an input feed-forward path[2], and the use of a single-bit quantizer. Therefore, the reference

[2]Lack of the input forward in the CRFF structure causes the loop filter to process both the input

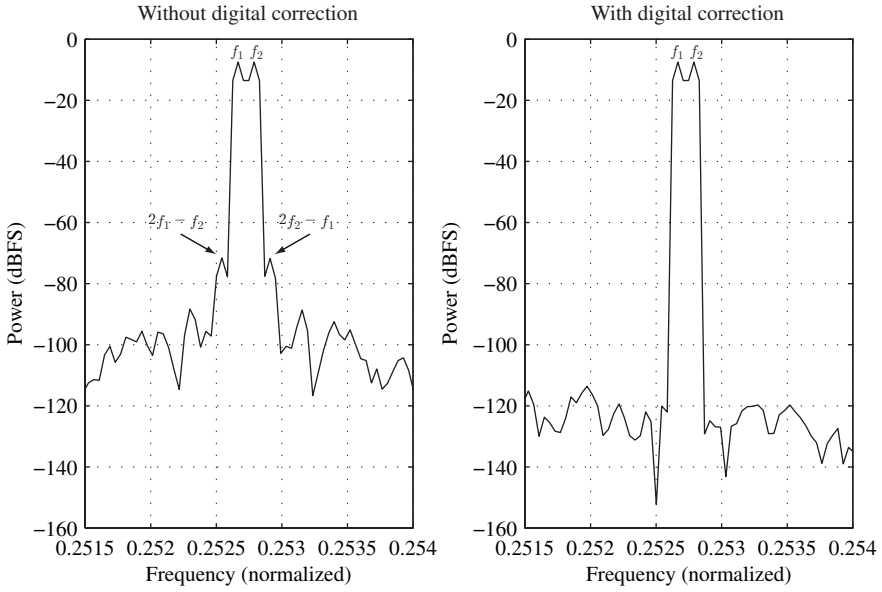

Figure 3.15: Modulator output spectra without and with digital correction.

voltages were reduced to 0.6 V_{pp} for the measurement of the multi-bit DAC output, in order to scale down the output swing of the integrators.

During the measurement of the DAC output, its digital input code is supplied externally and held constant while the modulator operates to obtain a digital representation of the DC DAC output. This is done by averaging the 1-bit output of the modulator over a long time window. According to [14], at least 2^N samples must be averaged for an N-bit accurate delta-sigma modulator.

For evaluation and simulations of the digital correction technique, mismatch of the DAC unit elements with a standard deviation of 0.5 % was assumed. Figure 3.15 compares the output of the simulated modulator without and with the digital correction technique. The intermodulation products due to the DAC nonlinearity disappear, and the noise floor is loweredl after digital correction. Figure 3.16 compares the SNDR achieved for different values of N used in the digital correction. $N = 15$ is insufficient because it limits the SNDR to about 92 dB. The thermal noise may lower it to a value below 90 dB. $N = 16$ is very marginal, and a value of $N = 17$ was chosen because it has enough margin to accommodate degradation due to thermal noise.

signal and the quantization noise [20].

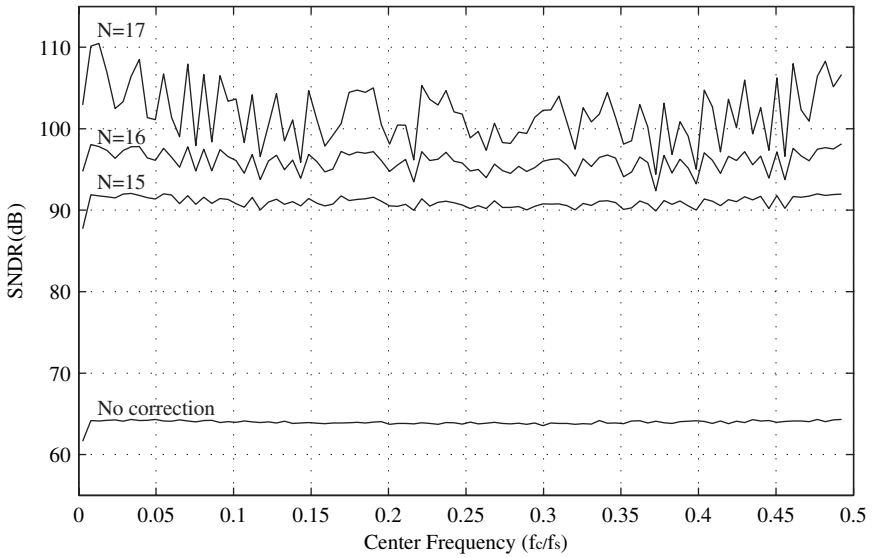

Figure 3.16: Comparison of SNDR without/with digital correction.

3.8.2 Effects of Nonidealities During DAC Output Measurement

In the previous section, an ideal operation of the modulator during DAC output measurement was assumed. In reality, due to a DC offset of the OTA and mismatch between capacitors, which changes STF of the modulator during measurement, digital representation of the DAC output is altered. Assuming excellent linearity of the modulator, the error in digital output can be classified into two categories: DC offset and gain error. Therefore, the output of the DAC is

$$V_{DAC}(V) = [V + e_{DAC}(V)](1 + \alpha) + e_{off}, \tag{3.10}$$

where V is the ideal output of the DAC, e_{DAC} is the actual DAC output error, α is the gain error, and e_{off} is the offset error. $V_{DAC}(V)$ replaces V during the normal operation of the modulator to perform digital correction. Substituting (3.10) into V of (3.7) yields the following result.

$$\begin{aligned} [V + e_{DAC}(V)](1 + \alpha) + e_{off} &= V + \alpha V + e_{DAC}(V) + \alpha e_{DAC}(V) + e_{off} \\ &= (1 + \alpha)\mathrm{STF}(z) \cdot U + (1 + \alpha)\mathrm{NTF}(z) \cdot e_Q \\ &\quad + e_{off}. \end{aligned} \tag{3.11}$$

Therefore, even with a gain error in the DAC output measurement, the DAC output error is still canceled although it introduces an offset and a gain error to the output. Since both the STF and the NTF are multiplied by the same factor $1 + \alpha$, the SNDR will not be affected by the gain error. Thus, as long as the DAC output is measured linearly, the effects of the DAC nonlinearity is well canceled even with an offset and gain error in the measurement. This was confirmed in simulations as well.

3.9 Thermal Noise and Capacitor Sizing

For a tunable delta-sigma modulator, its NTF and size of capacitors are programmable. This changes the contribution of the thermal sources to the SNR for different configurations. Therefore, a thermal noise analysis for all possible configurations is required.

Up to this point, the integrators have been assumed to be noiseless. However, thermal noise of the integrators actually tends to limit the SNR in switched-capacitor circuits [21]. Therefore, an analysis of thermal noise is indispensable for the design of delta-sigma modulators that utilize switched-capacitor circuits.

Since a delta-sigma modulator is a negative feedback system, noise injected anywhere in the loop filter is attenuated by the gain of the previous stages when referred to the input of the modulator. Therefore, for the tunable modulator, the effect of noise in the second resonator is attenuated by the gain of the first resonator. Since the resonators have a high gain in the band of interest, in-band noise of the second resonator is significantly reduced by the gain of the first resonator. Therefore, the noise in the second resonator can be considered negligible as long as its power is reasonable. For the first resonator, however, there is no preceding filter to attenuate its noise. Therefore, its contribution to thermal noise must be carefully studied.

Figure 3.17 is used to analyze the contribution of thermal noise from different switched-capacitor (SC) branches. There are three SC branches for the first integrator: Input sampling SC (b_1), DAC SC ($c1$), and feedback SC (g_1), and one SC branch for the second integrator: sampling SC (c_2). The input-referred noise power e_i in terms of these three noise sources is

$$e_i = e_{b_1} + e_{c_1}\left(\frac{c_1}{b_1}\right) + e_{g_1}\left(\frac{g_1}{b_1}\right) + e_{c_2}\left(\frac{1 - z^{-1}}{b_1}\right), \tag{3.12}$$

where e_{b_1}, e_{c_1}, e_{c_2}, and e_{g_1} are white and uncorrelated.

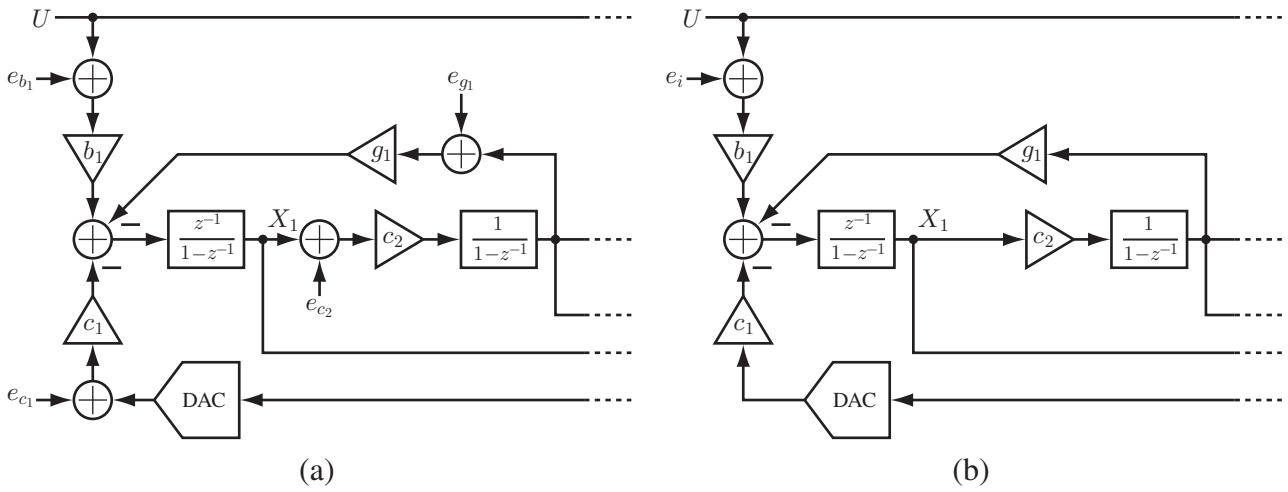

Figure 3.17: Noise sources of the first resonator and its input-referred thermal noise equivalent.

The power of the thermal noises e_{b_1}, e_{c_1}, e_{c_2}, and e_{g_1} is a function of the size of the sampling capacitors C_{sb_1}, $\sum C_D$, C_{sc_2}, and C_{sg_1}, respectively. For a fully differential switched-capacitor integrator, the input-referred noise can be approximated as $\frac{4kT}{C_s}$, where k is the Boltzmann constant ($1.38 \times 10^{-23}\mathrm{JK}^{-1}$), T is the temperature in Kelvin, and C_s is the capacitance of the sampling capacitor. Therefore,

$$\overline{{e_{b_1}}^2} = \frac{1}{\mathrm{OSR}} \cdot \frac{4kT}{C_{sb_1}} \quad \overline{{e_{c_1}}^2} = \frac{1}{\mathrm{OSR}} \cdot \frac{4kT}{\sum C_D} \quad \overline{{e_{c_2}}^2} = \frac{1}{\mathrm{OSR}} \cdot \frac{4kT}{C_{sc_2}} \quad \overline{{e_{g_1}}^2} = \frac{1}{\mathrm{OSR}} \cdot \frac{4kT}{C_{sg_1}} \tag{3.13}$$

Plugging these and the expressions in 3.1 into (3.12), the input-referred noise is given as

$$\overline{{e_i}^2} = \frac{4kT}{\mathrm{OSR}} \left[\frac{1}{C_{sb_1}} + \frac{\sum C_D}{{C_{sb_1}}^2} + \frac{C_{sg_1}}{{C_{sb_1}}^2} + \frac{1}{b_1^2 C_{sc_2}} \left| 1 - e^{-j2\pi f_c} \right|^2 \right] \tag{3.14}$$

where f_c is the normalized center frequency, and $|1 - z^{-1}|$ was assumed to be constant for a narrow frequency band around the center frequency f_c. (3.14) indicates that a smaller C_D is preferred for a lower input-referred noise power. Reduction of $\sum C_D$ requires an increase in the DAC reference voltage so that the charge transferred to the integrating capacitor of the first integrator by the DAC does not change, resulting in the same NTF and STF. This is the reason why a large reference voltage of 3.6 $\mathrm{V_{pp}}$ (differential) was assumed in the previous section. Unfortunately, use of this reference voltage is not very practical because it requires 1.8-V and 0-V reference voltages which are difficult to buffer with a 1.8-V power supply. Since this concern was overlooked during the design phase, these voltages were selected for the implementaion.

3.9.1 Capacitor Sizing

As shown in (3.14), the input-referred noise e_i is a function of the capacitance of the sampling capacitors such as C_{sg_1}. These capacitors are realized by digitally-programmable capacitor banks. Therefore, the capacitances are expressed as

$$C_{sb_1} = n_{b_1} C_{u1} \quad C_{sc_2} = n_{c_2} C_{u2} \quad C_{sg_1} = n_{g_1} C_{u1}, \tag{3.15}$$

where C_{u1} and C_{u2} are unit-sized capacitors, the n_x parameters are integers in the range of 0 to 2^{M_x-1}, and M_X is the number of bits used to quantize the capacitors C_{sx}. Since C_{sb_1}, C_{sc_1}, and C_{sg_1} share the same integrating capacitor C_{i1} as shown in Figure 3.10, they are realized with the same unit capacitor C_{u1}. At this point, C_{u1} and C_{u2} are the only parameters that can be chosen to control the power of the input referred noise $\overline{e_i^2}$ because all other parameters have been already determined.

Plugging (3.15) into (3.14),

$$\overline{e_i^2} = \frac{4kT}{\text{OSR}} \left[\frac{2}{n_{b_1} C_{u1}} + \left(\frac{n_{g_1}}{n_{b_1}^2 C_{u1}} + \frac{\left|1 - e^{-j2\pi f_c}\right|^2}{b_1^2 n_{c2} C_{u2}} \right) \right], \tag{3.16}$$

where we have assumed $C_{sb_1} = \sum C_D$ because $n_{b_1} = n_{c_1}$ in this modulator.

As explained in the previous section, C_{sb_1} and $\sum C_D$ are fixed. n_{b_1} is fixed as well. Therefore, the thermal noise contribution of the two SC branches associated with these two capacitors is constant for $\frac{4kT}{\text{OSR}} \cdot \frac{2}{n_{b_1}} C_{u1}$ for any center frequency of the modulator. On the other hand, n_{c_2}, b_1, and n_{g_1} are programmable. As shown in Figure 3.11, g_1 is near zero for very low center frequencies, so n_{g_1} is also very close to zero. $\left|1 - e^{-j2\pi f_c}\right|^2$ is also close to zero for low center frequencies. As the center frequency increases, the contribution of these increase. This center-frequency dependent contribution is $\frac{4kT}{\text{OSR}} \cdot \frac{n_{g_1}}{n_{b_1}^2 C_{u1}} + \frac{\left|1-e^{-j2\pi f_c}\right|^2}{b_1^2 n_{c2} C_{u2}}$. Note that the last term increases as f_c goes from 0 (DC) to 0.5. Also, n_g increases as f_c increases.

One approach to ensure a sufficient SNDR for all center frequencies is to have a very high SNDR at low center frequencies and to allow a large drop in the SNDR due to the center-frequency dependent noise term. The other approach is to have a lower SNDR at the low center frequencies and to minimize the drop in SNDR due to the center-frequency dependent noise term. The former approach was chosen to maximize the maximum achievable SNDR.

Maximum achievable SNDR for a very low center frequency is obtained by letting $f_c = 0$ and $n_{g1} = 0$ as

$$\text{SNDR} = \frac{P_s}{\overline{e_i^2}} = 10\log_{10}\left(\frac{n_{b_1} C_{u1} P_s \text{OSR}}{8kT}\right) \tag{3.17}$$

where $n_{b_1} = 45$, and $P_s = 1.15$ V^2 (-1.5 dBFS) is the input power providing peak SNDR. As shown in Figure 3.16, 100-dB SNDR for a very low center frequency is a reasonable target. From (3.17), $C_{u1} = 66$ fF is required for 100-dB SNDR. To provide a safety margin, $C_{u1} = 100$ fF is chosen.

The lowest SNDR occurs at a very high center frequency near $f_s/2$. Since n_{g_1} and $\frac{\left|1-e^{-j2\pi f_c}\right|^2}{n_{c2}}$ almost monotonically increase with center frequency, we assume that the lowest SNDR occurs at a center frequency very close to $f_s/2$. At this center frequency,

$$\text{SNDR} = 10\log_{10}\frac{P_s \text{OSR}}{4kT\left(\frac{2}{n_{b_1} C_{u1}} + \frac{n_{g_1}}{n_{b_1}^2 C_{b1}} + \frac{4}{b_1^2 n_{c_2} C_{u2}}\right)} \tag{3.18}$$

where $n_{g_1} = 79$, $b_1 = 1.75$ and $n_{c_2} = 21$. Solving (3.18) for C_{u2}, $C_{u2} = 25$ fF is required for a 93-dB SNDR at this center frequency. $C_{u2} = 50$ fF is chosen to provide a safety margin.

For the second resonator and the last gain stage, C_{u3}, C_{u4}, and C_{u5} are made equal to 25 fF, which is close to the smallest size permitted by the fabrication design rules, because very strong attenuation of their thermal noise is provided by the first resonator. This is verified with simulations.

Figure 3.18 shows the SNDR from a simulation with all of the thermal noise sources included. As expected, the SNDR is near 100 dB for a very low center frequency, and it drops down to almost 90 dB for the center frequency close to $f_s/2$.

3.10 Analysis of Circuit Non-idealities

It is quite difficult to simulate multiple configurations of the tunable delta-sigma modulator in transistor level because of the longer simulation times. Therefore, some of the circuit-level nonidealities are included in high-level simulations for more realistic analysis of the modulator.

So far in this chapter, the integrators have been assumed to be ideal (with thermal noise). In reality, the integrators have non-zero output time constants, finite slew rate, and

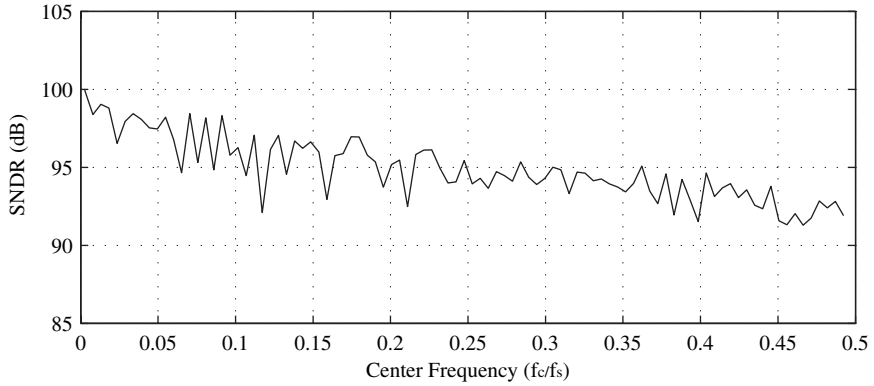

Figure 3.18: SNDR from a simulation with coefficient quantization and thermal noise sources.

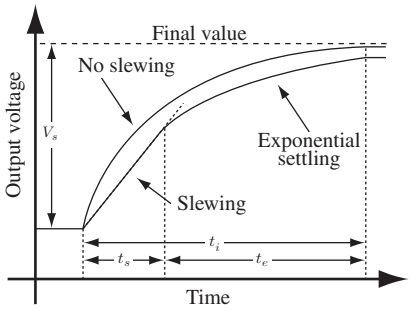

Figure 3.19: Effects of slewing and a non-zero time constant.

finite DC gain. System-level simulations must be used to determine specifications on these non-idealities before starting transistor-level design of the modulator because transistor-level simulations of a delta-sigma modulator are very time consuming. Fortunately, these circuit non-idealities can be simulated in a high-level discrete-time simulation in much less time.

3.10.1 Slewing and finite settling time of the OTAs

The two major factors limiting the settling accuracy of the integrator output are slewing and its non-zero time constant. A finite slew rate limits the maximum slope of the output voltage over time due to the finite bias current of an OTA which is used to charge and discharge the load capacitors [22, Ch.10]. On the other hand, the non-zero time constant is due to the finite transconductance (g_m) of the OTA, and the load capacitors [16, Ch.6]. Figure 3.19 illustrates the effects of these non-idealities.

Assuming a single-pole OTA, the effect of the finite slew rate and the non-zero time constant can be incorporated into a difference equation description of an integrator as shown below [23] given the known values of the slew rate (SR), the time constant (τ), the integration time(t_i), and the ideal output step (V_s).

$$V_o = \begin{cases} V_o z^{-1} + sgn(V_s)SRt_s + [V_s - sgn(V_s)SRt_s]\left(1 - e^{-\frac{t_i - t_s}{\tau}}\right) & t_s > 0 \\ V_o z^{-1} + V_s\left(1 - e^{-\frac{t_i}{\tau}}\right) & t_s \leq 0 \end{cases} \tag{3.19}$$

where $t_s = \frac{V_s}{SR} - \tau$.

For the circuit design of the OTAs, τ is not a useful parameter because it depends mainly on the transconductance g_m of the OTA, the load capacitance C_L, and the feedback coefficient β. According to [16, Ch.5], $\tau = \frac{1}{\beta\omega_{ut}}$, and $\omega_{ut} = \frac{g_m}{C_L}$ for a single-pole OTA. Therefore,

$$\tau = \frac{C_L}{\beta g_m}, \tag{3.20}$$

where β is the ratio of the sampling capacitors to the integrating capacitor. Figure 3.20 shows C_L, β, and $\frac{C_L}{\beta}$ for OTAs in the modulator. Figure 3.20(c) and (3.20) suggest that for a given time constant, τ, higher values of g_m are required for high center frequencies. Therefore, the tunable modulator requires much higher g_m than conventional lowpass delta-sigma modulators. This is one of the reasons why the tunable delta-sigma modulator cannot compete with lowpass delta-sigma modulators with a fixed center frequency in terms of FOMs.

3.10.2 Finite DC Gain of OTAs

The transfer functions $H(z) = \frac{z^{-1}}{1-z^{-1}}$ and $H(z) = \frac{1}{1-z^{-1}}$ assume an infinite DC gain for the OTAs used in the switched-capacitor realization. In reality, the DC gain is limited and depends on the OTA structure and IC fabrication technologies. By ensuring charge conservation with an OTA with a finite DC gain, the transfer functions of the delaying

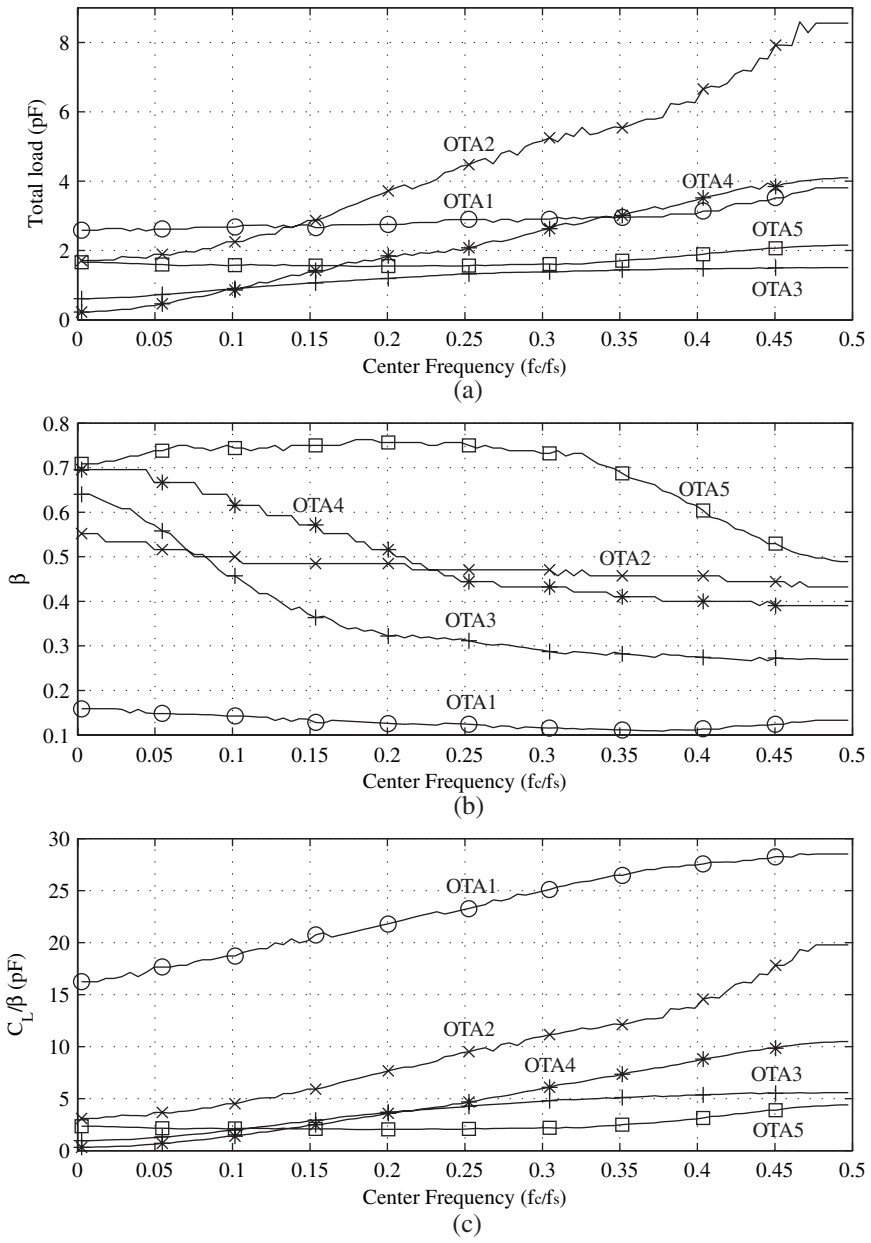

Figure 3.20: (a) Load capacitances (C_L), (b) feedback coefficients of OTAs (β), and (c) $\frac{C_L}{\beta}$.

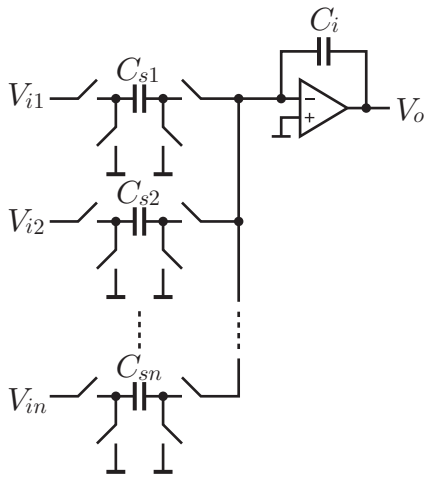

Figure 3.21: An integrator with multiple input SC branches.

and non-delaying integrators shown in Figure 3.21 with n SC branches are

$$V_o = \begin{cases} \dfrac{\sum_{j=1}^{n} V_{ij} C_{sj} z^{-1}}{C_i \left(1 + \dfrac{1}{A}\right)\left(1 - z^{-1}\right) + \dfrac{1}{A}\sum_{j=1}^{n} C_{sj}} & \text{Delaying integrator} \\ \dfrac{\sum_{j=1}^{n} V_{ij} C_{sj}}{C_i \left(1 + \dfrac{1}{A}\right)\left(1 - z^{-1}\right) - \dfrac{1}{A}\sum_{j=1}^{n} C_{sj}} & \text{Non-delaying integrator} \end{cases} \tag{3.21}$$

where A is the DC gain of the OTA, V_{ij} is the input of the j-th SC branch, C_{sj} is the capacitance of the j-th sampling capacitor, and C_i is the capacitance of the integrating capacitor.

3.10.3 Determination of OTA Specifications

Now that the effects of slewing, the non-zero time constant, and the finite DC gain of the OTAs have been mapped to discrete-time difference equations, these non-idealities can be incorporated into high-level discrete-time simulations in order to determine the required specifications of all OTAs required to achieve the targeted performance. Overdesign in the g_m and slew rate will increase the modulator's power consumption without increasing performance, and too high required DC gain makes the implementation very difficult.

Note that the nonlinearity of the OTAs, which greatly depends on their transistor-level

Table 3.3: Specifications of the OTAs.

	OTA1	OTA2	OTA3	OTA4	OTA5
DC gain (dB)	70	70	65	65	50
Slew rate (V/μs)	500	500	350	300	100
g_m (mS)	29	24	5.2	9.8	1.8

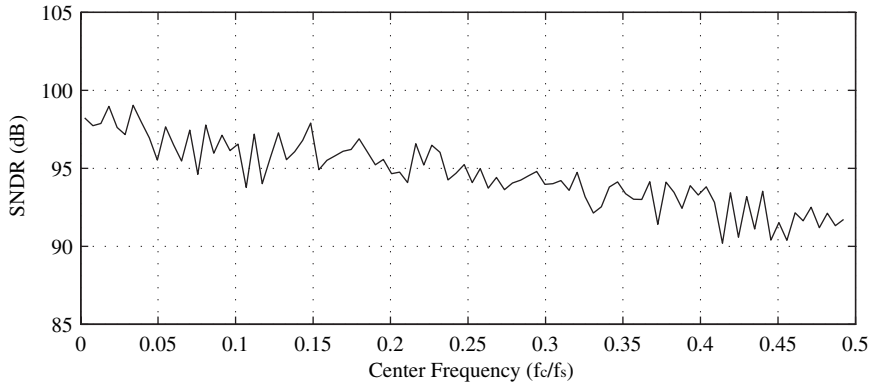

Figure 3.22: SNDR with thermal noise and circuit non-idealities.

design, is not included in the high-level simulation. Since this may influence the required DC gain, larger DC gain should be chosen.

Table 3.3 shows the required specifications of the five OTAs obtained from iterative simulations. The input capacitance of the ADC, which is unknown at this point, was assumed to be 1 pF. Unfortunately, g_m must be large enough for the worst case, which is the highpass configuration because of a large capacitive load in such a configuration. In other words, the OTAs are overdesigned for the lowpass and bandpass configurations.

3.10.4 Simulation Results with the Non-idealities

Figure 3.22 shows the SNDR obtained from simulations including finite DC gain, finite slew rates, non-zero time constants of OTAs, and the thermal noise in all of the SC branches. It barely satisfies the 90-dB requirement of the SNDR at any center frequency from DC to $f_s/2$.

A high-order delta-sigma modulator can have a significant improvement of the SQNR where the NTF zeros are located optimally [10, Ch.4]. As a side benefit of the programmability, the tunable modulator can be configured optimally for lowpass configurations for

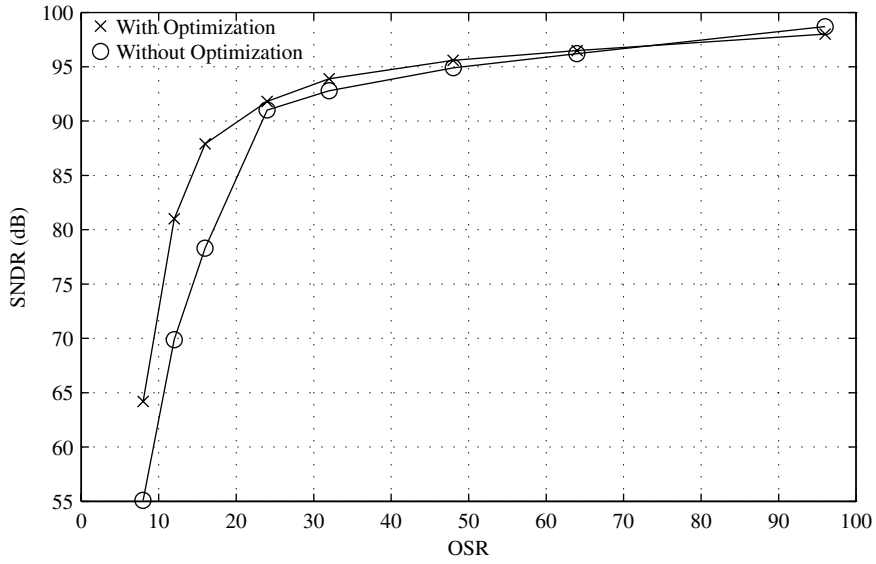

Figure 3.23: SNDR obtained with and without NTF zero optimization for the lowpass configuration.

a different OSR by moving some of the NTF zeros away from DC instead of putting all of them at DC. Figure 3.23 shows the SNDR obtained with and without NTF zero optimization from the tunable modulator configured for lowpass modulation. For a high OSR, there is no improvement in the SNDR. However, for a low OSR, approximately 10-dB improvement (1.5 bits) in SNDR is achieved with NTF zero optimization.

3.11 Summary

In this chapter, the fourth-order CRFF structure with four-bit quantizer was found to be the best choice to satisfy the required specification while ensuring stability. The modulator coefficients for all possible configurations were found for optimal NTFs with a help of computer programs. Those coefficients were quantized to fit in the digitally-programmable switched-capacitor circuits with optimal resolution without an excessive compromise of the SQNR. The digital correction technique is the best solution for DAC nonlinearity compensation, and it can be implemented with minor modifications in the modulator system due to the programmability. Thermal noise and other circuit nonidealities in the integrators such as finite slew rate, finite DC gain, and non-zero output time constants were studied and included in simulations to verify proper operation in more realistic

situations with all modulator configurations. From the iterative simulations, the required OTA specifications were also derived.

Chapter 4

Tunable Modulator Circuit Implementation

4.1 Overview

This chapter describes the transistor-level design of the tunable delta-sigma modulator. Most of the circuit blocks are similar to those in conventional discrete-time delta-sigma modulators for A-to-D conversion. The unique challenges for this design were the circuit design and layout of the programmable switched-capacitor circuits required to change the modulator coefficients, and the provision of the DAC output measurement mode for digital correction of the DAC nonlinearity. The wide variety of loading conditions for the OTAs also makes it difficult to ensure that they all have sufficient worst case phase margin.

First, the modulator's switched-capacitor representation is described. Specifically, the circuit timing and the extra circuit components for programmability and digital correction are explained. Then, the transistor-level design of the circuit components including the OTAs, programmable switched-capacitor circuits, the ADC, and the DAC are illustrated. In conclusion, transistor-level simulation results of the modulator are presented, and the IC layout of the modulator is briefly explained.

4.2 Circuit Representation of the Modulator

Figure 4.1 shows the switched-capacitor representation of the entire modulator. The first four OTAs and their switched-capacitor circuits form the integrators, and the last OTA is for the resettable-gain stage, which combines the feedforward signals from the integrators and the modulator input.

A common-mode voltage of 0.9 V (= $V_{DD}/2$), was used for the entire modulator. That is, both the input and the output common-mode voltages of the OTAs are 0.9 V. An output common-mode voltage of 0.9 V is desirable to maximize the output swing of the folded-cascode OTAs. However, the input common-mode should ideally have been made as low as possible to permit higher values of V_{GS} for the MOS switches at the OTA inputs. Higher V_{GS} would yield a lower on-resistance for switches of a given size. Therefore, the switches could have been made smaller if the input common-mode voltage was decreased. This is especially important for implementations in deep-submicron technologies whose transistor threshold voltage is close to $V_{DD}/2$.

Programmability of the modulator is realized with variable ratios of the integrators' sampling capacitors and integrating capacitors as explained in the previous chapter. The varactors in Figure 4.1 are digitally controlled by activating or deactivating smaller unit-sized capacitors in a parallel array. These varactors are shown only for a simple conceptual representation of the programmable switched capacitors. The actual circuit implementation of the programmable switched capacitors is described later in this chapter. Sign switching is only required for the a-parameters as shown in Figure 3.11. This is realized with four extra switches that interchange the polarity of the differential signals as shown in Figure 4.1.

Figure 4.2 shows the timing diagram of the modulator. In ϕ_1, the first and the third integrators sample their inputs, the second and the fourth integrators update their outputs, and the last summing stage updates its output by combining the outputs of all integrators. In ϕ_2, the first and the third integrators update their output, the second and the fourth integrators sample their input, and the summing stage resets its output. The key point is that the first integrator and the summing stage have to sample the input (V_{ip} and V_{in}) in the same phase (ϕ_1), and in the next phase (ϕ_2) the first integrator has to integrate the DAC output representing the ADC input in the previous phase ϕ_1. This requires that the A-to-D conversion be performed during the non-overlapping period

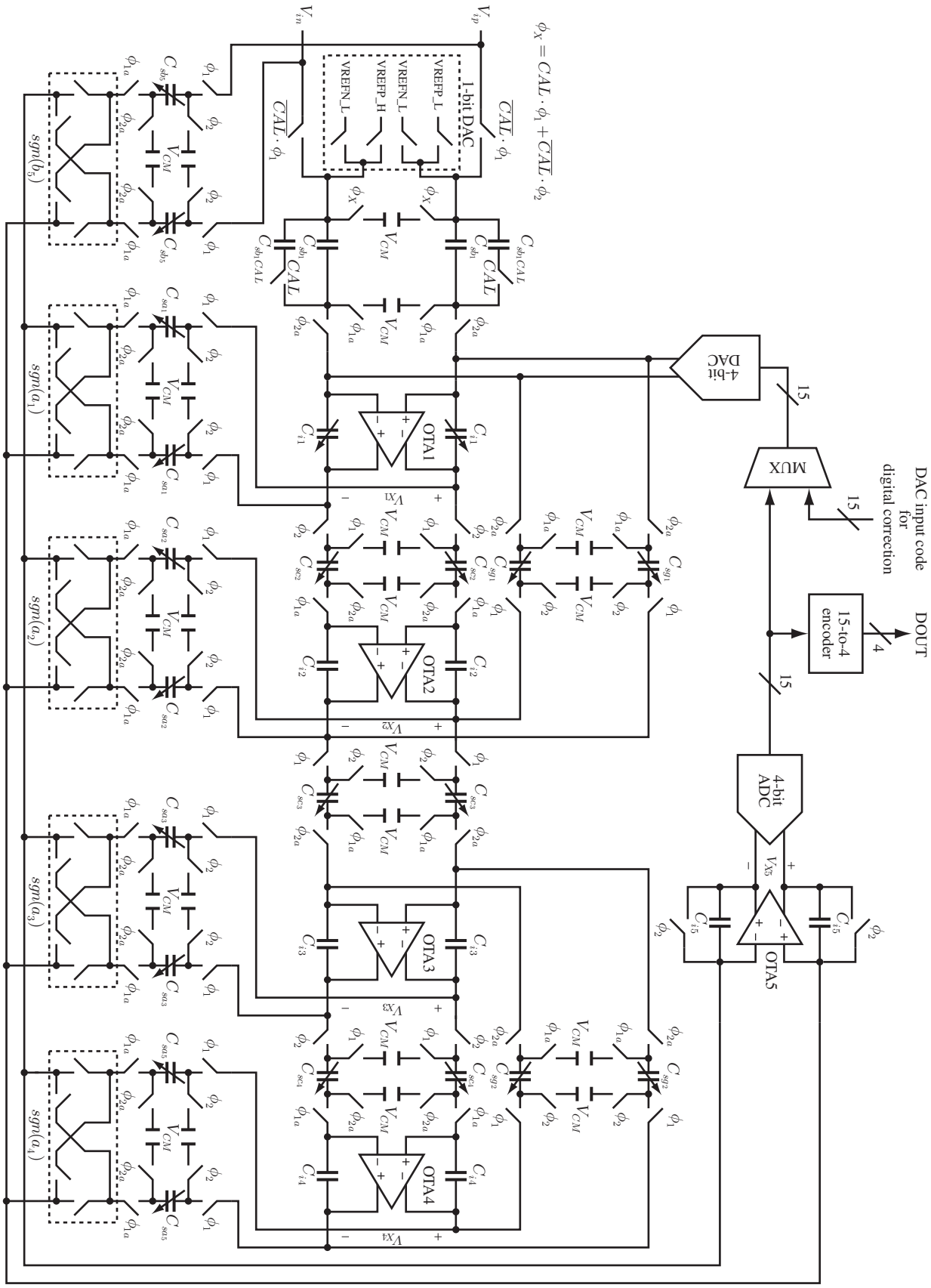

Figure 4.1: Schematic of the entire modulator.

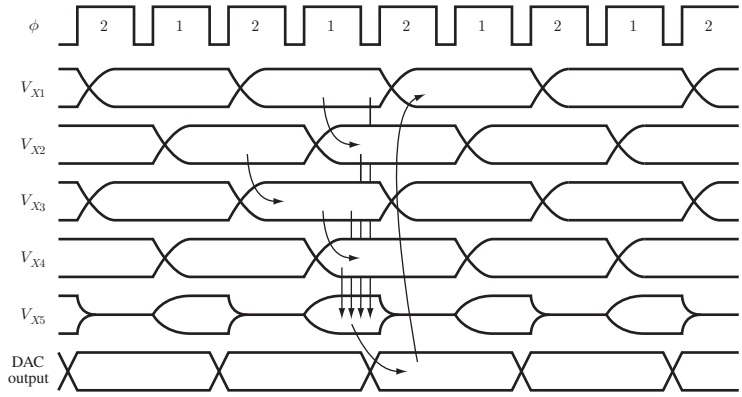

Figure 4.2: Timing Diagram of the Modulator.

between those two phases.

As explained in the previous chapter, the digital correction of the DAC nonlinearity requires a linear measurement of the output of the 4-bit DAC. The modulator can be reconfigured so that the DAC output is used as the modulator input, and the sampling capacitors of the first integrator ($C_{sb_1} + C_{sb_1CAL}$) are used to form a single-bit DAC by connecting them to the reference voltages with switches. The only modifications made for measurement of the DAC output are the addition of four switches to use the input sampling capacitors as a part of a single-bit DAC, the extra capacitors (C_{sb_1CAL}) for the single-bit DAC to make its output swing larger than the 4-bit DAC's output swing, and multiplexers to select the digital input of the DAC and the phase of ϕ_X. The digital input to the 4-bit DAC under measurement is provided by configuration registers.

4.3 OTAs

Discrete-time delta-sigma modulators are realized with switched-capacitor circuits and OTAs. The nonidealities of the OTAs such as their finite DC gain, transconductance, slew rate, and output swing, affect the modulator's performance. In the previous chapter, the OTAs' specifications were determined. In this section, OTAs that meet or exceed those requirements are designed at the transistor level.

Unlike normal delta-sigma modulators with a fixed configuration, the load capacitance of the OTAs in a tunable modulator varies significantly for different configurations. For typical two-stage OTAs, this complicates the compensation. The dominant pole of a two-

stage OTA is located at the output of the first stage, and the second pole is at the output of the second stage. To ensure stability with a sufficient phase margin, compensation is done to push these poles far apart. This requires a very low dominant pole frequency and/or a very high second pole frequency. The former increases the settling time of the OTA, and the latter increases power consumption.

On the other hand, for a single-stage OTA, the dominant pole is at the output, and the second pole is located at the internal node of the OTA. This makes compensation much easier because the second pole tends to be at very a high frequency, and the dominant pole is far separated from the second pole as long as sufficient capacitance appears at the output node.

The problem with a normal single-stage OTA is its low DC gain. As shown in Figure 3.3, the required gain is quite high for a normal single-stage OTA. In fact, it is very difficult to achieve 65-dB DC gain with a single-stage structure in 0.18-μm CMOS technology due to the relatively low output impedance of the transistors and, the low V_{DD} which prohibits the stacking of many transistors. However, the single-stage OTA is still attractive for its ease of compensation. Fortunately, a technique called "gain boosting" can be used to increase the DC gain of an OTA without stacking extra transistors or increasing the number of stages [24]. This technique significantly improves the DC gain of an OTA with a cascode load by amplifying the output resistance of the cascodes by the gain of auxiliary OTAs, called "gain boosters".

The values of g_m and slew rate specified for OTA1 and OTA2 in Table 3.3 are not very much different. Therefore, identical OTAs are used for them. Although the specifications for OTA3 and OTA4 are quite different, designing different OTAs for these two does not save very much power because their power consumption is much lower than that of OTA1 and OTA2. Therefore, OTA3 and OTA4 are made identical to save design time. OTA5's required DC gain is much smaller than the others, and the required g_m is much lower, too. However, again, to save design time, OTA5 was made same as OTA3 and OTA4 except that it does not have gain boosters.

For a high gain and large output swing, the folded-cascode structure was selected for the OTAs. Figure 4.3 shows the schematic of the OTA, which is common for all five OTAs except for OTA5, which does not have gain boosters. Table 4.1 shows the transistor sizes for each OTA, and Figure 4.4 shows the simulated performance of each OTA. C1 and C3 are for compensation of the gain boosting loop. Small compensation capacitors C2

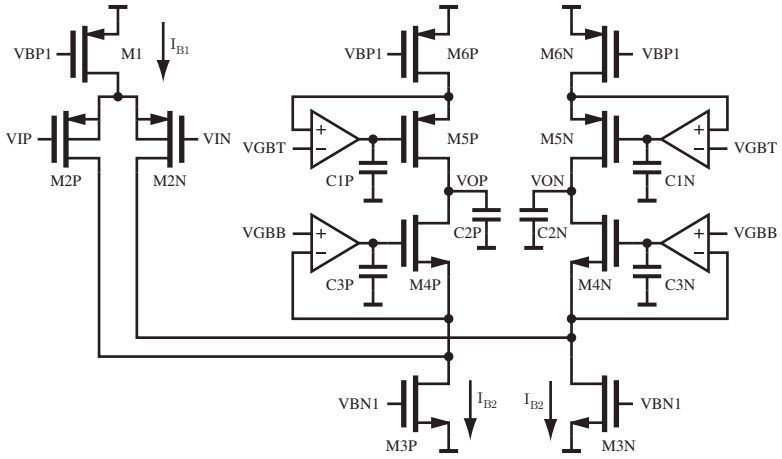

Figure 4.3: Schematic of the OTA.

are added to the output nodes to ensure sufficient phase margin even when only a very small load or no load is connected to the OTAs. This is a unique problem in a tunable delta-sigma modulator because the load capacitance of the integrators greatly change for different configurations.

4.3.1 Gain Boosters

A gain booster amplifies the output impedance of a cascode by its own gain [24]. Since the gain boosters do not require a high output swing, a differential cascode amplifier is preferred for the gain boosters to provide a high amplification factor of the output impedance. For the NMOS cascode, the gain booster will have a common mode input of approximately a few hundred mV, and must provide an output voltage around 1 V. The PMOS input folded-cascode OTA shown in Figure 4.5(a) satisfies these requirements. Similarly, the NMOS input folded-cascode OTA shown in Figure 4.5(b) is used for the PMOS cascodes. Transistor sizes for the gain boosters are shown in Table 4.2.

The gain boosting loops are stabilized with compensation capacitors C_1 and C_3 shown in Figure 4.3. The simulated phase margin is higher than 60 ° for all of the gain boosters of all OTAs over process variation corners and the temperature variation (from -40 °C to 80 °C).

Table 4.1: Circuit parameters for the OTAs.

	OTA1	OTA2	OTA3	OTA4	OTA5
M1, M2	256×4μm×0.25μm		64×4μm×0.25μm		
M3	40×4μm×0.25μm		24×2μm×0.25μm		
M4	20×4μm×0.25μm		12×2μm×0.25μm		
M5, M6	128×4μm×0.25μm		32×4μm×0.25μm		
C1	200 fF		100 fF		
C2	500 fF		200 fF		-
C3	300 fF		150 fF		-
I_{B1}	8.0 mA		2.0 mA		
I_{B2}	7.9 mA		2.0 mA		
C_{Lmin}	2.6 pF	1.7 pF	0.61 pF	0.22 pF	1.5 pF
C_{Lmax}	3.8 pF	8.6 pF	1.5 pF	4.1 pF	2.1 pF

Table 4.2: Circuit parameters of gain boosters for OTAs.

	For NMOS cascode		for PMOS cascode	
	OTA1 & OTA2	OTA3 & OTA4	OTA1 & OTA2	OTA3 & OTA4
M1, M2	24×1.5μm×0.25μm	8×2μm×0.25μm	8×1μm×0.25μm	8×1μm×0.70μm
M3	16×1.5μm×0.25μm	4×2μm×0.25μm	8×1μm×0.25μm	4×1μm×0.70μm
M4	8×1μm×0.4μm	4×1μm×0.35μm	16×2μm×0.25μm	16×1μm×0.25μm
M5	4×1μm×0.4μm	2×1μm×0.35μm	8×2μm×0.25μm	8×1μm×0.25μm
M6, M7	12×1.5μm×0.4μm	4×2μm×0.25μm	4×1μm×0.25μm	4×1μm×0.70μm
I_{B1}	256 μA	87.1 μA	340 μA	84.7 μ A
I_{B2}	256 μA	87.0 μA	341 μA	84.9 μ A

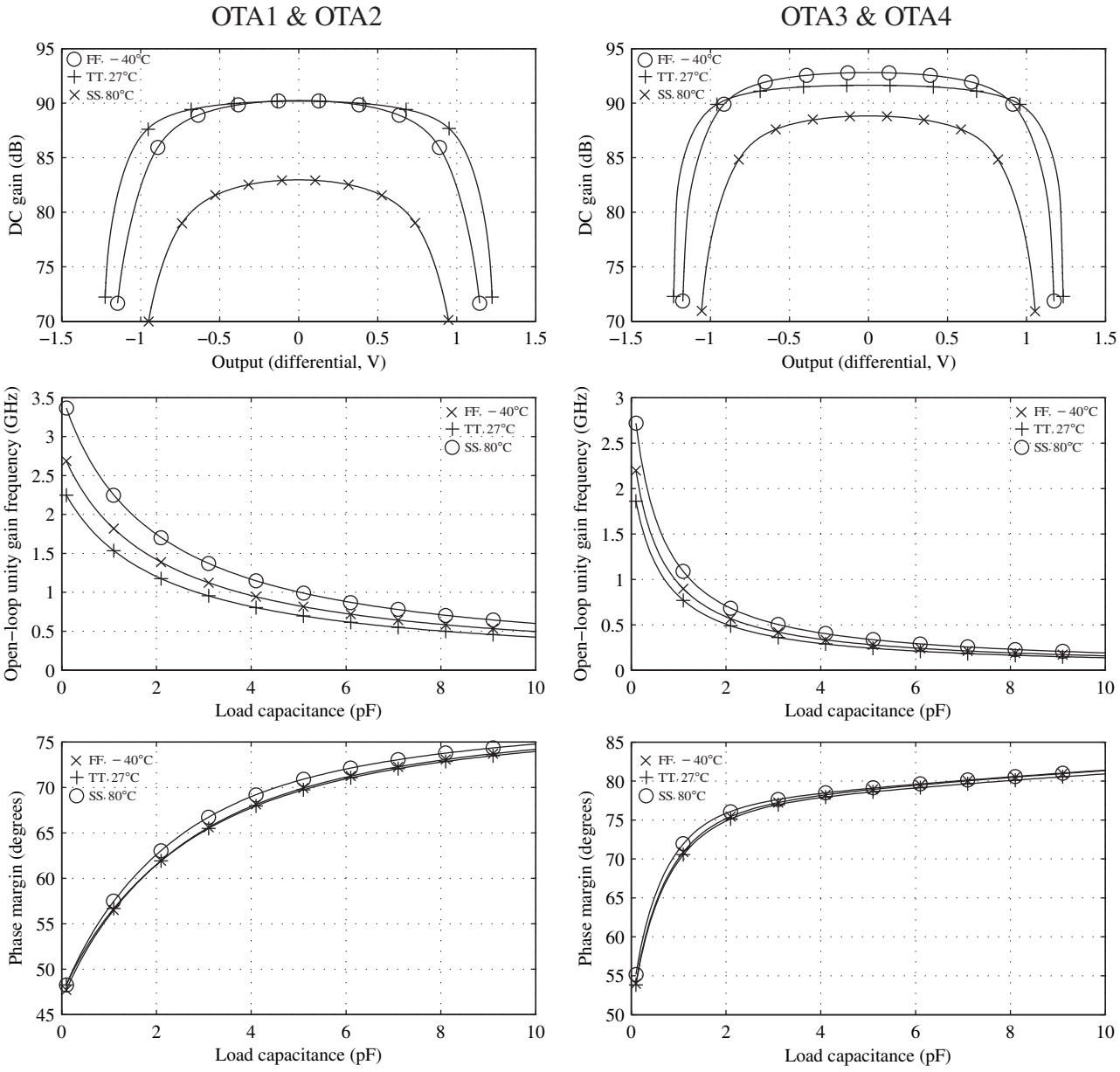

Figure 4.4: Performance of the OTAs.

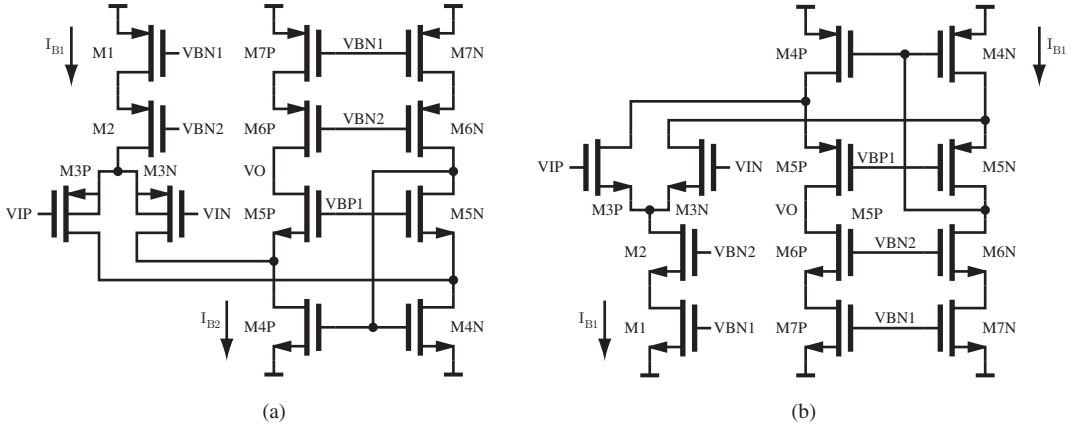

Figure 4.5: Schematics of gain boosters for (a) an NMOS cascode and (b) a PMOS cascode.

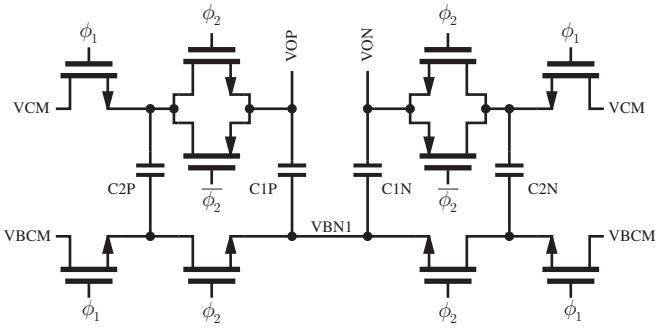

Figure 4.6: CMFB circuit.

4.3.2 Common Mode Feedback Circuits (CMFB)

The OTAs in the modulator are fully differential with active loads, so a common-mode feedback (CMFB) circuit is required to define their output common mode voltage. Either continuous-time or discrete-time techniques can be employed for CMFB. Continuous-time techniques tends to limit the output swing and/or the DC gain of the OTA [22, Ch.9], and are therefore, generally only used in continuous-time applications. Since the output swing of the OTAs is an important requirement for a high dynamic range of the integrator output, and the integrators are all discrete-time with appropriate clock signals always available, the discrete-time CMFB was chosen for all of the OTAs. The CMFB circuit is shown in Figure 4.6. A detailed description of its operation can be found in [25, Ch.26].

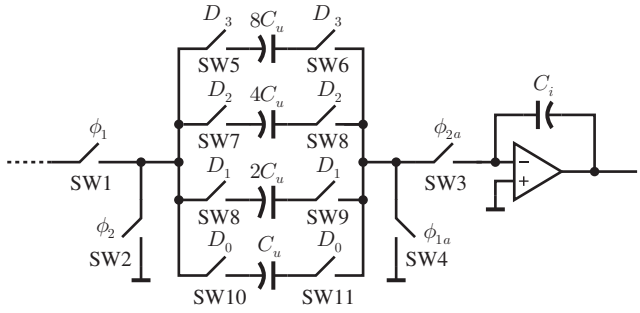

Figure 4.7: A possible implementation of a switched-capacitor integrator [1].

4.4 Programmable Switched Capacitors

Programmability of the tunable modulator is realized with programmable switched capacitors. The programmable switched-capacitor circuits are the most distinctive circuit blocks in a tunable delta-sigma modulator.

Figure 4.7 shows a possible implementation of a programmable switched-capacitor integrator [1]. The problem with the implementation in Figure 4.7 is that SW3 and SW4 have to be large enough to ensure sufficiently fast settling time for the worst case with all of the capacitors ($15C_u$) turned on. Therefore, when only the smallest capacitor, C_u, is activated, SW3 and SW4 are much larger than they need to be, and they change the charge stored in the capacitor significantly due to excessive charge injection. The amount of charge injected is ideally independent of the input signal [16, Ch.10], and should be canceled in a fully differential implementation because of the common-mode behavior of charge injection. However, any mismatch of the switch may cause a charge injection imbalance thus generating an excessive differential DC offset. In addition, the clock driver has to drive unnecessarily large switches wasting power associated with a large dynamic power.

Another problem with the structure in Figure 4.7 is the increased RC time constant of the switched-capacitor circuit due to the switches, SW5-SW11, in series with the sampling capacitors. In order to compensate for the increase of the time constant, switches SW1-4, have to be enlarged compared to a non-programmable integrator or switches SW5-11 have to be made so large that they cause negligible increase in the time constant. The former further increases the effects of excessive charge injection and the clock buffer power consumption, and the latter increases the effect of the substrate noise due to the switches' very large drain and source regions.

In order to avoid these undesirable effects, the structure shown in Figure 4.8 was chosen. In this structure, switches M3-M10 are sized in proportion to the size of the capacitors to which they are connected, and only the switches for the selected capacitors are clocked. This does not cause excessive charge injection to the sampling capacitor because only the selected switches, which are sized appropriately for the selected capacitors, are switched. Switches M1 and M2 still have to be made large enough for the largest sampling capacitor. However, the OTA of the previous stage sinks the charge injected by these switches, so the integrating capacitor of the previous stage will not be affected.

Transmission gates are used to select the switches to be activated. If not sized properly, they increase the rise and fall time of the clock signals. Local buffers near the switches can recover fast rise and fall times. However, delays in these buffers may cause skew between ϕ_{2a} and ϕ_2 as well ϕ_1 and ϕ_{1a}. Skew between the clock signals is very critical for switched-capacitor circuits because it may reduce the time available for sampling and integration, and may even cause overlapping of the sampling and integrating phases. The adjustment of skew for each buffer is very cumbersome to implement. In addition, such local buffers would be very noisy digital circuits near the sampling capacitors. Therefore, rather than buffering each gated the clock locally, the global clock buffers and the transmission gates were made large enough to maintain fast rise and fall time of the clock signals without additional local buffers.

4.4.1 Bootstrapped Switches

The first switch of the switched-capacitor integrator (M1) of Figure 4.8 must pass a wide range of voltages unlike the other switches. Its on-resistance must be sufficiently low over the entire range of terminal voltages. One simple way to realize such a switch is to use transmission gates. The NMOS transistor is conductive for low input voltages, and the PMOS transistor is conductive for high input voltages. However, the relationship between the on-resistance and the input voltage is highly nonlinear. The nonlinearity of the on resistance introduces input-dependent settling of the input causing a nonlinearity in the integrator.

In [26], a bootstrapping technique is presented. It maintains V_{GS} of the input switch at approximately V_{DD}, relatively independent of the input voltage. This requires a gate voltage above V_{DD}. The schematic of the bootstrapping circuit is shown in Figure 4.9. It generates the required gate voltage from the same V_{DD} supply as the rest of the circuit

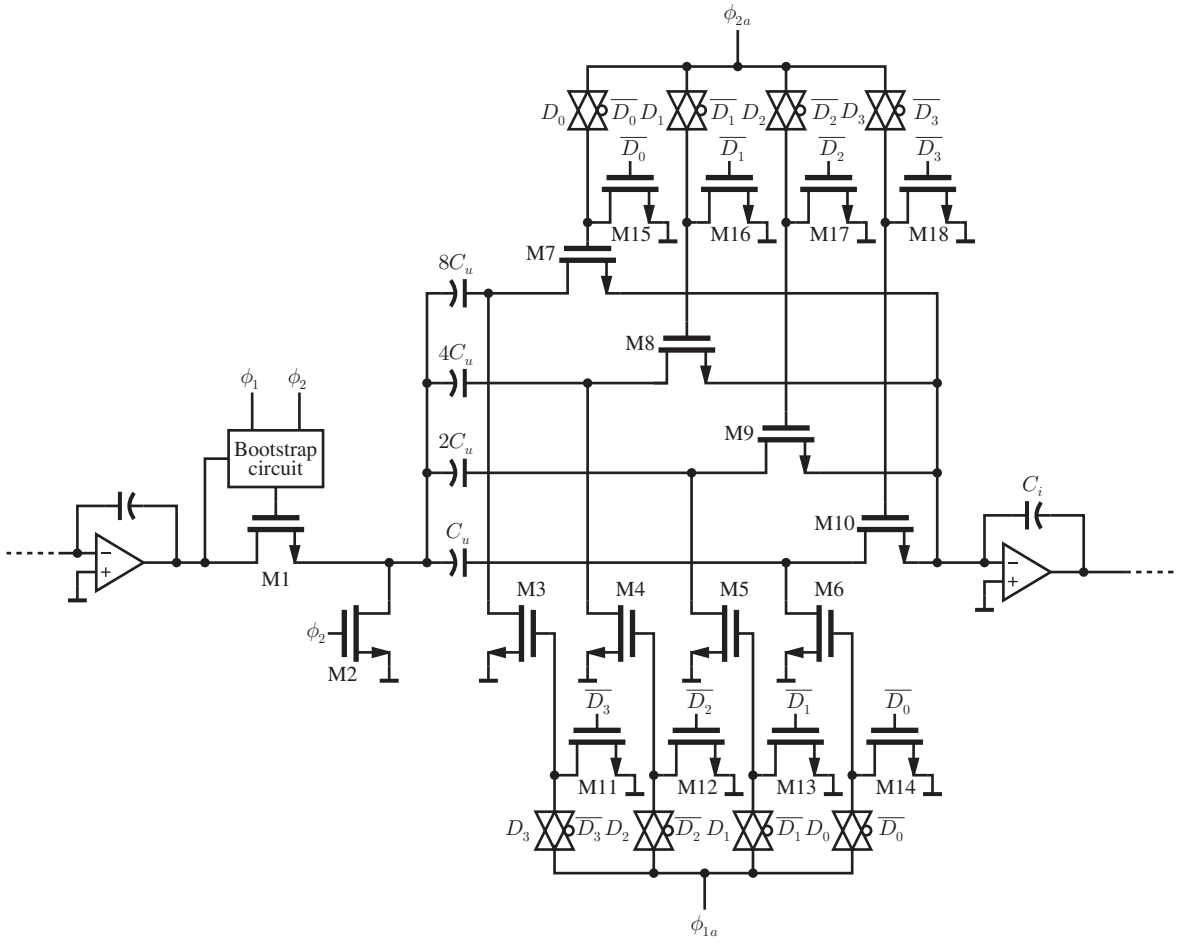

Figure 4.8: A more suitable programmable switched-capacitor integrator.

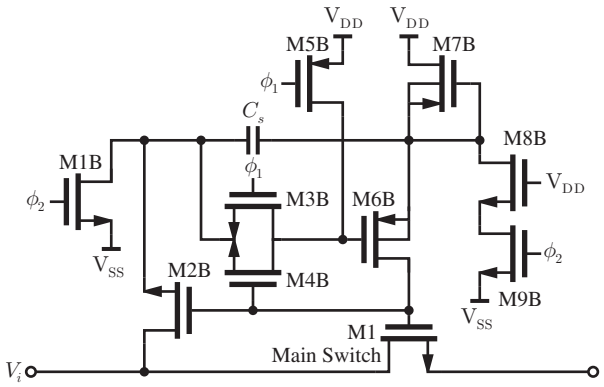

Figure 4.9: Bootstrapping circuit.

without causing V_{GS} or V_{GD} of any transistors to exceed V_{DD}. The same bootstrapping circuit was used for every input switch of the switched-capacitor circuits in the modulator. Ideally, the gate voltage of the main switch should be equal to $V_{DD} + V_i$ when it is turned on. However, due to charge sharing between C_s and the gate of the main switch, M1, the on-gate voltage is somewhat smaller than $V_i + V_{DD}$. This error can be reduced by increasing the size of C_s.

4.5 Flash ADC

The 4-bit ADC was implemented with a simple flash architecture for its speed, low latency, and simplicity. It consists of fifteen fully differential comparators and a resistive ladder for reference voltage generation as shown in Figure 4.10. Each comparator consists of a preamplifier, a latch, and an SR latch as shown in Figure 4.11. The preamplifier amplifies the difference between the differential input signal ($V_{ip} - V_{in}$) and the differential reference voltage ($V_{REFPn} - V_{REFPn}$). It prevents the kickback noise from the latch from influencing the previous analog stage, and its gain reduces the effect of latch offset [16, Ch.7]. The preamplifier output is further amplified to logic levels by the large gain of the latch with regeneration. The SR latch holds the output of the latch during the reset phase of the latch.

The reference voltages, V_{REFP} and V_{REFN} of the ADC were set to ± 0.3 V due to the limited input swing of the preamplifier. Therefore, in order to maintain the 4-bit resolution of the ADC, the offset of the comparators has to be less than half of an LSB ($=0.6\text{ V}/(2 \cdot 2^4) = 18.75$ mV). Since the offset of the latch is effectively divided by the gain

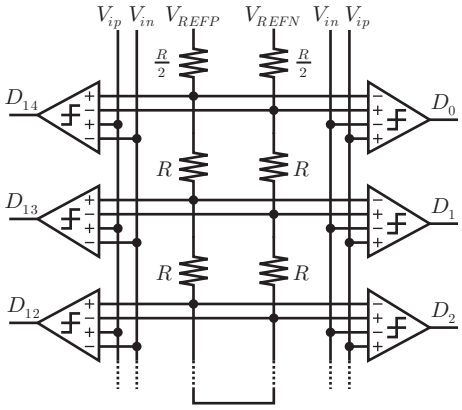

Figure 4.10: Flash ADC (clock signals omitted).

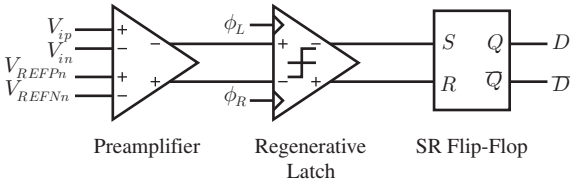

Figure 4.11: Block diagram of the comparator.

of the preamplifier [27, Ch.8], the input offset of the preamplifier dominates the offset of the entire comparator for a large gain with reasonable offset of the latch.

Due to the strict timing constraints of the system, only 1 ns is allocated for A-to-D conversion. It was verified that the comparators are fast enough for the allocated time slot.

4.5.1 Preamplifiers

The preamplifier amplifies the difference between two differential inputs. Figure 4.12 shows the schematic of the preamplifier. The input differential pairs are placed in a deep n-well to tie the body to the source so the allowable input range of the preamplifier is maximized. By connecting the source of M2P, M2N, M3P, and M3N to the body, the body effect is avoided so the required V_{GS} for a given overdrive voltage is minimized. The load is a parallel combination of a simple PMOS current source and a diode-connected PMOS transistor. This structure enables us to define the output common-mode voltage without CMFB while maintaining relatively high output impedance [22, Ch.3]. The DC

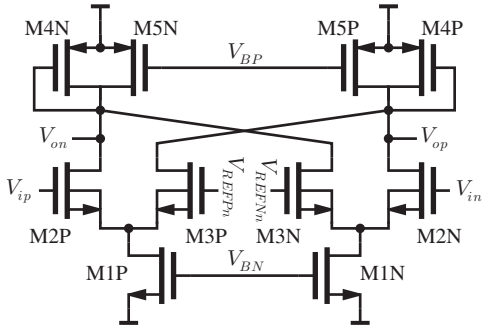

Figure 4.12: Preamplifier of the comparator.

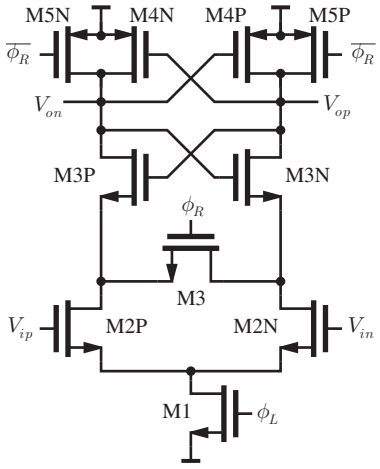

Figure 4.13: Latch of the comparator.

gain of the preamplifier is 4.2 (12.5 dB).

4.5.2 Latches

Figure 4.13 shows a schematic of the latch. It is very similar to the one used for the comparator in [28]. During ϕ_R (reset phase), transistors M5 precharge the output node to V_{DD}, and M3 ties together the drains of M2 to eliminate any hysteresis in the comparison in the next phase. During ϕ_L (latch phase), the difference at the gates of M2 is amplified to full CMOS logic levels by regeneration.

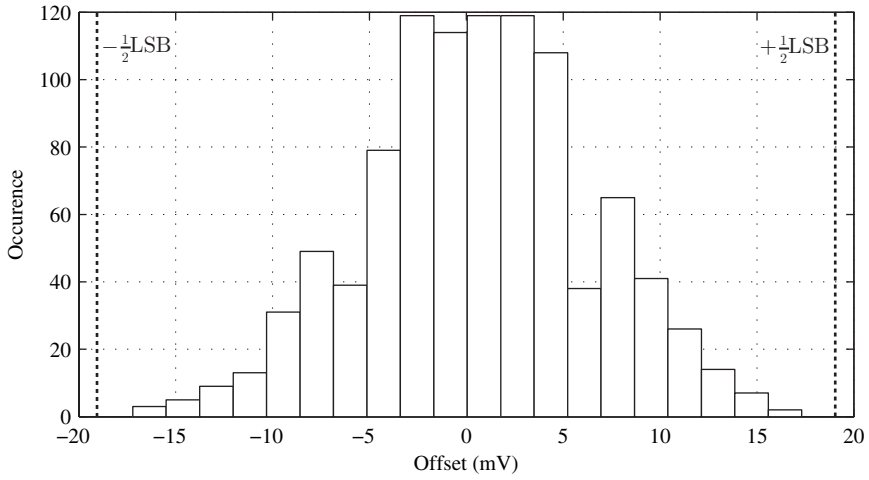

Figure 4.14: Histogram of the comparator input offset voltage for 1000 Monte-Carlo simulation runs.

4.5.3 Comparator Offset

Mismatch of the transistors in the preamplifier is the main source of the comparator input offset. In order to avoid bubble errors (1 within a string of 0s or 0 within a string of 1s) in the thermometer code at the output of ADC, offsets of the comparators should be less than 0.5 LSB (18.75 mV).

For an ideal ADC, the maximum quantization error is 0.5 LSB. However, for an ADC with comparator offsets of up to 0.5 LSB, the quantization error may reach 1 LSB in the worst case. A larger quantization error may overload the ADC in a delta-sigma modulator because the input of the ADC is expressed as $Y = \mathrm{STF}(z)U(z) + [\mathrm{NTF}(z) - 1]\, e_Q(z)$ where e_Q is the quantization error. Sensitivity of the modulator stability to the comparator offset should have been done in the system-level design phase.

In order to estimate the comparator's input offset, a statistical analysis was done using the transistor mismatch models. Figure 4.14 shows a histogram of the comparator offset for 1000 Monte-Carlo simulation runs. As shown in the histogram, the offset is within half a LSB for 100 % of the runs. The standard deviation of the input offset is 5.9 mV.

Comparator offset with the same standard deviation was applied to the system-level simulation, and it was confirmed that the modulator is still stable with negligible degradation of the SNDR.

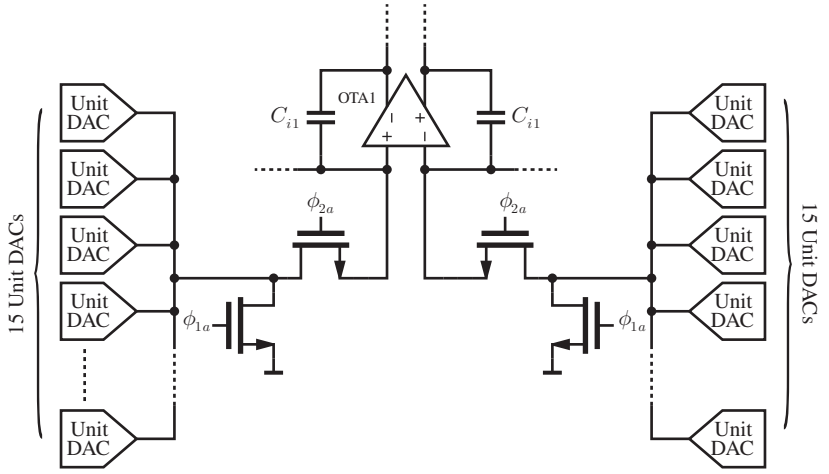

Figure 4.15: Multi-bit DAC implementation.

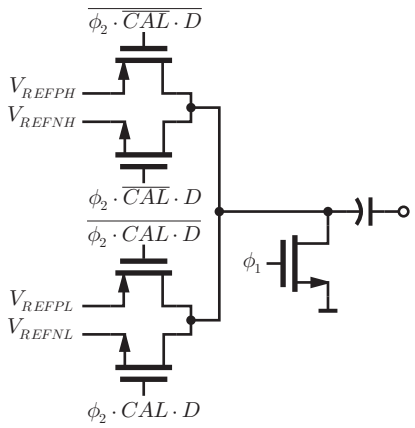

Figure 4.16: Schematic of a unit DAC.

4.6 DAC

The DAC consists of 15 pairs of switched-capacitor 1-bit unit DACs and OTA1 which is shared with other switched-capacitor circuits (to realize modulator coefficients b_1 and g_1), as shown in Figure 4.15 and 4.16. During the normal operation of the modulator, in ϕ_2, the sampling capacitors in the unit DACs are discharged. In ϕ_1, the sampling capacitors are charged to V_{REFPH}-V_{CM} (1.8 V-0.9 V) or V_{REFNH}-V_{CM} (0 V - 0.9 V) depending on their digital input, and the same amount of charge is transferred to the integrating capacitors (C_{i1}) of the first integrator. V_{REFNL} (0.75 V) and V_{REFPL} (1.05 V) are used for the digital correction mode to prevent overloading of the integrators.

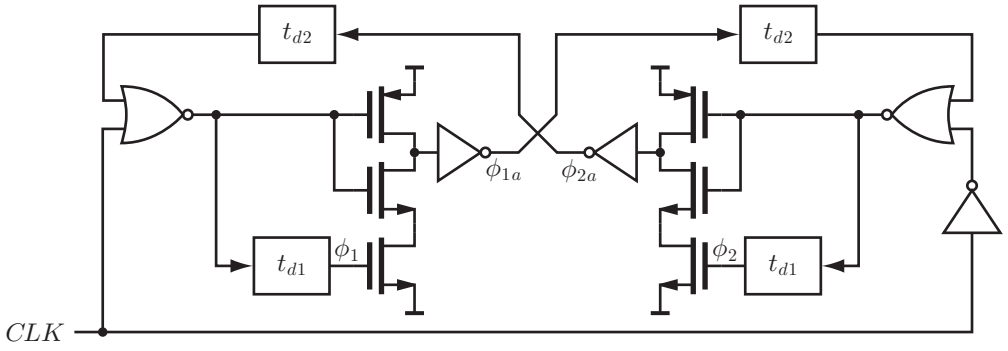

Figure 4.17: Clock generator.

Table 4.3: Clock signal timing parameters.

t_{d1}	t_{d2}	t_{da}	t_{db}	t_{dd}
470 ps	1.1 ns	1.0 ns	300 ps	150 ps

4.7 Clock Generator

The modulator requires two non-overlapping clocks (ϕ_1 and ϕ_2), two clocks with early falling edges (ϕ_{1a} and ϕ_{2a}), and inverted versions of them. In order to prevent signal-dependent charge injection in the switched-capacitor circuits, ϕ_{1a} and ϕ_{2a} are required [16, Ch.10]. In addition to these clock signals, the ADC requires two extra clock signals because it performs A-to-D conversion during the non-overlapping period between ϕ_1 and ϕ_2.

Figure 4.17 shows the clock generation circuit employed for the modulator. It is similar to the circuit presented in [29]. Unlike typical clock generation circuits, which have both the rising edges and the falling edges of ϕ_{1a} and ϕ_{2a} shifted relative to ϕ_1 and ϕ_2, this topology enables us to align the rising edges of the clocks while generating early falling edges. This maximizes the time available for sampling and integrating in the integrators. The output of the clock generator is passed to CMOS inverter clock buffers, which drive switches in the modulator and the associated interconnects. The ADC clock generator is shown in Figure 4.18. The timing of the clock signals is described in Figure 4.19 and Table 4.3.

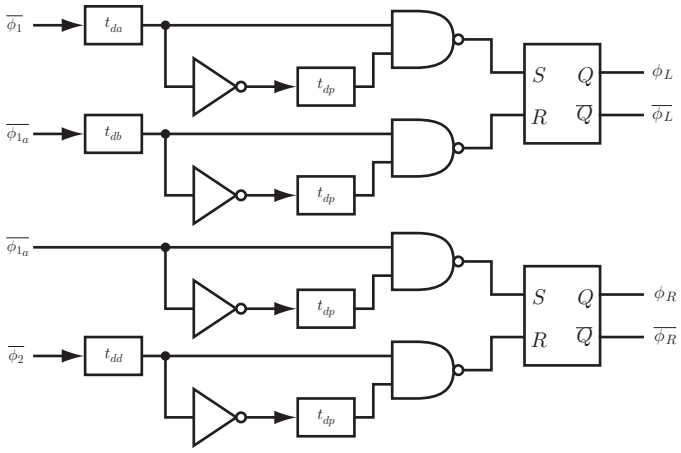

Figure 4.18: Clock generator for ADC.

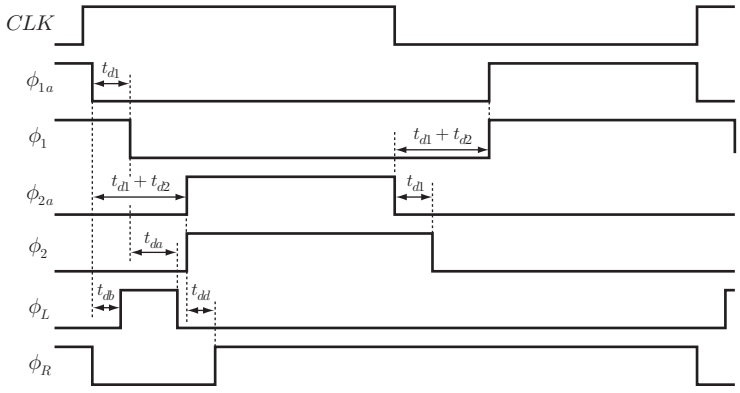

Figure 4.19: Clock signal timing.

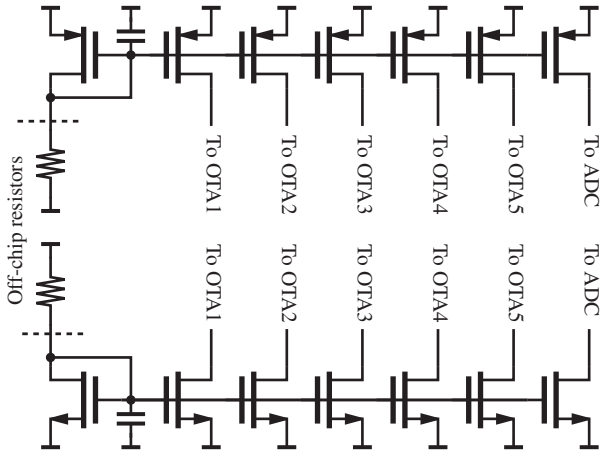

Figure 4.20: Master bias circuit.

4.8 Other Circuits

4.8.1 Bias Circuit

The OTAs and the ADC require bias voltages for their operation. Since they are located far away from each other in an IC, local bias circuits were incorporated within each of them, so the effects of transistor mismatch and power supply variations are reduced. Reference currents for the local bias circuits are generated at one location by mirroring off-chip reference currents as shown in Figure 4.20. The off-chip currents for NMOS and PMOS are supplied separately, so the V_{GS} of both NMOS and PMOS transistors on the fabricated chips for a given current can be measured. The deviation of these voltages from the simulated values allows for a very rough independent estimate of process variation or the NMOS and PMOS transistors.

4.8.2 Configuration Registers

The modulator requires 82 bits of data in total for the following reasons; to configure the modulator coefficients, to switch it to the DAC output measurement mode, and to set the digital DAC input for measurement of its analog output. A simple shift register was used as a memory element for the configuration data. It is loaded serially via four I/O pins: clock, serial data input, serial data output (for verification), and a strobe signal. The register map is shown in Table B.2.

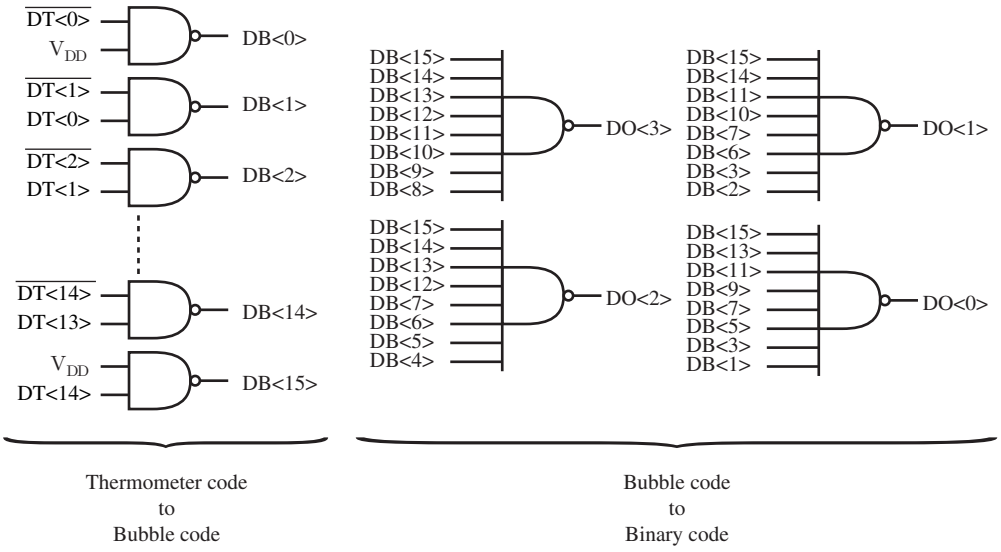

Figure 4.21: Thermometer to binary converter.

4.8.3 Thermometer-to-binary Converter

The output of the 4-bit ADC is a 15-bit thermometer code. The thermometer code is directly fed back to the DAC, but is not suitable for the output of the modulator because it would occupy too many output pins. The thermometer-to-binary code converter shown in Figure 4.21 is used to generate the 4-bit binary output code. The first stage of the converter converts the thermometer code to a bubble code (in which only one of the bits is 0). The bubble code is then passed to a second stage to obtain the final binary output. The latency of the thermometer-to-binary converter is not very important because it is outside the delta-sigma modulator loop.

4.9 Circuit Simulation Results

The entire circuit was simulated with Cadence Spectre® for several different configurations. It is impossible to simulate all of the possible configurations because of the long simulation time (each simulation (125 μs for $64 \times \text{OSR} = 6144$ data points with about 4000 transistors) takes about eight days even with a state-of-art computer and with non-critical digital circuits replaced by macro models). In addition, the digital correction feature could not be tested because it requires an extremely large number of samples (at least 2^{17} samples as shown in the previous chapter) for each input code of the DAC.

Therefore, mismatch of the unit DACs was not taken into account for the simulations.

4.9.1 Modulator Output

Figure 4.22 shows the spectra of the modulator output for five different configurations. The dotted lines in the zoomed spectra indicate the band of interest (260 kHz). Since the circuit simulations do not include thermal noise, expected thermal noise was added to the simulation results according to (3.12). Figure 4.23 shows the SNDR for the same configurations. The SNDR is a few dB less than the expected SNDR found in the system-level design except for the highpass configuration with a very high noise floor.

The highpass configuration was also simulated with zero input signal, and a deep noise floor was recovered. Therefore, the fact that the input signal is swinging very fast due to the high frequency may be the cause of the problem. The modulator input is fed to the first integrator and to the ADC through the feedforward-summing stage. Therefore, one or both of these are post probably the cause of the problem. Further investigation is still required.

The noise floor level (except for the highpass configuration) is dominated by that from circuit simulations for all of the configurations. One possible source of the noise floor is the circuit nonidealities that were not taken into account in the system-level design phase such as nonideal switches. Another possible cause is simulation inaccuracy of the transient analysis. There was a tendency for the noise floor to decrease as the simulation accuracy was increased. For example, a 10-dB improvement of the SNDR was observed for some modulator configurations by switching from "moderate mode" to "conservative mode" of the Spectre transient analysis. Therefore, the SNDR may improve even further with more accurate simulations. However, due to excessive simulation time, it is impractical to further increase the simulation accuracy. In fact, there has been a case such as [30] where fabricated chips outperformed simulated ones.

4.9.2 Power Consumption

Table 4.4 shows a breakdown of the power consumption for the lowpass configuration. Power consumption of the clock buffers changes with configurations because the load changes with configurations. However, the change is negligible since power consumption of the OTAs dominate the total power consumption.

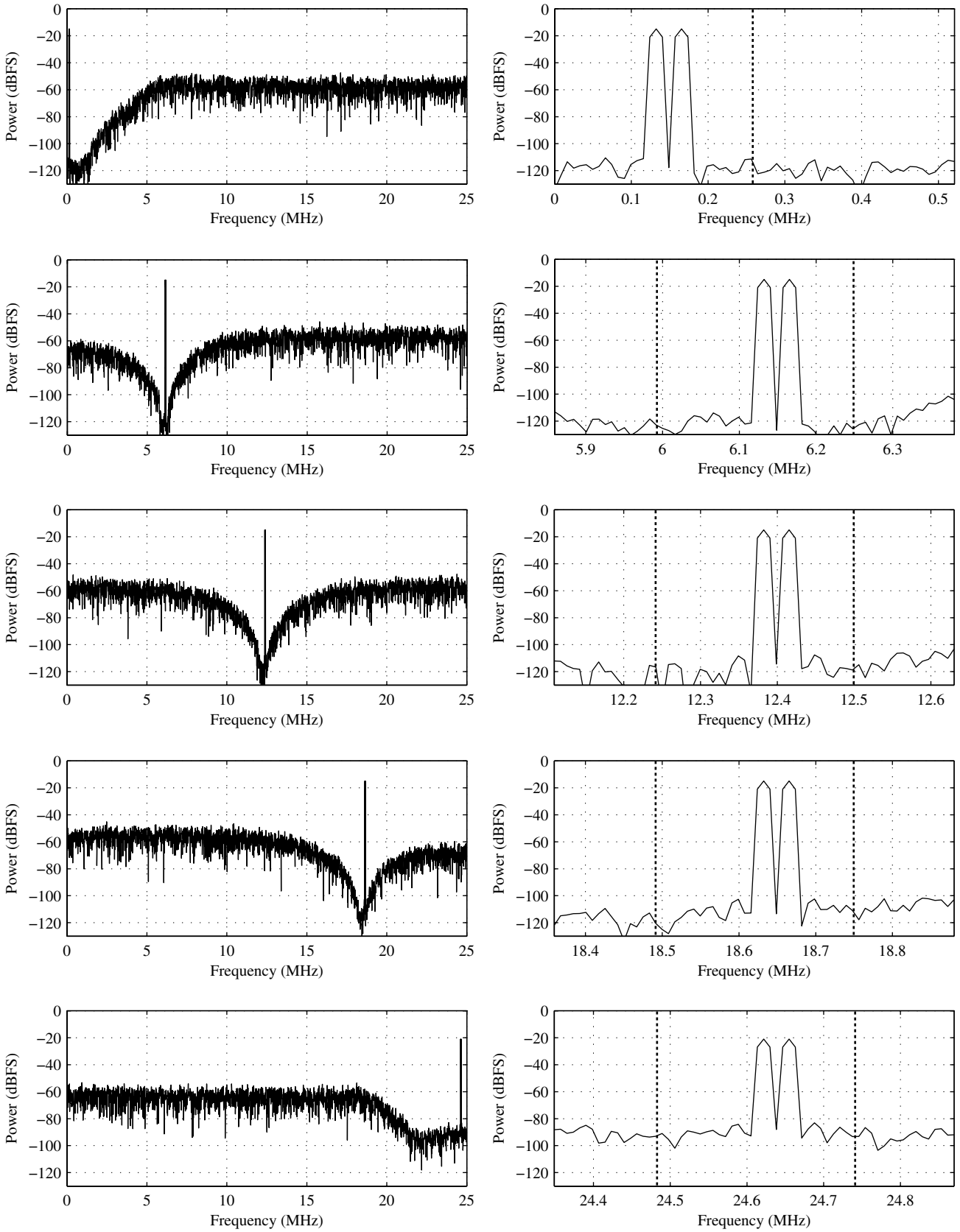

Figure 4.22: Modulator output spectra obtained from circuit simulations (6144-point DFT with Hann windowing).

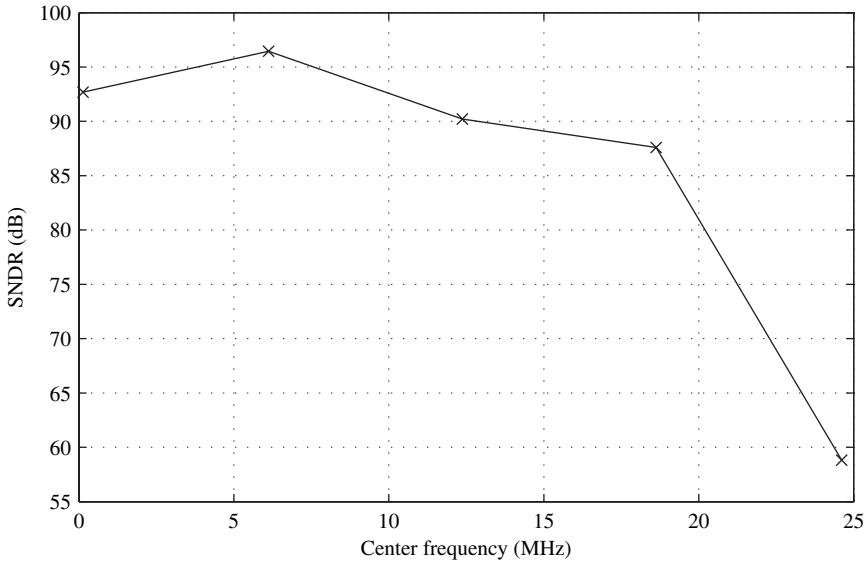

Figure 4.23: SNDR obtained from circuit simulations.

Table 4.4: Breakdown of the power consumption.

Supply	Description	Power (mW)
AVDD	OTA1	35.5
	OTA2	35.3
	OTA3	9.32
	OTA4	9.27
	OTA5	7.70
	ADC preamps	2.43
	Others	0.60
	Subtotal	100
BVDD	Bootstrapping	0.936
CVDD	Clock buffers	3.42
DVDD	Clock generator and output buffers	3.24
LVDD	ADC latches	0.234
Total		**108**

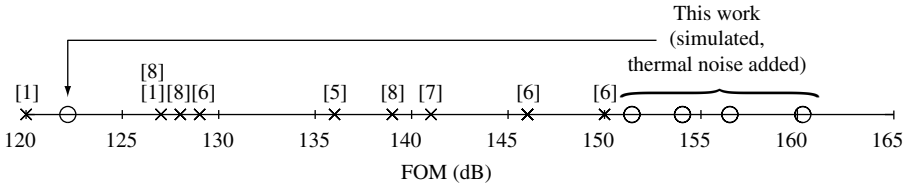

Figure 4.24: FOMs of various bandpass delta-sigma modulators.

4.9.3 FOMs

Finally, FOMs of the simulated tunable modulator are compared with recently published bandpass delta-sigma modulators with a fixed passband (except for [2], which is a tunable modulator) in Figure 4.24. The FOMs for the tunable modulator are higher those of the recently published bandpass delta-sigma modulators. Of course, the FOMs for the tunable modulator in Figure 4.24 are optimistic because they were derived from the simulation results. However, as long as the degradation of the FOMs is reasonable, FOMs of the fabricated chips should be still competitive with conventional bandpass delta-sigma modulators.

4.10 Layout

The modulator was implemented in a silicon area of 2.55 mm×1.77 mm in 1P6M 0.18-μm CMOS technology. Figure 4.25 and Figure 4.26 show the floor plan and the layout of the modulator, respectively. The functions of the pins are described in Table B.1. Most of the digital lines, integrator inputs and outputs were routed on upper metal layers and shielded from the substrate by a lower metal layer in order to prevent injection and coupling of noise to and from the substrate. All NMOS transistors except those in the configuration registers which do not switch during normal operation of the modulator were put inside deep n-wells to isolate them from the noisy substrate. All of the capacitors were also located above deep n-wells for the same reasons.

4.10.1 Capacitor array layout

In the layout-level design of a tunable modulator, binary-weighted capacitor arrays for programmable switched-capacitor circuits are very distinctive compared to conventional delta-sigma modulators. Figure 4.27 shows a layout of a 5-bit binary-weighted capacitor

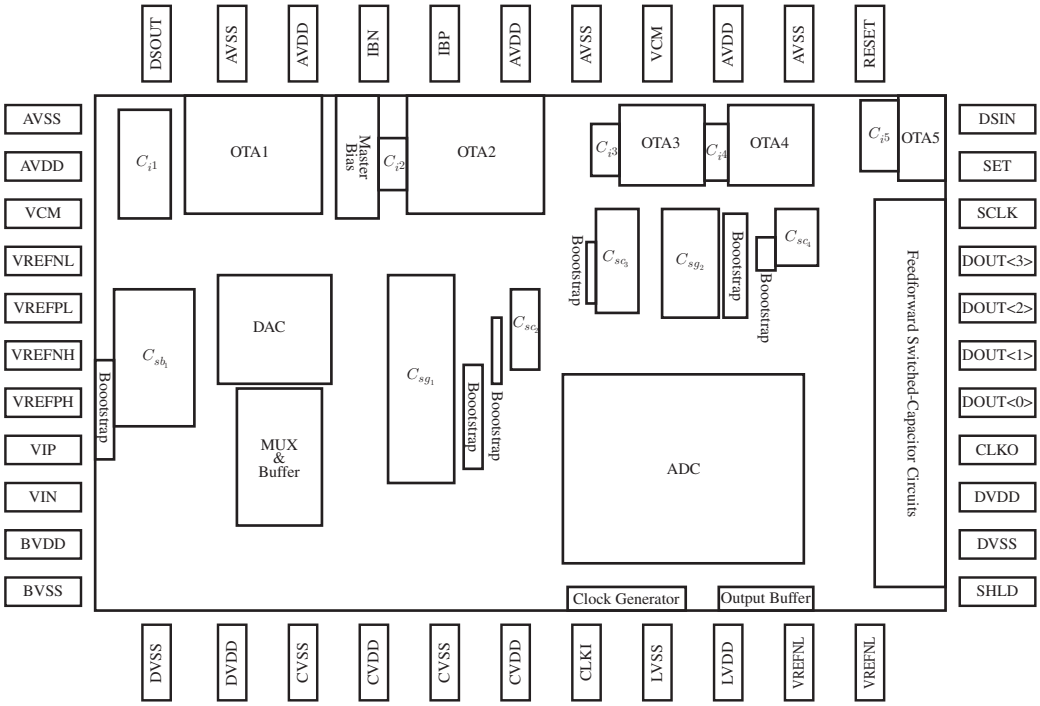

Figure 4.25: Modulator floor plan.

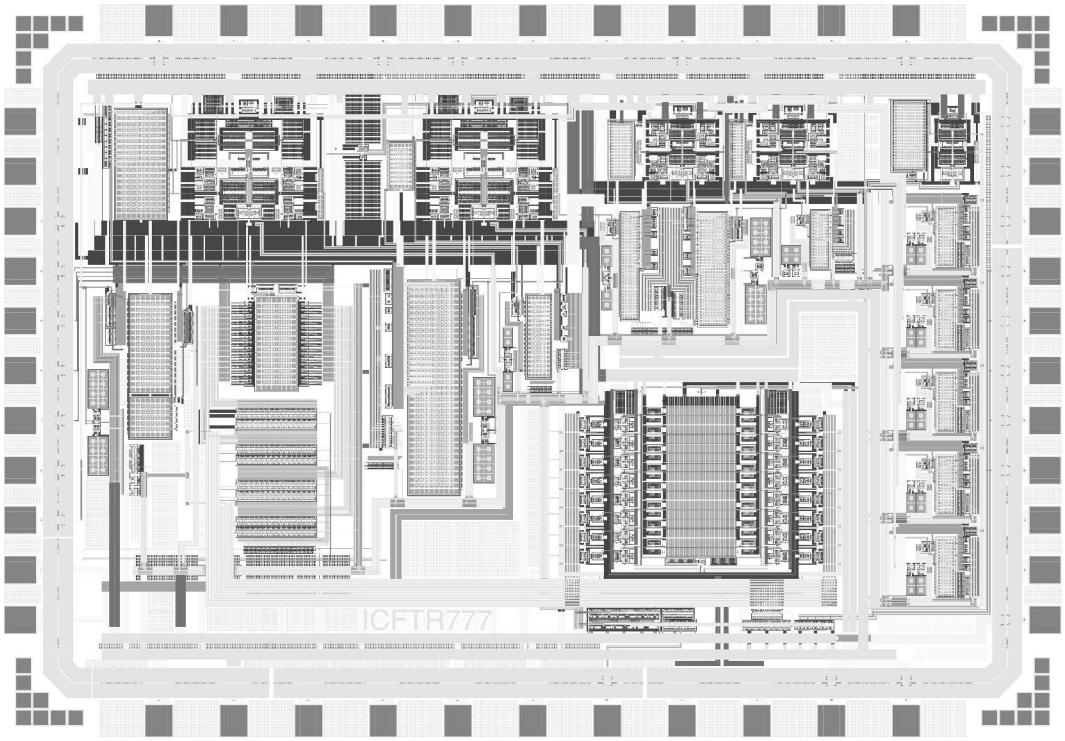

Figure 4.26: Modulator layout.

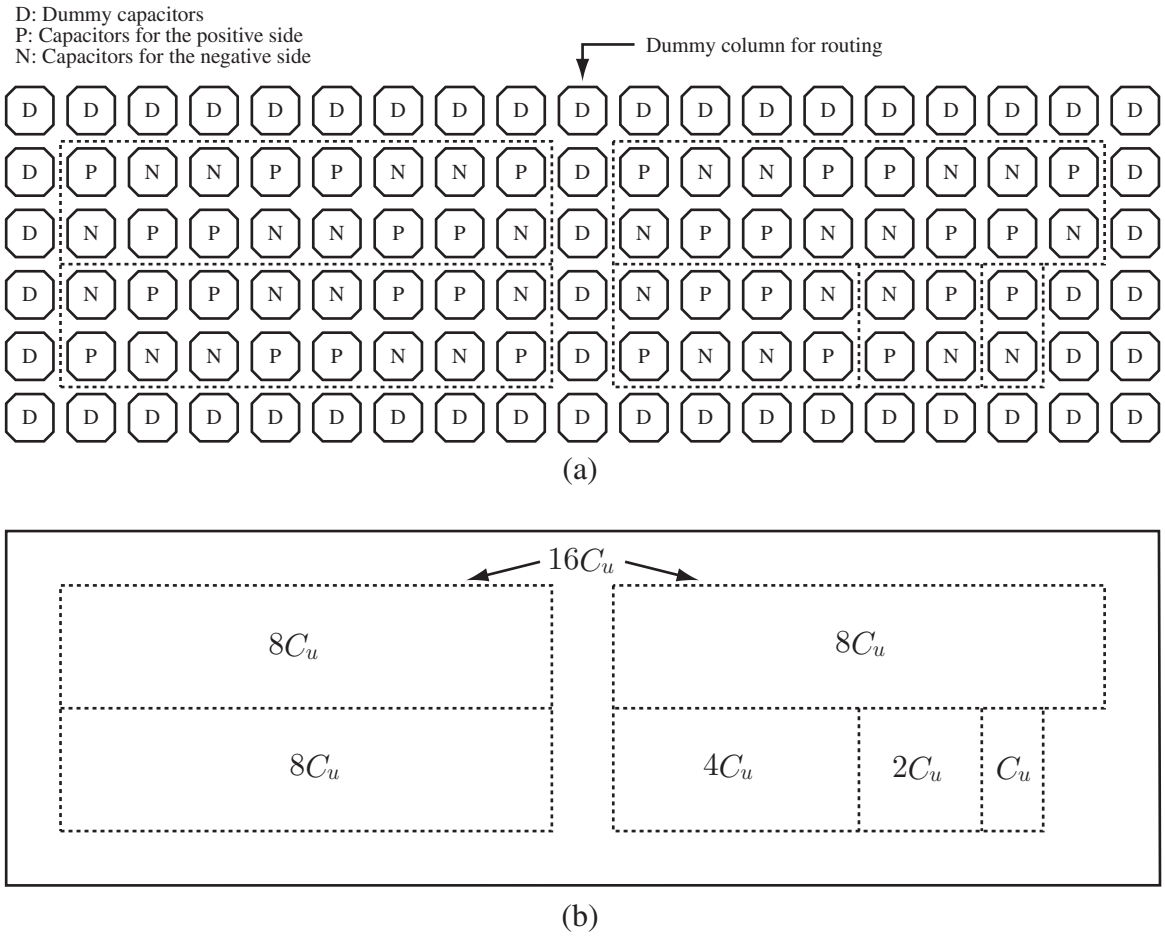

Figure 4.27: (a)5-bit Binary-weighted capacitor array (b)Capacitor array floorplan.

array. Matching between different binary weighted capacitors is not very important because a large error in the modulator coefficients has already been introduced by coefficient quantization. However, matching between the positive side and the negative side is still important for excellent noise rejection. Therefore, the common-centroid technique [31, Ch.7] was employed within each binary-weighted capacitor as shown in Figure 4.27. The same layout technique applies to capacitor arrays with different resolutions.

4.11 Summary

Transistor-level design of the tunable delta-sigma modulator was presented in this chapter. OTAs based on the specifications defined in the previous chapter were designed in the folded-cascode structure with gain boosters. The programmable switched-capacitors were

designed in such a way that excessive charge injection from large switches is prevented, and RC time constants of the switches and the capacitors do not increase. A peak SNDR of 96 dB was achieved in circuit simulations for four different center frequencies between DC to 25 MHz.

Chapter 5

Experimental Results

The tunable modulator was fabricated in the 1P6M (1 POLY layer + 6 metal layers) 0.18-μm CMOS technology with the MiM (Metal-insulator-Metal) capacitor and deep n-well options. Packaged chips were received a well in advance of the writing of this thesis. Unfortunately, many defects (shorted and disconnected circuits) in the top metal layer were found due to unrequested use of the thick-metal option by the fabrication service. These defects were found and reported immediately upon receipt of the chips. However, we are still waiting for chips that have a correct top metal thickness without defects.

For the rest of this chapter, the test setup prepared for the modulator is described.

5.1 Test Setup

5.1.1 PCB Design

The printed circuit board (PCB), shown in Figure 5.1 consists of an analog section and a digital section. A block diagram of the board is shown in Figure 5.2. The analog section provides various DC power voltages, reference voltages, and bias currents to the modulator. It also contains a transformer, which converts a single-ended signal to a differential input signal. The DC power voltages are generated by low-noise variable voltage regulators (TI TPS79101). Reference voltages are generated by potentiometers, and they are buffered by low-noise opamps (TI OPA2350). The transformer (Coilcraft WB2010) performs a single-ended to differential conversion. There are two SMA connecters in case a fully differential source is available. The main role of the digital section is to demultiplex

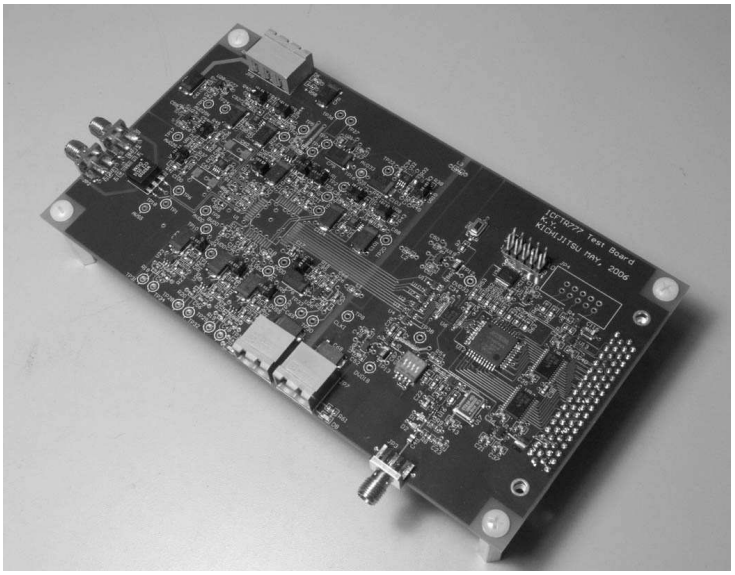

Figure 5.1: Assembled PCB.

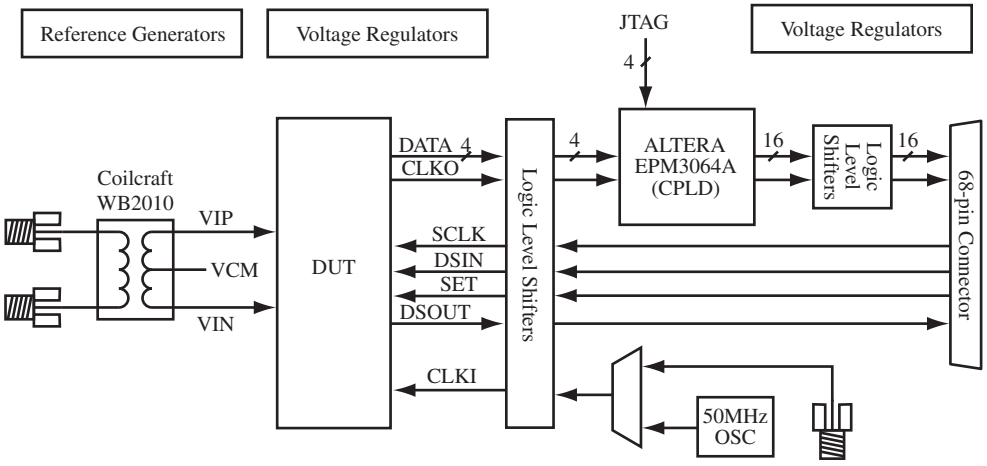

Figure 5.2: PCB block diagram.

the 4-bit output from the modulator to a 16-bit output. Demuxing is necessary because the maximum sampling rate of the interfacing PC digital I/O is 20 MHz although the sampling frequency of the modulator is 50 MHz. The modulator output in 1.8-V logic levels is converted to 3.3-V logic levels by level shifters. A CPLD (ALTERA EPM3064A) demuxes the data, and the demuxed data is converted to 5-V logic level to interface with a PC. The clock for the modulator is generated by an on-board 50-MHz crystal oscillator. In case a different clock frequency is required for testing, an external clock signal can be supplied through an SMA connector. Configuration signals from the PC are level-shifted to 1.8-V logic levels, and passed to the modulator.

Functionality of the PCB has been verified. It is ready for testing of the modulator.

5.1.2 Measurement Setup

Figure 5.3 shows a diagram of the planned test setup. Two signal generators are required for two-tone tests of the modulator. Their output is combined with a power combiner and the combined output is passed to the transformer for single-ended to differential conversion. The DC power supply powers the on-board voltage regulators. The digital output of the PCB is connected to a PCI Digital I/O (NI PCI-6534). A custom program that works with Matlab® continuously reads the digital input and performs the required processing such as DAC nonlinearity correction and spectral analysis. Since the output frequency of the sources has to be changed according to the center frequency, they are also controlled by the PC via a GP-IB interface for automated testing.

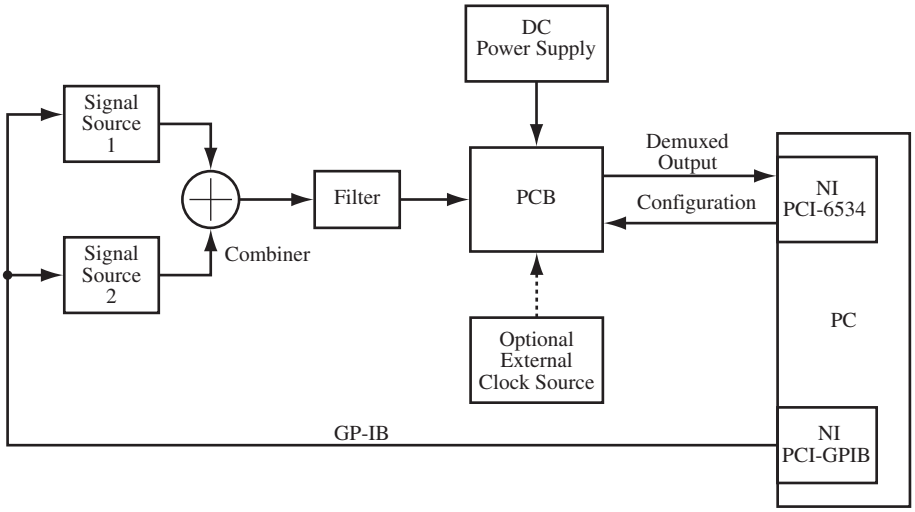

Figure 5.3: Planned test setup.

Chapter 6

Conclusions

Throughout this thesis, it was shown that a fully-tunable delta-sigma modulator can be implemented with an FOM competitive with conventional bandpass delta-sigma modulators with fixed passbands.

During the system-level design of the tunable modulator, the CRFF structure with the digital correction technique was found to be a suitable architecture for the tunable modulator. The NTF of the modulator and the output swing of the integrators are controlled by programmable coefficients. The resolution of the coefficients, which are realized by programmable switched-capacitor circuits, was made as low as possible in order to simplify programming and to save silicon area. It was found that simultaneous quantization of the modulator coefficients require very high-resolution quantization to maintain sufficient accuracy of the NTF zero locations because of a large error in the product of two quantized variables. However, the required resolution can be reduced by quantizing some of the variables with high resolution after coarse quantization of the other variables. Circuit nonidealities such as thermal noise and OTA settling time of all configurations were taken into account in the simulations in order to estimate the resulting degradation in SNDR of the circuit implementation.

The tunable modulator was implemented in a 0.18-μm CMOS technology. A proper structure for the programmable switched-capacitor circuits, which prevents excessive charge injection and does not increase the RC time constant of the capacitor and the switches, was used for coefficient programmability. Due to the programmability of the modulator, it can be easily transformed into a configuration for DAC output measurement, which is necessary for digital correction of the DAC nonlinearities.

The simulation results suggest that the SNDR of the modulator ranges from 96 dB to 86 dB with a 260-kHz bandwidth at a 50-MHz sampling rate for center frequencies varying from DC to 18.62 MHz, and a power consumption of 108 mW. The highpass modulator configuration with the center frequency very close to 25 MHz ($f_s/2$) did not function properly most probably because of the fast-changing nature of the modulator input that the first integrator, the summing stage, and/or the ADC cannot handle properly. It was confirmed that the highpass modulator configuration is functional for a lower sampling rate with a lower input frequency. The FOMs calculated from the simulation results are higher than any recently published fixed-band bandpass delta-sigma modulators. Therefore, very competitive FOMs are expected from the experimental device.

Fabricated chips did not function as expected due to defects in the top metal layer caused by unrequested use of the thick-top-metal option by the fabrication service. The test setup is ready, so testing can be started as soon as the new chips arrive.

6.1 Future Work

First of all, any system with a tunable delta-sigma modulator for A-to-D conversion will rely on extra digital hardware - a decimation filter and/or a digital mixer. An efficient way to perform these digital signal processing will be required for integration.

In addition, a quadrature signal is sometimes available from a preceding mixer for some radio receivers. In such a case, a quadrature delta-sigma is very attractive because it offers the same SQNR with a wider bandwidth due to spectral asymmetry in the frequency domain [10]. Therefore, a quadrature implementation of the tunable modulator is another possibility for future work.

Finally, the tunable modulator presented in this thesis consumes a large amount of power due to the fact that the OTAs were designed for the worst configuration. If any power scaling technique can be applied to the modulator, power may be saved for other configurations. The power consumption may be reduced for other configurations if any power scaling technique can be applied to the OTAs.

Appendix A

STF and NTF of the CRFF4 and CRFB4 structures

As explained in Section 2.2,

$$\mathrm{STF} = \frac{L_U}{1 - L_V} \tag{A.1}$$

$$\mathrm{NTF} = \frac{1}{1 - L_V}. \tag{A.2}$$

A.1 CRFF4 Structure

For this structure,

$$\begin{aligned} L_U \;=\; & \Big\{ a_1 H_D \left(b_1 - b_2 g_1 H_N\right)\left(1 + c_4 g_2 H_D H_N\right) + a_2 H_N \left(b_1 c_2 H_D + b_2\right)\left(1 + c_4 g_2 H_D H_N\right) \\ & + a_3 \left[c_3 H_D H_N \left(b_1 c_2 H_D + b_2\right) + b_3 H_D \left(1 + c_2 g_1 H_D H_N\right) H_D \left(b_3 - b_4 g_2 H_N\right)\left(1 + c_2 g_1 H_D H_N\right)\right] \\ & + a_4 \left[c_3 c_4 H_D {H_N}^2 \left(b_1 c_2 H_D + b_2\right) + b_3 b_4 H_D H_N \left(1 + c_2 g_1 H_D H_N\right)\right] \\ & + b_5 \left(1 + c_2 g_1 H_D H_N\right)\left(1 + c_4 g_2 H_D H_N\right) \Big\} \Big/ \left[\left(1 + c_2 g_1 H_D H_N\right)\left(1 + c_4 g_2 H_D H_N\right)\right] \end{aligned} \tag{A.3}$$

$$\begin{aligned} L_V \;=\; & \Big[- a_1 c_1 H_D \left(1 + c_4 g_2 H_D H_N\right) - a_2 c_1 c_2 H_D H_N \left(1 + c_4 g_2 H_D H_N\right) - a_3 c_1 c_2 c_3 {H_D}^2 H_N \\ & - a_4 c_1 c_2 c_3 c_4 {H_D}^2 {H_N}^2 \Big] \Big/ \left[\left(1 + c_2 g_1 H_D H_N\right)\left(1 + c_4 g_2 H_D H_N\right)\right], \end{aligned} \tag{A.4}$$

where $H_D = \frac{z^{-1}}{1-z^{-1}}$ and $H_N = \frac{1}{1-z^{-1}}$. NTF is independent of b_k because L_V is independent if b_k.

If we let $b_1 = c_1$, $b_2 = b_3 = b_4 = 0$, and $b_5 = 1$,

$$\text{STF} \;=\; 1 \tag{A.5}$$

$$\begin{aligned}\text{NTF} \;=\; & (1 + c_2 g_1 H_D H_N) \Big/ \Big[(1 + c_2 g_1 H_D H_N)(1 + c_4 g_2 H_D H_N) + a_1 c_1 H_D (1 + c_4 g_2 H_D H_N) \\ & + a_2 c_1 c_2 H_D H_N (1 + c_4 g_2 H_D H_N) + a_3 c_1 c_2 c_3 {H_D}^2 H_N + a_4 c_1 c_2 c_3 c_4 {H_D}^2 {H_N}^2 \Big].\end{aligned} \tag{A.6}$$

For $0 \geq c_2 g_1 \leq 4$ and $0 \geq c_4 g_2 \leq 4$, the NTF zeros are located at

$$\frac{2 - c_2 g_1 \pm j\sqrt{4 c_2 g_1 + {c_2}^2 {g_1}^2}}{2} \text{ and } \frac{2 - c_4 g_2 \pm j\sqrt{4 c_2 g_2 + {c_4}^2 {g_2}^2}}{2}, \tag{A.7}$$

respectively, and they travel from 0 to -1 on the unit circle in the z-domain via $\pm j$. These NTF zeros exactly coincide with the pole locations of the two resonators.

A.2 CRFB4 structure

For this structure,

$$\begin{aligned}L_U \;=\; & c_2 c_3 c_4 H_D {H_N}^2 (b_1 c_1 H_D + b_2) + c_4 H_N (b_3 c_3 H_D + b_4)(1 + c_1 g_1 H_D H_N) \\ & b_5 (1 + c_1 g_1 H_D H_N)(1 + c_3 g_2 H_D H_N) \Big/ (1 + c_1 g_1 H_D H_N)(1 + c_3 g_2 H_D H_N)\end{aligned} \tag{A.8}$$

$$L_V = \frac{-c_2 c_3 c_4 H_D {H_N}^2 (a_1 c_1 H_D + a_2) - c_4 H_N (a_3 c_3 H_D + a_4)(1 + c_1 g_1 H_D H_N)}{(1 + c_1 g_1 H_D H_N)(1 + c_3 g_2 H_D H_N)}, \tag{A.9}$$

where $H_D = \frac{z^{-1}}{1-z^{-1}}$ and $H_N = \frac{1}{1-z^{-1}}$. NTF is independent of b_k because L_V is independent if b_k. If we let $b_1 = a_1$, $b_2 = a_2$, $b_3 = a_3$,$b_4 = a_4$, and $b_5 = 1$,

$$\text{STF} = 1 \tag{A.10}$$

$$\begin{aligned}\text{NTF} \;=\; & (1 + c_1 g_1 H_D H_N)(1 + c_3 g_2 H_D H_N) \Big/ \Big[(1 + c_1 g_1 H_D H_N)(1 + c_3 g_2 H_D H_N) \\ & + c_2 c_3 c_4 H_D {H_N}^2 (a_1 c_1 H_D + a2) + c_4 H_N (a_3 c_3 H_D + a_4)(1 + c_1 g_1 H_D H_N) \Big].\end{aligned} \tag{A.11}$$

For $0 \geq c_1 g_1 \leq 4$ and $0 \geq c_3 g_2 \leq 4$ the NTF zeros are located at

$$\frac{2 - c_1 g_1 \pm j\sqrt{4c_1 g_1 + {c_1}^2 {g_1}^2}}{2} \text{ and } \frac{2 - c_3 g_2 \pm j\sqrt{4c_3 g_2 + {c_3}^2 {g_2}^2}}{2}, \tag{A.12}$$

respectively, and they travel from 0 to -1 on the unit circle in the z-domain via $\pm j$. These NTF zeros exactly coincide with the pole locations of the two resonators.

Appendix B

Chip Interface

B.1 Pin Description

The die was packaged in 44-pin CQFP package. Table B.1 shows descriptions of the pins.

B.2 Configuration Register Map

Configuration data are shifted into a shift register inside the chip. A bit at DSIN is loaded by a rising edge of SCLK. MSB is loaded first. Once all of the bits are loaded, SET is raised to activate the configuration. A register map is shown in Figure B.2.

Table B.1: Pin description.

Name	Description	Typical voltage	Pin number
AVDD	Analog VDD	1.8 V	25, 28, 31, 35
AVSS	Analog VSS	0 V	24, 27, 32, 34
BVDD	Bootstrapping VDD	1.8 V	43
BVSS	Bootstrapping VSS	0 V	44
CVDD	Clock VDD	1.8 V	4, 6
CVSS	Clock VSS	0 V	3, 5
DVDD	Digital VDD	1.8 V	2, 14
DVSS	Digital VSS	0 V	1, 13
LVDD	Latch VDD	1.8 V	9
LVSS	Latch VSS	0 V	8
IBN	NMOS bias	10 μA (into chip)	30
IBP	PMOS bias	10 μA (out of chip)	29
VREFPH	High positive reference	1.8 V	40
VREFNH	High negative reference	0 V	39
VREFPL	Low positive reference	1.05 V	11, 38
VREFNL	Low negative reference	0.75 V	10, 37
VCM	Common-mode voltage	0.9 V	26, 36
VIP	Positive input signal	-	41
VIN	Negative input signal	-	42
CLKO	Clock output	-	15
DOUT$\langle 0 \rangle$	Data output (LSB)	-	16
DOUT$\langle 1 \rangle$	Data output	-	17
DOUT$\langle 2 \rangle$	Data output	-	18
DOUT$\langle 3 \rangle$	Data output (MSB)	-	19
CLKI	Clock input	-	7
DSIN	Configuration register data input	-	22
DSOUT	Configuration register data output	-	33
SCLK	Configuration register clock	-	20
SET	Configuration register strobe	-	21
SHLD	Digital shield	0 V	12

Table B.2: Configuration register map.

Name	Description	Location
$n_{i1}\langle 5:0\rangle$	-	$\langle 81:76\rangle$
CAL	0: Normal operation, 1: DAC output measurement	75
DCAL$\langle 14:0\rangle$	DAC input in thermometer code	$\langle 74:60\rangle$
$n_{g1}\langle 6:0\rangle$	-	$\langle 59:53\rangle$
$n_{c2}\langle 4:0\rangle$	-	$\langle 52:48\rangle$
$n_{c3}\langle 5:0\rangle$	-	$\langle 47:42\rangle$
$n_{g2}\langle 6:0\rangle$	-	$\langle 41:35\rangle$
$n_{c4}\langle 4:0\rangle$	-	$\langle 34:30\rangle$
$sgn(a_5)$	0: positive, 1: negative	29
$n_{a5}\langle 4:0\rangle$	-	$\langle 28:24\rangle$
$sgn(a_4)$	0: positive, 1: negative	23
$n_{a4}\langle 4:0\rangle$	-	$\langle 22:18\rangle$
$sgn(a_3)$	0: positive, 1: negative	17
$n_{a3}\langle 4:0\rangle$	-	$\langle 16:12\rangle$
$sgn(a_2)$	0: positive, 1: negative	11
$n_{a2}\langle 4:0\rangle$	-	$\langle 10:6\rangle$
$sgn(a_1)$	0: positive, 1: negative	5
$n_{a1}\langle 4:0\rangle$	-	$\langle 4:0\rangle$

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