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Pre-FEC and Post-FEC BER as Criteria for Optimizing Wireline Transceivers

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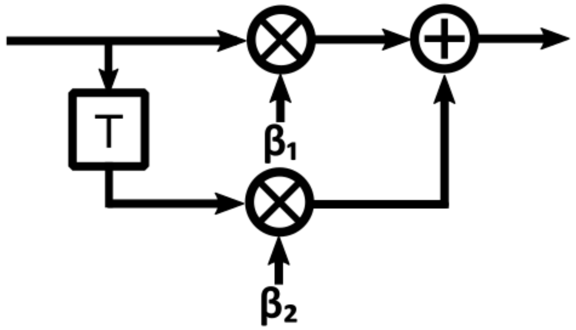
Outline

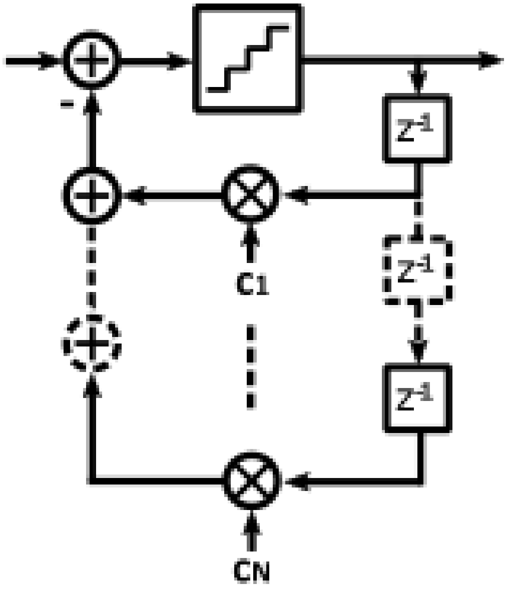
1. Motivation
2. Wireline Transceiver Model
3. Impact of Varying FFE and DFE Tap Weights on Pre-FEC and Post-FEC BER
4. 1/(1+D) Pre-Coding
5. Conclusion

Motivation

- Common receiver DSP equalizer blocks in 100Gb/s+ wireline applications:
  - Feed-forward Equalizer (FFE)
    - Noise amplification
    - High speed operation
    - No error propagation

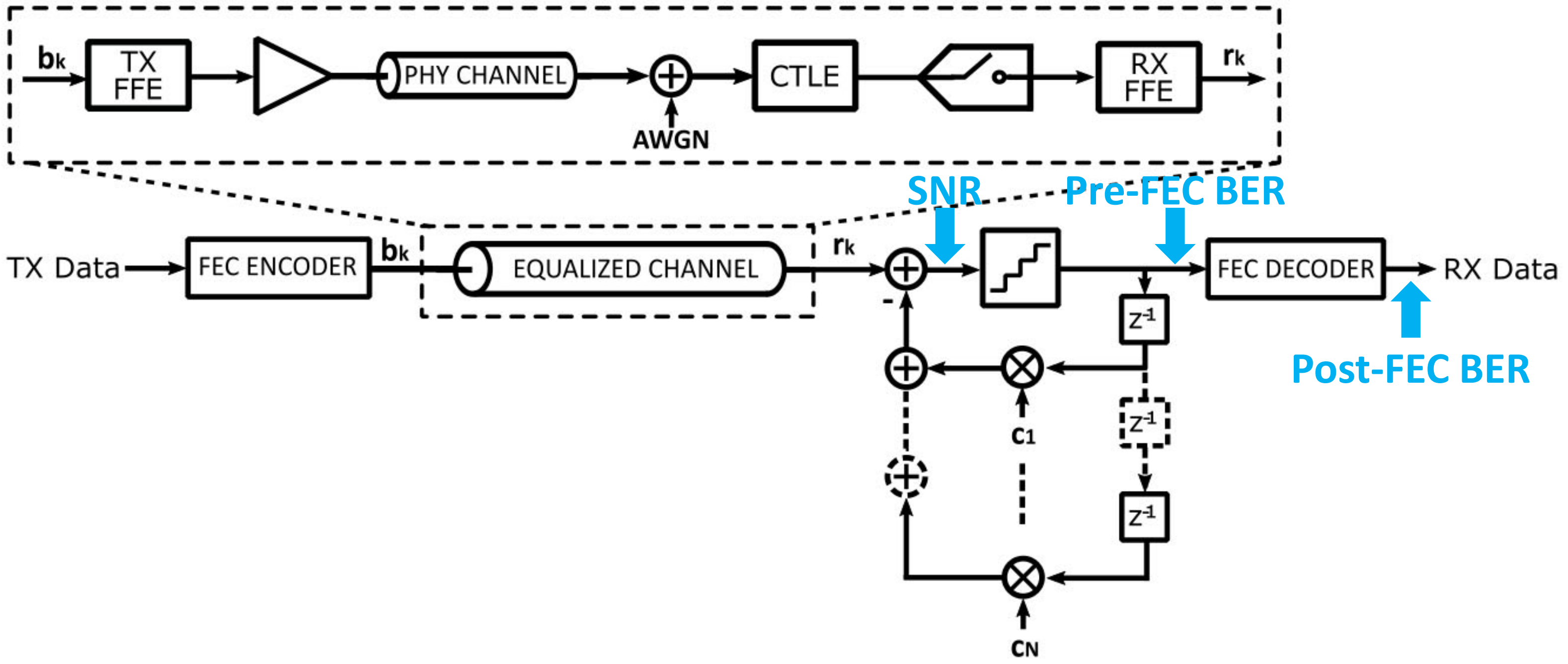


  - Decision-Feedback Equalizer (DFE)
    - Error propagation
    - Speed limited by critical feedback path
    - No noise amplification



- Forward-Error Correction (FEC) code have also become an integral part of the DSP
  - Standard Reed-Solomon (RS) to mitigate DFE error propagation
  - Ex: RS(544,514,15) KP4 code to achieve a targeted post-FEC BER <10^{-15}

Motivation



- Three performance metrics for optimizing equalizer coefficients in wireline transceivers:
  - SNR (Implicitly the optimization criteria when using LMS adaptation)
  - Pre-FEC BER
  - Post-FEC BER

Metric	FFE Noise Amplification	DFE Error Propagation	Sensitivity to Long Burst Errors at very low BER
SNR	✓	✖	✖
Pre-FEC BER	✓	✓	✖
Post-FEC BER	✓	✓	✓

Motivation

- FFE and DFE tap coefficients are typically optimized to maximize signal-to-noise ratio (SNR) or to minimize the mean-squared error (MMSE) or pre-FEC BER [1-3]
- Equalizer parameters found by conventional methods do not necessarily minimize post-FEC BER
- This paper presents an accurate and efficient methodology for finding the impact of wireline transceiver parameters, such as equalizer coefficients, on post-FEC BER

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1. Motivation
2. **Wireline Transceiver Model**
    a. System Overview
    b. DFE Error Propagation
3. Impact of Varying FFE and DFE Tap Weights on Pre-FEC and Post-FEC BER
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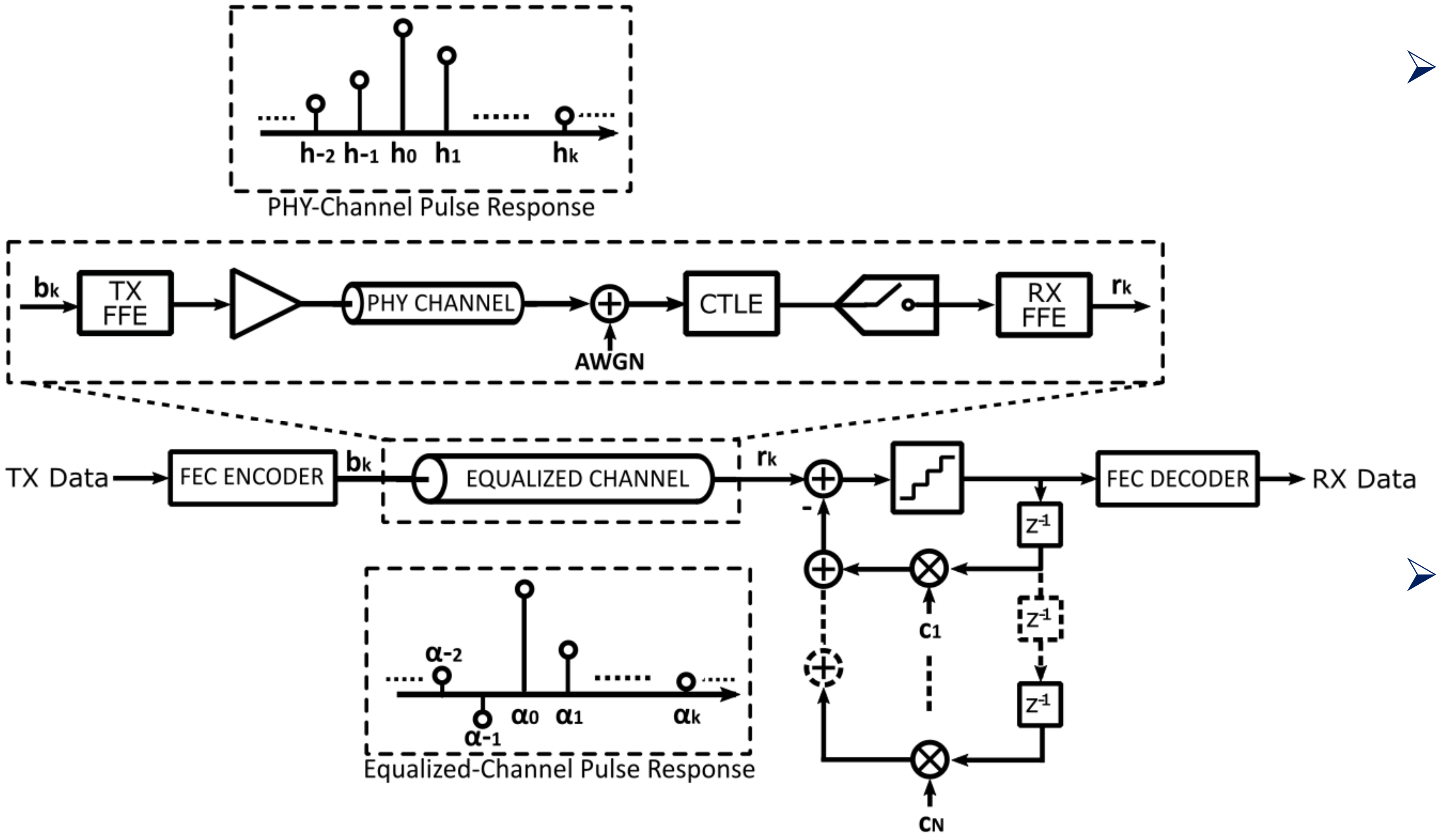
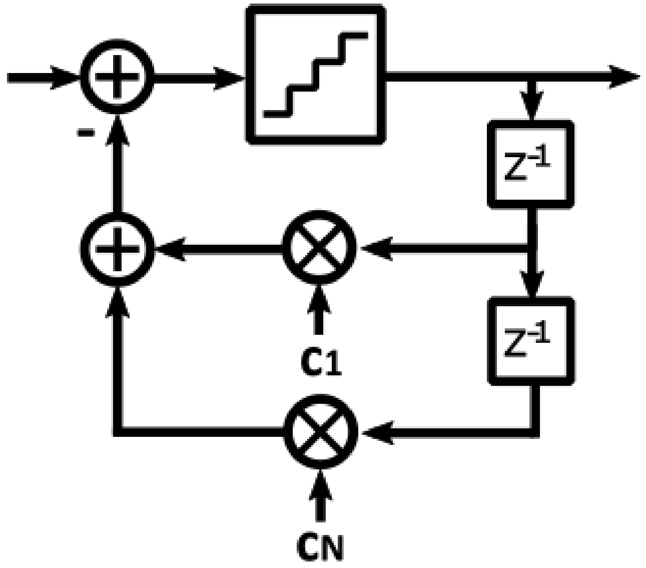
Transceiver Model – System Overview

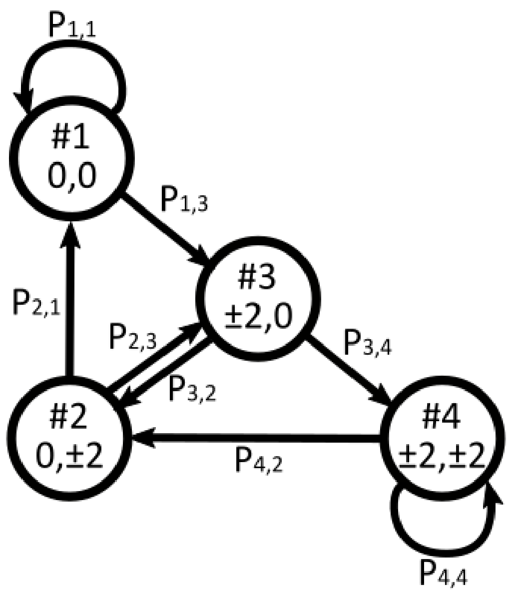


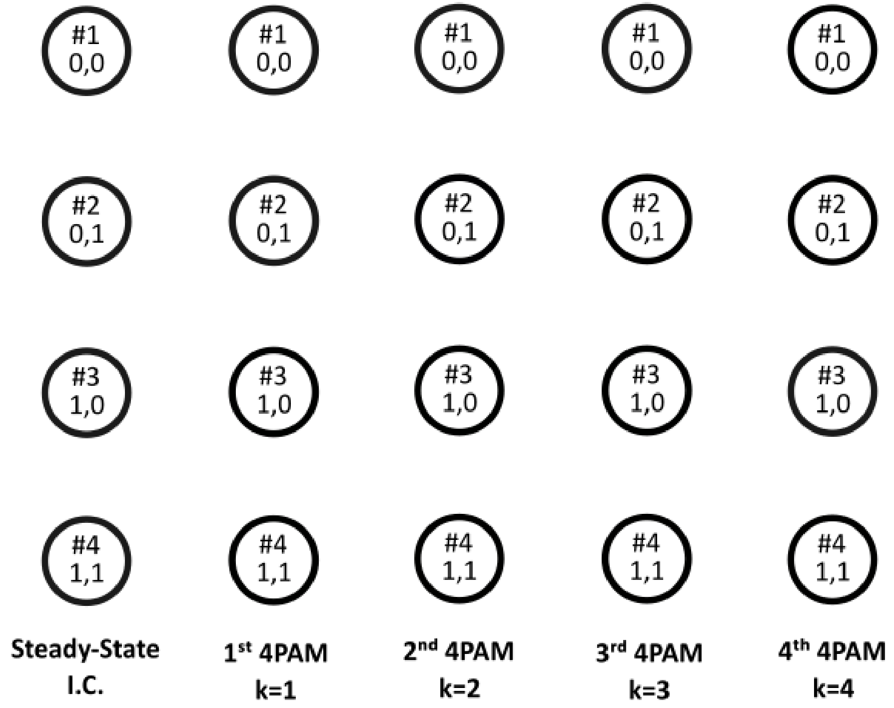
- Equalized pulse response $\alpha(z)$ is generated by convolving the physical channel's pulse with the impulse response of other components in the link, such as the TX FFE, TX driver, CTLE and RX FFE

- Additive white Gaussian noise (AWGN) assumed at CTLE input, creating correlated noise samples after CTLE filtering

Transceiver Model – DFE Error Propagation [Yang, TCAS-I, 2020]



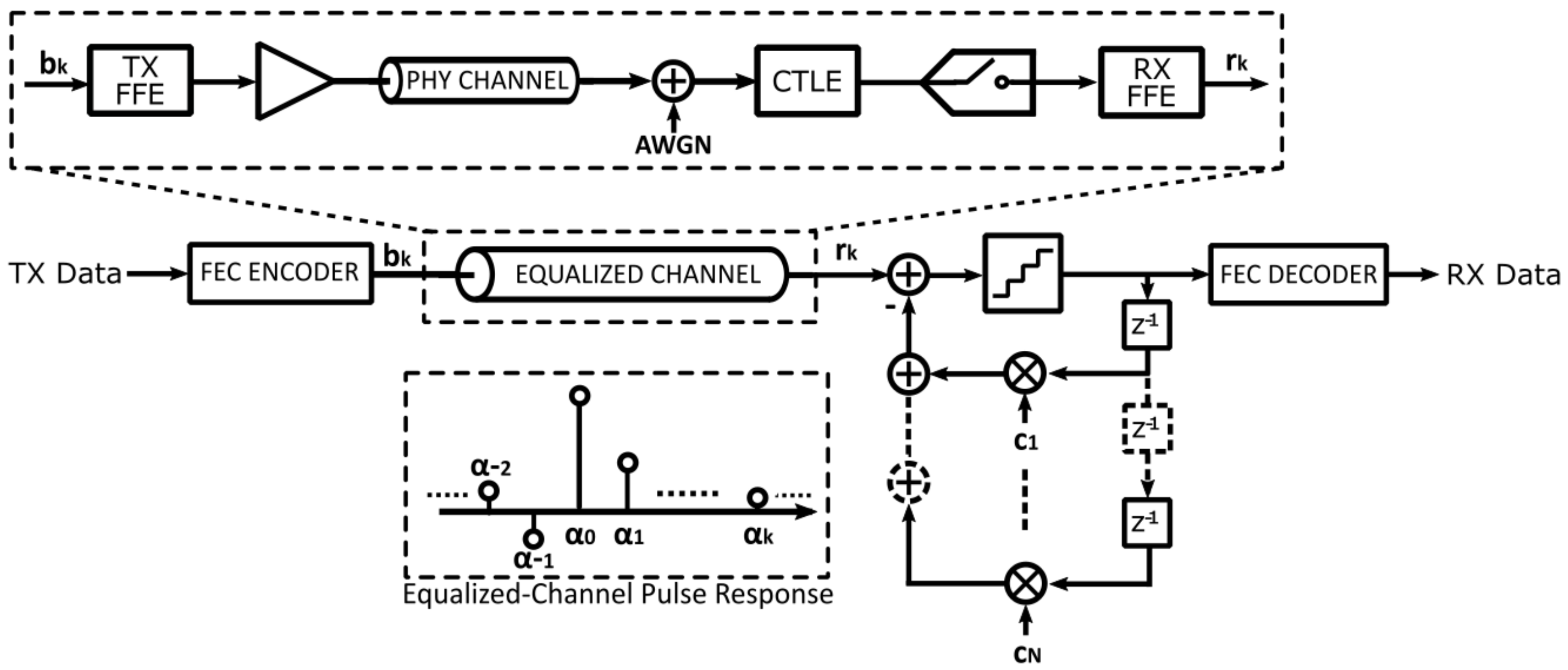


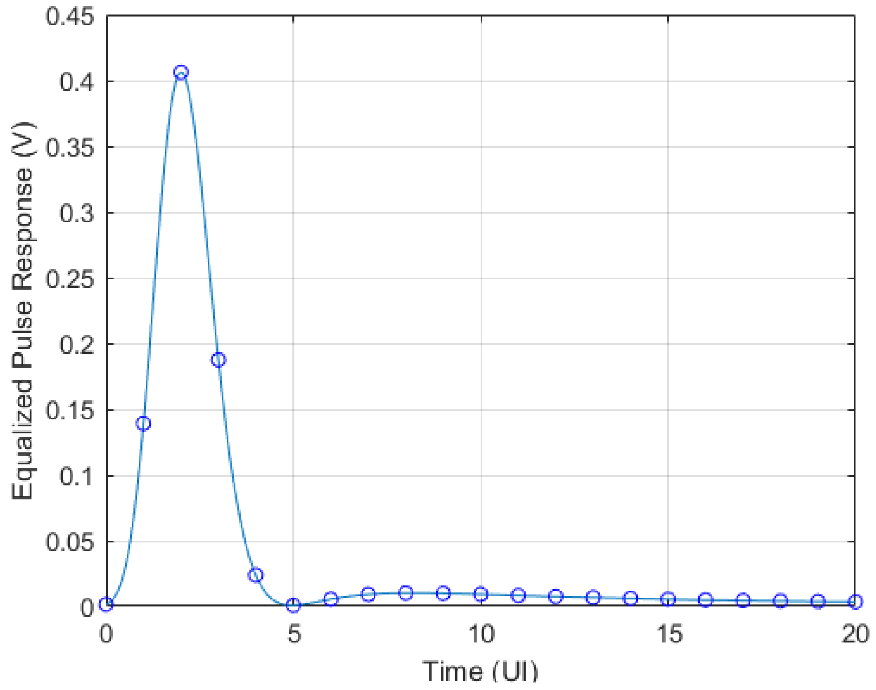


- Example of a 2-tap DFE represented by a simplified 4-state Markov model
- Time-unrolling the Markov DFE model to generate PAM trellis
- Apply trellis dynamic programming to the PAM trellis to efficiently collect all error patterns

Outline

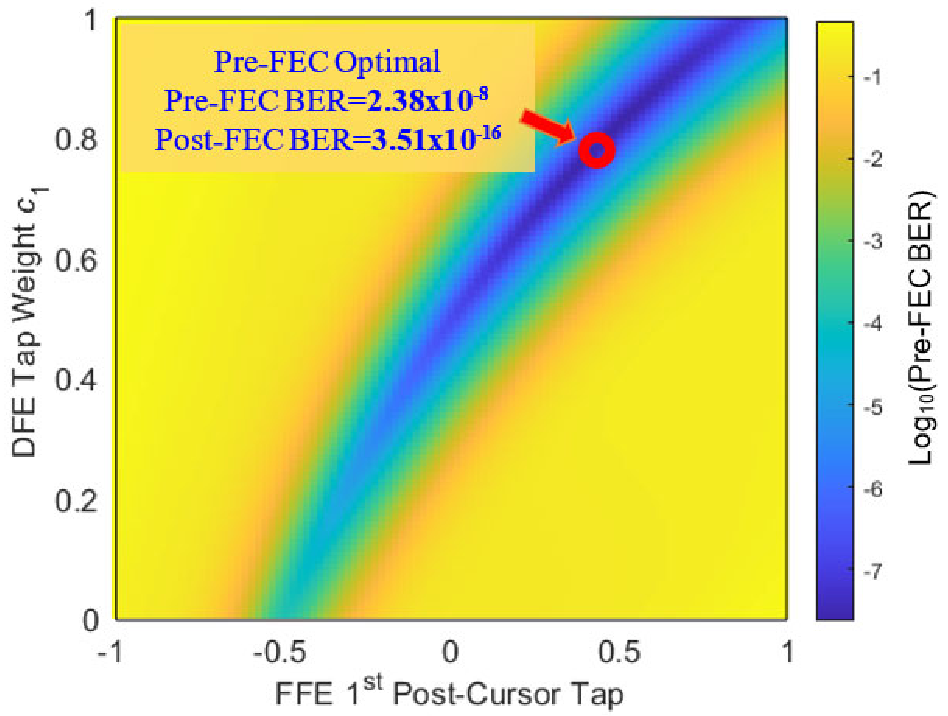
Pre-FEC vs Post-FEC BER Optimum - Link Setup

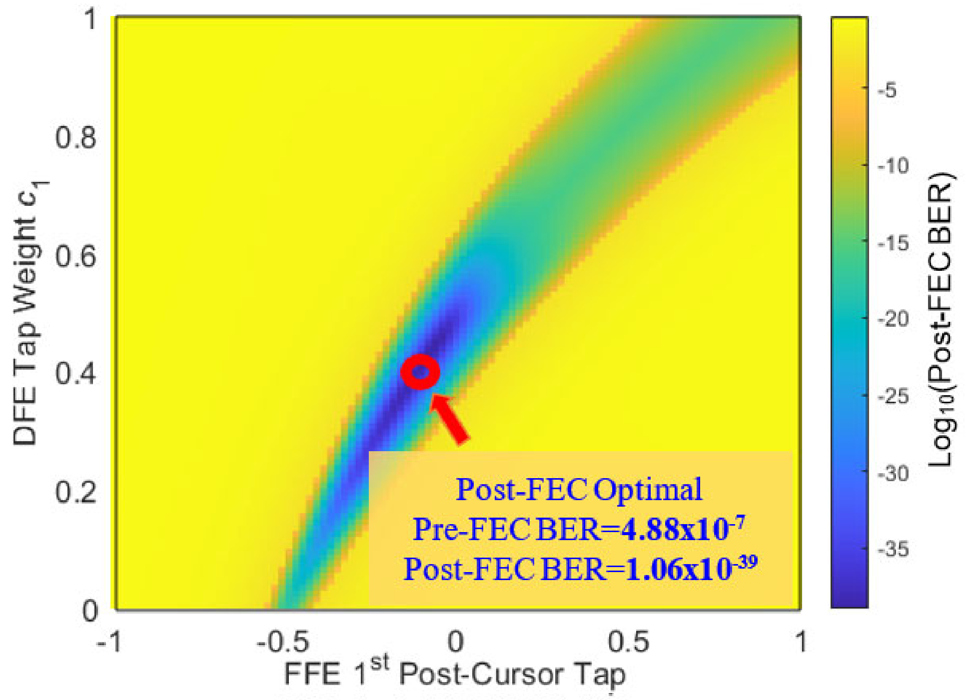




- A channel model with 30 dB insertion loss for a link communicating 4-PAM symbols at 56 GBaud/s subject to 0.55 $V_{P\text{-}P}$ swing at TX, 4.58 mV_{rms} integrated rms noise
- A simplified CTLE model provides 12 dB peaking gain with 0 dB gain at DC
- A 1-tap DFE and a 7-tap FFE with 2 pre-cursor and 4 post-cursor taps at RX
- The post-FEC BER is calculated assuming the standard KP4 RS(544,514, 15) code

Pre-FEC vs Post-FEC BER Optimum





- Vastly different optimal point with proposed optimization approach
- Tradeoff between FFE noise amplification and DFE error propagation

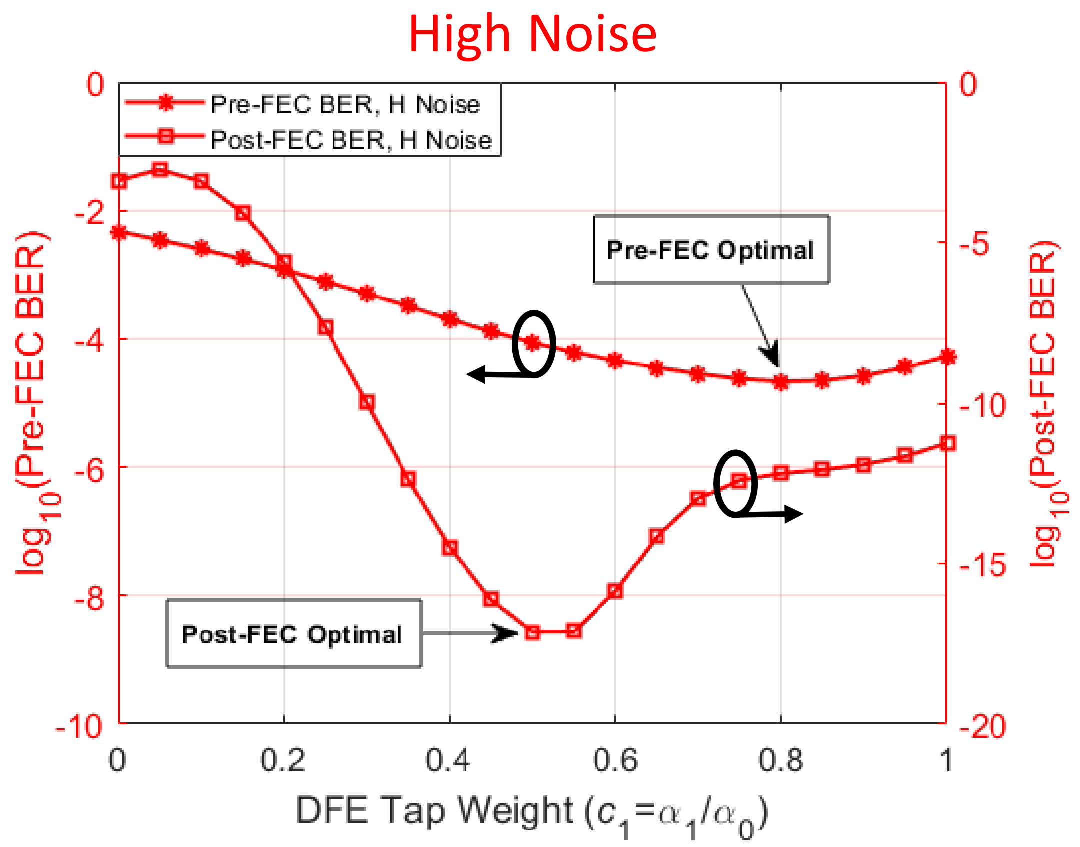
	Conventional Pre-FEC Optimization	Proposed Post-FEC Optimization
Pre-FEC BER	**2.38e-8**	**4.88e-7**
Post-FEC BER	**3.51e-16**	**1.06e-39**

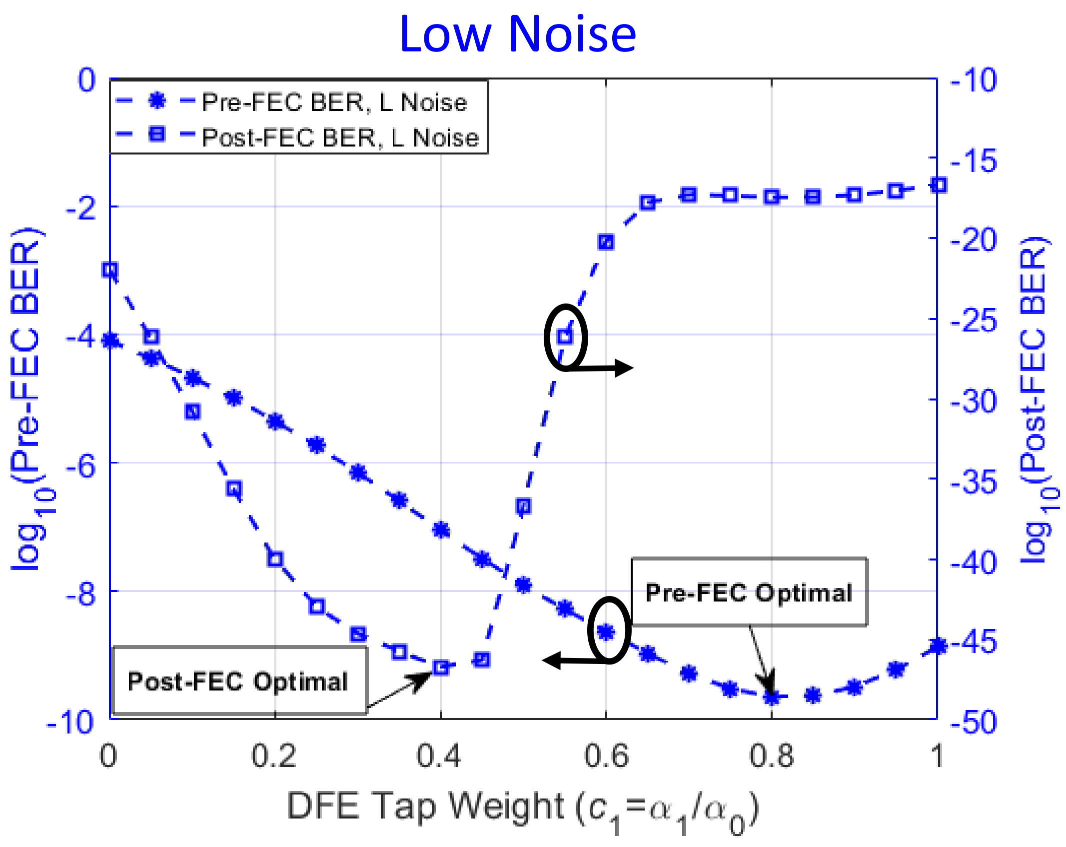
Significant improvement in post-FEC BER using proposed optimization approach

Simulation Results

- More extensive simulation results using six measured channel responses to validate our methodology using post-FEC BER
- TX has a 2-tap FFE providing 5 dB pre-emphasis, and the RX FFE has 15 taps, including 3 pre-cursor taps and 11 post-cursor taps
- An 8th-order CTLE model was applied to equalize all six channels having 30–40 dB insertion loss
- The equalized pulse responses including TX FFE, CTLE and PHY channel are tabulated in Table I of the paper

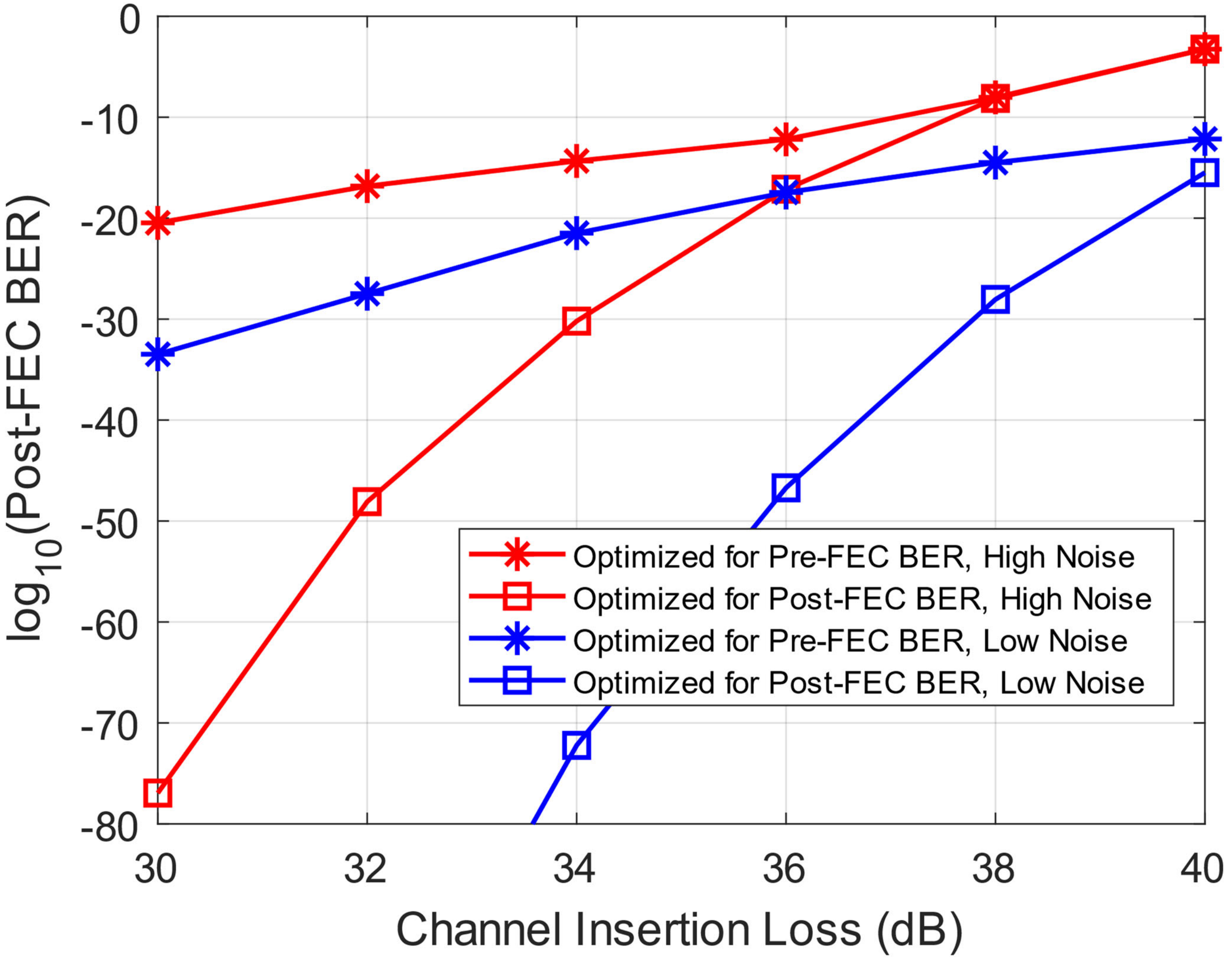
Simulation Results





- Plot both the pre-FEC BER and post-FEC BER as a function of DFE tap weight α_1/α_0 for the 36 dB channel
- Simulated at two integrated rms noise levels: 1.62 mV_{rms} (low noise) and 2.42 mV_{rms} (high noise)
- Different DFE coefficients at pre-FEC and post-FEC optimal
  - Post-FEC BER is minimized at a lower α_1/α_0 than pre-FEC

Simulation Results



- Repeating the same analysis for all six measured channels
- The optimal post-FEC BER obtained by post-FEC optimization is always superior

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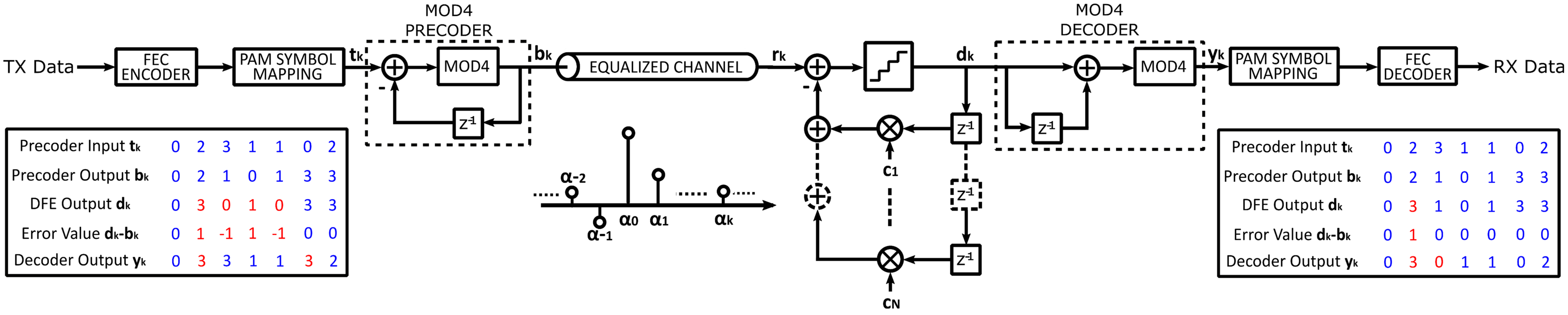
1/(1+D) Pre-Coding

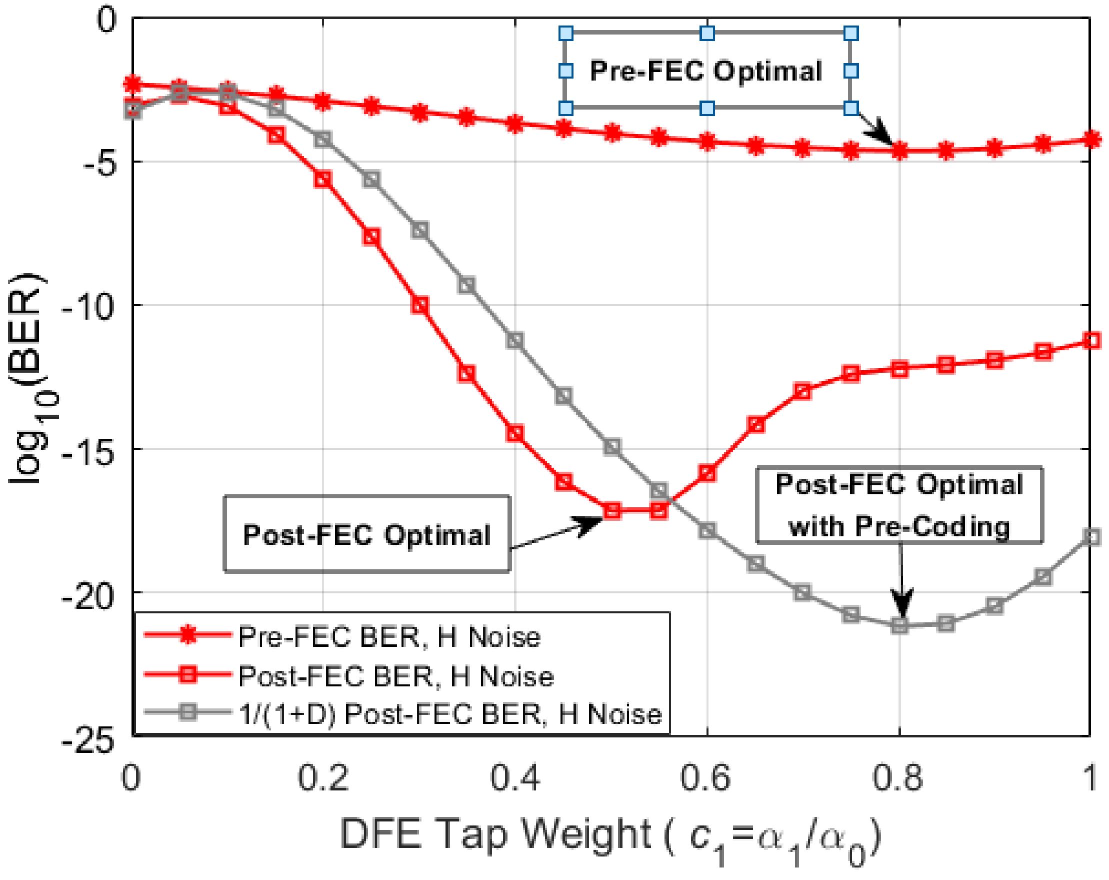


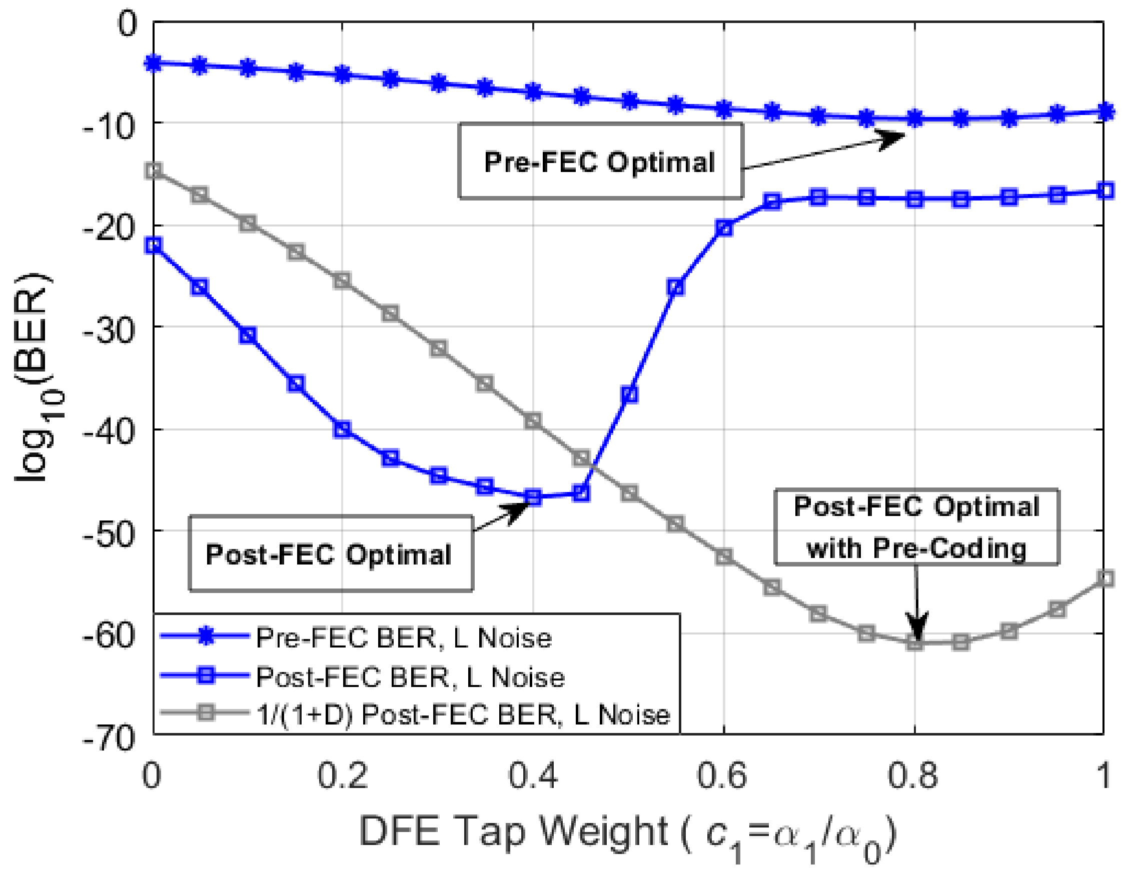
Precoder Input t_k	0	2	3	1	1	0	2
Precoder Output b_k	0	2	1	0	1	3	3
DFE Output d_k	0	3	0	1	0	3	3
Error Value d_k-b_k	0	1	-1	1	-1	0	0
Decoder Output y_k	0	3	3	1	1	3	2

Precoder Input t_k	0	2	3	1	1	0	2
Precoder Output b_k	0	2	1	0	1	3	3
DFE Output d_k	0	3	1	0	1	3	3
Error Value d_k-b_k	0	1	0	0	0	0	0
Decoder Output y_k	0	3	0	1	1	0	2

- A wireline transceiver model incorporating 1/(1+D) pre-coding to mitigate DFE error bursts
- 1/(1+D) decoder removes burst errors because the error d_k-b_k in the current received symbol is added to the error d_{k-1}-b_{k-1} in the previously received symbol
- Isolated individual symbol errors give rise to two consecutive symbol errors after decoding
- Method in [5] is used to generate the post-FEC BER results including 1/(1+D) pre-coding

1/(1+D) Pre-Coding





- Post-FEC BER of the previous 36dB channel case with and without 1/(1+D) pre-coding
- With pre-coding, both post-FEC and pre-FEC BER are minimized with the same equalizer coefficients

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Conclusion

- Using SNR or pre-FEC BER as performance metrics may not be effective in minimizing post-FEC BER when architecting and optimizing wireline links.

- Error propagation is not accurately accounted for when SNR or pre-FEC BER are used.

- In general, links attain their minimum post-FEC BER with equalizer coefficients very different from those that minimize pre-FEC BER.

- The introduction of 1/(1+D) pre-coding mitigates the impact of error bursts, ensuring that both pre-FEC and post-FEC BER are minimized with the same equalizer coefficients.

References

1. **M. Abdulrahman and D. D. Falconer, "Cyclostationary crosstalk suppression by decision feedback equalization on digital subscriber loops,", *IEEE J. Selected Areas Commun.*, vol. 10, no. 3, pp. 640–649, Apr. 1992.**

2. **Sheng Chen, L. Hanzo and B. Mulgrew, "Adaptive minimum symbol-error-rate decision feedback equalization for multilevel pulse-amplitude modulation," in *IEEE Transactions on Signal Processing*, vol. 52, no. 7, pp. 2092-2101, July 2004, doi: 10.1109/TSP.2004.828944.**

3. **Chen-Chu Yeh and J. R. Barry, "Adaptive minimum bit-error rate equalization for binary signaling," in *IEEE Transactions on Communications*, vol. 48, no. 7, pp. 1226-1235, July 2000, doi: 10.1109/26.855530.**

4. **M. Yang, S. Shahramian, H. Shakiba, H. Wong, P. Krotnev and A. C. Carusone, "Statistical BER Analysis of Wireline Links With Non-Binary Linear Block Codes Subject to DFE Error Propagation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 1, pp. 284-297, Jan. 2020, doi: 10.1109/TCSI.2019.2943569.**

5. **M. Yang, S. Shahramian, H. Shakiba, H. Wong, P. Krotnev and A. Carusone, "A Statistical Modeling Approach for FEC-Encoded High-Speed Wireline Links," *DesignCon 2020*, Santa Clara, CA, 2020.**

6. **K. Gopalakrishnan *et al.*, "A 40/50/100Gb/s PAM-4 ethernet transceiver in 28nm CMOS," *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2016, pp. 62-63.**

7. **A. Cevrero *et al*., "6.1 A 100Gb/s 1.1pJ/b PAM-4 RX with Dual-Mode 1-Tap PAM-4 / 3-Tap NRZ Speculative DFE in 14nm CMOS FinFET," *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2019, pp. 112-114, doi: 10.1109/ISSCC.2019.8662495.**

8. **R. Narasimha, N. Warke and N. Shanbhag, "Impact of DFE error propagation on FEC-based high-speed I/O links," *GLOBECOM 2009 - 2009 IEEE Global Telecommunications Conference*, Honolulu, HI, 2009, pp. 1-6.**

9. **A. Szczepanek, I. Ganga, C. Liu, and M. Valliappan, "10GBASE-KR FEC tutorial," Website, http://www.ieee802.org.**

10. ***Transcoding/FEC Options and Trade-offs for 100 Gb/s Backplane and Copper Cable*, IEEE Standard 802.3bj, Nov. 2011.**

11. ***FEC Codes for 400 Gbps 802.3bs*, IEEE Standard 802.3bs, Nov. 2014.**

12. **X. Dong, G. Zhang and C. Huang, "Improved engineering analysis in FEC system gain for 56G PAM4 applications," *DesignCon 2018*, Santa Clara, CA, 2018.**

13. **S. Kiran *et al*., "Modeling of ADC-Based Serial Link Receivers With Embedded and Digital Equalization," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 3, pp. 536-548, March 2019.**