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A Nano-Watt MOS-Only Voltage Reference with High-Slope PTAT Voltage Generators

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***Abstract*—This brief presents a MOS-only voltage reference circuit with high-slope proportional-to-absolute-temperature (PTAT) voltage generators for ultra-low-power applications. Biased by a nano-ampere current reference circuit, the PTAT voltage generator is realized by an asymmetrical differential cell with 2 additional cross-coupled NMOS/PMOS pairs, which enhance the slope of the PTAT voltage remarkably. As a result, only 2 cascaded PTAT stages are used to compensate the complementary-to-absolute-temperature (CTAT) voltage generated directly by a diode-connected NMOS in the current reference circuit. Therefore, much power and chip area can be saved. A trimming circuit is also adopted to compensate the process-related reference voltage variations. The experimental results of the proposed reference circuit fabricated in a 0.18-µm standard CMOS process demonstrate that the circuit could operate under a minimum supply voltage of 1 V, and generate a reference voltage of 756 mV with temperature coefficient of 74 and 49.6 ppm/°C under 1-V and 1.8-V power supply, respectively. The proposed circuit consumes only 23 nA under a 1-V power supply, and the active area is only 95 µm×170 µm.**

***Index Terms*—Voltage reference, analog integrated circuit, proportional-to-absolute-temperature (PTAT) voltage generator, low power, low voltage, nanowatt, high-slope, MOS-only**

I. Introduction

In recent years, many nano-watt voltage references have been developed for systems-on-a-chip (SoC) aimed at ultra low power applications such as implantable medical devices, wearable electronics, and the Internet of Things (IoT) [1]−[12].

Conventional bandgap references (BGRs) often employ the V_{BE} of a BJT as the complementary-to-absolute-temperature (CTAT) voltage, which is then compensated by a proportional-to-absolute-temperature (PTAT) voltage circuit with slope controlled by a ratio between resistors [8]. Power consumption in nano-watt range requires large resistors, occupying large chip area [6]. Therefore, resistor-less references have been developed for emerging low-power applications [1]−[6], [9]−[11]. BJTs have also been replaced by sub-threshold MOSFETs in low voltage references in [2]−[4], [7], [9] and [10].

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The MOS-only reference in [2] is realized with a sub-threshold NMOS biased by a current source with specific temperature coefficient (TC). It is then improved to structures with only 2 MOSFETs, achieving a extremely low power of only a few picowatt [3], and low supply voltage of 150 mV [4]. However, these references have relatively high sensitivity to process variations. Moreover, two different types of MOSFETs are used in [2] and [3], which increases the cost for additional masks. Similarly, the bulk-driven techniques for the MOS-only references in [9], [10] also require additional mask layers to implement NMOS in a deep N-well. In [6], nano-watt BGR and sub-BGR in standard CMOS utilize MOS-only PTAT voltage generators realized by asymmetrical differential cells to cancel the negative TC of a BJT's V_{BE}. However, because the slope of the PTAT voltage generated by a single cell is very low, 5 cascaded stages are required in the BGR, resulting in relatively large area and power consumption.

In this paper, a nano-watt MOS-only voltage reference with high-slope PTAT generators implemented in a standard CMOS technology is presented. With 2 cross-coupled NMOS/PMOS pairs added in the asymmetrical differential cell, the slope of the output PTAT voltage is enhanced remarkably. Only 2 stages of PTAT generators are needed to compensate the CTAT voltage, which is generated directly by a sub-threshold NMOS transistor in the bias circuit. Therefore, much chip area and power consumption can be saved.

II. Operation Principle and Circuit Architecture

The proposed voltage reference circuit consists of 2 stages of PTAT voltage generators biased by a nano-ampere current reference circuit. In order to reduce power consumption and chip area further, the CTAT voltage is obtained directly from the bias circuit, without using any extra circuitry. The operating principles and the structure of the proposed MOS-only reference circuit are described as follows.

A. Bias Circuit and CTAT Voltage Generator

The schematic of the current reference and CTAT voltage generator with transistor sizes is shown in Fig. 1. The operation of the start-up circuit is similar with that in [6], in which M_{N14} and M_{P7} force the current reference circuit to depart from the zero-current state by injecting a high voltage to the gate of M_{N3}. M_{P7} will then be turned off by M_{P8} automatically when the current reference approaches its normal state. M_{N7} ~ M_{N13} in the current mirror are designed with very low aspect ratios to

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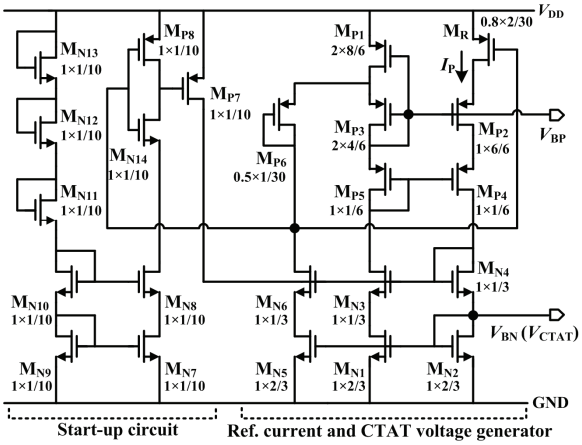

Fig. 1. Proposed reference current and CTAT voltage generator. (Sizes are given with a format of W(μm)×fingers/L(μm)).

achieve a current consumption of about 2 nA for the start-up circuit. Besides the start-up circuit, all transistors operate in sub-threshold region except for the PMOS resistor, M_R, which operates in strong-inversion and deep-triode region. The basic principle and structure of the proposed reference current circuit is similar to that in [6], [12]. However, the bias voltage of M_R in the proposed structure is obtained on the basis of the current reference circuit itself, eliminating the extra circuits to generate the bias voltage for the MOS resistor in [6], [12]. Therefore, the proposed structure is more area- and power-efficient.

If the $|V_{DS}|$ of a MOSFET is larger than $4V_T$, the drain current, I_D, is almost independent of V_{DS} and is given by

$$I_D = K\mu C_{OX} V_T^2 (\eta\text{-}1)\exp\left[\left(|V_{GS}| - |V_{TH}|\right)/(\eta V_T)\right] \quad (1)$$

where K is the aspect ratio (=W/L) of the MOSFET, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, η is the subthreshold slope factor, V_T(=k_BT/q) is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge [13]. The bias current I_P is determined by the V_{GS} and V_{DS} of M_R. When it operates in strong-inversion and deep-triode region, I_P is obtained as

$$I_P \approx K_R \mu_P C_{OX}\left(|V_{GS,MR}| - |V_{TH}|\right)\cdot|V_{DS,MR}| \quad (2)$$

where K_R is the aspect ratio of M_R, and μ_P is the hole mobility. From Fig. 1, we can obtain that $|V_{GS,MR}| = (|V_{GS,P1}| - |V_{GS,P3}| + |V_{GS,P6}|)$, and $|V_{DS,MR}| = |V_{GS,P1}| - |V_{GS,P2}|$. The expressions for $|V_{GS,MR}|$ and $|V_{DS,MR}|$ are similar to those in [12]. Thus, the exact derivation of I_P leads to an expression similar to that in [12]:

$$I_P = I_{P0} T^{2-m_P} \quad (3)$$

where I_{P0} is a current independent of temperature, and m_p is the temperature exponent of hole mobility.

As shown in Fig. 1, the V_{GS} of M_{N2} in the current reference circuit is directly used as the CTAT voltage, V_{CTAT}, without using any extra circuitry. Assuming that the electron mobility has a temperature dependence of $\mu_n = \mu_{n0}(T/T_0)^{m_N}$, V_{CTAT} can be obtained by substituting (3) into (1):

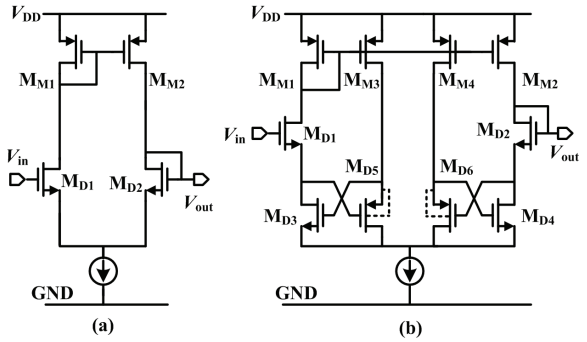

Fig. 2. (a) PTAT voltage generator in [6]; (b) proposed high-slope PTAT voltage generator.

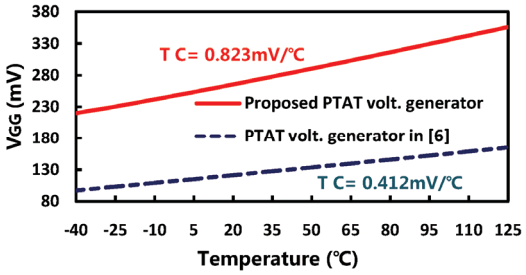

Fig. 3. Simulated temperature dependence of V_{GG}(=V_{out}−V_{in}) for the proposed PTAT voltage generator (Fig. 2(b)) and that in [6] (Fig. 2(a)).

$$V_{CTAT} = V_{TH} + \eta V_T \ln\left[\frac{I_{P0} T^{(m_N - m_P)}}{K_{N2}\mu_{n0} T_0^{m_N} C_{OX}(\eta - 1)(k_B/q)^2}\right] \quad (4)$$

where μ_{n0} is the mobility at T_0, and m_N is the temperature exponent of electron mobility [13]. Neglecting the difference between m_N and m_P, the term in the logarithm operator in (4) can be considered a constant independent of temperature.

The temperature dependence of the V_{TH} can be given by $V_{TH} = V_{TH0} + \kappa T$, where V_{TH0} is the threshold voltage at 0 K, and κ is the TC of V_{TH}, which is negative [1]. Therefore, the TC of V_{CTAT} can be obtained readily from its derivative:

$$k_1 = \frac{\partial V_{CTAT}}{\partial T} = \kappa + \eta\frac{k_B}{q}\ln\left[\frac{I_{P0}}{K_{N2}\mu_{n0} T_0^{m_N} C_{OX}(\eta - 1)(k_B/q)^2}\right] \quad (5)$$

The absolute value of the second term in (5) can be verified to be much less than that of κ. Therefore, V_{CTAT} is indeed a CTAT voltage. Simulated results show that V_{CTAT} is almost independent of V_{DD}, and has a TC of about -1.3 mV/ºC .

B. High-Slope PTAT Voltage Generator

Fig. 2(a) shows the MOS-only PTAT voltage generator in [6], which is essentially an asymmetrical differential cell with all MOSFETs operating in subthreshold region. The PTAT voltage is obtained as the gate-to-gate voltage of the differential pair. Based on (1), V_{GG} is derived as

$$V_{GG} = V_{out} - V_{in} = V_{GS,D2} - V_{GS,D1} = \eta V_T \cdot \ln\left(\frac{K_{D1}K_{M2}}{K_{D2}K_{M1}}\right) \quad (6)$$

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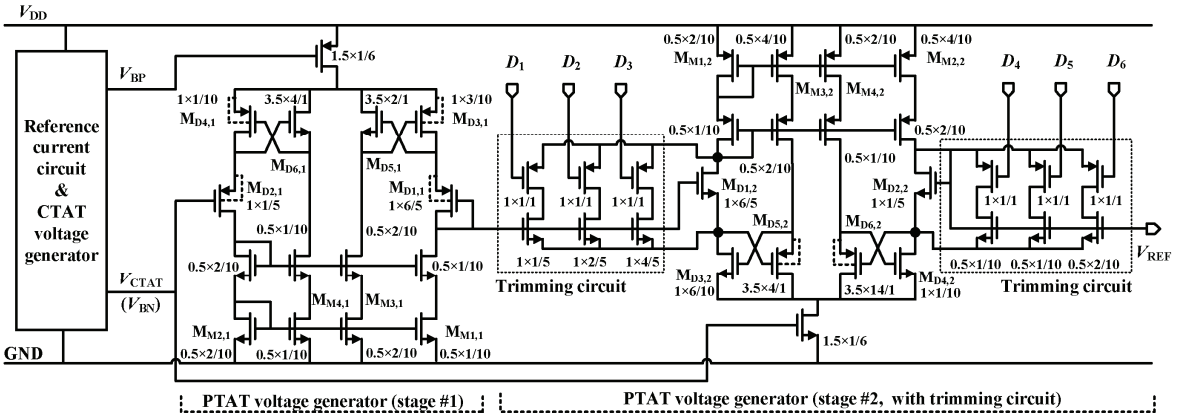

Fig. 4. Overall schematic of the proposed voltage reference circuit with transistor sizes.

where K_i is the aspect ratio of M_i [6]. If $K_{D1}K_{M2}/(K_{D2}K_{M1}) > 1$, V_{GG} is a PTAT voltage. An advantage of the circuit is that the PTAT slope is determined by size ratios of MOSFET pairs, which is accurate over process variations. However, because of the logarithm operation, the slope of the PTAT voltage is very low, and is difficult to be enlarged by using large transistors. Therefore, 5 stages are cascaded in [6] to cancel out the negative TC of V_{BE}, leading to relatively high power and area.

A modified asymmetrical differential cell has been presented in [14], in which a pair of BJTs with different areas is inserted between the source nodes of the differential pair (M_{D1} and M_{D2}) and the tail current source in Fig. 2(a). The added BJT pair increases the PTAT slope effectively, whereas the voltage headroom of the circuit is reduced by a V_{BE} (about 0.7 V), limiting its application in low voltage reference circuits.

The proposed PTAT voltage generator is given in Fig. 2 (b), which enhances the PTAT voltage slope remarkably, while consuming very small extra voltage headroom. As can be seen, 2 additional cross-coupled NMOS/PMOS pairs (M_{D3}/M_{D5} and M_{D4}/M_{D6}) are employed in the asymmetrical differential cell, in which M_{D5} and M_{D6} are biased by the currents provided by M_{M3} and M_{M4}, respectively. With a fixed tail current source, the exact allocation of current to each branch is determined by the exact sizes of the transistors in the cell. The gate-to-gate voltage of the proposed cell ($V_{GG} = V_{out} - V_{in}$) is given by

$$V_{GG} = \left(V_{GS,D2} + V_{GS,D4} - \left|V_{GS,D6}\right|\right) - \left(V_{GS,D1} + V_{GS,D3} - \left|V_{GS,D5}\right|\right) \quad (7)$$

As shown in Fig. 2(b), M_{D3} and M_{D4} have almost the same V_{TH} as their source voltages are same. The body nodes of M_{D5} and M_{D6} are tied to their source nodes to ensure almost equal V_{TH} for them. However, there still exists a difference between the V_{TH} of M_{D1} and M_{D2} caused by the body effect. Neglecting the small difference in η of PMOS and NMOS, V_{GG} can be derived as:

$$V_{GG} = \eta V_T \ln\left(\frac{K_{D1}K_{M2}}{K_{D2}K_{M1}}\frac{K_{D3}K_{M2}}{K_{D4}K_{M1}}\frac{K_{D6}K_{M3}}{K_{D5}K_{M4}}\right) + \Delta V_{TH,D21} \quad (8)$$

where $\Delta V_{TH,D21}=V_{TH,D2}-V_{TH,D1}$. The difference between the source voltages of M_{D2} and M_{D1} equals to $(V_{GS,D4}-V_{GS,D3})+(|V_{GS,D5}|-|V_{GS,D6}|)$, which is about 140 mV from the final simulation, resulting in a $\Delta V_{TH,D21}$ of about 35 mV for the technology used. The influences of $\Delta V_{TH,D21}$ on the slope of V_{GG} and the reference voltage value can be compensated by adjusting the transistor sizes based on simulation. We can see that the first term of (8) has more multiplication factors in the logarithm operator than (6) because there are 3 pairs of MOSFETs contributing difference in V_{GS} to the output. Therefore, the proposed circuit can provide much higher PTAT slope with proper aspect ratios of corresponding transistors.

Compared with the circuit in Fig. 2(a), the proposed circuit only consumes an extra voltage headroom of $V_{DS,D4}$ (or $V_{DS,D3}$), which can be as low as 0.1 V. Therefore, the proposed circuit is also suitable for low voltage applications. Moreover, the output voltage has little dependence on bias currents, thus, the proposed circuit can work under the same or even lower bias current than that of Fig. 2(a). Fig. 3 plots the simulated temperature dependence of V_{GG} for the two circuits. In simulation, the transistor sizes and bias current given in [6] are used for the circuit in Fig. 2(a), which has a total gate area of about 790 μm^2 and bias current of 10 nA. The transistor sizes in Fig. 4 (the second stage) are used for the proposed circuit, with a total gate area of only about 270 μm^2. The bias circuit in Fig. 1 is used to provides a bias current of only 2.5 nA for the proposed circuit. Both circuits are simulated under a 1.8-V power supply. As seen from Fig. 3, the proposed circuit achieves a PTAT slope of 0.82 mV/ºC, which is almost twice of that of Fig. 2(a), while consuming less power and area.

C. Overall Schematic

The overall schematic of the proposed voltage reference with transistor sizes is given in Fig. 4. Cascode current mirrors are employed in the 2 stages of PTAT voltage generators to improve the power supply rejection ratio (PSRR). Because the CTAT voltage is relatively low, the first-stage PTAT generator is realized as a PMOS-input differential cell, followed by a NMOS-input second stage. The numbering of transistors in the first stage is complementary to that of the second stage because of the complementary structures of the two stages. The body nodes of $M_{D1,1}$~$M_{D4,1}$ in the first stage are also tied to their source nodes to suppress the influence of body effect.

From (4) and (8), process variations and mismatch between the sizes and V_{TH} of the MOS pairs will cause variations in the slopes of the PTAT and CTAT voltages, as well as the value of V_{REF}. Corner simulation shows that V_{REF} varies from about 720

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to 806 mV at 27°C, and the CTAT and PTAT slopes vary in ranges of −1.27 ~ −1.32 mV/°C and 1.25 ~ 1.36 mV/°C, respectively. In order to correct these variations, a 6-bit (D_6~D_1) digital trimming structure is employed to adjust the effective aspect ratios of the input NMOS pair ($M_{D1,2}$ and $M_{D2,2}$) in the second stage. On the basis of (4) and (8), the output reference voltage can be derived as

$$V_{REF} = V_{TH0} + T\left\{k_1 + \eta\frac{k}{q}\left[\ln\left(\frac{K_{D1,1}K_{D3,1}K_{M2,1}^2K_{D6,1}K_{M3,1}}{K_{D2,1}K_{D4,1}K_{M1,1}^2K_{D5,1}K_{M4,1}}\right) + \ln\left(\frac{K_{M2,2}^2K_{D3,2}K_{D6,2}K_{M3,2}}{K_{M1,2}^2K_{D4,2}K_{D5,2}K_{M4,2}}\right) + \ln\left(\frac{K_{D1,2}+\Delta_{D1}}{K_{D2,2}+\Delta_{D2}}\right)\right]\right\} + \Delta V_{TH,tot} \quad (9)$$

where $\Delta V_{TH,tot}=(V_{TH,D5,1}-V_{TH,D6,1})+(V_{TH,D2,2}-V_{TH,D1,2})$, while Δ_{D1} and Δ_{D2} are additional aspect ratios for $M_{D1,2}$ and $M_{D2,2}$, respectively, which are controlled by the trimming digital bits. As an advantage, the trimming scheme has little influence on the power consumption of the reference circuit. In order to show the trimming range, we simulated the output voltage at room temperature and the slope of the 2nd-stage PTAT voltage as functions of the trimming code, which is a logic function of D_1~D_6 to realize monotonous trimming (only 34 non-repeated values of the adjustable fractional term in (9) can be obtained from trimming). The results are given in Fig. 5, showing a trimming range of 53 mV for V_{REF}. The PTAT slope of the 2nd stage can be trimmed in a range of 0.76mV/°C~ 0.91mV/°C. Although the voltage trimming range is insufficient and difficult to make linear because of the logarithm operation, it can still correct variations in V_{REF} and the TC to a large extent.

From Fig. 4, V_{REF} is about 0.76V, while the voltage headroom of the sub-threshold PMOS cascode current source in the output branch can be as low as 220 mV for normal operation based on simulation, resulting in a minimum V_{DD} of about 1V.

III. Measurement Results

The proposed voltage reference circuit was fabricated in the GlobalFoundries 0.18-μm standard CMOS technology with an active area of 95 μm × 170 μm, as shown in Fig. 6.

Fig.7 (a) plots the measured output reference voltages as a function of temperature from -40˚C to 125˚C at different V_{DD}. The results show that the proposed circuit generates a V_{REF} of about 0.76 V when the supply voltage is more than 1 V. From the measured voltages under different V_{DD} at room temperature, the line regulation is obtained as 0.524%/V. The TC is 47 ppm/˚C at 1.8-V V_{DD}, and increases to 74 ppm/˚C at 1-V V_{DD}.

Fig. 7(b) plots the measured voltages of V_{REF} under 1.8-V V_{DD} as a function of temperature from -40˚C to 125˚C in 63 samples on a same wafer before and after trimming. It shows relatively wide distribution before trimming because of possible mismatches and process variations. Digital trimming is carried out to adjust the slope of the PTAT voltage to achieve the best TC for each sample according to the simulated trimming curve in Fig. 5. As shown in Fig. 7(b), both TC and voltage distribution are improved after trimming. The histograms of V_{REF} at room temperature and the TC are given in Fig. 8. The average TC is about 58.1ppm/˚C before trimming and is reduced to 49.6 ppm/˚C after trimming. The coefficients

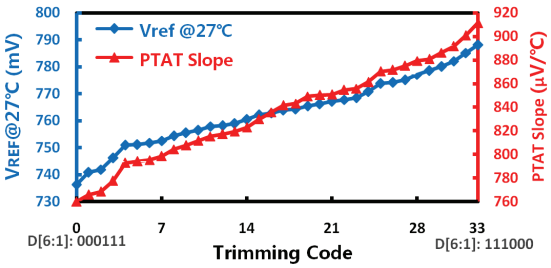


Fig. 5. Simulated trimming range of V_{REF} and PTAT slope of the 2nd stage.

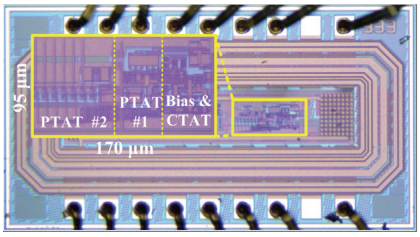
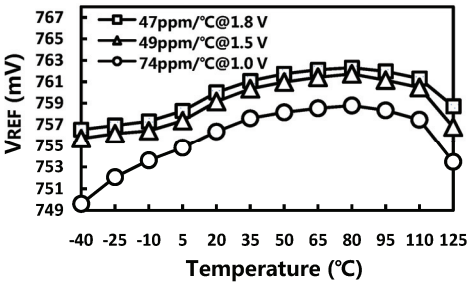
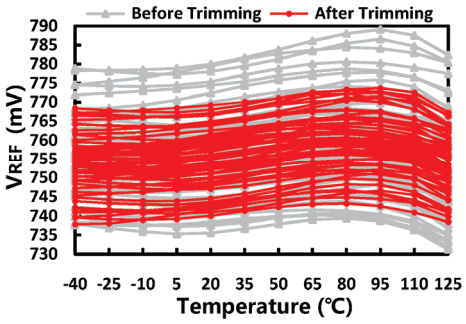


Fig. 6. Chip micrograph of the proposed voltage reference circuit.



(a)



(b)

Fig. 7. Measured temperature dependence of V_{REF} : (a) single sample under 3 different V_{DD}; (b) 63 samples under 1.8-V V_{DD} before and after trimming.

of variation (= σ/μ, where σ and μ are the standard deviation and the mean value) of V_{REF} is 1.51% before trimming, and is reduced to 0.95% after trimming. The improvement of voltage distribution from trimming is not so great because the trimming is carried out to obtain optimum TC for each sample. Another reason is that the range of adjustment is limited by the logarithm operation in (9).

The measured PSRRs are -52 and -37 dB at 100 Hz and 1 MHz, respectively. The post-layout simulated noise density at 100Hz is $4.56\mu V/\sqrt{Hz}$ with a 10-pF on-chip capacitor. Lower noise can be achieved with larger decoupling capacitor

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameter	This work	[6] JSSC'13		[7] TCAS-II'14	[8] TCAS-I'15		[9] TCAS-II'15	[10] TCAS-I'16	[11] TCAS-II'16
CMOS Tech.	0.18μm	0.18μm		0.18μm	90 nm		0.18μm	0.18μm	0.18μm
Min. supply voltage (V)	1	1.2	0.7	0.7	1.15		0.45	0.45	1.35
V_{REF} (V)	0.756	1.09	0.548	0.438	0.72		0.118	0.118	0.63
Temp. range (°C)	-40 – 125	-40 – 120		-25 – 85	10–80	0–100	-40 – 125	-40 – 125	-20 – 80
TC (ppm/°C)	49.6@1.8V-V_{DD} 74 @ 1V-V_{DD}	147	114	22.11	10.1	43.5	63.6	59.4	14.1
Linear Regulation (%/V)	0.524	-	-	1.30	0.3		1.01	0.033	0.047
PSRR (dB)@Freq. (Hz)	-52@100	-62@100	-56@100	-	-51@100		-44.2@100	-50.3@100	-75.7@DC
$V_{REF}(\sigma/\mu)$ (%)	0.95	0.737	1.05	-	1.3		0.6	0.58	-
Active area (mm^2)	0.0162	0.0294	0.0246	0.041	0.028		0.012	0.013	0.015
Power@room temp. (nW) (Cur. (nA) @ V_{DD} (V))	23 (23@1V)	100 (83@1.2)	52.5 (75@0.7)	19 (27@0.7)	576 (480@1.2)		14.6 (32@0.45)	15.6 (35@0.45)	1188 (880@1.35)
Devices used	MOS-only	MOS, BJT		MOS, Res.	MOS, BJT, Res.		MOS-only	MOS-only	MOS, BJT
Trimming	YES	NO		YES	NO		YES	YES	YES

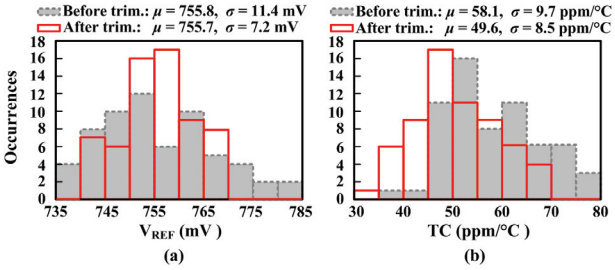

Fig. 8. Histograms before and after trimming: (a) $V_{REF,}$ (b) TC.

at the cost of longer start-up time [6], [8]. The measured current consumptions at room temperature are 23 nA and 24 nA under 1-V and 1.8-V V_{DD}, respectively. According to simulation, the current distribution under 1.8 V are 2 nA, 17 nA and 5 nA for the start-up, bias & CTAT, and 2-stage PTAT circuits, respectively. Under 1-V V_{DD}, measured current consumptions are 21 nA and 27 nA at -40˚C to 125˚C, respectively.

The performances of the proposed voltage reference circuit with comparison to other recently reported state-of-the-art ultra-low power reference circuits are summarized in Table I. Because only 2 stages of high-slope PTAT generators are employed and the CTAT voltage generator is also combined into the current reference circuit, the proposed circuit achieves lower area and power consumption compared with those of [6]. The process-related variations are relatively larger because of the MOS-based CTAT voltage generator. When compared with other voltage reference circuits in Table I, the proposed circuit also shows very low area and current consumption.

IV. CONCLUSION

A MOS-only ultra-low-power reference circuit has been presented. To save chip area and power consumption, high-slope PTAT voltage generator is developed to minimize the number of PTAT stages required to compensate the CTAT voltage. Moreover, the CTAT voltage is directly generated by a diode-connected NMOS in the current reference circuit for the PTAT stages to save area and power consumption further. Fabricated in a 0.18-μm CMOS process, the proposed reference circuit generates a 0.756-V reference voltage with TC of 49.6 ppm/˚C, while consuming 23-nA under a 1-V power supply. The area of the core circuits is only 0.0162 mm^2.

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