A Low-Power Pipelined-SAR ADC Using Boosted Bucket-Brigade Device for Residue Charge Processing

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***Abstract*— A low-power pipelined-successive approximation register (SAR) analog-to-digital converter (ADC) using boosted bucket-brigade device (BBD) for residue charge processing is presented. Boosted BBDs have been used as low-power and high-precision residue charge transfers in multistage pipelined ADCs, with drawbacks of large nonlinearity and severe accumulated common-mode (CM) charge error, which requires power-hungry real-time calibration circuits to control the CM level in each stage. When used in a two-stage pipelined-SAR ADC, only one boosted BBD pair is needed and its input signal range is attenuated remarkably by the first-stage SAR. Thus, zero-power power-up correction circuit can be used to stabilize the output CM level, and the nonlinear error of the boosted BBD is negligible. In addition, with top-plate sampling in the first-stage SAR, two reference voltages for the conventional BBD are also eliminated. A proof-of-principle 10-bit two-stage pipelined-SAR ADC is implemented in a 0.18-μm CMOS, showing an signal-to-noise-and-distortion ratio/spurious-free dynamic range of 57.1 dB/71.4 dB at 3.1-MHz input, while consuming 1.87 mW at 40 MS/s for a figure of merit of 78.9 fJ/step. The boosted BBD residue circuit consumes only 0.06 mW or 3% of the total power.**

***Index Terms*— Boosted, bucket-brigade device (BBD), low power, pipelined-successive approximation register (SAR) analog-to-digital converter (ADC), residue processing.**

I. Introduction

THE conversion rate of successive approximation register (SAR) analog-to-digital converter (ADC) increases dramatically with the advancement of CMOS technology because it mainly consists of digital circuits [1]–[4]. To further enhance SAR ADC's speed while maintain or improve its resolution, pipelined-SAR ADCs have been proposed in recent years and become popular in portable applications such as communication and video systems [5], [6].

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Normally, the pipelined-SAR ADC realizes high resolution using two stages of low-resolution SAR ADCs and a residue processing circuit operating in pipelined fashion. This architecture has several advantages. First, the first-stage SAR acts as a sampler, which can eliminate the timing misalignment problem in high-speed SHA-less pipelined ADCs [7]. Second, a multiple-bit first stage (10 bit in [5] and 5 bit in [6], as examples) relaxes the linearity requirement of the back-end stage. Third, the voltage gain of the residue amplifier (RA) relaxes the stringent comparator noise requirement for high-resolution SAR ADCs [8]. However, the speed of the pipelined-SAR ADC is much lower than that of the pipelined ADCs because of the slow SAR operation in each stage. Fortunately, many efforts have pushed the conversion speed of pipelined-SAR ADCs to hundreds of MS/s, even several GS/s, using techniques such as resolving multi bits per SAR step [5], [9], multiple SAR stages [10], [11], sub-ranging [12], time interleaving [13]–[16], or the combinations of these techniques [17]–[21].

Moreover, the residue processing circuit imposes significant influence on the power consumption and speed of pipelined-SAR ADCs. Conventionally, opamps with high gain–bandwidth product are employed in pipelined-SAR ADCs to realize the high-precision closed-loop RA, which is power consuming for high-speed operations [5], [6], [9], [12]–[15], [18]. The ring amplifier [22] and low-gain opamp [23] have been used to replace the high-gain opamp in the conventional closed-loop RAs to reduce the power consumption. However, the design of the ring amplifier is plagued by hard design tradeoffs between accuracy, power, and speed [24], and the gain error of the low-gain opamp in [23] necessitates relatively complex background calibration. Besides the closed-loop structures, open-loop RAs based on open-loop amplifier [25], zero-crossing-detector [26], dynamic integrator [16], and dynamic amplifier [21], [27], [28] have been proposed to further improve the operation speed and reduce the power consumption. However, complex calibration schemes such as those based on pseudorandom noise injection [16], [27], [28] are usually required to correct the open-loop RA's gain error caused by PVT variations, increasing the total power consumption as well as the design complexity. Passive residue transfers with direct charge sharing [21], [29], [30], or a source follower buffer [31] can realize high-speed and

ultra low-power consumption. However, the second-stage comparator noise limits the ADC's resolution to 6–8 bits due to the lack of voltage gain in residue processing.

The boosted bucket-brigade device (BBD), which consists of a simple cascode amplifier and several passive components, has been used as the residue charge transfer for high-speed and high-resolution charge-domain pipelined ADCs [32]–[34], showing its potential for fast, low-power, and accurate residue processing. The pulsed BBD in [35] further reduces the power consumption by replacing the cascode amplifier with a passive *RC* circuit, which generates a pulse signal to mimic the output of the cascode amplifier. Because of the imprecise settling of the pulse signal, off-chip continuous calibration is adopted in [35] to calibrate the linear and nonlinear errors of the pulsed BBDs, which increases the system-level power consumption and complexity. Although featured with low-power consumption, a serious problem of the BBD-based pipelined ADC is that the common-mode (CM) charge error induced by PVT variations accumulates along the pipelined stages, which may saturate the backend stages, resulting in malfunction of the ADC. Therefore, complex mixed-signal and digital calibration circuits are employed to stabilize the CM charge of each stage in real time, consuming considerable power and chip area [33], [34], [36]. Another drawback of the boosted BBD is the nonlinearity in the charge transfer characteristic [37], which is especially serious for pipelined ADCs because the first-stage BBD needs to process the full-scale input signal.

A pipelined-SAR ADC using a differential boosted BBD pair as the residue charge transfer is presented in this paper. Apart from keeping the boosted BBD's advantage of low-power and high-precision residue charge processing, it is shown in this paper that the two problems of the boosted BBD are alleviated significantly when it is used in a pipelined-SAR ADC.

1) As only one BBD stage is used, the CM charge error does not accumulate and has much smaller influence on the circuit; thus, a simple zero-power power-up CM control scheme is integrated to stabilize the CM charge.
2) As the BBD's input is only the small residue voltage, the nonlinear error in the charge transfer is negligible.

Furthermore, two reference voltages for the original boosted BBD are eliminated because of the top-plate sampling structure of the first-stage SAR in the proposed ADC. The proposed idea is demonstrated with a 1.87-mW, 10-bit, 40-MS/s pipelined SAR ADC fabricated in a 0.18-μm CMOS technology. Measurement results show that the boosted BBD consumes only 0.06 mW or 3% of the total power.

The remainder of this paper is organized as follows. The drawbacks of the boosted BBD for pipelined ADCs are analyzed in Section II. Section III shows the architecture of the proposed ADC, while circuit implementation is described in Section IV. Section V presents the measurement results and the conclusion is drawn in Section VI.

II. Boosted BBD Analysis

Although boosted BBD-based pipelined ADCs are featured with high-resolution and low-power consumption, they have not drawn extensive attentions so far because of the issues of CM charge error and nonlinearity. The two issues are analyzed in this section after a brief introduction of the boosted BBD structure and a boosted BBD-based pipelined stage example.

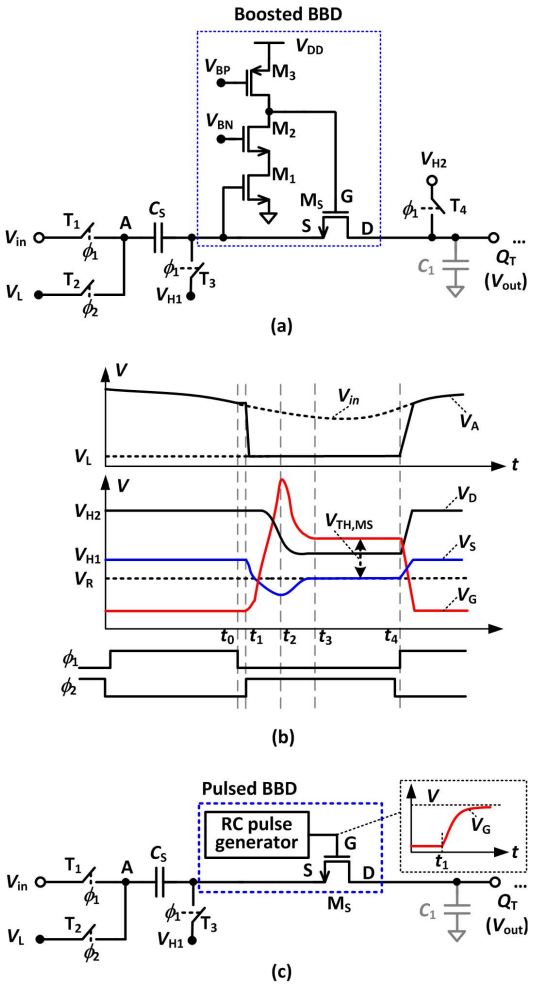

Fig. 1. (a) Schematic of boosted BBD. (b) Boosted BBD's operation waveforms [32], [33]. (c) Structure of pulsed BBD [35].

A. Boosted BBD Structure

The boosted BBD reported in [32] and [33] aims to speed up the charge transferring of conventional BBD, making it suitable for high-speed pipelined ADCs, as shown in Fig. 1(a). With a simple cascode amplifier added between the gate and source of M_S, it is verified that the charge transfer speed is increased by a factor of about A, where A is the cascode amplifier's gain [32].

The conceptual operation waveforms of the boosted BBD are given in Fig. 1(b). In ϕ_1 phase, V_{in} is tracked by C_S, and V_{H1} is high enough to turn OFF M_S. Charge transferring is triggered by the rising edge of ϕ_2, at which both terminals of C_S are pulled down by V_L. The gate voltage (V_G) of M_S is then pulled up abruptly by the amplifier, which turns ON M_S. With the charge on C_S transferred to C_1 through M_S, V_S increases while V_D decreases gradually. When V_S increases to the cut-off voltage (V_R) at t_3, the difference between V_G and V_S equals to the threshold voltage of M_S, $V_{TH,MS}$, and

the charge transferring process is then terminated because M_S is off again. The charge transferred from C_S to C_1 can be expressed in terms of the voltage change across C_S in the entire process

$$Q_T = C_S[(V_L - V_{in}) - (V_R - V_{H1})] \quad (1)$$

where V_{in} is the input at t_0. Then, Q_T can be rewritten as

$$Q_T = -V_{in}C_S + Q_M \quad (2)$$

where $Q_M = C_S(V_{H1} + V_L - V_R)$. The value of V_R (cut-off voltage) is determined inherently by the input/output characteristic of the amplifier and V_{TH} of M_S. As V_{H1} and V_L are reference voltages, Q_M can be thought as a constant for simplicity at first.

Furthermore, Q_T can also be given in terms of the voltage change on C_1

$$Q_T = C_1[(V_{out} - V_{H2})] = V_{out}C_1 + Q_N \quad (3)$$

where $Q_N = V_{H2}C_1$, can also be thought as a constant.

If two BBDs are used differentially, the differential-mode (DM) charge, $Q_{T,DM}$, can be obtained from (2) and (3) as

$$Q_{T,DM} = -V_{in,DM}C_S = V_{out,DM}C_1 \quad (4)$$

where $V_{in,DM}$ and $V_{out,DM}$ are the DM input voltage and output voltage, respectively. Therefore, from (4), a pair of differential boosted BBDs can realize linear charge transferring.

To save the power consumed by the cascode amplifier, the pulsed BBD in the pipelined ADC [35] adopts an *RC* pulse generator to mimic the output waveform of the amplifier, as shown in Fig. 1(c). The linear and nonlinear error caused by imprecise settling of the pulse signal is corrected by off-chip continuous calibration in [35], which increases the system-level power consumption and complexity.

B. BBD-Based Substage for Pipelined ADC

To realize a BBD-based substage for pipelined ADC, voltage comparators and charge subtracting devices are needed to form the sub-ADC and sub-DAC [33]. A 1.5-bit stage with redundancy is shown in Fig. 2(a) as an example. The C_{C1} pair is used to process the CM charge, while the two pairs of C_{D1} together with four reference voltage multiplexers act as the sub-DAC to generate the residue charge. Two clock signals for resetting are added to realize pipelining of multiple stages (ϕ_{1R} and ϕ_{2R}), as given in Fig. 2(b).

Input sampling is also realized in ϕ_1 phase by C_S. In ϕ_2 phase, the charge is received by all the capacitors (C_{C1} and C_{D1}). The two voltage comparators then generate the 2-bit thermometer-coded output in the interval from t_3 to t_4 in Fig. 1(b). From (4), the BBDs transfer a charge packet of $Q_{T,DM} = -V_{in,DM}C_S$ from C_S to $(C_{C1} + 2C_{D1})$, resulting in a differential voltage of

$$V_{1,DM} = \frac{Q_{T,DM}}{C_{C1} + 2C_{D1}} = \frac{-V_{in,DM} \cdot C_S}{C_{C1} + 2C_{D1}}. \quad (5)$$

Therefore, the voltage gain is $C_S/(C_{C1} + 2C_{D1})$. The two comparators compare this voltage with two reference voltages,

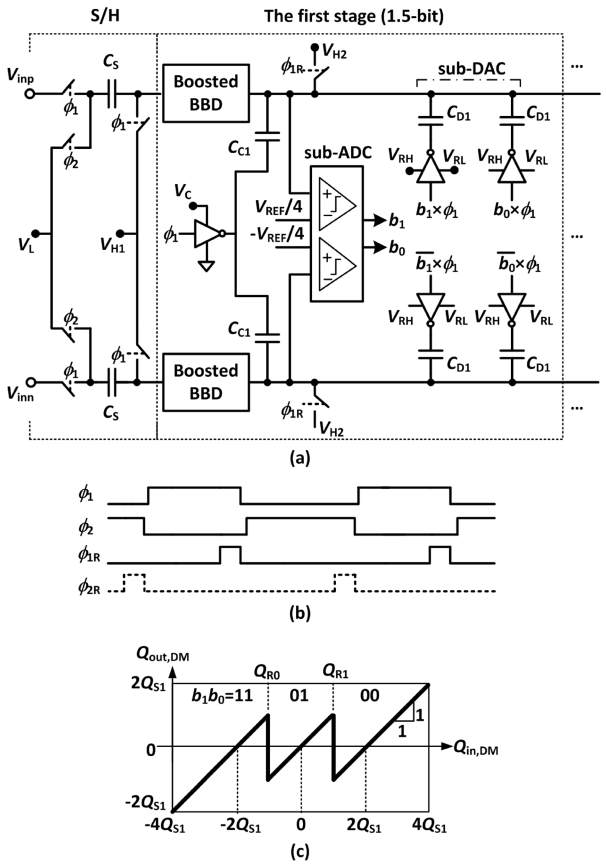

Fig. 2. BBD-based 1.5-bit pipelined substage. (a) Structure. (b) Clock timing. (c) Ideal residue curve.

$V_{REF}/4$ and $-V_{REF}/4$, respectively. This is equivalent to compare Q_T to two charge references, Q_{R0} and Q_{R1}

$$\begin{cases} Q_{R0} = -V_{REF}(C_{C,1} + 2C_{D,1})/4 \\ Q_{R1} = V_{REF}(C_{C,1} + 2C_{D,1})/4. \end{cases} \quad (6)$$

In the next ϕ_1 phase, residue charge is generated according to the sub-ADC results and transferred to the next stage through the BBDs in the next stage. The input charge for the stage is $Q_{in1,DM} = Q_{T,DM}$, while the output charge can be calculated as

$$Q_{out1,DM} = Q_{in1,DM} - [(2b_1 - 1)Q_{S,1} + (2b_0 - 1)Q_{S,1}] \quad (7)$$

where $Q_{S,1}$ is the elementary charge of stage-1 that is defined as

$$Q_{S,1} = (V_{RH} - V_{RL})C_{D,1} \quad (8)$$

where V_{RH} and V_{RL} are the high and low reference voltages for the sub-DAC, respectively.

The residue charge curve obtained from (7) is given in Fig. 2(c), which is similar to that of a voltage-domain 1.5-bit pipeline stage except for that the gain is fixed at 1. If all the subsequent stages are 1.5-bit stages with equal references, they should observe the relationship $Q_{S,n} = 2Q_{S,n+1}$, translating to a relationship between the DAC capacitors in adjacent stages of

$$C_{D,n} = 2C_{D,n+1}. \quad (9)$$

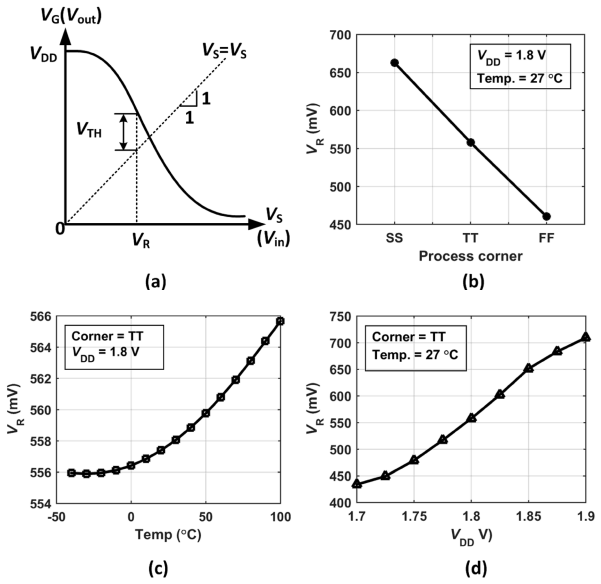

Fig. 3. (a) Conceptual representation of V_R, and simulated V_R as functions of (b) process corner, (c) temperature, and (d) supply voltage.

Therefore, binary scaling down in capacitance can be observed along the pipelined stages, which helps to reduce the chip area. More importantly, although the gain for charge residue is unity, a voltage gain of larger than one is obtained inherently by the scaling down of the capacitors, as given by (5).

C. CM Charge Error in BBD-Based Pipelined ADC

From (4) and (9), the BBD-based pipelined ADC has the potential to realize high resolution because the precision of the DM charge processing is mainly determined by the matching between capacitors. However, the CM charge error has serious impact on the operation of BBD-based pipelined ADCs. From (1), the CM charge transferred can be expressed as

$$Q_{\mathrm{T,CM}} = -V_{\mathrm{in,CM}}C_{\mathrm{S}} + C_{\mathrm{S}}(V_{\mathrm{H1}} + V_{\mathrm{L}} - V_{\mathrm{R}}). \qquad (10)$$

As seen from (10), the CM charge is determined by the input CM level ($V_{\mathrm{in,CM}}$), absolute values of capacitors and reference voltages, as well as the cut-off voltage (V_{R}) of the boosted BBD itself, which are influenced by PVT variations.

Among others, V_{R} is the most sensitive factor to PVT variations. The exact value of V_{R} is determined by the inherent input/output characteristic of the cascode amplifier and the V_{TH} of the main switch, which can be comprehended with the assistance of Fig. 3(a). Fig. 3(b)–(d) shows the simulated V_{R} of a typical boosted BBD in 0.18-μm CMOS as functions of process corner, temperature, and supply voltage, respectively. (The value of V_{R} is obtained as the value of V_{S} after the charge transfer process is terminated.) The large variation of V_{R} may result in large CM charge error in each pipelined stage, as given by (10). Moreover, in a multiple-stage pipelined ADC, the CM charge error accumulates stage by stage along the pipeline. Because the charge range is limited by the capacitor values, a small CM variation in the front-end stage will cause large accumulated CM error in the backend stages with very small capacitors, which may saturate the stage and cause remarkable performance degradation of the ADC.

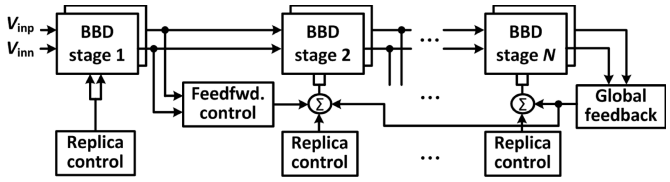

Fig. 4. Conceptual circuit for CM charge error correction in boosted-BBD-based pipelined ADC [33], [34], [36].

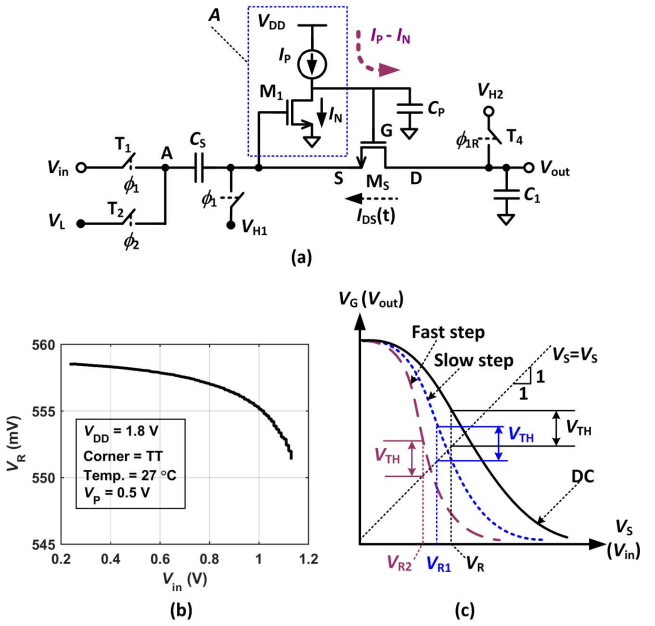

Fig. 5. (a) Simplified structure of boosted BBD for nonlinearity analysis. (b) Simulated V_{R} as a function of V_{in}. (c) Transient input/output characteristics with different input steps.

To suppress the PVT-induced CM charge error, complex mixed-signal calibration circuits combining replica control, feedforward, and global feedback are adopted to stabilize V_{R} and hence the CM charge of each stage [33], [34], as shown in Fig. 4 (circuit details can be found in [36]), consuming considerable power and chip area. Similarly, the pulsed BBD in Fig. 1(c) also has the problem of CM charge accumulation. To avoid complex error calibration circuits, the last eight stages of the ADC in [35] are realized as conventional SC pipelined stages, which are also power consuming (account for 60% of the total power).

D. Nonlinearity of Boosted BBD

Besides the CM charge error, the magnitude of the input voltage also influences V_{R}, which causes nonlinear distortion in the ADC. If the cascode amplifier always operates according to the static input/output curve in Fig. 3(a), V_{R} could be independent of the input voltage. However, as the charge transfer is a dynamic process, V_{R} indeed varies with the sampled value of V_{in}. In order to find the exact relationship between V_{R} and V_{in}, large-signal analysis is carried out using the simplified structure shown in Fig. 5(a), in which the amplifier is simplified to a common-source stage with a current

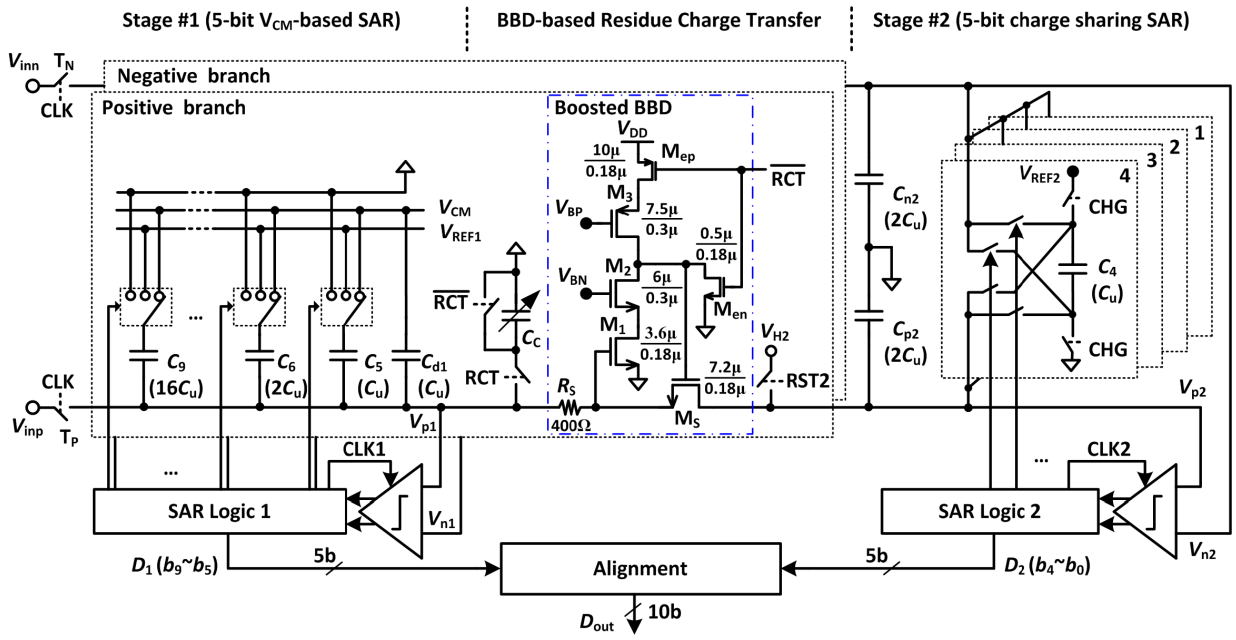

Fig. 6. Proposed ADC architecture.

source load (I_P), and C_P is the parasitic capacitance at node G. In the charge transferring process, V_G, V_S, and I_{DS} of M_S are functions of time.

Assuming that the charge transferring process starts at t_0, as shown in Fig. 1(b), V_S is pulled down to its initial value of

$$V_S(t_0) = V_{H1} - (V_{in} - V_L) \tag{11}$$

which turns on M_S immediately. With charge on C_S transferred to C_1, $V_S(t)$ can be expressed as

$$V_S(t) = V_S(t_0) + \int_{t_0}^{t} I_{DS}(t)dt/C_S \tag{12}$$

with $I_{DS}(t)$ given as

$$I_{DS}(t) = (\mu_n C_{ox}/2) \cdot K_S \cdot [V_G(t) - V_S(t) - V_{TH}]^2 \tag{13}$$

where K_S is the aspect ratio ($= W/L$) of M_S, μ_n is the carrier mobility, and C_{ox} is the specific gate-oxide capacitance. Normally, M_1 is off at beginning because $V_S(t_0)$ is low; therefore, V_G is pulled up with C_P charged by I_P. When $V_S(t)$ increases to a value larger than V_{TH} of M_1 at a given time t_{ON}, the charging current decreases to $I_P - I_N$. Assuming a initial value of $V_G(t_0)$, $V_G(t)$ can be expressed by a piecewise equation

$$V_G(t) = \begin{cases} (1/C_P)\cdot \int_{t_0}^{t} I_P dt + V_G(t_0), & (\text{for } t_0 < t \le t_{ON}) \\ V_G(t_{ON}) + \dfrac{1}{C_P}\int_{t_{ON}}^{t} [I_P - I_N(t)]dt, & (\text{for } t > t_{ON}) \end{cases} \tag{14}$$

where $I_N(t)$ is the current in M_1, and can be expressed as

$$I_N(t) = (\mu_n C_{ox}/2) \cdot K_1 \cdot [V_S(t) - V_{TH1}]^2. \tag{15}$$

Obviously, $V_G(t)$ starts to drop after $I_N(t)$ increases to be larger than I_P, and the charge transfer process is terminated eventually when $V_G(t) - V_S(t) = V_{TH}$.

The combination of (11)–(15) leads to a piecewise differential equation of $V_S(t)$ over t, which has a second-order form before t_{ON} and third-order form after t_{ON}. Although it is difficult to obtain a closed-form solution for $V_S(t)$, numerical methods reveal that the final value of $V_S(t)$ (i.e., V_R) is indeed not a constant but varies with V_{in}. Fig. 5(b) shows the simulated V_R as a function of V_{in}, which shows obvious signal-dependence of V_R.

The nonlinearity can also be illustrated intuitively by Fig. 5(c), which is actually caused by the deviation of the transient input/output characteristic from the static (dc) curve. Moreover, in [37], we have verified through simulation that the BBD's linearity degrades remarkably with the increase of V_{H1}. The spurious-free dynamic range (SFDR) can be lower than 60 dB for large values of V_{H1}.

Obviously, the nonlinearity is an intrinsic issue of the boosted BBD. For a pipelined ADC, the first-stage BBD must process the full-scale input voltage, which may result in large nonlinear error in the output spectrum of the ADC. When the boosted BBD is applied to a pipelined-SAR ADC, the signal processed by the BBD is attenuated significantly by the first-stage SAR; therefore, the nonlinearity is no longer a problem even with a relatively large variation in the input CM level.

III. Proposed ADC Architecture

Above analysis shows that the differential boosted BBD can be used to realize low-power and high-precision residue charge transfer, whereas it also shows drawbacks of accumulated CM charge error and severe nonlinearity when used in pipelined ADCs. Fortunately, for a two-stage pipelined-SAR ADC, only a pair of boosted BBDs is needed for residue transferring, which permits the usage of zero-power power-up CM charge correction circuit. Moreover, as the boosted BBD only needs to process the small residue of the first-stage SAR, the resulting

nonlinear error is usually negligible and requires no specific calibration.

To demonstrate the effectiveness of using boosted BBD for residue charge processing in pipelined-SAR ADCs, a 10-bit two-stage pipelined-SAR ADC with boosted BBD is proposed in this paper, as given in Fig. 6. The ADC consists of a 5-bit V_{cm}-based SAR as the first stage [3], a pair of boosted BBDs for residue charge transferring, and a 5-bit charge-sharing SAR as the second stage [38]. A digital circuit block is employed to align the outputs of the two stages (D_1 and D_2) and generate an overall 10-bit output, D_{out}.

As shown in Fig. 6, there are three main differences for the boosted BBD in the proposed pipelined-SAR ADC compared to the original boosted BBD in Fig. 1(a) for pipelined ADC.

1) The input signal is sampled onto the top plates of the first-stage DAC capacitors; therefore, the reference voltage V_{H1} in Fig. 2(a) is eliminated.
2) The reference voltage V_L in Fig. 2(a) is also eliminated, and the pull-down function that triggers the charge transferring is realized by connecting the CM capacitor C_C to the input of the BBD at the rising edge of RCT.
3) The power-consuming CM calibration circuits for pipelined ADC in Fig. 5 are replaced by a simple power-on correction circuit that adjusts the value of C_C by detecting the second-stage CM level.

Detailed description of the CM control circuit is given in Section V. The operation of the ADC is described briefly as follows.

The first-stage SAR converts the input voltage into the 5-bit MSB results, and the residue voltage is processed as charge and transferred onto the charge receiving capacitors (C_{p2} and C_{n2}) in the second stage by the boosted BBDs. The second-stage charge-sharing SAR is then in operation to generate the 5-bit LSB results. The voltage gain between the two stages is obtained as the ratio of the total capacitance of the first stage over C_{p2} (C_{n2}), while the precise charge relation between the two stages is determined by the capacitance values in the charge-sharing array as well as the reference voltage of the second stage (V_{REF2}). Because the physical quantity processed in the second stage is charge, any unit capacitance mismatch between the two stages can be compensated by adjusting V_{REF2}. Therefore, strict capacitance matching between the two stages is not required.

In order to correct the first-stage comparator offset and the offset in the BBD cut-off voltages, the charge processing range of the second stage is increased to about 1.3 times of the ideal value, offering about 0.4-bit redundancy. The exact gain factor is extracted from the histogram of the second-stage digital output, which is discussed in detail in the following section.

The timing diagram is given in Fig. 7. The main clock, CLK, is provided externally with 15% duty cycle (on time is about 3.5 ns at 40-MS/s). In order to avoid using high-frequency clock signals, other clock and control signals are generated asynchronously from CLK by an on-chip clock generator and the SAR control logic using techniques similar with those described in [39]. In the first stage, the input signal is sampled onto the capacitor array when CLK is high. The first-stage

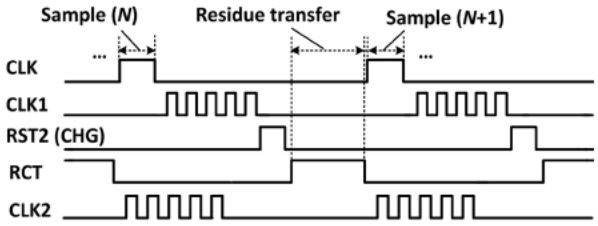

Fig. 7. Timing of clock signals for the proposed ADC.

A/D conversion is then carried out in the following serial SAR process, after which the charge receiving capacitors (C_{p2} and C_{n2}) are initialized with V_{H2} when RST2 is high. The time for the SAR phase is about 17.5 ns at 40-MS/s (including the on time for RST2). The following residue charge transferring process is completed in the interval when RCT is high (about 4 ns). At the same interval, given amount of binary charge is also stored onto the charge-sharing capacitors of the second stage. The A/D conversion of the second stage is completed before the next rising edge of RST2. In order to save power consumption further, the boosted BBDs are only turned ON in the interval when RCT is high. To ensure the clock jitter induced sampling error be less than 1/4 of the quantization error for a 20-MHz input signal, the clock jitter's standard deviation is calculated to be less than 2.8 ps.

IV. Circuit Implementation

A. First-Stage SAR ADC

In order to reduce the switching energy caused by the capacitive DAC (CDAC), the popular V_{cm}-based switching scheme is selected for the first-stage SAR [3]. However, as the residue voltage must be generated for the second stage, there are still five binary weighted capacitors ($C_9 \sim C_5$) and a dummy capacitor ($C_{d1} = C_u$) in each differential branch, as shown in Fig. 6. Considering the linearity requirement, calculation and behavioral simulation show that δ_u/C_u should be less than 0.18% to ensure the standard deviation of the ADC's DNL be less than LSB/6. (δ_u is the standard deviation of the unit capacitance's mismatch error.) Based on the documents for the technology used, the minimum C_u is calculated to be about 110 fF. The reference voltage V_{REF1} is designed with a value of 0.8 V to permit a differential input range of 1.6 V_{pk-pk}.

The bootstrapped switches (T_P and T_N) sample the input signal when CLK is high. After sampling, the comparator is enabled by the SAR logic to compare V_{p1} and V_{n1}, and the highest bit, b_9, is obtained directly without consuming any switching energy. After that, $b_8 \sim b_5$ are obtained in a serial decision making process according to the V_{cm}-based switching scheme. After the SAR process of the first stage, the residue voltages of V_{p1} and V_{n1} can be obtained as

$$\begin{cases} V_{p1} = V_{inp} - \dfrac{V_{REF1}}{2}\left[\displaystyle\sum_{n=5}^{9}(2b_n - 1)C_n\right] \Big/ (C_{tot1} + C_{par1}) \\ V_{n1} = V_{inn} + \dfrac{V_{REF1}}{2}\left[\displaystyle\sum_{n=5}^{9}(2b_n - 1)C_n\right] \Big/ (C_{tot1} + C_{par1}) \end{cases} \tag{16}$$

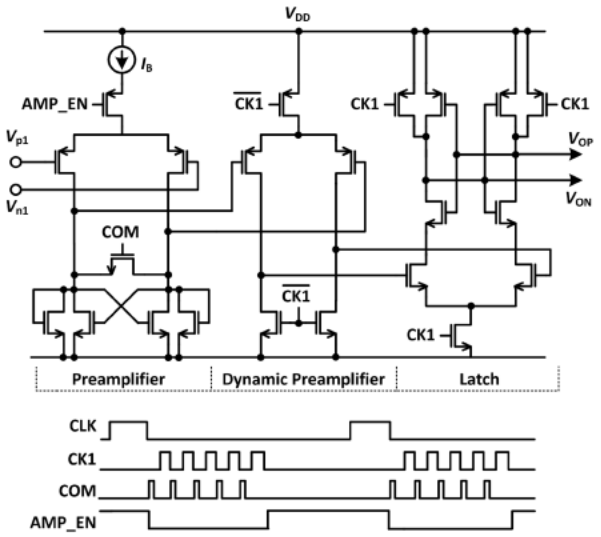

Fig. 8. Stage-1 comparator schematic and control timing.

where C_{tot1} (=$32C_u$) is the total capacitance in each branch of the first-stage CDAC array, b_n is 1 or 0, and C_{par1} is the parasitic capacitance at V_{p1} and V_{n1} nodes. The small C_{par1} has negligible influence on the SNR of the first-stage SAR, but reduces the input range of the ADC slightly.

The CM level of V_{p1} and V_{n1} keeps the same as the CM level of the input signal (about 0.6 V) throughout the SAR process. On the other hand, it can be easily obtained that the DM residue voltage range is approximately from $-V_{REF1}/32$ to $V_{REF1}/32$.

The schematic of the first-stage comparator and its control timing diagram are given in Fig. 8. In order to reduce the redundancy range of the second stage to decrease the quantization noise, a small offset is required for the first-stage comparator. Therefore, a continuous time preamplifier with combined cross-coupled load is added to the popular structure with a dynamic preamplifier and a latch to reduce the overall input-referred offset [9]. Simulation shows that the offset voltage's standard deviation is less than 3 mV. The latch resolves the comparison result after every rising edge of CK1. The signal COM is employed to speed up the preamplifier by resetting its differential output before each comparison, while AMP_EN is used to reduce power consumption by turning off the preamplifier when it is not in operation.

B. Boosted BBD Residue Charge Transfer With CM Control

As seen from the timing diagram, the boosted BBD circuit only needs to operate in a short interval of an entire clock period. Therefore, to save power consumption further, two control transistors M_{ep} and M_{en} are added to disable the cascode amplifier and M_S when RCT is low, as shown in Fig. 6. Besides, a small resistor R_S is added in series with the BBD to improve the stability [32]. The bias voltages, V_{BP} and V_{BN}, are generated by an on-chip current-mirror-based bias circuit. The value of reference voltage V_{H2} is designed with a value of 1.5 V.

To speed up the charge transferring process of the BBD, the cascode amplifier needs to provide enough gain and bandwidth. With the assistance of simulation, an amplifier of 35-dB gain and 2-GHz gain–bandwidth product is enough for the target design. The cascode amplifier in Fig. 6 can provide a 40-dB gain and 2.8-GHz gain–bandwidth product at its biasing point. Although the accumulation of CM charge error is no longer a problem in the two-stage BBD-based pipelined ADC, the CM charge still needs to be controlled because the ratio of the total capacitance in stage 1 (C_{tot1}) to the charge receiving capacitance (C_{p2} or C_{n2}) is large (16 in this paper) to realize a large DM voltage gain. In order to control the CM charge, a power-up CM charge control method with an adjustable CM capacitor, C_C, is proposed in this paper, as shown in Fig. 6. When RCT is low, both terminals of C_C are reset to ground. Once the residue charge transfer process starts at the rising edge of RCT, C_C is connected to $V_{p1}(V_{n1})$, which contributes a given amount of CM charge to be transmitted. Neglecting the C_{par1} in the first stage, the transferred charge in each branch can be obtained as

$$\begin{cases} Q_{outp} = (V_R - V_{p1})C_{tot1} + V_R C_C \\ Q_{outn} = (V_R - V_{n1})C_{tot1} + V_R C_C. \end{cases} \tag{17}$$

The voltages on the charge receiving capacitors after the charge transferring process can then be expressed as

$$\begin{cases} V_{p2} = V_{H2} - Q_{outp}/C_{p2} \\ V_{n2} = V_{H2} - Q_{outn}/C_{n2}. \end{cases} \tag{18}$$

Therefore, the second-stage CM level can be obtained as

$$V_{CM2} = \frac{V_{p2} + V_{n2}}{2} = V_{H2} - \frac{V_R C_{tot1} - V_{CM1} C_{tot1} + V_R C_C}{C_{p2,\,n2}} \tag{19}$$

where $V_{CM1}[= (V_{p1} + V_{n1})/2]$ is the first-stage CM level. From (19), without C_C, the variation of V_R would be amplified by a factor of $C_{tot1}/C_{n2,p2}$, resulting in a large variation in V_{CM2}. From Fig. 3, the variations of V_R resulted from process and supply voltage variations are much larger than that from temperature, which may lead to malfunction of the boosted BBD in extreme conditions. In order to solve this problem, a power-up self CM level correction scheme is employed to control the CM charge through adjusting C_C to compensate the variation in V_R due to process and supply voltage variations. The value of C_C can be adjusted with a range from C_u to $31C_u$ by a 5-bit digital word $b_{C4} \sim b_{C0}$, as given in Fig. 9(a). A differential-difference comparator is used to compare V_{CM2} with a reference voltage V_{RCM2} at the rising edge of CLK, and the result is then processed by the SAR control logic, as shown in Fig. 9(b). The SAR logic determines the values of $b_{C4} \sim b_{C0}$ in a serial decision making process. As a result, V_{CM2} is adjusted to a value close to V_{RCM2}. To save power, the digital logic ensures that the self CM correction circuit operates only in the first six clock periods after power-up reset, as shown by the timing diagram in Fig. 9(c), and consumes zero power after the CM correction process. The capacitance adjusting range is determined based on corner simulation combined with $\pm$ 10% power supply variation.

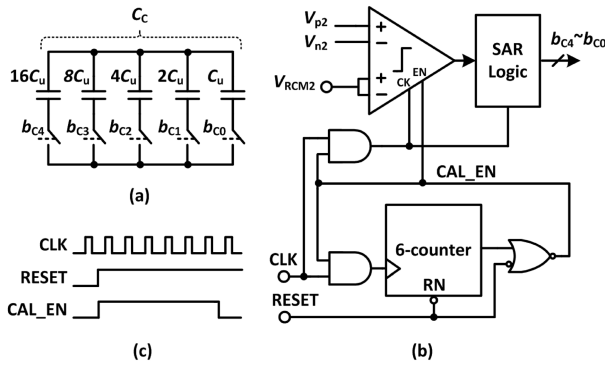

Fig. 9. (a) Adjustable C_C. (b) SAR-based power-up CM control scheme. (c) Power-up CM control timing.

On the other hand, the DM residue charge output from the boosted BBDs can be obtained from (17)

$$Q_{\text{res, diff}} = Q_{\text{outp}} - Q_{\text{outn}} = -(V_{\text{p1}} - V_{\text{n1}})(C_{\text{tot1}} + C_{\text{par1}}). \quad (20)$$

The resulted DM voltage on C_{p2} and C_{n2} is

$$V_{\text{p2}} - V_{\text{n2}} = -(V_{\text{p1}} - V_{\text{n1}})\frac{C_{\text{tot1}} + C_{\text{par1}}}{C_{\text{p2, n2}}}. \quad (21)$$

The ideal voltage gain is 16 in this design, which can tolerate large comparator noise in the second stage. The parasitic C_{par1} increases the voltage gain and the total charge transferred to the second-stage slightly. Even though the value of C_{par1} varies from the first-stage's SAR phase to the residue charge transfer phase, the resulting small fixed gain error can be easily corrected by gain calibration of the proposed ADC.

As implied by Fig. 6, the drain/source capacitance, C_{DS}, of M_S may cause coupling between the two stages, which would degrade the signal-to-noise-and-distortion ratio (SNDR) of the ADC. In order to obtain a small-enough C_{DS} that brings negligible coupling between the two stages, single-finger gate structure and relatively large space between the metal routing for the drain and source nodes have been employed in the layout of M_S.

C. Second-Stage SAR ADC

In order to ensure the interstage voltage gain of 16 while avoid using unit capacitors smaller than the minimum available capacitor in our technology (31 fF), the power efficient charge-sharing SAR structure in [38] is adopted for the second stage. In addition, the basic quantity processed is charge in the charge-sharing SAR ADC, which is easy to be combined with the boosted BBDs.

As shown in Fig. 6, a series of capacitors is used to store a charge array with binary relationship in the second-stage charge-sharing SAR. After the residue charge transferring process, the comparator compares V_{p2} and V_{n2} directly to resolve the highest bit of the second stage (b_4). Then, the SAR logic connects C_4 between C_{p2} and C_{n2} with a polarity determined by the value of b_4, which means that the charge on C_4 is subtracted from the received charge on C_{p2} and C_{n2}. The comparator then resolves b_3 based on the resulted differential voltage. Similarly, $b_2 \sim b_0$ are resolved in the following SAR process. As the offset requirement is looser than that for the first stage, the second-stage comparator is realized with a dynamic preamplifier and a latch without the continuous amplifier in Fig. 8 to save power, which can ensure an offset voltage of less than 10 mV.

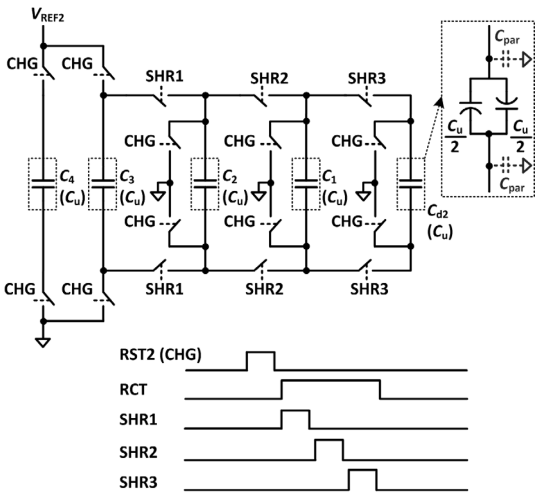

Fig. 10. Stage-2 DAC capacitor array and timing for binary charge storing.

The binary charge array could be obtained by charging a binary capacitor array with given reference voltage. However, this would result in a very small capacitance for the LSB capacitor, deteriorating the matching performance. In order to realize the same capacitance for each capacitor, we adopt the structure in [38] with a modification to obtain better symmetry, as shown in Fig. 10. With the three charge-sharing switches added at the bottom, the additional clock signal that connect the bottom plates of all capacitors to ground in the whole charge storing process in [38] is also eliminated. All capacitors in the array have a capacitance of C_{u} which is realized with two parallel capacitors of $C_{\text{u}}/2$ connected in back to back to ensure almost equal parasitic capacitance at the two terminals. When CHG is high, both C_4 and C_3 are charged to V_{REF2}, while all terminals of C_2, C_1, and C_{d2} are reset to ground. Then, when SHR1 is high, half of the charge on C_3 is shared to C_2. Similarly, SHR2 and SHR3 control the charge-sharing between C_2 and C_1, and C_1 and C_{d2}, respectively. After the charge storing and sharing process, the charge on C_4 is $Q_{\text{C4}} = V_{\text{REF2}}C_{\text{u}}$, while the charge on other capacitors are $Q_{\text{C4}} = 2Q_{\text{C3}} = 4Q_{\text{C2}} = 8Q_{\text{C1}} = 8Q_{\text{Cd2}}$. The capacitor C_{d2} that halves the charge on C_1 is not used in the succeeding SAR A/D conversion process. In addition, several dummy switches are connected to C_4 and C_3 to ensure almost equal parasitic capacitance for all capacitors in the array (not shown in Fig. 10).

As $C_4 \sim C_1$ are connected between C_{p2} and C_{n2} in the succeeding SAR process, twice of the their charge are subtracted from the received charge with selected polarity. Therefore, the remaining differential charge on C_{p2} and C_{n2} after subtraction of $Q_{\text{C4}} \sim Q_{\text{C1}}$ can be obtained as

$$Q_{\text{diff}} = Q_{\text{res, diff}} - \sum_{n=1}^{4} 2Q_{\text{C}n}(2b_n - 1). \quad (22)$$

Obviously, with a binary charge array, $Q_{\text{C}n}$, (22) guarantees a binary SAR process for quantization of $Q_{\text{res,diff}}$. However, as one more capacitor is connected to C_{p2} and C_{n2} after each

TABLE I
INPUT-REFERRED NOISE BREAKDOWN ($C_C = 32C_u$ AND $V_{FS} = 1.6V_{pp,diff}$)

Sampl. noise (V^2)	COMP1 noise (V^2)	BBD noise (V^2)	COMP2 noise (V^2)	Quanti. noise (V^2)	Total noise (V^2)	SNR (dB)
2.4e-9	8.4e-9	9.4e-9	5.4e-9	4.3e-7	4.56e-7	58.4
0.5%	1.8%	2.1%	1.2%	94.4%	100%	

SAR step, the resulted differential voltage is not changed in a binary SAR fashion. The remaining differential voltage on C_{p2} and C_{n2} after subtraction of $Q_{C4} \sim Q_{C1}$can be derived as

$$V_{p2} - V_{n2} = \frac{Q_{res,\,diff} - 2\sum_{n=1}^{4} Q_{Cn}(2b_n - 1)}{C_{p2,n2} + 2C_4 \times 4}. \quad (23)$$

The SAR logic then resolves the last bit, b_0, based on the comparison result made from the voltage expressed by (23).

In order to show the noise contribution from different blocks of the ADC, the noise breakdown is simulated and given in Table I. Because the first-stage is a coarse ADC, the noise from the sample switch and the first-stage comparator (COMP1) has little influence on first-stage output. When the residue charge is transferred to the second stage, the noise in the first stage is added as charge noise to the residue charge which is referred to as "*kTC*" noise. The charge noise transferred by the BBD is contributed by all the capacitance in the first stage including the CM control capacitance (C_C). The worst case is that C_C has a maximum value of $32C_u$ [total single-ended capacitance in the first-stage is $64C_u(\approx 7$ pF)]. This charge noise is transferred to the second stage and converted into voltage on the second-stage capacitance (total of $10C_u$ in the last conversion step), resulting in a noise voltage power of 4.8×10^8 V^2 at room temperature. Considering the worst-case voltage gain of 3.2, input-referred noise power for the differential BBD is about 9.4×10^9 V^2. As shown in Table I, the quantization noise dominates the SNR of the proposed ADC. This means that the proposed ADC architecture has the potential to achieve higher SNDR if more bits could be realized by the two stages. In that case, better capacitance matching may be required for the DAC capacitor arrays.

D. Redundancy and Statistics-Based Gain Error Calibration

From (16) and (20), the ideal range of the differential residue charge can be easily derived as

$$-V_{REF1}C_u \le Q_{res,\,diff} \le V_{REF1}C_u. \quad (24)$$

On the other hand, from (22), the differential input charge range of the second stage is from $-4Q_{C4}$ to $4Q_{C4}$. Considering $Q_{C4} = V_{REF2}C_u$, the second-stage input charge is rewritten as

$$-4V_{REF2}C_u \le Q_{in2,\,diff} \le 4V_{REF2}C_u. \quad (25)$$

To realize an ideal 10-bit resolution, the residue charge range should match the input range of the second stage. Therefore,

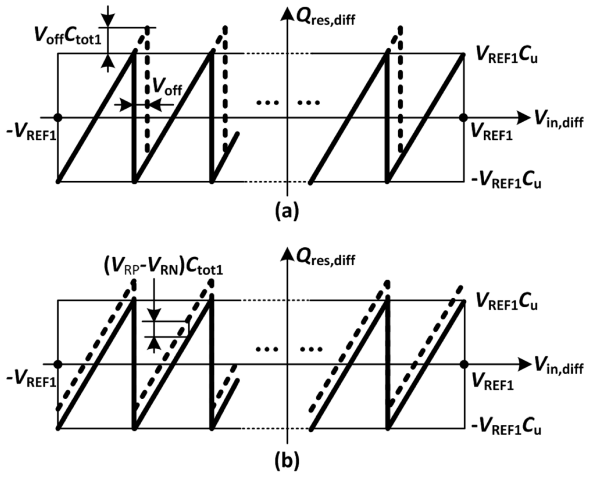

Fig. 11. Residue charge curves considering (a) first-stage comparator offset and (b) offset between the cutoff voltages in the differential boosted BBDs.

if the two stages have equal unit capacitance, C_u, the reference voltages of the two stages should have an ideal relationship of

$$V_{REF2} = V_{REF1}/4. \quad (26)$$

However, the offset voltage of the first-stage comparator, the offset between the cut-off voltages of the boosted BBD pair, and the mismatch between the differential DAC capacitor arrays will cause some offset in the residue charge. As seen from Fig. 11(a), an offset voltage of V_{OFF} in the comparator results in a residue charge offset of $V_{OFF}C_{tot1}$. Also shown in Fig. 11(b), if the differential boosted BBDs have unequal cutoff voltages of V_{RP} and V_{RN} due to circuit mismatch, the resulting residue charge offset is $(V_{RP} - V_{RN})C_{tot1}$. Similarly, the capacitance mismatch between the differential DAC array also contributes a residue charge offset of $V_R(C_{tot1,P} - C_{tot1,N})$. Under these situations, if the DAC capacitors and V_{REF2} in the second stage are still designed with the ideal values, the residue charge would exceed the second-stage quantization range, leading to clipping error in the second stage.

Similar with the voltage-domain pipelined ADC, the offset in the residue charge can be corrected by proper redundancy. In this charge-domain ADC, redundancy can be easily implemented with a wider input charge range for the second stage to accommodate the residue charge with offset, which can be realized through increasing either V_{REF2} or the unit capacitance in the second stage. In circuit implementation, the effective unit capacitance is larger than the designed value because of the parasitic capacitance. As seen from Fig. 10, with a parasitic capacitor of C_{par} at both terminals of each capacitor in the array, the effective differential charge stored on the unit capacitors is increased. It can be verified that the charge contribution from C_{par} is equivalent to that from a capacitor of $C_{par}/2$ parallel to C_u. Therefore, the overall range of $Q_{in2,diff}$ changes to

$$-4\left(C_u + \frac{C_{par}}{2}\right)V_{REF2} \le Q_{in2,\,diff} \le 4\left(C_u + \frac{C_{par}}{2}\right)V_{REF2}. \quad (27)$$

TABLE II
SUMMARY OF DESIGN SPECIFICATIONS

Stage-1 SAR	ADC resolution	5 bit
	Comparator offset, σ_{Voff1}	< 3 mV
	Unit capacitance, C_U	110 fF
	Unit capacitance mismatch σ_U/C_U	< 0.18%
Amplifier of Boosted BBD	DC gain	36 dB
	Gain-bandwidth product	2 GHz
Stage-2 SAR	ADC resolution	5 bit
	Comparator offset, σ_{Voff2}	< 10 mV
	Unit capacitance, C_U	110 fF
Clock	Clock frequency	40 MHz
	Clock jitter standard deviation (σ_j)	< 2.8 ps
Reference Voltage	V_{REF1}	0.8 V
	V_{REF2}	0.22 V

Simulation shows that all the offset charge can be accommodated if the second-stage input range is enlarged by a factor of 1.2. Therefore, a redundancy of 1-bit would be an overdesign that will unnecessarily increase the quantization noise of the ADC. Instead, a smaller redundancy range is used in this paper. The parasitic capacitance is about 20% of C_u from postlayout extraction. Based on this, V_{REF2} is designed to 0.22 V, which is 10% larger than its ideal value. Therefore, the second-stage input range is increased by a factor of about 1.3 including some margin, corresponding to a redundancy of about 0.4 bit.

Although the residue charge is transferred to the second stage with a gain of one, enlarging the second-stage input range by a factor of α is equivalent to divide the transferred charge by α. As analyzed above, the exact input charge range of the second-stage is influenced by parasitic capacitance, which introduces an uncertain error into the gain between the two stages. An idea similar to the histogram-based calibration method in [18] is used to extract value of α from the statistics of the second-stage digital output with a sinusoid or ramp input

$$\alpha = 2^{N_2}/[\max(D_2) - \min(D_2)] \tag{28}$$

where $N_2(=5)$ is the number of bits for the second stage, while D_2 is the digital output code of the second stage. The calibration is realized through multiplying the second-stage digital output by the extracted α. For flexibility in the prototype, the gain factor extraction and calibration are implemented by an off-chip DSP, which could also be easily integrated on the chip.

The important design specifications for the proposed ADC are summarized in Table II. These are chosen based upon a target sampling rate of 40 MS/s and SNDR of 59 dB.

V. MEASUREMENT RESULTS

The prototype ADC including the core ADC circuits, a clock generator and a reference circuit is fabricated in an one-poly-six-metal (1P6M) 1.8-V, 0.18-μm CMOS technology. The ADC occupies a small active area of 0.57×0.6 mm^2, as shown in the die microphotograph in Fig. 12. With a 0.8-V V_{REF1}, the ADC supports a full-scale differential input signal range of 1.6 V_{pk-pk}.

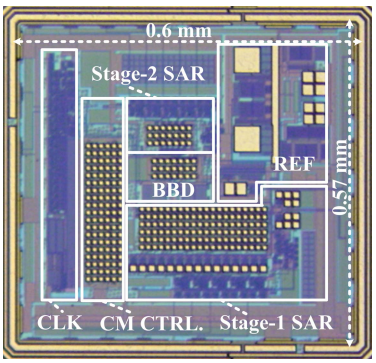

Fig. 12. Die microphotograph.

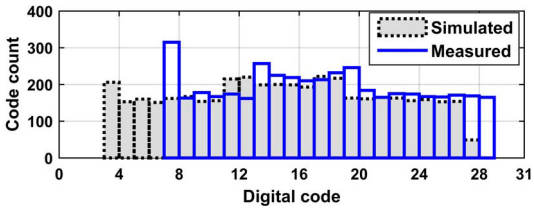

Fig. 13. Simulated and measured histograms of stage-2 output code.

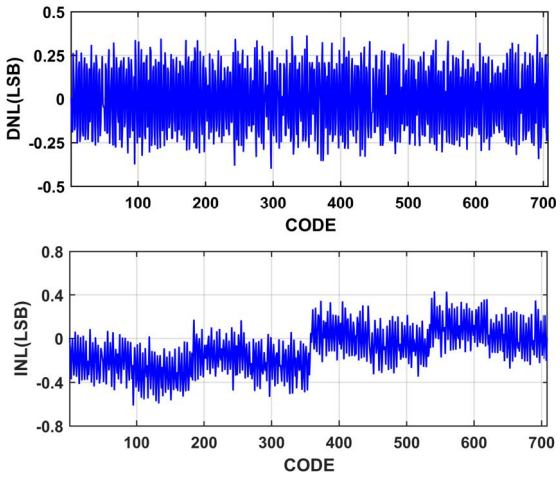

Fig. 14. Measured DNL and INL.

Fig. 13 shows the comparison between the simulated and measured histograms of the second-stage digital output code. The simulated code is obtained without offset in the first stage, and the maximum and minimum codes are 3 and 28, respectively, corresponding to an α of 1.28 from (28). The measured histogram shifts to right because of the offset, and has a maximum and minimum codes of 7 and 29, respectively, resulting in an α of about 1.45. The measured α is larger than the simulated value because the actual C_{par} in the second-stage DAC is larger than the estimated value from layout.

The INL and DNL are measured using a sine wave histogram test at 200 kHz. After calibration with α of 1.45, the ADC has 704 valid output levels, corresponding to about 9.5-bit resolution. The measured maximum INL and DNL are $+0.43/-0.62$ and $+0.36/-0.4$ LSB, respectively, as shown in Fig. 14.

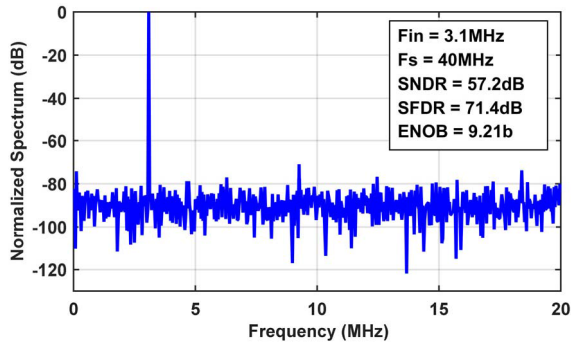

Fig. 15. Normalized output spectrum at 40 MS/s with 1.6-Vpp input sinusoid.

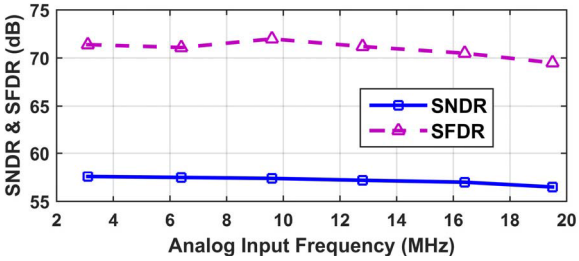

Fig. 16. Measured SNDR and SFDR as functions of the input frequency.

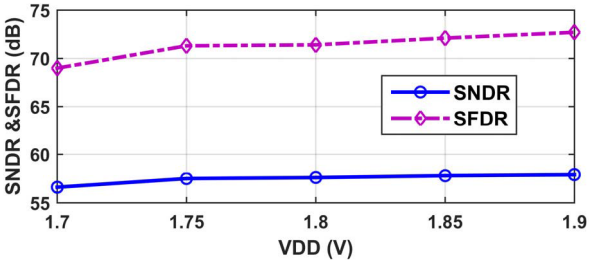

Fig. 17. Measured SNDR and SFDR as functions of supply voltage.

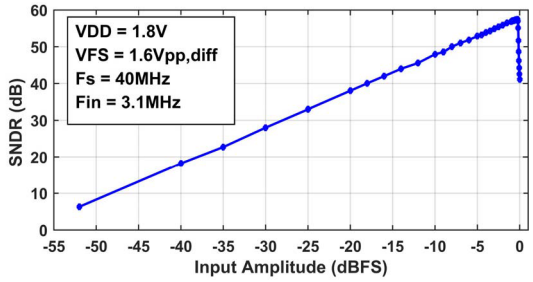

Fig. 18. Measured SNDR versus input amplitude.

As shown in the measured spectrum in Fig. 15 after gain calibration, at 40-MS/s sampling rate with 1.8-V power supply, the ADC achieves an SNDR of 57.2 dB and an SFDR of 71.4 dB for a 3.1-MHz full-scale sinusoidal input. The corresponding effective number of bits (ENOB) is 9.21 bit. The measured SNDR and SFDR as functions of input frequency are summarized in Fig. 16, showing an SNDR of 56.5 dB (9.09-bit ENOB) and an SFDR 69.5 dB at an input (19.5 MHz) close to the Nyquist frequency. We also sweep the supply voltage to check the robustness of the boosted BBD. For a 3.1-MHz sinusoidal input, the SFDR and SNDR remain almost flat over a supply voltage ranging from 1.7 to 1.9 V (Fig. 17), showing the lowest values of 56.6 and 69 dB at 1.7 V, respectively. The CM level is recalibrated for each supply

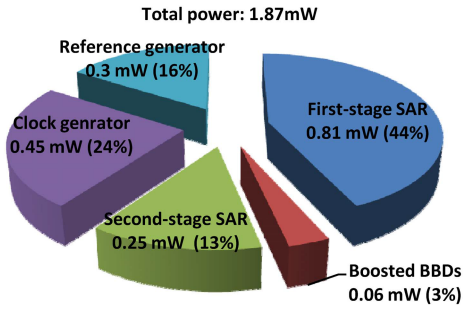

Fig. 19. Power breakdown.

voltage point for Fig. 17. Fig. 18 shows the measured SNDR versus input amplitude for 3.1-MHz input under 1.8-V power supply, showing that the ADC has linear SNDR response up to the full-scale input. Because of the input range attenuation provided by the first-stage SAR, the nonlinearity of the boosted BBD is suppressed significantly. Simulation shows that the input bootstrapped switch also achieves a SFDR about 80 dB. The remaining relatively small third harmonic in the FFT spectrum and the visible pattern in the INL curve are probably caused by the systematic mismatch in the DAC capacitor array. Further measurement results for 25 samples with a 3.1-MHz input show that the SNDR varies from 56.3 to 57.7 dB with average of 57.3 dB and the SFDR varies from 69.3 to 79.9 dB with average of 73.9 dB.

The total power consumption including the clock and reference circuits is 1.87 mW, with power breakdown shown in Fig. 19. The power for charging the CM control capacitance, C_C, is by reference voltage V_{H2}. As can be seen, because relatively large unit capacitance is adopted for good matching, the two SAR stages in this paper consume relatively high power. The differential boosted BBDs consumes only 0.06 mW, corresponding to about only 3% of the total power. The figure of merit (FoM) is calculated with the popular definition of

$$\text{FoM} = \frac{\text{power}}{2^{\text{ENOB}} \cdot f_{\text{sample}}}. \tag{29}$$

The FoM of the proposed ADC is obtained as 78.9 fJ/conv. from (29). The performance of the proposed ADC is summarized in Table III with comparison to other pipelined-SAR ADCs using active residue processing circuits. As can be seen, although the conversion rate and FoM of the proposed ADC are not as good as others, the boosted BBD consumes the lowest power among the active residue circuits with explicitly reported power consumption values in Table III, showing its low power potential for residue processing in pipelined SAR ADCs.

As also seen from Table III, the prototype ADC in this paper adopts relatively larger unit capacitance to minimize the influence of parasitic capacitance and also for better matching, resulting in relatively larger power consumption. The FoM could thus be improved if smaller unit capacitance is used. On the other hand, the conversion rate of the proposed ADC is mainly limited by the 0.18-μm CMOS technology used. The average delay for one bit cycle is about 3.5 ns (including the delays of the digital logic, DAC, and comparator) for the

TABLE III
PERFORMANCE SUMMARY AND COMPARISON TO PIPELINED-SAR ADCS WITH ACTIVE RESIDUE CIRCUITS

	[5] JSSC'10	[6] JSSC'11	[28] VLSIC'13	[25] CICC '14	[26] JSSC'14	[22] JSSC'15	[11] TCAS-I'16	This work
Pipe.-SAR architecture	2 stages	2 stages	2 stages	2 stages	3 stages	2 stages	3 stages	2 stages
Technology(nm)	250	65	28	65	65	65	65	180
Area (mm2)	6	0.16	0.11	0.09	1.1	0.054	0.48	0.34
Supply voltage (V)	2.5/5	1.3	0.9	1.0/1.2	1.3	1.2	1	1.8
Full-scale V_{in}_pp (V)	-	2	-	1.3	-	2.4	1.6	1.6
Fs (MS/s)	12.5	50	410	160	50	50	210	40
Resolution (bit)	18	12	11	13	12.1	13	12	10
SNDR (dB) / ENOB	92/15b	66 /10.7b	59.8/9.6b	68.3/11b	66/10.7b	70.9/11.5b	63.48/10.3b	57.2/9.2b
FoM (fJ/conv)	256.3	52	12	32.6	57	6.9	30.3	78.9
Unit capacitance (fF)	-	31.2, 15.6 (St.1, 2)	-	25, 0.75 (St. 1, 2)	3750*, 5.4 (St.1&2, 3)	7.9, 2.6 (St.1, 2)	125, 1.9, 1.9 (St. 1, 2 ,3)	110, 110 (St. 1, 2)
Total Power, P_{TOT} (mW)	105	3.5	2.1	11.1	4.8	1	5.3	1.87
Residue circuit type	Opamp based	Opamp based	Dynamic amp.	Open-lp. amp.	ZCD based	Ring amp.	Passive +opamp	Boosted BBD
Power of residue cir., P_{RES} (mW)	-	2.6	-	4.3	0.59 (St.-1 ZCD)	0.366	1.3 (St.2 opamp)	0.06
P_{RES}/P_{TOT} (%)	-	74%	-	38.7%	12%	36.6%	24.5%	3%

*The total single-end capacitance of stage 1 and stage 2 are 3pF and 0.75 pF respectively.

first-stage SAR and the residue transferring time for the boosted BBD is about 4 ns, resulting in a 40-MS/s conversion rate with some margin. The speed's dependence on technology can also be observed in reported pure SAR ADCs. Most 10-bit pure SAR ADCs in 0.18-μm CMOS operate at conversion rates ranging from tens of kS/s to several MS/s [1], and some of them can reach up to 30 MS/s [2]. Because the SAR delay reduces dramatically with the scaling down of the CMOS technology, the 10-bit pure SAR ADC in 90-nm CMOS [3] and the 11-bit SAR ADC as a sub-ADC in the time-interleaved ADC in 28-nm CMOS [4] realize conversion rates of 100 and over 400 MS/s, respectively. Similarly, much smaller SAR delay could be expected for the proposed ADC in a more advanced technology. Moreover, the boosted BBD is inherently suitable for more advanced technologies and can operate under lower supply voltage. Hence, higher conversion rate and better FoM are expected to be achieved if the ADC is implemented in a more advanced technology.

VI. CONCLUSION

Boosted BBDs have been used as low-power and high-precision residue charge transfers in multistage pipelined ADCs, while showing drawbacks of large nonlinearity and severe accumulated CM charge error, which requires power-hungry real-time calibration circuits to control the CM level in each stage. It is shown in this paper that the problems are alleviated significantly when the boosted BBDs are used in two-stage pipelined-SAR ADCs. The idea is verified with a 10-bit pipelined-SAR ADC implemented in 0.18-μm CMOS which shows an SNDR/SFDR of 57.1 dB/71.4 dB while consuming 1.87 mW at 40 MS/s. The boosted BBD residue circuits consumes only 0.06 mW or 3% of the total power, showing its low-power potential to be applied in pipelined-SAR ADCs.

REFERENCES

[1] Z. Zhu, Z. Qiu, M. Liu, and R. Ding, "A 6-to-10-Bit 0.5 V-to-0.9 V reconfigurable 2 MS/s power scalable SAR ADC in 0.18-μm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 689–696, Mar. 2015.

[2] B. G. Lee, "Power and bandwidth scalable 10-b 30-MS/s SAR ADC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 6, pp. 1103–1110, Jun. 2015.

[3] Y. Zhu *et al.*, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[4] J. Fang *et al.*, "A 5-GS/s 10-b 76-mW time-interleaved SAR ADC in 28 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2015, pp. 1–4.

[5] C. P. Hurrell, C. Lyden, D. Laing, D. Hummerston, and M. Vickery, "An 18 b 12.5 MS/s ADC With 93 dB SNR," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2647–2654, Dec. 2010.

[6] C. C. Lee and M. P. Flynn, "A SAR-assisted two-stage pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

[7] A. M. A. Ali *et al.*, "A 14 Bit 1 GS/s RF sampling pipelined ADC with background calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2857–2867, Dec. 2014.

[8] M. KrÃ¤mer, E. Janssen, K. Doris, and B. Murmann, "A 14-bit 30-MS/s 38-mW SAR ADC using noise filter gear shifting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 2, pp. 116–120, Feb. 2017.

[9] M. Furuta, M. Nozawa, and T. Itakura, "A 10-bit, 40-MS/s, 1.21 mW pipelined SAR ADC using single-ended 1.5-bit/cycle conversion technique," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1360–1370, Jun. 2011.

[10] R. Wang, U. F. Chio, S. W. Sin, U. Seng-Pan, Z. Wang, and R. P. Martins, "A 12-bit 110MS/s 4-stage single-opamp pipelined SAR ADC with ratio-based GEC technique," in *Proc. ESSCIRC*, Bordeaux, France, Sep. 2012, pp. 265–268.

[11] C.-Y. Lin and T.-C. Lee, "A 12-bit 210-MS/s 2-times interleaved pipelined-SAR ADC with a passive residue transfer technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 7, pp. 929–938, Jul. 2016.

[12] Y. Zhu, C.-H. Chan, S.-P. U, and R. P. Martins, "An 11b 900 MS/s time-interleaved sub-ranging pipelined-SAR ADC," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Venice Lido, Italy, Sep. 2014, pp. 211–214.

[13] S.-W. Sin *et al.*, "An 11b 60MS/s 2.1 mW two-step time-interleaved SAR-ADC with reused S&H," in *Proc. ESSCIRC*, Seville, Spain, Sep. 2010, pp. 218–221.

[14] Y.-D. Jeon *et al.*, "A 9.15 mW 0.22 mm^2 10 b 204 MS/s pipelined SAR ADC in 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2010, pp. 1–4.

[15] Y. Zhu, C.-H. Chan, S.-W. Sin, S.-P. U, R. P. Martins, and F. Maloberti, "A 50-fJ 10-b 160-MS/s pipelined-SAR ADC decoupled flip-around MDAC and self-embedded offset cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2614–2626, Nov. 2012.

[16] F. van der Goes *et al.*, "A 1.5 mW 68 dB SNDR 80 Ms/s 2× interleaved pipelined SAR ADC in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2835–2845, Dec. 2014.

[17] B. Verbruggen, K. Deguchi, B. Malki, and J. Craninckx, "A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28 nm digital CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, Jun. 2014, pp. 1–2.

[18] Y. Zhu, C.-H. Chan, S. P. U, and R. P. Martins, "A 10-bit 500-MS/s partial-interleaving pipelined SAR ADC with offset and reference mismatch calibrations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 1, pp. 354–363, Jan. 2017.

[19] M. Brandolini *et al.*, "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.

[20] J. Zhong, Y. Zhu, C.-H. Chan, S.-W. Sin, S.-P. U, and R. P. Martins, "A 12b 180 MS/s 0.068 mm^2 pipelined-SAR ADC with merged-residue DAC for noise reduction," in *Proc. Conf. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, Lausanne, Switzerland, Sep. 2016, pp. 169–172.

[21] H. Huang, L. Du, and Y. Chiu, "A 1.2-GS/s 8-bit two-step SAR ADC in 65-nm CMOS with passive residue transfer," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Xiamen, China, Nov. 2015, pp. 1–4.

[22] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/s 13 bit fully differential ring amplifier based SAR-assisted pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015.

[23] Y. Zhou, B. Xu, and Y. Chiu, "A 12 bit 160 MS/s two-step SAR ADC with background bit-weight calibration using a time-domain proximity detector," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 920–931, Apr. 2015.

[24] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring amplifiers for switched capacitor circuits," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012.

[25] V. Tripathi and B. Murmann, "A 160 MS/s, 11.1 mW, single-channel pipelined SAR ADC with 68.3 dB SNDR," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2014, pp. 1–4.

[26] J. Kuppambatti and P. R. Kinget, "Current reference pre-charging techniques for low-power zero-crossing pipeline-SAR ADCs," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 683–694, Mar. 2014.

[27] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2× interleaved fully dynamic pipelined SAR ADC in 40 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2012, pp. 466–468.

[28] B. Verbruggen *et al.*, "A 2.1 mW 11b 410 MS/s dynamic pipelined SAR ADC with background calibration in 28 nm digital CMOS," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, Jun. 2013, pp. C268–C269.

[29] J. Gao, G. Li, and Q. Li, "An amplifier-free pipeline-SAR ADC architecture with enhanced speed and energy efficiency," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 4, pp. 341–345, Apr. 2016.

[30] Y. S. Hu, P. C. Huang, H. Y. Tai, and H. S. Chen, "A 12.5-fJ/conversion-step 8-bit 800-MS/s two-step SAR ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 12, pp. 1166–1170, Dec. 2016.

[31] H.-Y. Tai, C.-H. Tsai, P.-Y. Tsai, H.-W. Chen, and H.-S. Chen, "A 6-bit 1-GS/s Two-Step SAR ADC in 40-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 339–343, May 2014.

[32] M. P. Anthony, "Boosted charge transfer circuit," U.S. Patent 8 385 498, Feb. 26, 2013. [Online]. Available: http://www.freepatentsonline.com/8385498.html

[33] M. Anthony, E. Kohler, J. Kurtze, L. Kushner, and G. Sollner, "A process-scalable low-power charge-domain 13-bit pipeline ADC," in *Proc. IEEE Symp. VLSI Circuits*, Honolulu, HI, USA, Jun. 2008, pp. 222–223.

[34] M. Anthony and G. Sollner, "Ultra-low-power 500-MSPS 12-bit A/D converter using interleaving and CMOS charge-domain technology," in *Proc. Annu. IEEE Compound Semiconductor Integr. Circuit Symp.*, Greensboro, NC, USA, Oct. 2009, pp. 1–4.

[35] N. Dolev, M. Kramer, and B. Murmann, "A 12-bit, 200-MS/s, 11.5-mW pipeline ADC using a pulsed bucket brigade front-end," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, Jun. 2013, pp. C98–C99.

[36] M. P. Anthony, "Common-mode charge control in a pipelined charge-domain signal-processing circuit," U.S. Patent 7 576 586, Aug. 18, 2009. [Online]. Available: http://www.freepatentsonline.com/7576586.html

[37] X. Wang, H. Zhang, D. Li, J. Cheng, and R. Zhang, "Nonlinearity analysis of the boosted bucket brigade device for high-speed charge-domain ADCs," in *Proc. 12th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Guilin, China, Oct. 2014, pp. 1–3.

[38] J. Craninckx and G. van der Plas, "A 65fJ/conversion-step 0-to-50 MS/s 0-to-0.7 mW 9b charge-sharing SAR ADC in 90 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2007, pp. 246–600.

[39] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

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