Crosstalk-Aware Transmitter Pulse-Shaping for Parallel Chip-to-Chip Links

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ISCAS 2007
Board-to-Board Channel

- Chips
- Daughtercards
- Connectors
- Board
Characterize the Channel

Chip1

\[ Z_0 = 50 \, \Omega \]

Chip2

Through crosstalk 1

Through crosstalk 2

Voltage (V)

Time (ns)

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System Model

Crosstalk-Aware Equalization Over Chip-to-Chip Links

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Conventional Solutions

- **slew-rate limiting**
  - pro: simple
  - con: not good when ISI is severe

- **crosstalk cancellation** in addition to transmit filter G
  - pro: good performance
  - con: hardware cost

Chip-to-Chip Channel

- Transmit Filter

(many links in parallel)
Example: Different Pulse Shapes

- **Square Pulse**: 1 UI, 1 total tap, 1 tap per UI
- **Pre-emphasis Pulse**: 1 UI, 2 total taps, 1 tap per UI
- **Fractionally-spaced**: 1 UI, 6 total taps, 3 taps per UI
Example: Different Pulse Shapes

- **Square Pulse**
  - 1 UI
  - 1 total tap
  - 1 tap per UI

- **Pre-emphasis Pulse**
  - 1 UI
  - 2 total taps
  - 1 tap per UI

- **Fractionally-Spaced Pulse**
  - 1 UI
  - 6 total taps
  - 3 taps per UI
Example: Different Pulse Shapes

- Square pulse:
  - 1 total tap
  - 1 tap per UI

- Pre-emphasis pulse:
  - 2 total taps
  - 1 tap per UI

- Fractionally-spaced pulse:
  - 6 total taps
  - 3 taps per UI
Definition

\[ E2C = \frac{\text{crosstalk-free eye opening}}{\text{maximum possible crosstalk}} \]
Find E2C for each Pulse Shape

PRBS7

\[ E2C = \frac{485 \text{ mV}}{2 \times 157 \text{ mV}} = 1.54 \]

Repeat calculation for all candidate pulse shapes
Maximum E2C for Various Filter Types at 2.7 Gb/s

Increasing E2C

Taps per UI

Total Taps

E2C

Tap Delay (in UI)

1/6

1/5

1/4

1/3

1/2

1
Increasing Total Taps

Taps per UI vs. Total Taps

E2C

Tap Delay (in UI)

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Increasing Granularity

**Graph:**
- **Y-axis:** Taps per UI
- **X-axis:** Total Taps
- **Legend:** E2C
- **Annotations:**
  - 1/6, 1/5, 1/4, 1/3, 1/2, 5.5, 5, 4.5
- **Highlights:**
  - Green arrow indicating increasing granularity
  - Red dots at Taps per UI: 2, 3, 4, 5, 6

**Equation:**
- **Total Taps:** \( T \)
- **Taps per UI:** \( T_{\text{per UI}} \)

**Equation Details:**
- **Tap Delay:** \( \text{Tap Delay (in UI)} \)

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**Title:**
- Crosstalk-Aware Equalization Over Chip-to-Chip Links
Increasing Taps per UI

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Hardware Proof-of-Concept

ParBERT

Power Combiner

Power Combiner

Power Combiner

Chip-to-Chip Channel

Oscilloscope
Channel Introduces ISI and Crosstalk

- 2.7 Gb/s
- PRBS: $2^{31} - 1$

- input to channel
- square pulse

- output from channel
- no aggressors

- output from channel
- two aggressors
Filter Opens the Eye

- output from channel
- two aggressors
- square pulse input
- $jitter_{RMS} = 53 \text{ ps}$

- pulse shape chosen to maximize E2C
- 3 total taps
- 2 taps per UI
- $jitter_{RMS} = 33 \text{ ps}$
Filter Improves Bit Error Rate

- **square pulse:**
  \[ BER = 10^{-5} \]

- **crosstalk-aware pulse:**
  \[ BER < 10^{-12} \]

- **pre-emphasis pulse:**
  \[ BER = 10^{-7} \]

- **crosstalk-aware pulse:**
  \[ BER = 10^{-5} \]
Crosstalk is significant in board-to-board channels.

Received eye opening can be increased by taking crosstalk into account when equalizing.

Crosstalk-aware pulse shape decreased BER by $10^2$ at 2.7 Gb/s.