The Effect of Redundancy on Mismatch-Induced Offset and Random Noise in a Dynamic Comparator

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***Abstract*–We present an analysis of offset voltage and noise in a dynamic comparator. To limit the offset and noise to acceptable levels, a single comparator must be sized quite large. We show that better use can be made of this die area by dividing it into an array of redundant comparators from which the lowest-offset device is chosen. Monte Carlo simulations with a 45 nm CMOS process confirm that the input-offset standard deviation can be reduced arbitrarily in the absence of noise. As the area is divided into a greater number of smaller comparators, random noise overtakes offset as the factor limiting the sensitivity. The competing effects of offset and noise combine to give an optimum number of comparators that maximizes sensitivity for a given total area.**

I. Introduction

Comparators are an important part of analog-to-digital converters as well as high-speed digital communication systems. The accuracy of an ADC depends on the input offset voltage of the comparators it uses, as well as their input-referred noise. In high-speed communication channels the received eye opening can be severely attenuated, requiring a low-offset, low-noise comparator to distinguish between ones and zeros.

Dynamic comparators are popular because of their low power consumption and high speed. However, they suffer from being harder to analyze because they do not operate around a static bias point. Specifically, analytical expressions for the input offset due to mismatch and the input-referred noise are not easily derived.

Some work has been done in this area recently, however, with a method for offset voltage prediction being presented in [1]. This method uses DC node voltages at the instant the clock goes high as a starting point. The circuit is then perturbed by a mismatch between two transistors. Finally, the input voltage required to return the circuit to a balanced condition is calculated; this is the input-offset voltage. Statistical calculations can then be performed to determine the standard deviation of this offset term.

The technique of designing a circuit with redundant components has been used to design ADCs with reduced matching requirements [2], [3]. The poorly-matched components are identified in calibration and are swapped with redundant components with better matching. The probability distribution of offset voltage has also been exploited to perform

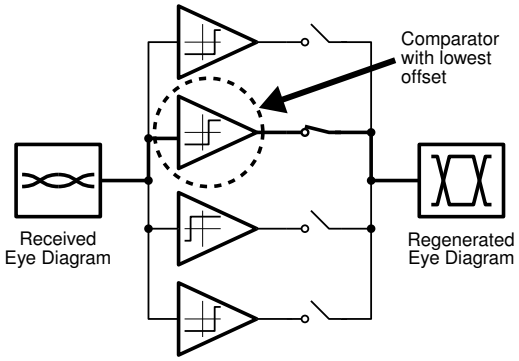

Fig. 1. An array of four redundant comparators used to recover a 1-bit signal with a small eye opening. Each comparator has an input-offset voltage caused by mismatch. Only the comparator with the lowest offset is powered during operation.

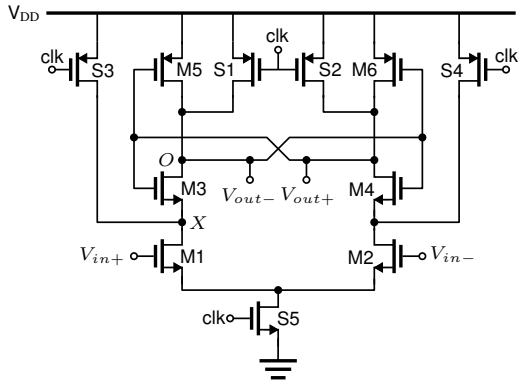

Fig. 2. Schematic of the reference comparator design.

up to 6-bit analog-to-digital conversion with a nominally 1-bit comparator [4], [5], [6]. This paper considers the use of redundant comparators in the receiver of a 1-bit communication channel where the received eye opening may be only a few millivolts. The proposed system is shown in Fig. 1. The offset of each comparator is characterized before use, and only the comparator with the lowest offset is powered during operation. The reference comparator topology used to explore this concept is shown in Fig. 2.

Sec. II analyzes the offset voltage of a single comparator. Sec. III calculates how much the offset can be reduced by using an array of proportionally smaller comparators. Sec. IV analyzes the input-referred noise of the comparators discussed

in the previous two sections to determine the optimal size for a comparator while considering both offset and noise. Sec. V concludes the paper.

II. Random Offset Voltage in a Single Dynamic Comparator

The authors in [1] were able to derive analytical expressions relating the offset voltage of a comparator to threshold voltage and mobility mismatch in its transistors. Those expressions showed good agreement with monte carlo simulations of offset voltage for a 0.25 μm CMOS process. While output resistance and body effect were neglected, these had negligible impact on offset for this process.

In 45 nm CMOS the mismatch between transistors is larger while output resistance is smaller. Therefore output resistance and body effect must be taken into account in order to evaluate input-offset accurately. Unfortunately, these effects make the offset-mismatch relationship nonlinear and difficult to calculate.

One mitigating factor is that in 45 nm CMOS the mismatch in V_t and μ is no longer uncorrelated. This means that we can no longer consider the V_t-mismatch-induced offset separately from the offset caused by μ mismatch. While the relationship between mismatch and offset has become more complicated, V_t and μ are positively correlated so that an increase in V_t (which reduces current) tends to be partially compensated by an increase in μ (which increases current). The variation in source-drain series resistance R_S is also inversely proportional to mobility variation, which further compensates for V_t mismatch.

As a baseline for our analysis, we performed a monte carlo analysis on the dynamic comparator in Fig. 2 with the following device sizes:

$$\begin{aligned} W_{S5} &= 0.24\,\mu\text{m} \\ \text{all other transistor widths} &= 0.12\,\mu\text{m} \\ \text{all transistor lengths} &= 40\,\text{nm} \end{aligned}$$

This monte carlo simulation produced a distribution of offset voltages with $\sigma_{V_{os}} = 58.8\,\text{mV}$. Now, since threshold-voltage and mobility mismatch are inversely proportional to device area

$$\sigma_{V_t} \propto \frac{1}{\sqrt{WL}} \tag{1}$$

$$\sigma_{V_\mu} \propto \frac{1}{\sqrt{WL}}, \tag{2}$$

if the area of the comparator is doubled the offset will be reduced by a factor of $\sqrt{2}$. Values of $\sigma_{V_{os}}$ are plotted in Fig. 3 along with the area required by directly scaling all device widths. According to this graph an area of 236 μm^2 is required to achieve offset less than 1 mV.

III. Random Offset Voltage in an Array of Dynamic Comparators

By introducing an array of redundant transistors, we can take advantage of the fact that most of the mismatch is fixed at fabrication time to choose the best comparator from the array. In this case, the best comparator is the one with an offset voltage closest to zero. The unused comparators would be powered off.

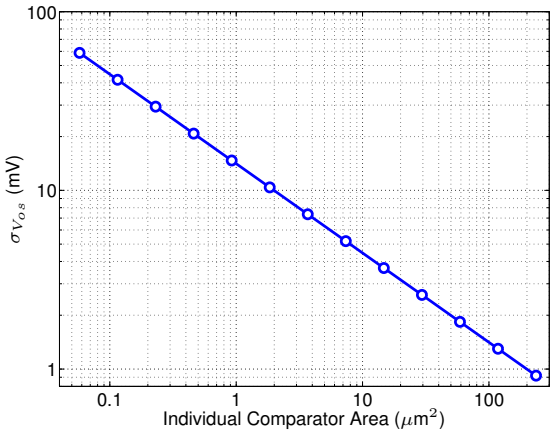

Fig. 3. Achievable offset, $\sigma_{V_{os}}$, vs. total area (sum of all $W_i L_i$).

To compare this scheme with the single comparator, the probability distribution function (PDF) of the offset is needed. The PDF of offset for a single comparator is

$$\phi(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\mu)^2}{2\sigma^2}}. \tag{3}$$

The chance that the lowest-offset comparator (out of k total comparators) has offset with magnitude greater than some value a is

$$p(|x| > a) = \left[1 - \int_{-a}^{a} \phi(x)dx\right]^k. \tag{4}$$

The fraction of comparators with absolute offset less than a is:

$$p(|x| < a) = 1 - \left[1 - \int_{-a}^{a} \phi(x)dx\right]^k. \tag{5}$$

We can now convert this into a cumulative distribution function (CDF), assuming a symmetrical distribution:

$$p(x < a) = \frac{1}{2} + sign(a)\frac{1}{2}\left(1 - \left[1 - \int_{-|a|}^{|a|} \phi(x)dx\right]^k\right). \tag{6}$$

The PDF of the offset voltage is then the derivative of Eq. (6). We can see the benefit of redundant comparators by plotting the PDFs of input-offset for three cases:

- one standard-size comparator ($1x$)
- an array of four standard-size comparators from which the lowest-offset comparator is chosen
- one comparator with area four times larger ($4x$) and hence offset half as large as the standard-size comparator

The resulting probability density functions are shown in Fig. 4. We can see that a standard-size comparator has an offset standard deviation that is twice that of the $4x$ comparator. With an array of four standard-size transistors, the offset is less than that of the $4x$ comparator if we are free to choose

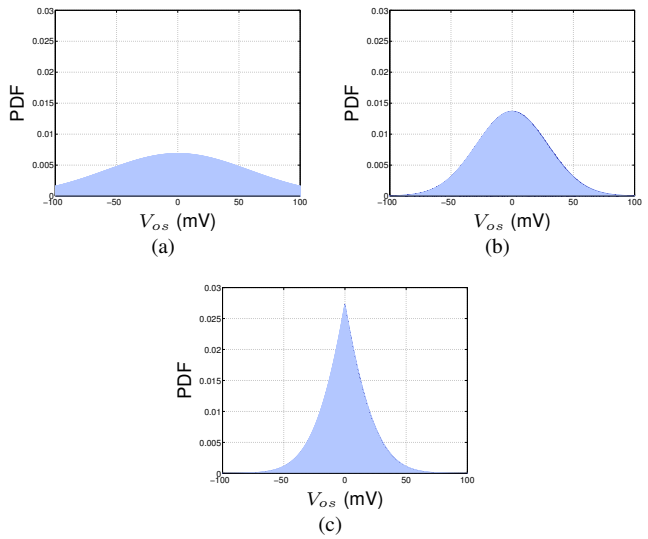

Fig. 4. (a) pdf of offset for standard-size comparator (b) pdf of offset for $4x$ comparator (c) pdf of offset for the lowest-offset comparator in an array of four standard-size comparators.

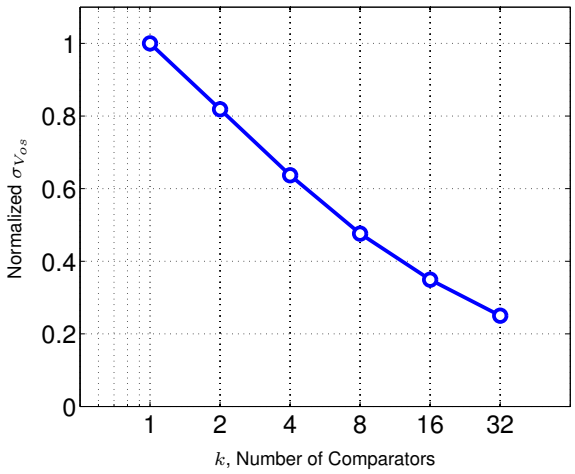

Fig. 5. Offset decreases for a fixed total area as number of proportionally-smaller comparators increases.

the comparator with the lowest offset after fabrication. The distribution in Fig. 4(c) has a significantly lower standard deviation that the distribution in Fig. 4(b).

We can visualize the offset reduction caused by redundancy by imagining a fixed total die area that can be divided into any number of comparators. A single comparator has an associated offset. A lower offset can be achieved for the same area by using a larger number of proportionally smaller comparators, even though the smaller comparators individually have higher offset. Fig. 5 shows how the offset standard deviation, $\sigma_{V_{os}}$, decreases as the number of comparators increases for a constant total area.

Since the standard deviation of the CDF in Eq. (6) is monotonically decreasing with increasing k, redundancy can be used to achieve $\sigma_{V_{os}} < 1\,\text{mV}$ for any size comparator in

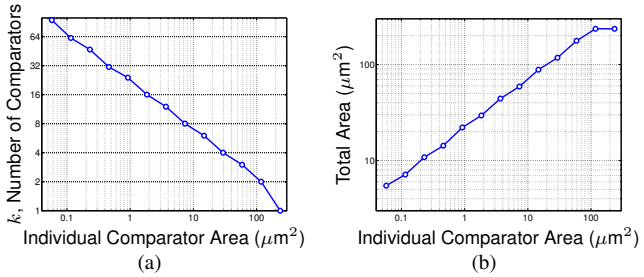

Fig. 6. (a) Number of comparators, and (b) total area required to achieve $\sigma_{V_{os}} < 1\,\text{mV}$ for each size of individual comparator.

Fig. 3 simply by choosing k large enough. Fig. 6(a) shows the number of comparators required of each size in order to drive $\sigma_{V_{os}}$ below 1 mV. Fig. 6(b) shows the total area of the comparator array required for each size.

Fig. 6 reveals that the most area-efficient way to achieve $\sigma_{V_{os}} < 1\,\text{mV}$ is to use an array of 95 minimum-size comparators each with area $0.0575\,\mu\text{m}^2$ for a total area of $5.472\,\mu\text{m}^2$.

IV. Random Noise in a Dynamic Comparator

While it was shown in Sec. III that an array of redundant comparators resulted in reduced offset voltage, as the device sizes are reduced random noise becomes more important. The array of redundant devices allows the choice of the one with the lowest offset, but in the end a single comparator is used. There is a tradeoff between decreased offset and increased noise.

To determine the optimal number of comparators, we follow the analysis in [7] to determine the input-referred random noise generated by the comparator. A single transient analysis is sufficient to estimate the input-referred rms noise voltage. In [7] the sampling period is divided into three phases which are defined by the operating region of transistors M_1–M_6. The noise power within a phase is calculated using stochastic differential equations, with the noise power at the end of a phase being used as the intial noise power of the next phase.

The result is an equation for the input-referred noise power, broken down by device:

$$\sigma_n^2 = \sigma_{M_{1,2}}^2 + \sigma_{S_{1,2}}^2 + \sigma_{M_{3,4,5,6}}^2 + \sigma_{S_{3,4}}^2 \tag{7}$$

The individual contributions are as follows:

$$\sigma_{M_{1,2}}^2 = \frac{2kT\gamma}{C_X\mathcal{F}} \tag{8}$$

$$\sigma_{S_{1,2}}^2 = \frac{kT}{2C_O\mathcal{F}^2} + \frac{kT}{2C_X\mathcal{F}^2\mathcal{H}} + \frac{kTC_O}{8C_X^2\mathcal{F}^2\mathcal{H}^2} \tag{9}$$

$$\sigma_{M_{3,4,5,6}}^2 = \frac{kT\gamma}{2C_X\mathcal{F}^2\mathcal{H}} + \frac{kT\gamma C_O}{8C_X^2\mathcal{F}^2\mathcal{H}^2} \tag{10}$$

$$\sigma_{S_{3,4}}^2 = \frac{kT}{2C_X\mathcal{F}^2} \tag{11}$$

where:

$$\mathcal{F} = \frac{V_{Tn3}}{V_{ov1,1}} \tag{12}$$

$$\mathcal{H} = \frac{V_{DD} - V_{CM}}{V_{ov3,2}} \frac{I_{D3,2}}{I_{D1,2} - I_{D3,2}} \tag{13}$$

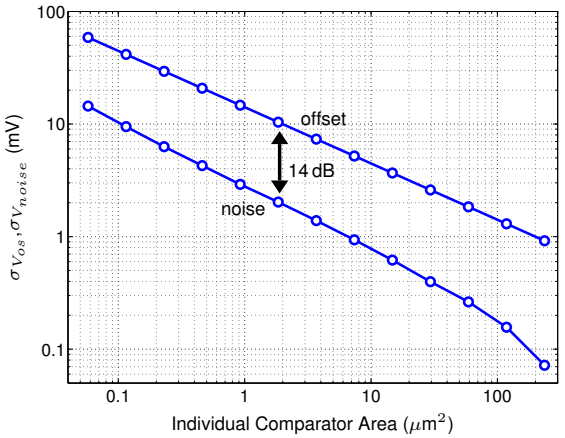

Fig. 7. Input-referred noise and offset for a single comparator.

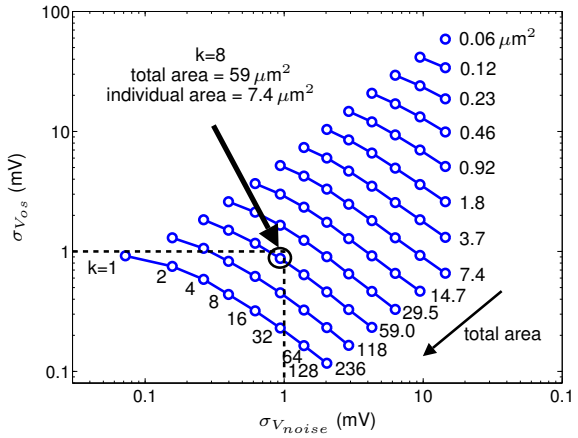

Fig. 8. Offset vs. input-referred noise plotted on lines of constant total area. The dotted lines indicate where offset and noise are equal to 1 mV.

$I_{Dj,k}$ refers to the drain current through transistor M_j during phase k.

Applying these equations to the single comparator in Sec. II, we find that the input-referred noise decreases along with the offset as the area of the comparator increases. Fig. 7 shows this relationship. The rms noise is consistently 14 dB below the level of the offset; the circuit is dominated by offset.

By using redundancy we can reduce the offset voltage to the point where it becomes comparable to the noise. To choose the optimal number of comparators Fig. 8 shows offset vs. noise on lines of constant total area. Each line represents a constant total area split up into different numbers of individual comparators.

The dashed lines in Fig. 8 show the area where offset and noise are both below 1 mV. There are ten different configurations that satisfy these conditions. However, the highlighted solution with $k = 8$ requires only one quarter the area of the solution with no redundancy ($k = 1$).

A circuit with a single comparator ($k = 1$) is overdesigned to reduce noise relative to offset. Adding redundancy changes the relationship between offset and noise for the dynamic comparator in Fig. 2 so that a more balanced design can be achieved.

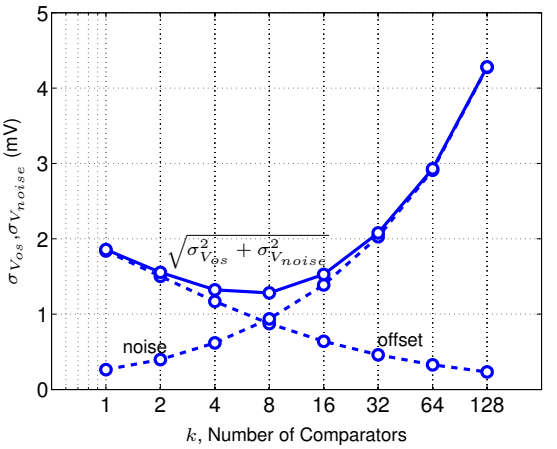

Fig. 9. Noise and offset for an array of k comparators with total area=59.0μm^2.

V. Conclusion

This paper examined offset and random noise in a dynamic comparator. Using monte carlo simulation and results from [7] it was shown that the dynamic comparator is dominated by mismatch-induced offset rather than random noise. By using an array of redundant comparators, it was shown that offset decreases at the expense of increased noise. For a circuit specification where offset and noise should be of similar magnitude the area required has been reduced by a factor of four.

Acknowledgment

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