A 6.5 Gb/s Backplane Transmitter with 6-tap FIR Equalizer and Variable Tap Spacing

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***Abstract*–This paper presents a 6.5 Gb/s transmitter for use in backplane links. This transmitter incorporates a finite impulse response filter with programmable tap spacing in the output driver to compensate for intersymbol interference. Using jitter-minimizing tap weights computed using a behavioral model of the transmitter, it is shown that at 6.5 Gb/s peak-to-peak data-dependent jitter is reduced by over 50% by using a tap spacing of 0.53 unit intervals (UI) instead of the usual 1 UI.**

I. Introduction

In high-speed backplane communication links, the limited channel bandwidth introduces inter-symbol interference (ISI) into the received signal. Equalizers in the transmitter and receiver have been widely used to compensate for loss at high frequency and allow data to be sent at rates higher than the bandwidth of the channel. A common configuration involves a decision feedback equalizer (DFE) in the receiver and a feed-forward equalizer (FFE) in the transmitter [1]. These equalizers consist of a delay line that generates phase-shifted versions of the input signal and an output driver for each tap. The taps are typically baud-spaced, and are generated by a cascade of flip-flops clocked at the bit rate. The useful number of taps is determined by the length of the impulse response of the channel. For high-loss channels with long impulse responses, up to five baud-spaced taps have been used at multi- Gb/s data rates [2, 3].

Fractionally-spaced equalizers can increase the useful number of taps by inserting additional taps between the baud-spaced ones. The precise delays between taps can be generated by lumped LC structures that absorb the parasitic capacitance of the output driver [4]. Alternatively, the taps can be generated using a variable delay line that references its delay to the period of the data signal, such as in the receiver equalizer proposed in [5]. A variable delay line dissipates more power than the cascade of flip-flops typically used to generate baud-spaced taps, but it has the advantage of being easily reconfigured to provide fractional tap spacings. This reconfigurability can permit lower jitter when equalizing backplane links and is also desirable because of the need for bandwidth and power scalability [6].

Using an equalizer with a variable tap spacing allows us to investigate the effect of varying the tap spacing on the jitter performance of a backplane communication link. We show that the optimal tap spacing is not necessarily one unit interval (UI) or a simple fraction thereof. For the 24" backplane channel considered here, choosing the optimal tap spacing can significantly reduce received jitter.

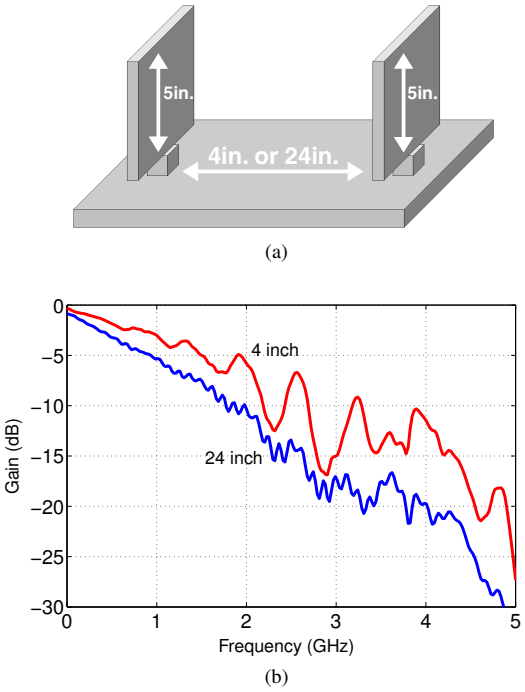


Fig. 1. (a) Backplane channel, (b) Measured frequency response of the 4" and 24" Tyco backplane channels.

II. Circuit Description

This paper describes a transmit-side equalizer for communication over backplane channels such as the one pictured in Fig. 1(a). This channel is typical of legacy backplanes in use today. The proposed finite impulse response (FIR) equalizer, shown in Fig. 2, consists of a six-tap delay line with a variable gain stage for each tap. The delay line is tuneable to allow the use of different tap spacings and different bit rates. Each tap has adjustable gain with 4-bit resolution.

The variable gain stage is broken into six slices, one for each tap of the delay line. The currents from the six slices are summed in 50 Ω load resistors to produce the output voltage. As shown in Fig. 3, each slice of the gain stage consists of a sign selection switch followed by a preamplifier and a 3-bit adjustable output driver, for a total of 4 bits. When a given filter tap is not in use,

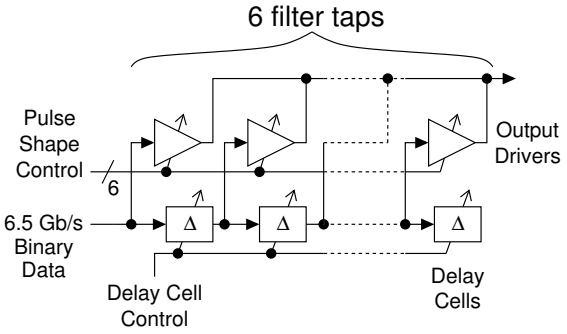


Fig. 2. Transmitter block diagram.

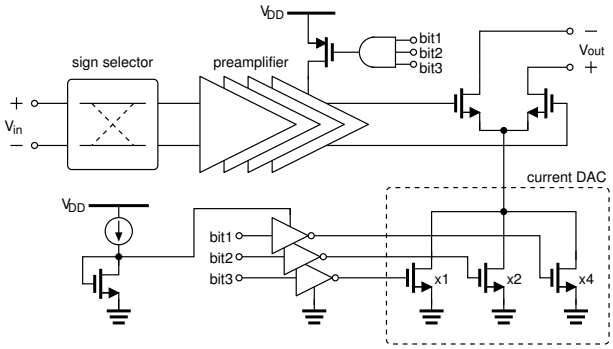


Fig. 3. Schematic diagram of one output driver slice.

the corresponding gain stage slice is automatically shut down in order to save the power that would have been burned in the preamplifier. Unfortunately, the linearity of the current-mode D/A converter (DAC) used in this stage is not very good. However, as long as we can characterize the nonlinearity we can take the nonlinearity into account when optimizing the pulse shape for equalization of a given channel.

The delay line generates six phase-shifted versions of the input data using five delay cells. Each delay cell consists of four stages like the one in Fig. 4(a) with a differential pair driving symmetric loads. This type of load acts as a resistance with an adjustable value. As the resistance increases, the delay of the stage increases while the voltage swing is kept constant by a replica bias feedback loop that reduces the tail current. Four stages are required in order for each cell to generate a significant delay while still maintaining the required bandwidth. With fewer stages the delay per cell would be too small.

The delay cell is tuneable from 62–216 ps, as shown in Fig. 4(b). Increasing the delay reduces the power dissipation from 40 down to 12 mW, providing power scaling for slower data rates. At a delay of 120 ps the bandwidth of the delay line is sufficient for data rates only up to 5 Gb/s. To achieve higher delay while maintaining bandwidth, multiple delay cells can be used as one by simply turning off the intervening taps. For example, to generate a 125 ps tap spacing, we can use either one delay cell with a delay of 125 ps or two cascaded delay cells each with a delay of 62.5 ps. The latter option will result in higher bandwidth.

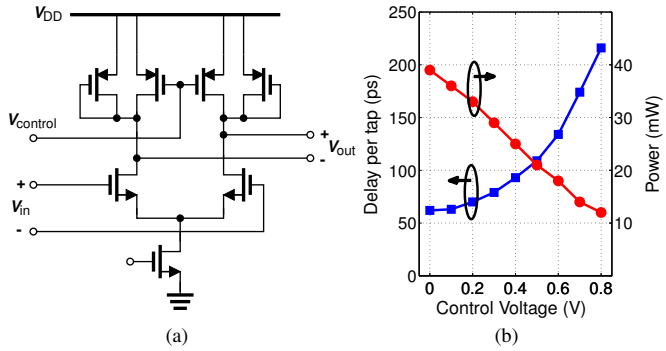


Fig. 4. (a) Delay stage. Each delay cell block in Fig. 2 contains four such stages, (b) measured tap delay and total power of the delay line.

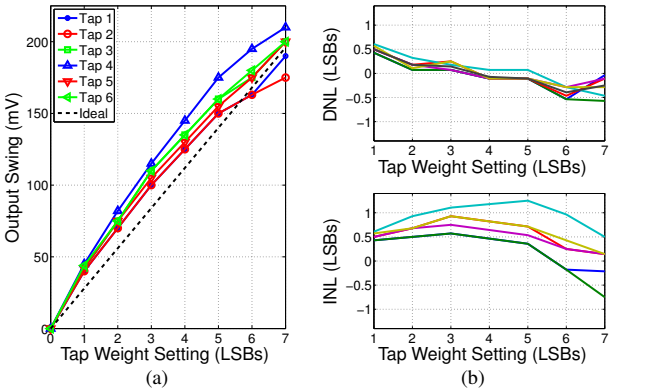


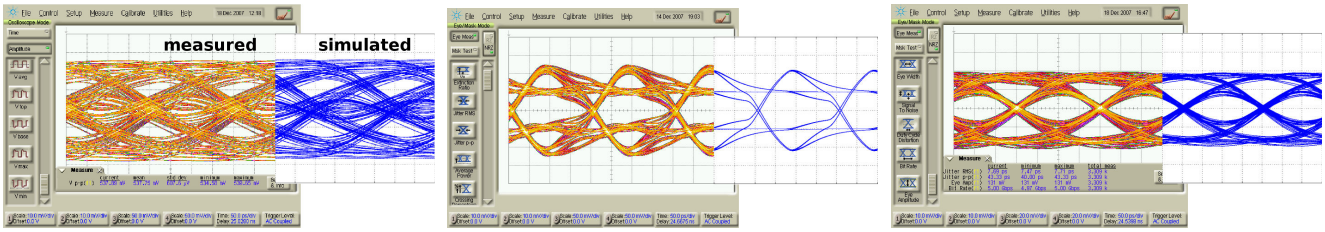
Fig. 5. Linearity of the output driver DAC. (a) Output swing for each digital code, (b) DNL and INL.

III. Channel and Circuit Modeling

The intended channel for this transmitter is a backplane with two 5" daughtercards connected to a 16-layer non-backdrilled motherboard. The frequency response of the channel is shown in Fig. 1(b). The 24" channel has more attenuation but the 4" channel suffers more from reflections. These reflections are caused by impedance discontinuites at the vias and connectors and they show up as ripples in the frequency response.

or a 6-tap filter with 4-bit resolution for each tap weight, there are $(2^4)^6 \approx 1.6$ million possible filter configurations. To help with tap weight selection a behavioral model of the transmitter and channel was created. To start, we first measure the nonlinearity of the output driver DAC. The nonlinearity was characterized by measuring the output swing for all tap weight settings with only one tap operational. The linearity of the output driver DAC is shown in Fig. 5. While the linearity is far from ideal, we compensate for this deficiency by choosing the transmitted pulse shape appropriately. This flexibility loosens the requirements on the DAC which means it can be designed to consume less voltage headroom and area.

FThe slew rate in simulation is then limited to the value that is observed in measurement. With six output driver slices whose currents are summed together, there is significant parasitic capacitance at the output node that limits the slew rate.



(a) (b) (c)

Fig. 6. Measured and simulated behavioral model 5 Gb/s eye diagrams for a PRBS7 pattern: (a) Output of unequalized 24" backplane channel, (b) transmitter output for half-baud-spaced jitter-minimizing pulse shape, (c) equalized 24" backplane channel.

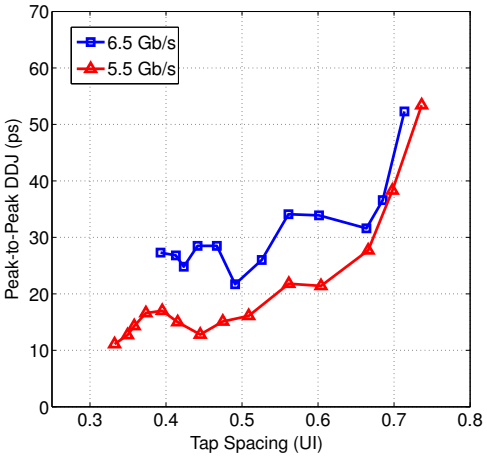


Fig. 7. Transmit-side DDJ vs. delay per cell of the delay line.

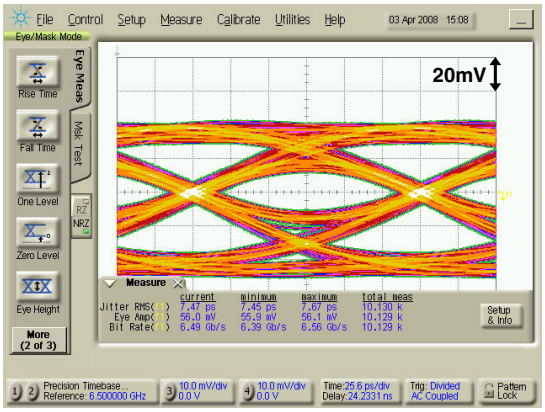


Fig. 8. Received 6.5 Gb/s equalized eye diagram for the 24" backplane channel. Tap spacing is 0.53 UI and the optimal tap weights are [+2 -1]. Total transmitter power for this configuration is 42 mW.

This slew-rate-limited signal is then put through an RLC circuit that models the parasitics of the QFN package. Finally the measured s-parameters of the backplane channel give us the receive-side signal that results.

Using this model, behavioral simulations were performed to evaluate all possible tap weight settings. For each configuration (channel length, number of taps, and tap spacing) the tap weights resulting in the lowest simulated jitter were selected.

Fig. 6 shows the match between model and measurement for three sample eye diagrams at 5 Gb/s. Fig. 6(a) shows the unequalized signal received over a 24" backplane, while Figs. 6(b) and (c) show the transmit- and receive-side signals for the optimal transmitted pulse shape. The tap weights for the optimal pulse in this case are [+1 +5 -3] with a tap spacing of 100 ps.

IV. Measurement Results

We first consider the bandwidth of the delay line. As the delay generated by the line increases the bandwidth of the line decreases. The increase in transmit-side jitter as the tap spacing increases can be seen in Fig. 7. When the delay becomes 0.7 of a UI the delay line can no longer operate as the jitter has increased too much. This limitation forces us to use multiple delay cells in cascade when implementing longer delays.

An eye diagram of the received signal over 24" backplane for optimal tap weights and tap spacing at 6.5 Gb/s is shown in Fig. 8. In this case, the optimal tap spacing was 0.53 UI, much less than the typical tap spacing of 1 UI.

The tap weights were chosen only to minimize data-dependent jitter (DDJ), so we use the jitter decomposition feature of the oscilloscope to examine only the part of the jitter that is due to ISI. Random jitter remains roughly constant across all transmitter configurations around 1 ps rms.

Fig. 9 shows the improvement in DDJ as the tap spacing is varied for a data rate of 6.5 Gb/s. Since DDJ, unlike random jitter, is bounded, peak-to-peak DDJ is plotted. At 6.5 Gb/s the equalizer benefits significantly from using a smaller tap spacing; DDJ can be halved compared with conventional baud-rate tap spacing. As shown in Fig. 10, even at 5.5 Gb/s the jitter varies by almost 10 ps as the tap spacing is changed, underlining the importance of choosing the optimal tap spacing. The total power of the delay line is also plotted for both of these graphs. Note that the jump in the middle of these graphs is caused by the limited bandwidth of the delay line. Once the desired tap spacing is greater than twice the minimum delay of the line (62.5 ps), two delay cells are combined with their individual delays halved.

A die photo of the transmitter, implemented in 90 nm CMOS, is shown in Fig. 11. The power varies from 40–80 mW depending on the tap spacing and output swing. At 5 Gb/s with half-baud tap spacing and a 500 mV output swing, 63 mW is consumed. Of this, 23 mW is consumed in the delay line and 40 mW is consumed in the output drivers. This is comparable to the power reported in [1, 7] considering that those baud-spaced equalizers have a smaller number of taps as seen in Table I.

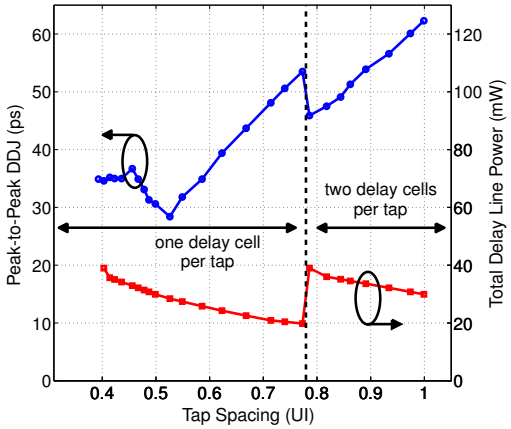


Fig. 9. Measured receive-side DDJ for the 24" backplane channel at 6.5 Gb/s. Optimal tap weights are recalculated for each tap spacing individually.

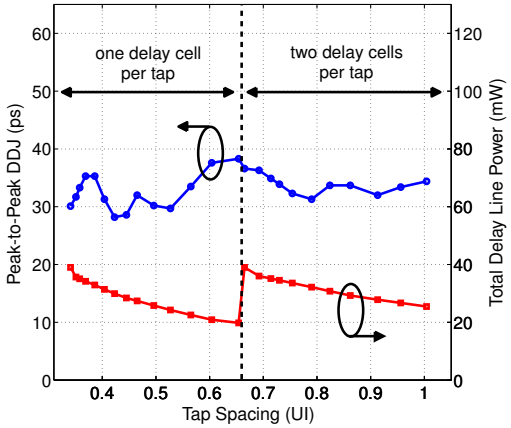


Fig. 10. Measured receive-side DDJ for the 24" backplane channel at 5.5 Gb/s. Optimal tap weights are recalculated for each tap spacing individually.

V. Conclusion

A 6.5 Gb/s transmit-side equalizer with the flexibility to use variable fractional tap spacings was presented. While the output driver DAC used here is slightly nonlinear, this nonideality is taken into account in the transmitter model. This transmitter model is then used with a channel model to choose the tap weights that minimize received jitter. The spacing between filter taps was shown to strongly influence the received peak-to-peak DDJ. For example, at 6.5 Gb/s over a 24" backplane channel, the DDJ could be cut in half, from 62.3 ps to 28.4 ps, by decreasing the tap spacing from the typical 1 UI to 0.53 UI.

Acknowledgment

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TABLE I
Transmit-side equalizer performance comparison.

	This work	[1]	[7]
Process	90 nm	90 nm	90 nm
Area	0.105 mm^2	0.16 mm^2	0.036 mm^2
Voltage	1.2 V	1.0 V	1.0 V
Power	40–80 mW	70 mW	24 mW
Data Rate	6.5 Gb/s	10 Gb/s	6 Gb/s
No. of taps	6	4	2
Tap Spacing	variable	baud	baud

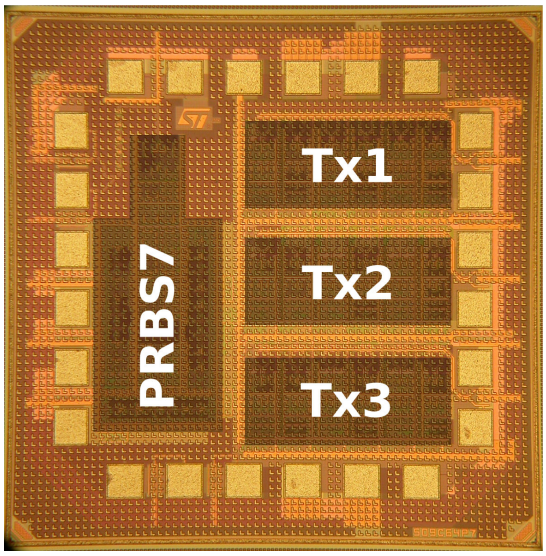

Fig. 11. The transmitter prototype was implemented in 90 nm CMOS. Die size is 1 mm × 1 mm.

References

[1] J. F. Bulzacchelli, *et al.*, "A 10-Gb/s 5-tap DFE/4-tap FFE transceiver in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2885–2900, Dec. 2006.

[2] R. Payne, *et al.*, "A 6.25-Gb/s binary transceiver in 0.13-μm CMOS for serial data transmission across high loss legacy backplane channels," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2646–2657, Dec. 2005.

[3] W. Gai, *et al.*, "A 4-channel 3.125Gb/s/ch CMOS transceiver with 30dB equalization," in *Symp. on VLSI Circuits Dig. Tech. Papers*, 2004, pp. 138–141.

[4] C. Pelard, *et al.*, "Realization of multigigabit channel equalization and crosstalk cancellation integrated circuits," *IEEE J. Solid-State Circuits*, pp. 1659–1670, Oct. 2004.

[5] X. Lin, H. Lee, and J. Liu, "A continuous-time adaptive FIR equalizer with INV-AIL delay line for 2.5Gb/s data communication," in *IEEE Custom Integrated Circuits Conf. (CICC) Dig. Tech. Papers*, 2005, pp. 413–416.

[6] G. Balamurugan, *et al.*, "A scalable 5-15Gbps 14-75mW low power I/O transceiver in 65nm CMOS," in *Symp. on VLSI Circuits Dig. Tech. Papers*, 2007, pp. 270–271.

[7] J. F. Buckwalter, M. Meghelli, D. J. Friedman, and A. Hajimiri, "Phase and amplitude pre-emphasis techniques for low-power serial links," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1391–1399, June 2006.