Progress and Trends in Multi-Gbps Optical Receivers with CMOS Integrated Photodetectors

Anthony Chan Carusone, Hemesh Yasotharan, Tony Kao
Department of Electrical and Computer Engineering
University of Toronto
Toronto, Canada

***Abstract*—There has been significant recent progress towards the realization of multi-Gbps optical receivers fully integrated into standard CMOS processes. Although CMOS photodetectors exhibit performance inferior to discrete photodetectors, they offer the potential for a low-cost highly-integrated solution that suits growing and emerging applications in short-reach optical communication. Past work has focused on using the pn-junctions and depletion regions available in standard CMOS process flows to eliminate, minimize, or cancel the slowly diffusing photocarriers that usually limit the bandwidth of CMOS photodetectors. However, if considered simply as a form of ISI, the slowly diffusing carriers can be dealt with using the same signal processing tools in wide use for other wireline communication applications, including decision feedback equalization. A combination of spatially-modulated light detection, analog equalization, and modest decision feedback equalization appears to offer a path towards data rates in excess of 10-Gbps using integrated photodetectors. Nanoscale CMOS is particularly well suited to the implementation of such signal processing functions. Measured results of photodetectors implemented in a standard 65-nm CMOS process are presented.**

Keywords-optical communication, CMOS photodetectors, decision feedback equalization, nanoscale CMOS

I. INTRODUCTION

Short-reach optical interconnect is finally coming of age. Wide deployment of optical communication began in the 80's carrying traffic for wide-area networks over fiber links kilometers in length. In the late 90's optical cabling began seeing use in local area networks at distances of less than a kilometer. The trend has continued to the present day when rack-to-rack connections within data centers and computing clusters employ optical cabling with lengths on the order of 10 meters. Although predictions of optical links between silicon dies just a few centimeters apart have been greatly exaggerated over the past decade [1], it now appears that optical links of only a few metres will enter the consumer market within 5 years.

There are fundamental reasons for these trends. The reach and robustness of high-speed electrical interconnect is increasingly limited by crosstalk. To reduce crosstalk, metal shielding is required, increasing the cost and reducing the flexibility of electrical cables. For example, the reach of 10GBASE-T ethernet cabling is limited by crosstalk, particularly when many cables with active links are bundled together. To increase the reach of 10GBASE-T, new Cat-7 cabling is under development with improved electrical shielding and attendant increases in cost, weight, and stiffness. In the meantime, a competing optical ethernet standard, 10GBASE-LRM, offers longer reach and lower power consumption per link.

By contrast, advances in optical technologies have improved the robustness, convenience and cost of optical interconnect. Optical fibres, of course, are immune to crosstalk. New fibres have been developed with improved flexibility and inexpensive optical connectors can now offer high density and easy installation. Compared with copper cabling, optical cabling permits improved airflow for cooling in rack-mounted equipment and their light weight eliminates the mechanical stresses that cause failure in electrical connectors.

The number of links required in data centres and for consumer connectivity far exceeds the number required in past decades for long-haul optical infrastructure. Hence, the trend towards short-reach optical links foretells high volumes for the semiconductor components of optical transceivers. For example, volumes for active optical cables alone are projected to reach 70 million units by 2013[1]. Other growing and emerging applications include FTTx, communication within automobiles and airplanes, and light-on-board interconnect. However, the need to convert electrical signals into light at the transmitter and light into current at the receiver has made it impossible to devise optical transceivers that are entirely integrated in standard CMOS. Transmit lasers are particularly

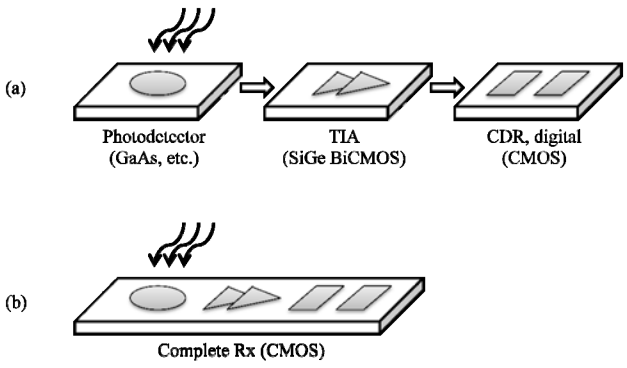

Figure 1. (a) A typical optical receive path solution. (b) A fully-integrated CMOS optical receiver

[1] www.igigroup.com

978-1-4244-5759-5/10/$26.00 ©2010 IEEE

difficult to integrate, and are likely to remain separate components in the foreseeable future. On the receiver side, high-speed photodetectors are the most difficult components to integrate.

A typical optical receiver solution comprises three components, as shown in Fig. 1(a), with a discrete photodetector, BiCMOS transimpedance amplifier (TIA), and finally a CMOS die incorporating a clock and data recovery unit (CDR) and data processing. It is certainly possible to integrate the TIA in CMOS, but the photodetector generally remains discrete. This permits the photodetector to be implemented in an optimized semiconductor material providing high optoelectronic responsivity.

There has been some success integrating the photodetector and TIA in customized manufacturing processes. For example, a SiGe BiCMOS process may be modified to permit the fabrication of PIN photodiodes combining excellent responsivity and bandwidth directly alongside the TIA [16]. A solution with the photodetector implemented on-die with CMOS circuitry is reported in [7] with excellent performance for single-mode fiber links. However, it employs a proprietary process flow and the technology is not easily applied to the multimode or plastic optical fibers most common in short-reach optical applications.

This paper focuses upon the growing body of work on high-speed photodetectors realized in *standard* CMOS processes directly alongside receiver circuitry, as shown in Fig. 1b. This offers the potential for a compact and low cost receiver solution, avoiding the signal integrity challenges and yield losses associated with hybrid integration of the photodetectors and TIA. This paper also considers how these integrated receivers might be implemented in nanoscale CMOS where high-throughput processors may benefit from optical I/O.

II. Background

A. Basics of Photodetection

Photodetection occurs when incident photons are absorbed in a semiconductor, producing an electron-hole pair. The absorption is a stochastic process governed by the Beer-Lambert law; the depth at which each photon is absorbed is a random variable with an exponentially-distributed probability density function (PDF) having a mean penetration depth, d_0. The PDF expressed in terms of the distance below the surface of the semicondurcor, x, is

$$p_d(x) = \frac{e^{-x/d_0}}{d_0}. \quad (1)$$

The mean penetration depth, d_0, depends upon the semiconductor used and the wavelength of light. The most common wavelength (λ) for short-reach optical communication is around 850 nm since low-cost VCSELs can be used as light sources at this wavelength for transmission over multimode fibre. At λ = 850 nm, the most popular semiconductors for use in photodetectors are Ge, GaAs, InGaAs, and InP, which have mean penetration depths in the range of 0.1 to 1.0 μm. By contrast, silicon has a mean penetration depth of d_0 = 18 μm at λ = 850 nm.

Typically, a diode under reverse bias is used to absorb the photons (the photodiode). Electron-hole pairs generated in the intrinsic region of the diode are quickly swept to the diode terminals by the reverse electric field resulting in a reverse current through the diode proportional to the absorbed light intensity.

When a photon is absorbed in a doped region of the photodetector, there is little or no electric field acting on the resulting carriers. They diffuse from areas of greater concentration to areas of lesser concentration at a velocity much slower than carriers swept by an electric field. Some electrons and holes generated in this way recombine within the semiconductor, and therefore do not result in any current at the photodetector terminals. Other carriers do eventually emerge, but the resulting diffusion current persists for microseconds after the initial arrival of a light pulse, resulting in intersymbol interference (ISI) if used for multi-Gbps communication.

Clearly for high-speed operation, it is desirable to ensure that the intrinsic (depleted, high-electric-field) region of the

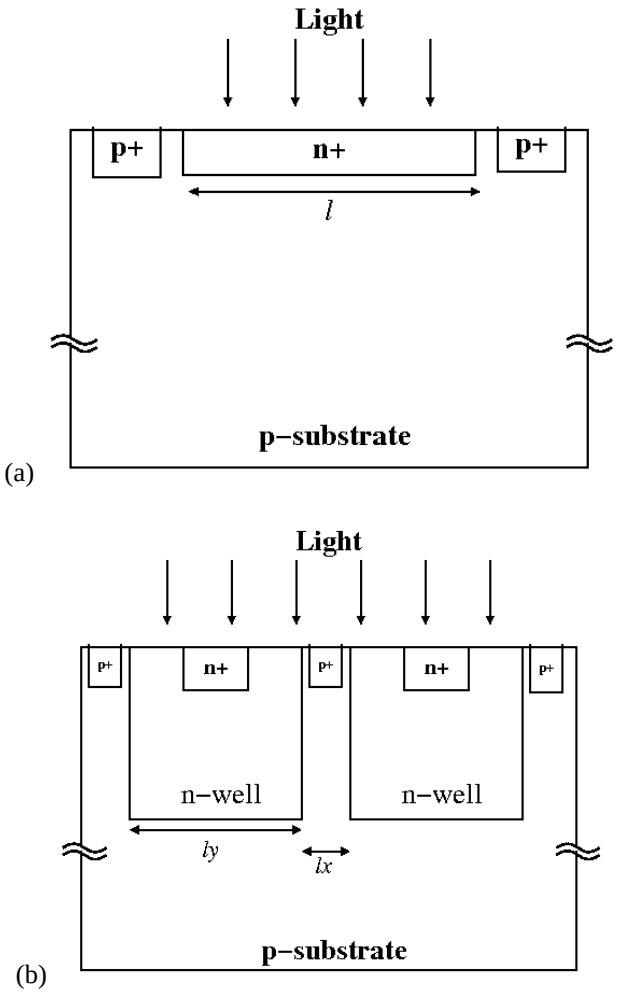

Figure 2. CMOS photodiodes in standard CMOS: (a) n+/p-substrate junction; (b) n-well/p-substrate junction

photodiode coincides with the areas where most charge carriers are generated. If a silicon photodiode is illuminated from above, as shown in Fig. 2, the depletion region must span 10's of μm to satisfy this requirement, which is impossible to achieve in modern standard CMOS processes. Diffusion currents are, therefore, the main speed limitation of CMOS photodetectors.

B. Photodetector Specifications

Doubling the power of incident light doubles the number of photons and the number of electron-hole pairs generated when they are absorbed. Hence, current in the detector, I_{det}, is proportional to incident light power, P_{light}, with a constant of proportionality, R, called the responsivity.

$$I_{det} = R \cdot P_{light} \tag{2}$$

If all photons are absorbed in a detector, each delivering the energy hc/λ and generating a single elementary charge, q, to the detector terminals, its responsivity would be $\lambda q/hc$. The quantum efficiency, η, of a photodiode is the ratio of its measured responsivity and the maximum possible, $(\lambda q/hc) \approx$ 0.7 A/W for 850-nm light.

$$R = \eta \lambda q/hc \tag{3}$$

Commercial photodetectors for 850-nm light made of Ge, GaAs or InP exhibit responsivities in the range of 0.6 – 0.7 A/W. The responsivity of CMOS photodetctors is lower since significant recombination is observed amongst carriers generated in doped regions. Responsivity can be improved significantly, however, if very high reverse bias voltages are applied to the photodiodes so that the depletion regions are large and any photocurrent is amplified by avalanching.

The capacitance of a photodiode, C_{PD}, is also an important consideration for high-speed operation. Again, a wide depletion region is desirable since that provides the lowest possible capacitance.

In summary, the narrow depletion region of pn diodes in standard CMOS generates a relatively high capacitance for high-speed application and is too narrow to capture most incident photons. Carriers that are instead generated in doped regions either recombine reducing dc responsivity, or result in slow diffusion currents that limit bandwidth. These effects are all generally exacerbated in nanoscale CMOS where doping levels in the active devices are high resulting in very narrow depletion regions.

III. CMOS PHOTODETECTORS

A. Simple photodiodes

The most common CMOS photodetector used for high-speed operation is a simple reverse-biased diode. For example, a n+/p-substrate diode may be used as shown in Fig. 2(a). Alternatively, one may use the diode formed between an n-well and the surrounding p-substrate as in Fig. 2(b) (e.g. [2], [3]). Assuming the p-substrate is lightly doped, a wide depletion region is formed. Having a process that incorporates a very lightly-doped p-type epitaxial layer is beneficial since that maximizes the width of the depletion region and, hence, the photocarriers generated within it. Responsivities on the order of 0.3 A/W and photodiode capacitances of approximately 0.5 - 1 pF have been reported in 0.18-μm CMOS for this type of detector using standard supply voltages for biasing [3], [4]. Both responsivity and capacitance are improved by using higher reverse-bias voltages [6].

Since the current comprises a complex combination of drift currents and electron and hole diffusion currents in all three dimensions, its frequency response does not exhibit a first-order -20-dB/decade response. Instead, it exhibits a slow rolloff in the range of 3 – 10 dB/decade [5]. For example, although 3-dB bandwidths on the order of 1 – 10 MHz are typical in 0.18-μm CMOS [3], [4], [5], the relative attenuation at 1 GHz is still a modest 20-30 dB.

The photodiode's cathode and anode must be periodically contacted as shown in Fig. 2. Note that by contacting the diode at frequent intervals (small values of l, l_x, and l_y) the photodiode's intrinsic bandwidth is improved since the series resistances inside the photodiode are minimized. Also, the added junction sidewalls aid in collecting fast photocurrent. In fact, if l or l_x, and l_y is minimized, most of the fast drift current will flow laterally between neighbouring p and n-type regions [11]. However, more of the photodiode surface is then shielded from light by the contacts' metallization reducing responsivity. Hence, layout influences the photodiode's tradeoff between speed and responsivity [4].

B. Shielding diffusion currents

Several techniques are available to reduce the slow diffusion currents arriving at the photodiode terminals; all improve photodiode intrinsic speed at the expense of decreased responsivity. The general approach is to isolate the photodiode junction from the substrate where the slowest diffusing carriers appear.

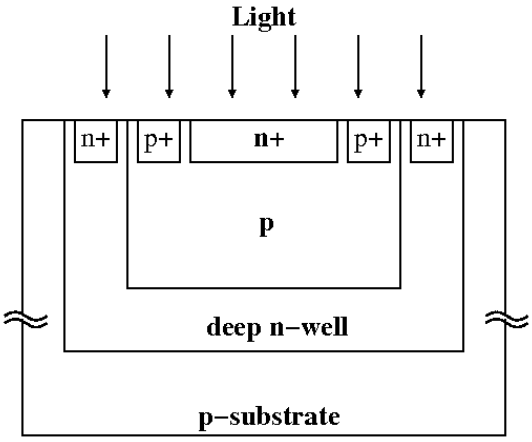

Figure 3. A CMOS npn structure using a buried deep n-well. The n+/p junction near the surface may be used as a photodiode with the deep n-well shielding it from diffusing charge carriers generated by photon absorbtion in the p-substrate. Alternatively it can be used as an npn phototransistor where the base region is not electrically contacted, and photocurrent is amplified by bipolar junction transistor action.

A deep n-well may be used for this purpose, as shown in Fig. 3 [11]. Alternatively, a simple p+/n-well photodiode has been used where the reverse bias between n-well and p-substrate shields the photodiode from carriers generated in the p-substrate [8], [19]. In a CMOS silicon-on-insulator process, the buried oxide provides an effective shield and lateral photodiodes are employed [9], [10]. In all cases, most of the photons (i.e. all those that penetrate more than about 1 - 2 μm) do not result in diode current and responsivity is less than 0.1 A/W.

C. Spatially-modulated light (SML) detector

An alternative approach to mitigating the effect of slow diffusing carriers is the so-called spatially-modulated light (SML) detector [14]. An SML detector is comprised of alternately covered and exposed pn junctions as illustrated in Fig. 4(a). All covered pn junctions are connected in parallel, and so are all exposed junctions. No drift current will arise in the covered photodiode, but carriers absorbed deep in the p-substrate may diffuse in any direction and be collected by either the covered or exposed junctions. The result is that the exposed photodiode conducts both drift and diffusion currents whereas the covered photodiode conducts only diffusion currents. Subtracting the two currents with a differential circuit roughly cancels the slow diffusion currents resulting in a faster response [14]. However, not only is one-half of the incident light reflected away from the photodetector, much of the generated photocurrent is now ignored by subtraction resulting in substatially lower responsivity.

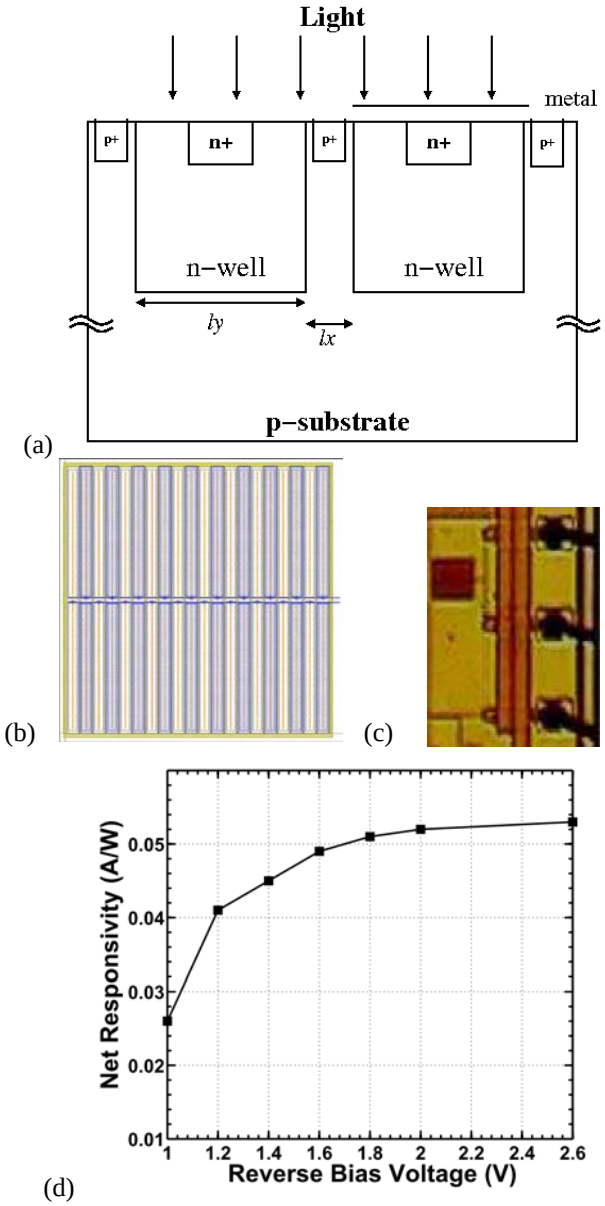

Figure 4. A CMOS SML photodetector: (a) cross-section; (b) layout of a 75 μm × 75 μm detector in 0.18-μm CMOS; (c) prototype photo; (d) measured net responsivity (exposed – covered photodetector) of the fabricated SML detector.

A prototype SML detector layout and die photo are shown in Fig. 4(b) and (c). Metal-1 is used for the diode contacts and metal-2 is used to cover alternating diode fingers. The measured net responsivity (exposed – covered current) is plotted in Fig. 4(d) as a function of reverse bias voltage. At 2-V reverse bias, 0.136 A/W is measured in the exposed photodiode and 0.083 A/W in the covered one for a net responsivity of 0.053 A/W.

The cancellation of the diffusion currents is more precise if the structure has a smaller spatial periodicity (l_x and l_y in Fig. 4(a)). In an effort to optimize the cancellation, a checkerboard pattern of alternating covered/exposed junctions is employed in [13] which, in combination with a very high reverse bias voltage of 14 V, enabled low-BER operation up to 10 Gbps.

D. Phototransistors

Usually used for light sensing applications rather than high-speed communication, phototransistors provide better responsivity than simple photodiodes in a CMOS process. A bipolar junction transistor is exposed to light and photocarriers generated in the base region act as a base current, which is then amplified by the transistor action providing increased responsivity. A npn example is shown in Fig. 3 utilizing a deep n-well. In this case, the p-type base region is not electrically contacted, and a positive bias voltage is applied between collector and emitter. Note that diffusive carriers generated below the deep n-well in the p-substrate are not collected. Alternatively, a pnp device may be formed even when no deep n-well is available. The generally slow speed of BJTs in standard CMOS has led most researchers to forgo this detector in favor of those with higher intrinsic speed, but the responsivity of simple CMOS photodiodes in nanoscale CMOS may be so poor that phototransistors may be needed. A phototransistor is characterized up to high frequencies in 65-nm CMOS later in this paper.

E. Summary

Photodetectors realized in CMOS generally exhibit a tradeoff between responsivity and speed. A simple pn junction exhibits an impulse response with a long tail due to slow diffusive carriers generated deep below the depletion region. The junction may be shielded from below by additional depletion regions or a buried oxide layer. Alternatively, the diffusive currents may be sensed and cancelled as in an SML detector. In both cases, decreased responsivity is the result.

IV. Transimpedance Amplifiers

In the last section, it was shown that high-speed CMOS photodetectors can exhibit responsivities roughly one order of magnitude lower than those of discrete photodetectors and capacitances up to one order of magnitude higher, both of which makes transimpedance amplifier design very difficult.

A few works have employed a regulated cascode input stage to present the photodetector with a very low input impedance [17], but since regulated cascodes introduce additional noise they are more often avoided. Instead, research has focused on developing high-gain shunt-shunt feedback transimpedance amplifiers. In [20], a two-stage amplifier employs negative Miller capacitances to provide high gain and bandwidth. Up to 4 stages have been used to provide the required gain [18].

V. Equalization of CMOS Photodetectors

With the possible exception of SML detectors under extremely high reverse bias voltage [13], photodetectors in standard CMOS processes require equalization to achieve data rates of 5+Gbps. Linear equalization has been applied to both a standard CMOS photodetector [3] and SML detectors [12], [15], [17], [18], [20]. Decision feedback equalization (DFE) will also be considered here.

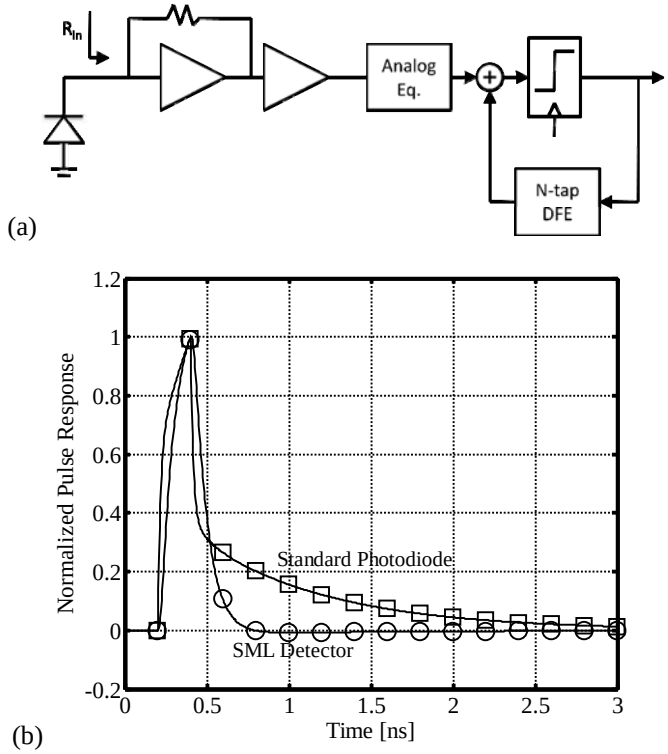

Figure 5. (a) Pulse responses at 5 Gbps for CMOS photodetectors in a 0.18-µm process followed by an analog equalizer: a standard n-well/p-substrate photodiode (squares), and a SML detector (circles).
(b) Receiver model used to evaluate the efficacy of the DFE with CMOS integrated photodetectors.

A. Linear Equalization

Compared to the SML detector, a standard n-well/p-substrate photodetector has much better responsivity. When combined with linear equalization, a receiver with good overall sensitivity is possible (-19 dBm at 3 Gbps in [3]). Since its intrinsic bandwidth is on the order of a few MHz, the equalizer must accurately compensate for the photodiode's response over several decades of frequency to accommodate multi-Gbps operation. This necessitates a high-order equalization filter [3].

On the other hand, SML detectors can exhibit intrinsic bandwidths on the order of 1 GHz. This combined with a high-frequency rolloff of roughly 5 dB/decade suggests that a SML detector's intrinsic bandwidth can be extended to accommodate 5 Gbps operation with only modest equalization. For example, in [20] only a single RC-degenerated stage was used to achieve 5-Gbps operation. In that case, the electrical (RC) bandwidth at the TIA input and the receiver's input-referred noise became the limiting factors – not the photodetector's slow diffusive carriers.

B. Decision Feedback Equalization (DFE)

Rather than using a linear equalizer to provide amplification at frequencies where CMOS photodetectors are providing poor SNR, a DFE can be used to compensate for frequency-dependent losses without noise enhancement. To study the potential for this approach, a standard CMOS n-well/p-substrate photodiode and SML detector in a 0.18-µm CMOS technology are modeled following the approach in [5] and incorporated into the model shown in Fig. 5(a). Shown in Fig. 5(b) are normalized 5-Gbps pulse responses for the standard and SML detectors. For these plots, a TIA input resistance of R_{in} = 160 Ω is assumed, along with C_{PD} = 1 pF for the standard photodiode and C_{PD} = 0.5 pF for the SML detector (since the active area is split between the covered and uncovered photodiodes). Analog equalizers are also included as described above in section V-A. For the standard photodiode, three first-order equalizers were connected in parallel [3]. For the SML detector, a simpler equalizer with 1 zero and 2 poles was assumed [20]. In both cases the pole and zero locations were chosen to provide a maximally-flat overall link response.

The pulse responses in Fig. 5(b) include markers at time intervals of 1 UI at 5 Gbps, for reference. Notice that the ISI is mostly postcursor, and in the case of the standard photodiode persists over many symbol periods. Hence, performance continues to improve steadily as the number of DFE taps is increased. However, for the SML detector with analog equalization, only 1 post-cursor ISI term is significant, increasing to 2 when the data rate is doubled to 10 Gbps. Hence, the data rate can exceed 10 Gbps with only 2 DFE taps. However, the amplitude of the plotted pulse responses are normalized; since SML detectors have inferior dc responsivity, they demand a more sensitive (lower-noise) TIA.

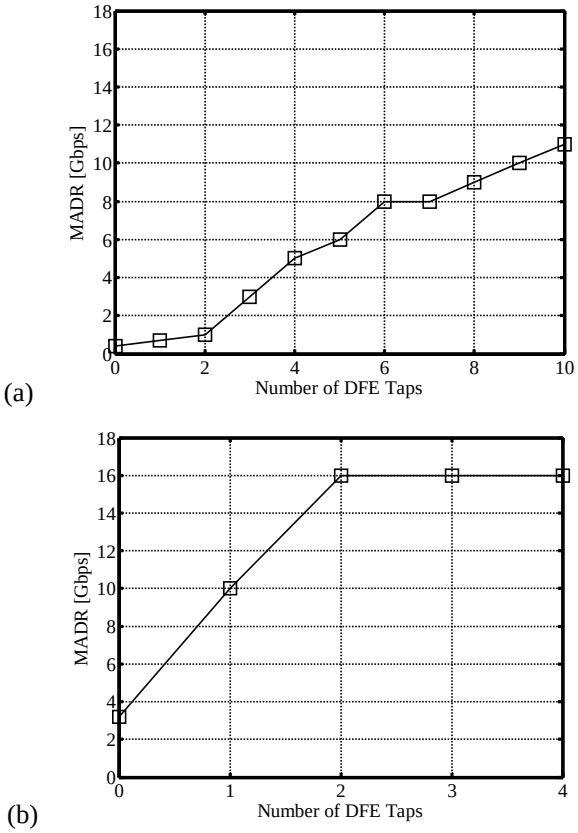

Figure 6. (a) Maximum achievable data rate (MADR) for a n-well/p-substrate photodiode followed by an analog equalizer and DFE. (b) Maximum achievable data rate (MADR) for a SML photodetector followed by an analog equalizer and DFE.

The maximum achievable data rate (MADR)[2] is plotted in Fig. 6(a) and (b) for the standard and SML detectors respectively when followed by a DFE with a varying number of taps. Since the standard photodiode has a longer pulse response, more taps are required to effect a significant improvement. A SML detector, on the other hand, has the potential operate above 10 Gbps with only a few taps of DFE, although at lower sensitivities.

VI. 65NM CMOS PHOTODETECTOR CHARACTERIZATION

In a constant-field scaling regime [21], it is clear that distinct advantages are offered by photodetectors in *larger* feature-size CMOS processes. Higher supply voltages and lower doping levels give rise to wider depletion regions, increasing responsivity and decreasing junction capacitance. Hence, photodetectors in finer feature-size CMOS processes require TIAs with more gain, lower input resistance, and lower input-referred noise. As a result, extensive work has been done on CMOS photodetectors in technologies ranging from 0.8-μm to 0.13-μm CMOS, and little work has been done in sub-100-nm CMOS. However, in sub-100-nm nodes, doping profiles are more complex, supply voltage scaling is muted, and the trends are less evident. Moreover, integrated optical receivers may prove very useful in nanoscale CMOS where systems are often limited by I/O bandwidth.

[2] The MADR is the data rate at which data dependent jitter (DDJ) for a PRBS (2^7-1) pattern after application of the DFE is 0.3 UI_{pp}. DDJ is determined in the presence of the DFE by sweeping receiver sampling phase with constant tap weights.

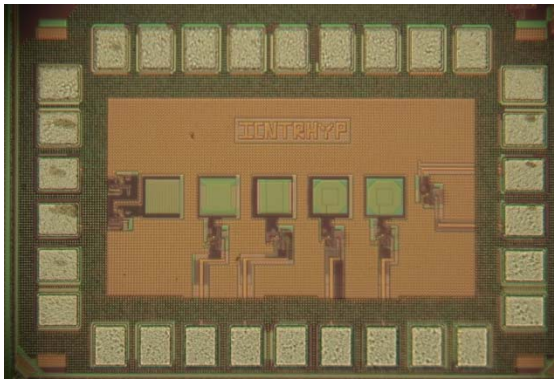

Figure 7. CMOS photodetector array in a standard 65-nm CMOS process.

A test chip was developed to characterize the performance of photodetectors in a 65-nm CMOS technology. A die photo is shown in Fig. 7. Two types of phtodiodes were tested, both 60 μm x 60 μm in size: a simple n+/p-substrate photodiode, as shown in Fig. 2(a), and a phototransistor as in Fig. 3.

A. Measurements

In order to more accurately measure the responsivity and frequency response of the integrated photodetectors, an amplifier and 50-Ohm buffer is integrated alongside the test structures. An overall block diagram and schematic of the measurement circuit is shown in Fig. 8. All measurements were made with a supply voltage of 1.3V resulting in a photodetector reverse bias voltage of 670 mV.

An electrical test of the entire amplifier chain was performed so that its gain could be deembedded from the photodetector measurements. Its design is simple and not optimized for low power. It comprises a common source first stage with shunt-shunt feedback to provide a low input impedance, three more common-source stages for more gain, and finally a 50-Ohm output buffer to interface with test equipment. A dc transimpedance gain of 1kOhm a 3-dB bandwidth of 2GHz were measured. Since this bandwidth far exceeds that of the measured photodetectors, a flat magnitude response was assumed when plotting the frequency response.

Measurement results from the standard n+/p-substrate photodiode are plotted in Fig. 9. A dc responsivity of just over 0.03 A/W, a 3-dB bandwidth of 2.5 MHz and a high-frequency rolloff of 5 dB/decade are observed. Measurements of the 65-nm npn (n+/p-tub/deep n-well) phototransistor are shown in Fig. 10. It exhibits of 3-dB bandwidth of only 150 kHz and a rolloff of 9 dB/decade, but an impressive dc responsivity of 0.34 A/W, comparable to the very best obtained from any CMOS high-speed photodetectors. Hence, if the improved transistor speed available in 65-nm CMOS can be leveraged to provide better equalization, multi-Gbps operation should be possible using either photodetector. A summary of the results is provided in Table I.

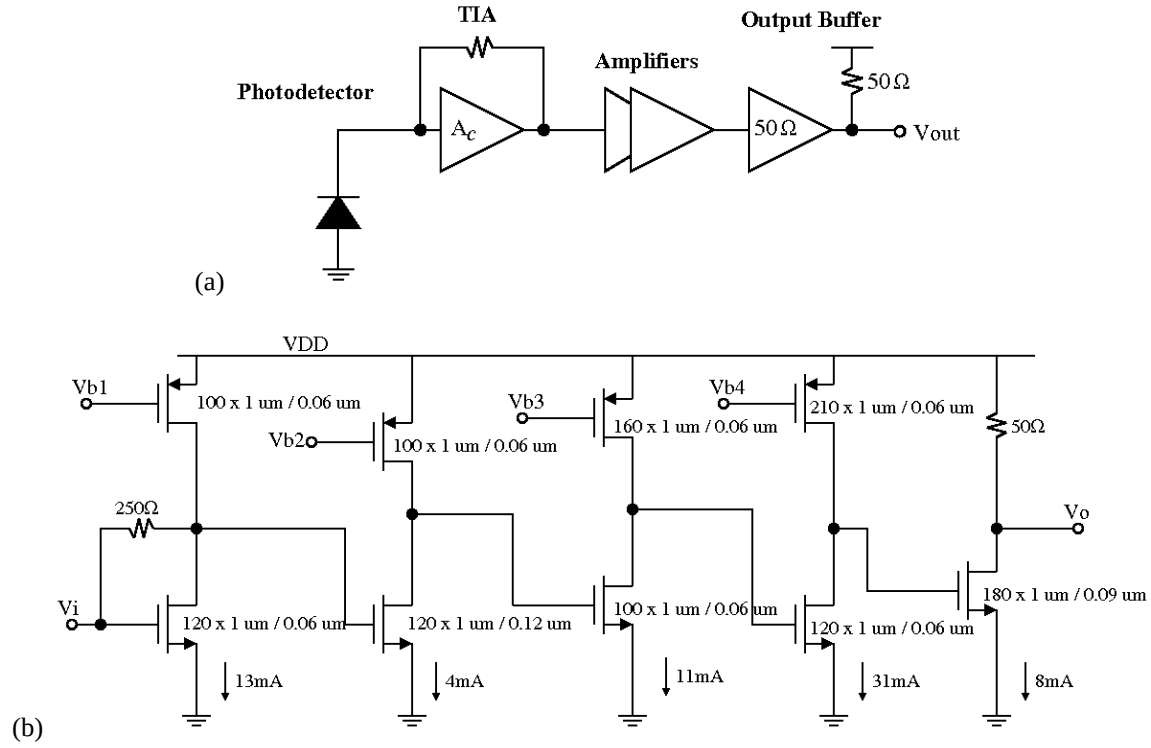

Figure 8. Prototype 65-nm CMOS photodetectors and measurement circuitry: (a) block diagram; (b) schematic.

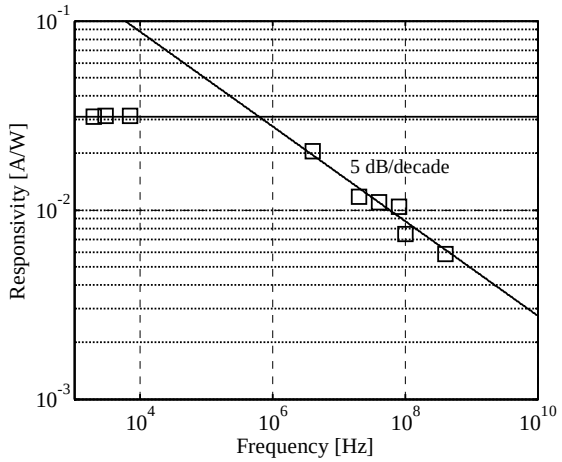

Figure 9. Characterization of a n+/p-substrate photodetector in 65-nm CMOS.

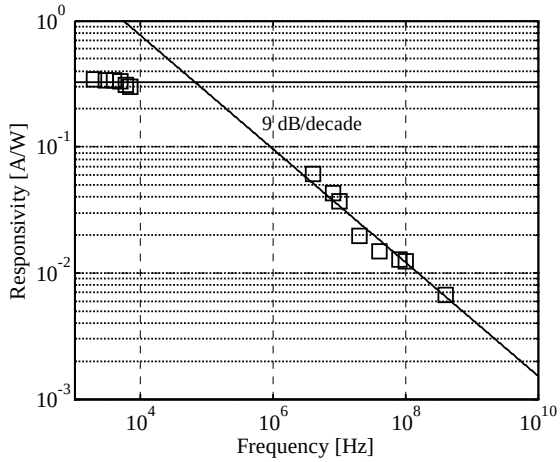

Figure 10. Characterization of a n+/p-tub/deep n-well npn phototransistor in 65-nm CMOS.

VII. Conclusions

Although sophisticated equalization is now commonplace in other wireline receivers, so far only linear equalization has been used to combat the intrinsic bandwidth limitations of CMOS photodetectors. Decision feedback equalization offers potential for significantly higher data rates. Implementing such a receiver in nanoscale CMOS may require new photodetector structures, such as phototransistors, to provide reasonable responsivity.

TABLE I. Summary of 65-nm CMOS Photodetector Measurements

Photodetector	DC Responsivity [A/W]	3-dB Bandwidth [MHz]	Rolloff
n+/p-substrate photodiode	0.03	2.5	5 dB/dec
n+/p-tub/deep n-well phototransistor	0.34	0.15	9 dB/dec

REFERENCES

[1] Savage, N.; , "Linking with light [high-speed optical interconnects]," *Spectrum, IEEE* , vol.39, no.8, pp. 32- 36, Aug 2002.

[2] Hermans, C.; Leroux, P.; Steyaert, M.; , "Two high-speed optical front-ends with integrated photodiodes in standard 0.18 μm CMOS," *European Solid-State Circuits Conference*, pp. 275- 278, Sept. 2004.

[3] Radovanovic, S.; Annema, A.-J.; Nauta, B.; , "A 3-Gb/s optical detector in standard CMOS for 850-nm optical communication," *Solid-State Circuits, IEEE Journal of* , vol.40, no.8, pp. 1706- 1717, Aug. 2005.

[4] C. Hermans and M. Steyaert, *Broadband Opto-Electrical Receivers in Standard CMOS*, Springer, 2007.

[5] Genoe, J.; Coppee, D.; Stiens, J.H.; Vonekx, R.A.; Kuijk, M.; , "Calculation of the current response of the spatially modulated light CMOS detector," *Electron Devices, IEEE Transactions on* , vol.48, no.9, pp.1892-1902, Sep 2001.

[6] W.-K. Huang, Y.-C. Liu, and Y.-M. Hsin, "Bandwidth enhancement in Si photodiode by eliminating slow diffusion photocarriers," *Electronics Letters*, vol. 44, no. 1, pp. 52–53, 3 2008.

[7] D. Kucharski, D. Guckenberger, G. Masini, S. Abdalla, J. Witzens, S. Sahni, "10Gb/s 15mW Optical Receiver with Integrated Germanium Photodetector and Hybrid Inductor Peaking in 0.13mm SOI CMOS Technology," *Int. Solid-State Circ. Conf.*, pp. 360-361, Feb. 2010.

[8] Lim, P.J.-W.; Tzeng, A.Y.C.; Chuang, H.L.; St. Onge, S.A.; , "A 3.3-V monolithic photodetector/CMOS-preamplifier for 531 Mb/s optical data link applications," *Solid-State Circuits Conference, 1993. Digest of Technical Papers. 40th ISSCC., 1993 IEEE International* , vol., no., pp.96-97, 268, 24-26 Feb 1993.

[9] Ghioni, M.; Zappa, F.; Kesan, V.P.; Warnock, J.; , "A VLSI-compatible high-speed silicon photodetector for optical data link applications," *Electron Devices, IEEE Transactions on* , vol.43, no.7, pp.1054-1060, Jul 1996.

[10] Csutak, S.M.; Schaub, J.D.; Wu, W.E.; Campbell, J.C.; , "High-speed monolithically integrated silicon optical receiver fabricated in 130-nm CMOS technology," *Photonics Technology Letters, IEEE* , vol.14, no.4, pp.516-518, Apr 2002.

[11] Wei-Zen Chen; Shih-Hao Huang; , "A 2.5 Gbps CMOS Fully Integrated Optical Receicer with Lateral PIN Detector," *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE* , vol., no., pp.293-296, 16-19 Sept. 2007.

[12] Wei-Zen Chen; Shih-Hao Huang; Guo-Wei Wu; Chuan-Chang Liu; Yang-Tung Huang; Chin-Fong Chin; Wen-Hsu Chang; Ying-Zong Juang; , "A 3.125 Gbps CMOS fully integrated optical receiver with adaptive analog equalizer," *Solid-State Circuits Conference, 2007. ASSCC '07. IEEE Asian* , vol., no., pp.396-399, 12-14 Nov. 2007.

[13] Shih-Hao Huang; Wei-Zen Chen; , "A 10-Gbps CMOS single chip optical receiver with 2-D meshed spatially-modulated light detector," *Custom Integrated Circuits Conference, 2009. CICC '09. IEEE* , vol., no., pp.129-132, 13-16 Sept. 2009.

[14] Kuijk, M.; Coppee, D.; Vounckx, R.; , "Spatially modulated light detector in CMOS with sense-amplifier receiver operating at 180 Mb/s for optical data link applications and parallel optical interconnects between chips," *IEEE Journal of Selected Topics in Quantum Electronics,* , vol.4, no.6, pp.1040-1045, Nov/Dec 1998.

[15] Hermans, C.; Tavernier, F.; Steyaert, M.; , "A Gigabit Optical Receiver with Monolithically Integrated Photodiode in 0.18 μm CMOS," *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European* , vol., no., pp.476-479, 19-21 Sept. 2006.

[16] Swoboda, R.; Zimmermann, H.; , "11Gb/s monolithically integrated silicon optical receiver for 850nm wavelength," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International* , vol., no., pp.904-911, 6-9 Feb. 2006.

[17] Lee, Dongmyung; Han, Jungwon; Chang, Eunsoo; Han, Gunhee; Park, Sung Min; , "An 8.5Gb/s CMOS OEIC with on-chip photodiode for short-distance optical communications," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* , vol., no., pp.362-363, 7-11 Feb. 2010.

[18] Tavernier, F.; Steyaert, M.S.J.; , "High-Speed Optical Receivers With Integrated Photodiode in 130 nm CMOS," *Solid-State Circuits, IEEE Journal of* , vol.44, no.10, pp.2856-2867, Oct. 2009.

[19] Woodward, T.K.; Krishnamoorthy, A.V.; , "1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies," *Selected Topics in Quantum Electronics, IEEE Journal of* , vol.5, no.2, pp.146-156, Mar/Apr 1999.

[20] T. Shuo-Chun Kao and A. Chan Carusone, "A 5-Gbps Optical Receiver with Monolithically Integrated Photodetector in 0.18-um CMOS," *IEEE RFIC Symposium*, Boston, MA, June 2009.

[21] R. Dennard, et al., "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE Journal of Solid State Circuits*, pp. 256-268, Oct. 1974.