A 32/16 Gb/s 4/2-PAM Transmitter with PWM Pre-Emphasis and 1.2 Vpp per side Output Swing in 0.13-μm CMOS

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***Abstract*– A dual-mode 4/2-PAM transmitter is described that extends pulse-width modulated pre-emphasis to data rates of 16 Gb/s and 32 Gb/s in 2-PAM and 4-PAM modes respectively. Implemented in a 0.13-μm CMOS process to accommodate the wide output swing of 1.2 Vpp per side, the transmitter compensates for 30 dB and 9 dB of loss at one-half the symbol rate in 2-PAM and 4-PAM modes respectively.**

I. INTRODUCTION

This paper describes a CMOS transmitter for high-loss wireline channels at data rates exceeding 10-Gb/s. In general, these losses may be combated by equalization and, in severe cases, through the use of 4-level Pulse Amplitude Modulation (4-PAM). Ultimately, large output swing is also required for high-loss channels. This transmitter combines wide output swing (1.2 Vpp per side) with large loss compensation (up to 30-dB at one-half the symbol rate) and the option to operate in 4-PAM mode at 16 GSymbols/s. The state-of-the-art in transmit equalization for multi-Gb/s electrical wireline links is described in [1] where a Pulse-Width Modulation Pre-Emphasis (PWM-PE) technique is used to achieve low-BER operation at 5 Gb/s over a cable with 33-dB loss at 2.5 GHz. However, with an output swing of 600 mVpp only approximately 15 mV of eye opening remained at the receiver-end of the cable. In an attempt to increase the eye opening, the output swing was increased to 1.8 Vpp per side in [2] but the performance at 5 Gb/s suffered considerably. In this paper, a high-speed Current Mode Logic (CML) implementation extends PWM-PE to 16-Gb/s for binary (2-PAM) signals with an output swing of 1.2 Vpp per side providing approximately 30 mV of eye opening after a cable with over 30 dB of loss at one-half the symbol rate.

Furthermore, in this work the PWM-PE technique is applied for the first time to 4-PAM signals. 4-PAM transmitters require particularly accurate Inter-Symbol Interference (ISI)-cancelation due to their reduced level-spacing. To ensure ample eye opening at the receiver, 4-PAM transmitters generally require many Finite Impulse Response (FIR) pre-emphasis taps. For example, 4 taps of pre-emphasis with 500-mVpp swing per side were used in a 4-PAM 25-Gb/s transmitter to compensate for approximately 3 dB of loss at one-half the symbol rate [3]. To compensate for 14.5 dB of loss in a 4-PAM 24-Gb/s transmitter, the pre-emphasis filter length was increased to 13 taps and the output swing increased to 800 mVpp per side [4]. All of

these tap weights must be accurately optimized to ensure the received 4-PAM eye patterns are open. In this work, by adjusting only one pre-emphasis parameter, up to 9 dB of loss is compensated at one-half the symbol rate for a 32-Gb/s 4-PAM link.

II. PRE-EMPHASIS

In order to reduce ISI at the receiver input, the overall frequency response of the transmitter and channel should be as flat as possible up to at least one-half of the symbol rate. Pre-emphasis at the transmitter generally attenuates the low-frequency content of the signal, in order to flatten the overall response.

Pre-emphasis based on Pulse-Width Modulation (PWM), as proposed in [2], has the following pulse response:

$$
p_{\text{PWM}}(t) = \begin{cases} 0 & t < 0 \\ 1 & 0 \le t < d \cdot T_s \\ -1 & d \cdot T_s \le t < T_s \\ 0 & t \ge T_s \end{cases}
$$

The PWM-PE pulse response spans only one unit interval and its low-frequency attenuation is controlled by varying its duty cycle, the parameter d ($0.5 \le d \le 1$).

Similarly, a 2-tap Finite Impulse Response Pre-Emphasis (FIR-PE) transmitter has only one adjustable parameter (assuming the peak output level is constrained). Its output pulse response is,

$$
p_{\text{FIR}}(t) = \begin{cases} 0 & t < 0 \\ r & 0 \le t < T_s \\ r - 1 & T_s \le t < 2 \cdot T_s \\ 0 & t \ge 2 \cdot T_s \end{cases}
$$

The pulse response spans two Unit Interval (UI) with the amount of pre-emphasis controlled by the parameter r ($0.5 \le r \le 1$). However, PWM-PE provides a better match to the inverse of the channel response for electrical wireline links dominated by skin effect losses.

A channel comprising a total of 36 meters of coaxial cable and six connectors was characterized using a Vector Network Analyzer (VNA). The measured channel response is shown as triangular markers in Fig. 1. A model of the cable including skin-effect and dielectric losses was fitted to the measurements and is plotted as the dashed line in Fig. 1. Both the 2-tap FIR and PWM pulses were optimized and the resulting combined pre-emphasis pulse and channel responses are also plotted in Fig.

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1. The overall frequency response of the PWM-PE matches the inverse of the channel loss curve more closely, resulting in an overall flatter response and subsequently less ISI. However, note that the flattened response has an attenuation of roughly 30 dB from dc to 10 GHz. Hence, the transmitter requires a wide output swing of 1.2 Vpp to ensure reasonable eye amplitude. Fig. 2 shows the simulated eye diagram at the receiver for a PWM-PE transmitter with a duty-cycle of $d = 0.52$ and swing of 1.2 Vpp per side.
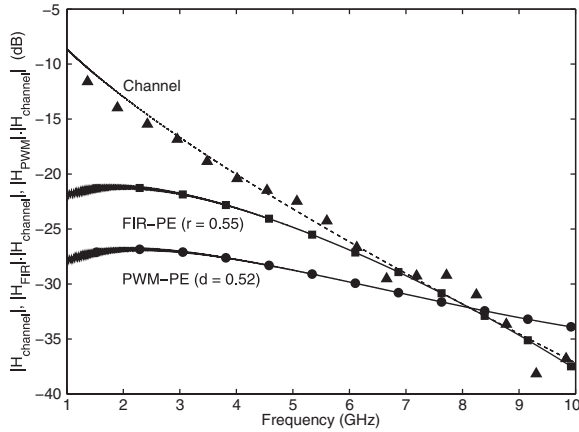

Fig. 1. Channel characterization and combined pre-emphasis pulses with channel frequency responses.

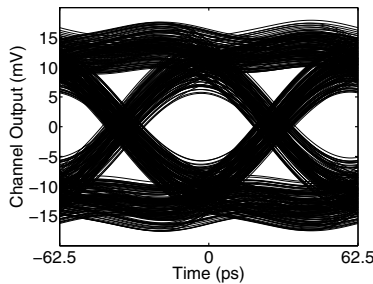Fig. 2. System-level simulation eye diagram of channel output with PWM-PE (52% duty-cycle) and transmitter output 1.2 Vpp per side.

Although previously only applied to binary signals, PWM-PE is a linear operation and, hence, can be applied to a 4-PAM system. The corresponding 4-PAM symbol pulse shapes are shown in Fig. 3, assuming a Gray line code.
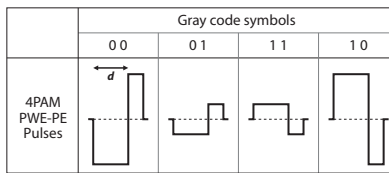

Fig. 3. Output pulses of the Gray-coded 4-PAM transmitter with PWM-PE.

III. SYSTEM-LEVEL DESIGN

A 0.13-μm CMOS process was chosen because its drain-source breakdown voltage of 1.6 V, can accommodate the 1.2

Vpp per side output swing. However, achieving the required speed in 0.13-μm CMOS was a significant challenge.

A. System Architecture

Fig. 4 illustrates a functional block diagram of the transmitter. When operating in 4-PAM mode at the maximum data rate of 32Gb/s, two single-ended data inputs at 16 Gb/s are translated into a three-bit thermometer code through a Gray encoder. The single-ended clock input at 16 GHz passes through several buffers and the Duty Cycle Control (DCC) circuit to generate a differential PWM clock. The PWM clock and the three encoded data streams combine at XOR gates to create three equally-weighted binary PWM data streams. These are combined at the output stage to create a 4-PAM output signal at 16 GSymbol/s. When operating in 2-PAM mode, the input Least Significant Bit (LSB) is connected to ground and a full-rate binary signal is applied to the Most Significant Bit (MSB) input. The Gray coding ensures a full-swing output. All logic was implemented with CML.
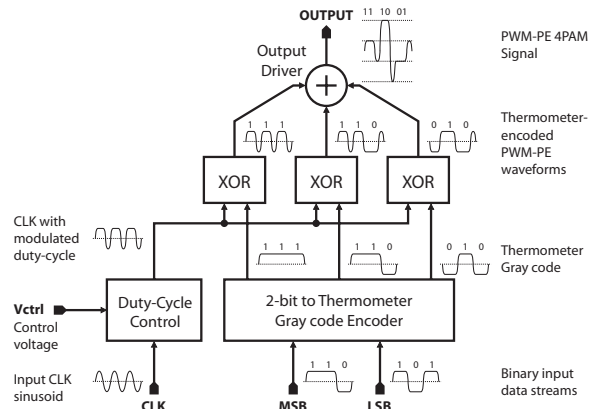

Fig. 4. Functional block diagram of transmitter system architecture.

IV. CIRCUIT DESIGN

A. Current Mode Logic (CML) Design

A good understanding of CMOS CML design was essential to achieving the required speed in 0.13-μm CMOS. It was found that by biasing the differential pair transistors with high current densities and relaxing the full-switching criterion usually enforced in CML design, higher operating speed can be achieved. Specifically, approximately 5% to 10% of the total tail current continues to flow through the "off" branch of all CML buffers, providing approximately a 48% increase in the logic's maximum switching speed. In addition, very low fanout had to be maintained to reduce the capacitive load on each CML stage. Moreover, in CML stages where high self-loading exists, such as the DCC circuit and XOR gates, inverse scaling (i.e. a fanout less than unity) is used [5]. All CML gates employ inductive peaking and operate from a 1.8-V supply.

B. Duty Cycle Control (DCC)

The DCC schematic is shown in Fig. 5. The differential offset inputs, $V_{offset+}$ and $V_{offset-}$, are derived from a single control voltage (not shown). The resulting dc offset current adjusts the duty-cycle of the differential clock. The output duty-cycle ranges from 50% to 75%. PWM-PE can be turned off for

low loss channels by terminating the single-ended clock input and full-switching of dc offset differential pair resulting in standard Non-Return-to-Zero (NRZ) 4/2-PAM transmitted symbols. Note the use of inverse scaling at the DCC output due to its high capacitive self-load. A fanout ratio of only 0.36 is required to maintain sufficient bandwidth there, followed by several fanout-of-1 high-gain stages to generate a clean PWM clock.
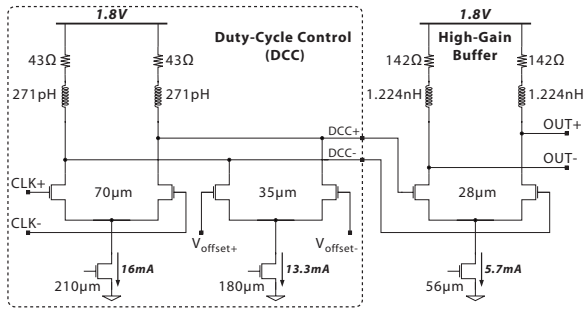

Fig. 5. Schematic of DCC stage.

C. Output Driver

A cascode topology is chosen for the output stage to provide wide swing. Fig. 6 illustrates the schematic. It operates from a separate 3-V power supply. The cascode devices shield the input differential pairs from excessive drain-source voltages and reduce the input Miller capacitance. Standard 0.13-μm NFETs with minimal gate lengths are used throughout. The output driver is designed to provide a return loss of better than -10 dB in either 75-Ω or 50-Ω environments. Bias-tees provide ac-coupling to test equipment while presenting the output with the expected dc load. It is possible to reduce the transmitter output swing for low loss channels to a minimum of 400 mVpp per side by adjusting the output stage tail currents.
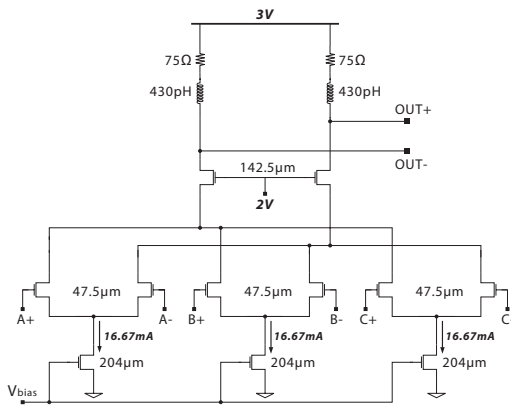

Fig. 6. Schematic of output driver.

V. EXPERIMENTAL RESULTS

The prototype transmitter integrates 165 spiral inductors and 80 CML gates into a die area of 1.71mm × 1.83mm in a 0.13-μm CMOS technology. Fig. 7 is a die photo of the transmitter. All measurements were performed on-die.

The transmitter draws a total power of 1.578 W from the two power supplies. The output driver consumes 147 mW of power
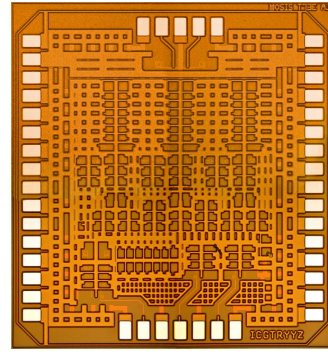

Fig. 7. Die photo of transmitter.

from 3-V power supply. The remaining 1.43 W is consumed from the 1.8-V supply, of which 35% is consumed by the clock distribution, 37% by the encoder, and the rest for the generation and buffering of the PWM-PE data. For applications that call for a lower output swing, the same architecture can be implemented in a more advanced CMOS technology (with lower drain-source breakdown voltages) permitting the use of fewer stages of higher fanout buffers and lower supply voltages, thus resulting in a large power savings.

To characterize the channel loss compensation in 2-PAM mode of operation, the same 36-meter coaxial cable channel (as shown in Fig. 1) is used. Fig. 8a illustrates the transmitter output with 53.2% duty-cycle. The corresponding channel output eye diagram is shown in Fig. 8b and has an eye amplitude of approximately 30 mV, which agrees with the simulated eye diagram shown in Fig. 2. After 2×10^7 measurements, the oscilloscope extrapolated a Bit-Error Rate (BER) of better than 10^{-12} with approximately 0.25 UI margin at the channel output.

In 4-PAM mode, its maximum data rate is 32 Gb/s. The test channel comprises six sections of 1-meter coaxial cables with associated connectors has a loss of 8.9 dB at half the symbol rate (8 GHz) and 17.2 dB at half the bit rate (16 GHz). By manually adjusting the duty-cycle of the transmit pulse, and thus the amount of pre-emphasis, it is possible to obtain an open eye at the output of the channel. Fig. 9a illustrates the transmitter 4-PAM output with 64% duty-cycle. The corresponding channel output eye diagram is shown in Fig. 9b. The 4-PAM eye opening is approximately 30 mV at the output of the channel.

VI. CONCLUSIONS

Table I compares this work with current state-of-the-art CMOS binary transmitters. It compares favorably in terms of loss compensation, output swing, and speed. A comparison with published CMOS 4-PAM transmitters is provided in Table II. This transmitter is the first of its kind to incorporate PWM-PE in 4-PAM in addition to being the fastest implementation in CMOS reported to date. The capability to switch between 4-PAM and 2-PAM, adjustable pre-emphasis (50%–75% duty-cycle, or NRZ), and adjustable output amplitude makes it suitable for use in a wide range of electrical wireline links.

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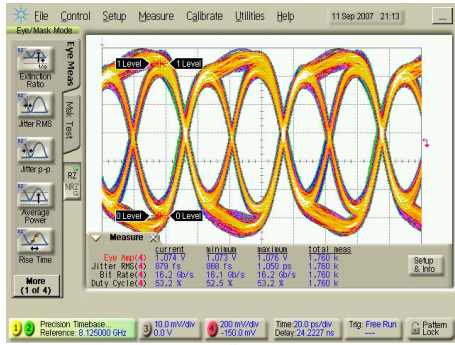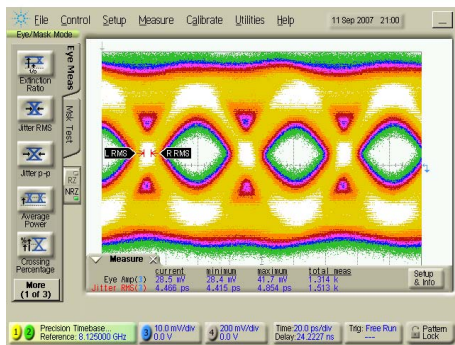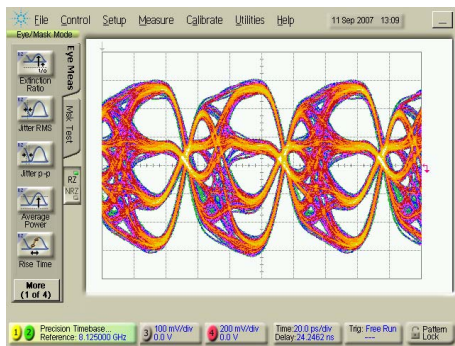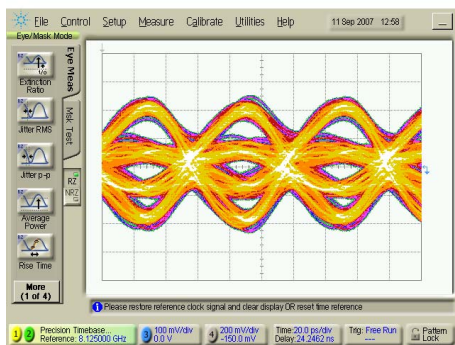
Fig. 8. Eye diagrams of 2-PAM mode pre-emphasis experiment: (a) Transmitter output; 53.2% duty-cycle and (b) Channel output.

Fig. 9. Eye diagrams of 4-PAM mode pre-emphasis experiment: (a) Transmitter output; 64% duty-cycle and (b) Channel output.

TABLE I
COMPARSION OF 2-PAM TRANSMITTERS

	CMOS Process	Output Swing (mV)	Data Rate (Gb/s)	Loss Compensation (dB)	Power (mW)
[6]	0.13-μm	260	40	-	~2700
[7]	0.13-μm	350	30	-	150
[8]	0.18-μm	4000	13.6	-	600
[1]	0.13-μm	600	5	31 (@ 2.5GHz)	110
[2]	90-nm	700	4	22 (@ 1.25GHz)	-
This work	0.13-μm	1250	16	30.3 (@ 8 GHz)	1578

TABLE II
COMPARSION OF 4-PAM TRANSMITTERS

	CMOS Process	Output Swing (mV)	Data Rate (Gb/s)	Loss Compensation (dB)	Power (mW)
[3]	90-nm SOI	520	25	3 (@ 6.25GHz)	101.8
[4]	90-nm	800	24	14.5 (@ 6GHz)	510
[9]	0.18-μm	600	10	-	120
[10]	0.25-μm	600	10	3.7 (@ 2.5GHz)	222
[11]	0.4-μm	1100	10	-	1000
This work	0.13-μm	1250	32	8.9 (@ 8 GHz)	1578

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