A 40 Gb/s Transversal Filter in 0.18 μm CMOS Using Distributed Amplifiers

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Abstract— **This paper describes a fully-differential 3-tap transversal filter in 0.18 μm CMOS capable of equalizing NRZ data up to 40 Gb/s. Each tap gain comprises a cascade of two distributed amplifiers with adjustable gain. Passive-LC delay lines in the distributed amplifiers also provide the 25 ps tap delays. The design is 1 mm × 1 mm (900 μm × 600 μm active area) and consumes up to 70 mW from a 1.8 V supply depending on the tap gains. It is the first reported CMOS transversal filter operating at 40 Gb/s.**

I. INTRODUCTION

In this paper, a new circuit architecture is described that combines distributed amplification with traveling wave finite impulse response (FIR) filtering to extend the bandwidth of these filters. FIR filters with programmable tap gains are essential building blocks in many high speed integrated circuits. They are used on their own as linear equalizers or as part of a decision feedback equalizer to compensate intersymbol interference in optical fibre [1] and chip-to-chip links [2].

Previous implementations at data rates of 10+ Gb/s generally operate in continuous-time using a traveling wave filter (TWF) architecture. For instance, [1] and [2] report programmable FIR filters at data rates up to 49 Gb/s in InP/InGaAs and SiGe technologies, each consuming several hundred mW. At 10 Gb/s, TWFs have been implemented with much lower power consumption including a 7 tap (50 ps tap spacing) design in 0.18 μm SiGe BiCMOS consuming 40 mW [3] and a 4 tap equalizer with 33 ps tap spacing in 0.18 μm CMOS consuming only 7.3 mW [4]. Other circuit blocks for 40 Gb/s systems have been demonstrated in 0.18 μm CMOS [5], [6], [7], but no equalizers for these applications have been demonstrated in any similar technology.

In [8], a 30 Gb/s equalizer in 90 nm CMOS was presented, making use of a crossover topology to extend the bandwidth of each tap in the FIR filter by a factor of two. In this work, the taps' bandwidth is further increased by implementing each as a cascade of two distributed amplifiers. The same passive-LC delay line is used for the TWF and the distributed tap amplifiers. This new architecture, referred to as a "folded-cascade TWF", enables equalization at 40 Gb/s in a 0.18 μm CMOS process that has a maximum f_t of only 45 GHz. The filter is 4× faster than previously reported equalizers in similar technologies.

The remainder of this paper is organized as follows: Section II of this paper describes the folded-cascade TWF in relation to a traditional TWF; Section III describes an integrated implementation of the folded-cascade TWF; and Section IV summarizes prototype test results.

II. TRAVELING WAVE FILTERS IN CMOS

The basic TWF design uses transmission lines as passive continuous-time delay elements. To achieve the delays required for a 40 Gb/s equalizer, a microstrip, stripline or coplanar transmission
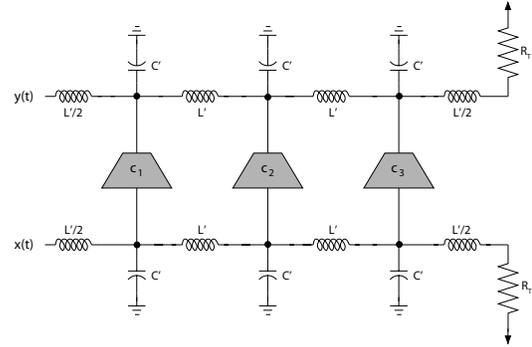

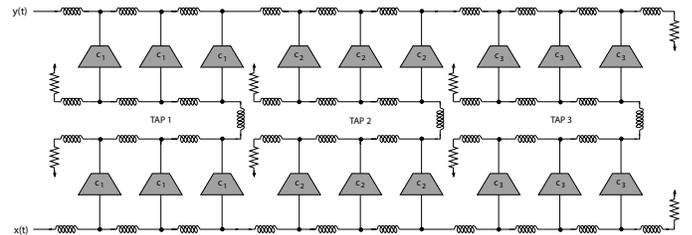Fig. 1.   A conventional 3-tap FIR traveling wave filter (TWF) using artificial transmission lines.

Fig. 2.   3-tap FIR filter using the folded-cascade TWF topology.

line must be very long (on the order of several millimeters). As a result, the size of the equalizer IC can become prohibitively large. In addition, long transmission lines introduce significant series loss.

To combat these problems, often artificial transmission lines made up of lumped inductors and capacitors are used. By winding the transmission line into spiral inductors, the inductance per unit length is greatly increased because of the mutual inductance between adjacent windings. Thus, the overall wire-length is decreased, reducing the chip area as well as any resistive losses.

A conventional 3-tap TWF is shown in Figure 1. The input and output transmission lines must have a characteristic impedance matched to the system impedance, $Z_0 = \sqrt{L'/C'}$, where L' is the value of the lumped spiral inductors and C' is the total capacitance at each internal node comprising mostly the tap amplifiers' input capacitance. Since larger devices are required to increase the gain in each tap amplifier, each node capacitance C' is proportional to the maximum tap gain.

The tap spacing is also determined by the size of the lumped LC elements, $\tau = 2\sqrt{L'C'}$. The 3-dB bandwidth of a lumped LC transmission line section is equal to $f_{3dB} = 1/\pi\sqrt{L'C'}$. Therefore, the tap spacing and bandwidth of a conventional TWF are inversely
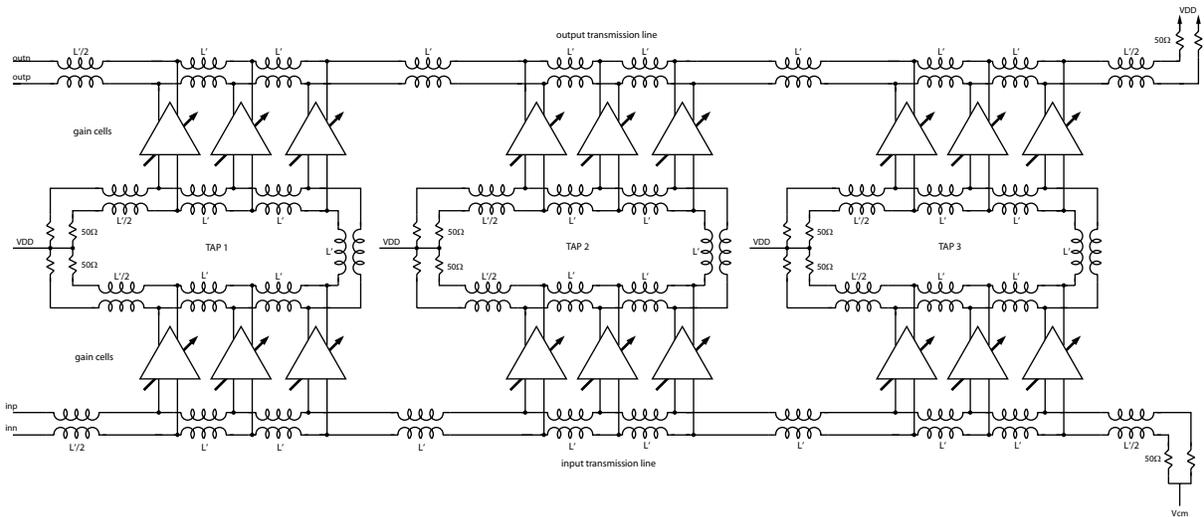
Fig. 3. Symbolic top-level schematic of the fabricated FIR filter.

related,

$$f_{3\text{dB}} = \frac{2}{\pi \tau} \tag{1}$$

The crossover TWF topology in [8] is a slightly modified version of the TWF topology, using a 6-section transmission line to implement a 3-tap filter. Since twice as many sections are used, to keep the same delay per tap the inductances L' and capacitances C' per section are halved. Hence, the bandwidth of this architecture is expected to be $2\times$ greater than a traditional TWF having the same tap spacing and tap gain. Unfortunately, it is not practical to decrease the lumpiness of the transmission lines by a factor greater than 2 using the crossover TWF topology. If 3 or more amplifiers per tap were used, the crossover routing would introduce mismatch and skew between the paths of different lengths.

Instead, we introduce the folded-cascade TWF topology, shown in Figure 2 for a 3-tap filter. In this example, each tap delay is divided into 3 series LC sections. Hence, the lumped inductances and capacitances have been reduced by a factor of 3 compared with the conventional topology. Each tap is essentially a cascade of two distributed amplifiers. The input and output delay lines also serve as the transmission lines for the distributed amplifiers.

This topology is not without certain drawbacks. First, because it requires two cascaded stages per tap, the power requirement is basically doubled. Also, distributed amplifiers generally have more group delay variation than lumped amplifiers, and cascading them increases this variation. Careful design is required to ensure that the group delay performance is acceptable.

III. PROTOTYPE CIRCUIT DESIGN

A block diagram of the entire fabricated circuit is shown in Figure 3. It is essentially a fully-differential version of Figure 2 with programmable tap gains designed for use with a 100 Ω (differential) system impedance. It has been shown in [9] that a 3 tap FIR filter provides sufficient performance for a wide range of optical fibre applications when combined with a DFE.

The supply voltage used for the equalizer is 1.8 V. Three analog control voltages control the gain for each of the taps. A fourth control voltage controls the common-mode voltage at the far end of the input transmission line, V_{cm}. By setting this voltage to be equal to the input common-mode voltage, no DC current flows through the input

transmission line, resulting in more constant bias voltages along the length of the transmission line.

A. Transmission Lines

A total of five lumped differential transmission lines are used in the design of this equalizer: one at the input, one at the output, and one internal to each of the three taps.

The values for the inductance L' and capacitance C' of each transmission line section are calculated to provide a characteristic impedance of 50 Ω (100 Ω differential) and a tap spacing of 25 ps (one bit period at 40 Gb/s). Since each tap delay is comprised of 6 LC-sections, the product $\sqrt{L'C'}$ must equal to one sixth of a bit period, or 4.17 ps. The resulting values of L' and C' are 209 pH and 83 fF, respectively. The node capacitances are made up purely of transistor and inductor parasitics. The inductances are spiral coils.

The input transmission line is designed to have a characteristic impedance of 50 Ω per side for matching to the 100 Ω (differential) system impedance. The inductors in each path of this differential transmission line are isolated as much as possible from one another to minimize coupling between the two paths. Using separate, isolated transmission lines ensures good differential *and* single-ended matching at the input, which is important since single-ended sources were used for testing.

The other four transmission lines are made up of coupled differential inductors which minimize both area and series loss. Differential inductors can be used for these lines even if the input is driven single-endedly because the first stage of differential pairs converts an unbalanced input into balanced differential signals.

B. Gain Cell

The gain cell is a simple differential pair, as shown in Figure 4. Six of these differential pairs make up each of the three equalizer taps. Because 40-Gb/s operation is only possible in this technology when distributed circuit techniques are used, more complicated structures such as cascodes were not an option. Cascode structures have a circuit node that is not connected to one of the transmission lines. The pole due to this node would limit the speed unacceptably for this application. The size of the gain cell devices was chosen so that the device capacitances, when added to the inductor parasitic capacitances, make up the required transmission line capacitances,
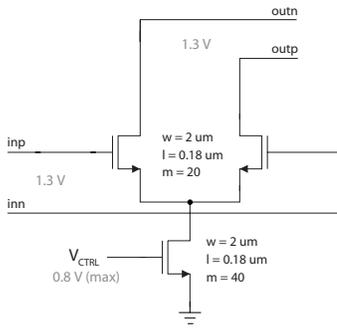
Fig. 4. Schematic of equalizer gain cell. Six of these cells are used in each tap of the equalizer.

Fig. 5. Die photo of 0.18-μm equalizer. The total area is 1 mm $\times$ 1 mm

Fig. 6. Measured tap delays with a 200 mV peak-to-peak 10 GHz sinusoidal input.

$C' = 83$fF. The gain of each of the gain cells is controlled by an analog control voltage (V_{CTRL}) that is provided off-chip. There are three control voltages, one for each tap. The control voltage for a given tap is connected to the gates of the current source transistors of each of the six differential pairs making up the tap. By varying V_{CTRL}, the currents through the differential pairs are varied, allowing control of the gain.

The maximum total current through the output stage of all three taps combined is limited to 20 mA. This is due to the restriction that the output common-mode voltage must not drop any lower than approximately 1.3 V for all transistors to remain in saturation while allowing differential signal swings in excess of 1 V_{p-p}.

Each of the three taps has a fixed polarity. The first tap is positive, the second is negative, and the third is positive. These polarities provide a high-pass response, which is typically required to equalize the generally lowpass channels. The polarities were fixed to maintain a reasonable level of gain through each equalizer tap. A Gilbert cell mixer for implementing signed tap weights is not possible since the internal circuit nodes would limit bandwidth as described above. Therefore, positive and negative tap weights would have to be implemented with two parallel gain cells connected with opposite polarity. Since the total node capacitances C' are fixed, the size of each gain cell would have to be halved, resulting in a halving of the gain. Hence, fixing the polarities provided a 6 dB increase in the maximum tap gains.

C. Circuit Layout

A die photo of the circuit layout is given in Figure 5. The overall dimensions of the equalizer IC are 1 mm $\times$ 1 mm. The active area is approximately 900 μm $\times$ 600 μm. The input pads appear on the left, the output at the top, and power and control signals at the bottom.

IV. MEASUREMENT RESULTS

All circuit measurements were made on-wafer. Figure 6 shows the tap delays measured with a 10 GHz sinusoidal input. The tap spacings are 23 ps, approximately one baud interval at 40 Gb/s. Note that the polarity of tap 2 is reversed compared with taps 1 and 3.

Figure 7 shows the magnitude and phase response of each tap measured with a two-port network analyzer. Since the measurements are single-ended, the differential gains would be 6 dB greater than shown here. The increase in tap gains near dc is due to the trans-mission lines' series losses which appear as an additional resistive load in series with the termination resistors at low frequencies. This can be compensated for by appropriately tuning the tap gains, which occurs automatically in adaptive equalizers. The phase is linear, with
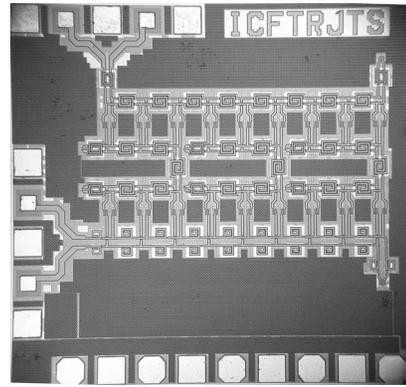
group delays differing by approximately 21 ps per tap, in general agreement with the time-domain measurements in Figure 6.

Figure 8 plots the magnitude of the input and output return loss measured with a two-port network analyzer. The input return loss was greater than 15 dB from 5 to 40 GHz while the output return loss was better than 16 dB up to 40 GHz. An input return loss as low as 10 dB is observed below 5 GHz, again due to the dc resistance of the input transmission line which appears in series with the 50 Ω terminations at low frequencies.

The filter was used to equalize 10 Gb/s PRBS $2^{31} - 1$ NRZ data transmitted over approximately 5 meters of cable. The cable had 8 dB of attenuation at one-half the bit rate (5 GHz). The tap gains were manually adjusted to open the eye at the equalizer output. No adaptation circuitry was integrated in the design. The unequalized single-ended equalizer input is shown in Figure 9a, and one-half of the fully-differential output is shown in Figure 10a.
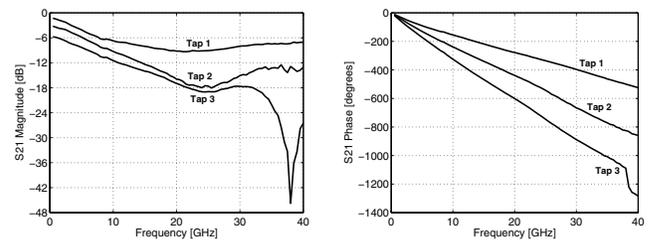

Fig. 7. Single-ended S_{21} magnitude and phase measurements made with a 2-port network analyzer. (For differential S_{21}, add 6 dB.)
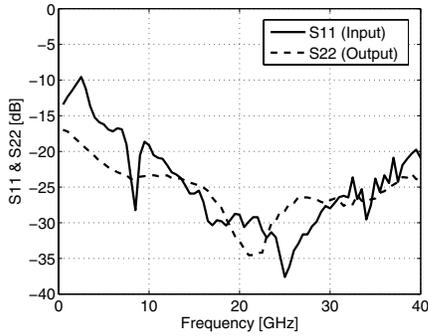
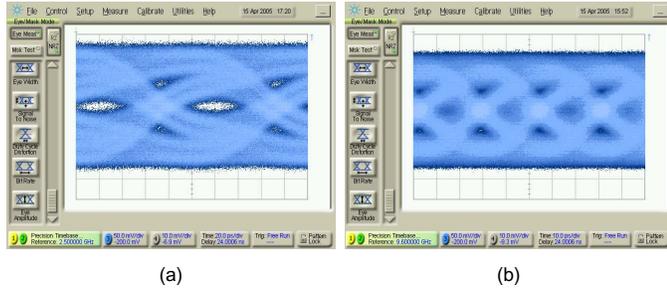Fig. 8.   Input and output return loss of the filter measured with a 2-port network analyzer.

(a)   (b)

Fig. 9.   Unequalized eye diagrams for (a) 10 Gb/s and (b) 40 Gb/s NRZ data.

Fig. 10.   Equalized eye diagrams at (a) 10 Gb/s and (b) 40 Gb/s. These are taken from one side of the differential output.

The filter was also tested with 40 Gb/s NRZ data. Figure 9b shows the unequalized filter input observed at the end of a 4 meter cable. The pattern was formed by multiplexing four independent PRBS $2^{31} - 1$ 10 Gb/s patterns.[1] The cable used for this test demonstrated 15 dB of attenuation at one-half the bit rate (20 GHz). The resulting equalized filter output is shown in Figure 10b; it has a modest eye opening that may require forward error correction for low-BER operation.

V. CONCLUSION

The bandwidth of a conventional traveling wave filter is inversely related to its tap spacing according to (1). This paper described the folded-cascade TWF topology which is capable of increasing the bandwidth beyond this limit. Transmission lines in the traveling wave filter are used to implement distributed amplifiers for each tap gain. The topology was demonstrated by implementing a 3-tap fully-differential continuous time FIR filter in 0.18 μm CMOS. The filter is capable of baud-rate linear equalization of 40 Gb/s NRZ data making it faster than any previously reported CMOS equalizer. At 70 mW it consumes less power than other 40 Gb/s equalizers implemented in more advanced technologies.

[1]There was no way to properly synchronize the 10 Gb/s patterns to produce a true PRBS output sequence, but the resulting 40 Gb/s pattern's broadband spectrum was verified on a spectrum analyzer.
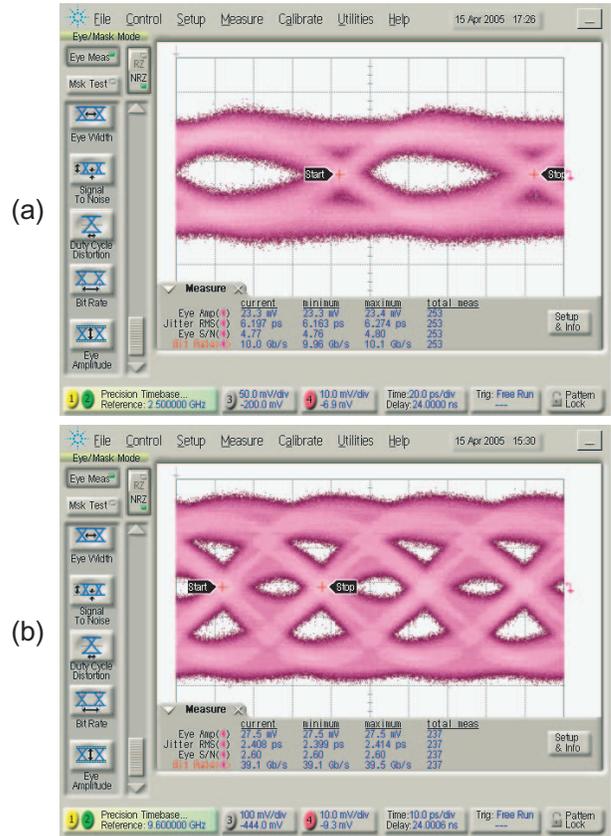
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