

A 40 Gb/s Transversal Filter in 0.18 μm CMOS Using Distributed Amplifiers

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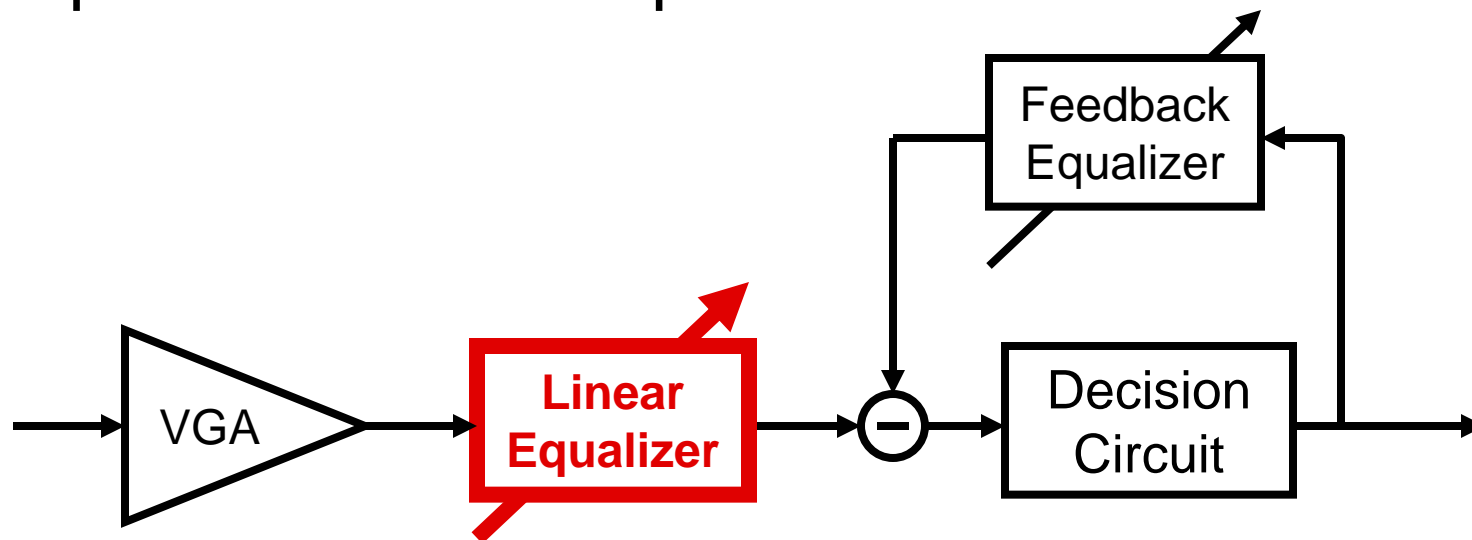
September 20, 2005

Outline

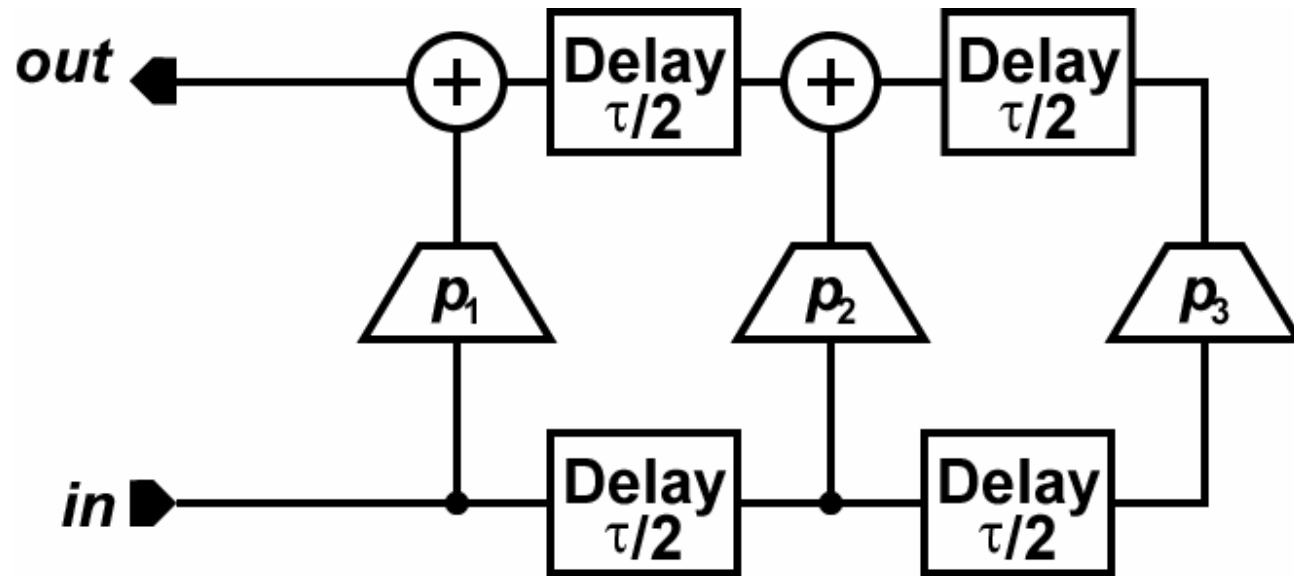
- Background on lumped-LC traveling wave filters
- “Folded-Cascade” traveling wave filter topology
- Prototype design in 0.18- μm CMOS
- Measurements
- Conclusions

Equalization

- Applications include chip-to-chip communication and optical fibre communication
- This work focuses on the programmable filter required for linear equalization in a receiver



Traveling Wave Filter



Passive implementation of the delays:

✓ Low power

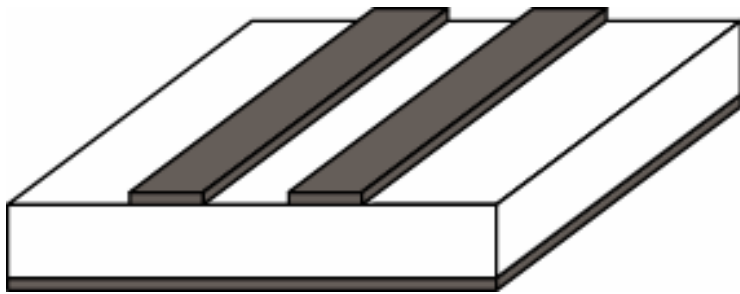
✗ High area

✓ Linear

✗ Lossy

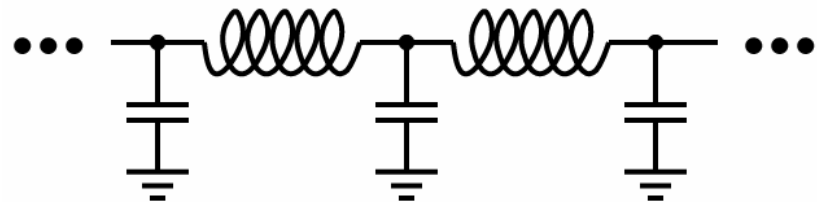
Passive Delays

Transmission lines



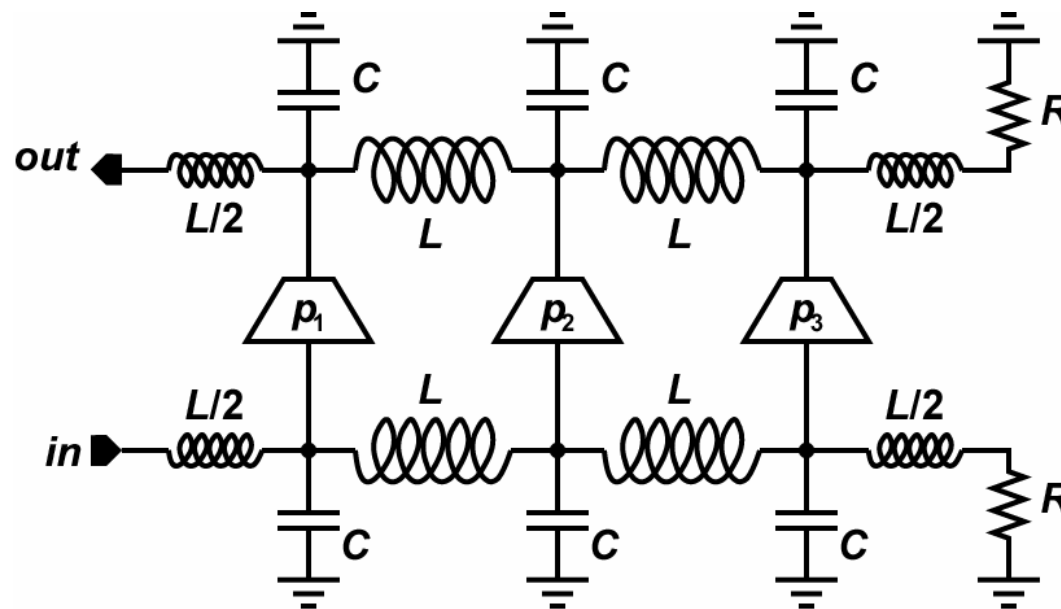
- Several mm needed to achieve the required delays
- ✗ Large area

Lumped-LC



- Forms a lowpass network
- ✗ Limited bandwidth

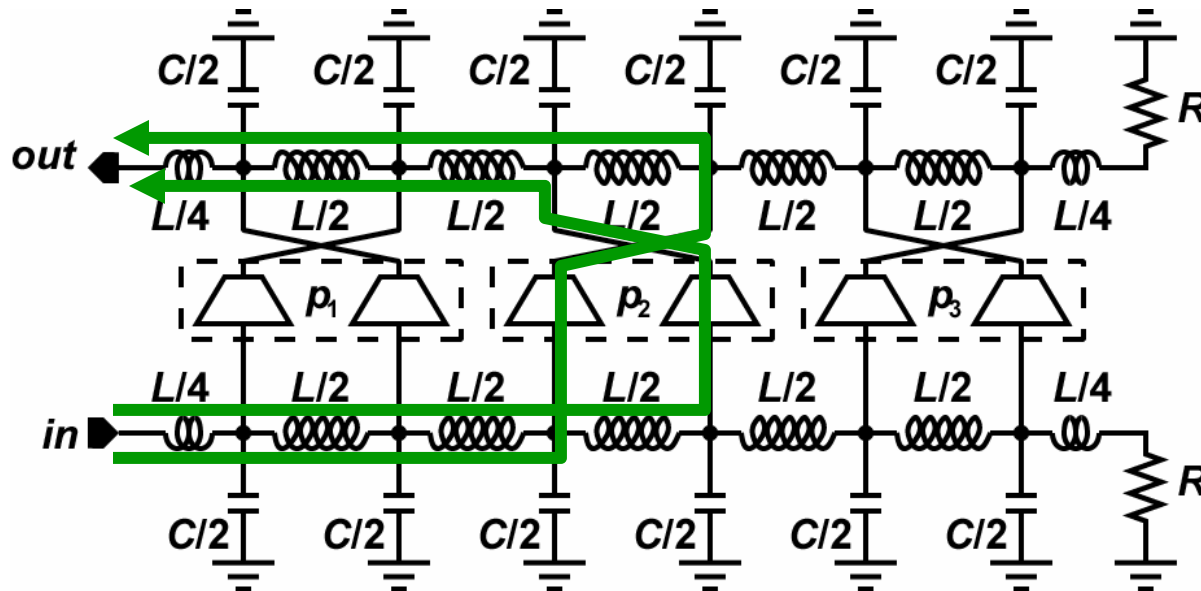
3-Tap Traveling Wave Filter



$$\text{Tap spacing : } \tau = 2\sqrt{LC}$$

$$\text{Delay Line Bandwidth : } f_{3\text{dB}} = \frac{1}{\pi\sqrt{LC}} = \frac{2}{\pi\tau}$$

3-Tap Crossover TWF

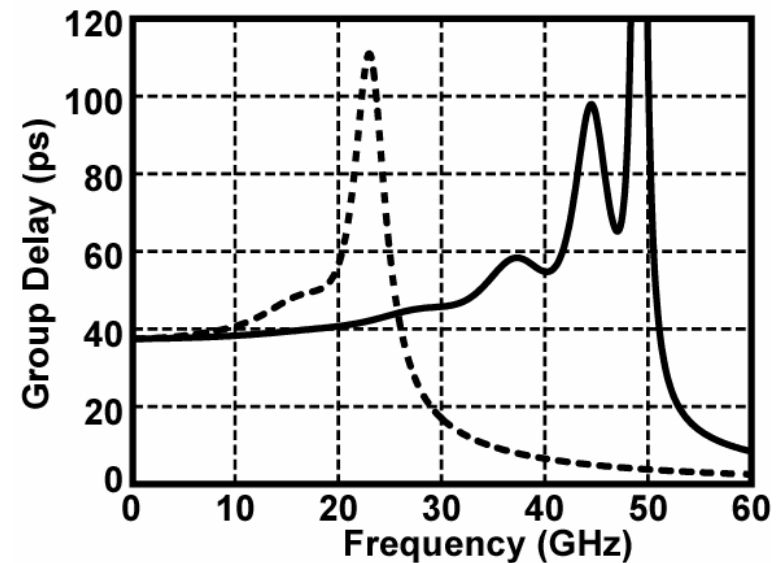
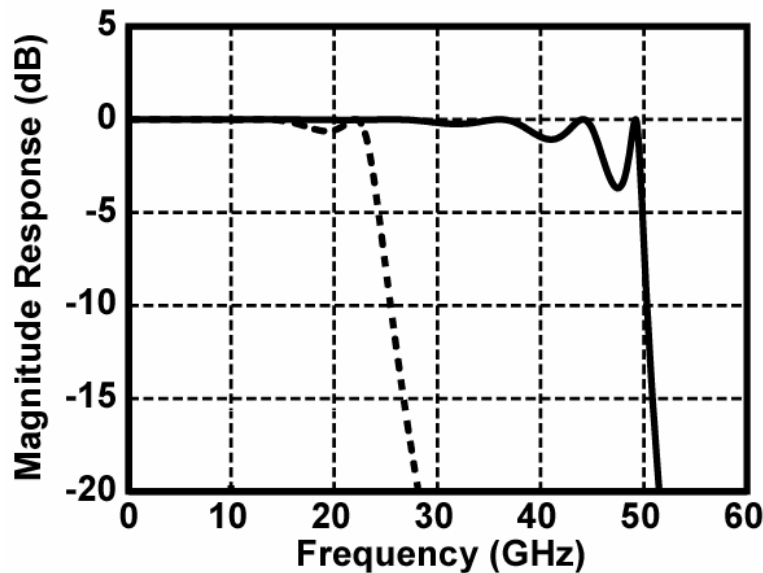


$$\text{Tap spacing : } \tau = 2\sqrt{LC}$$

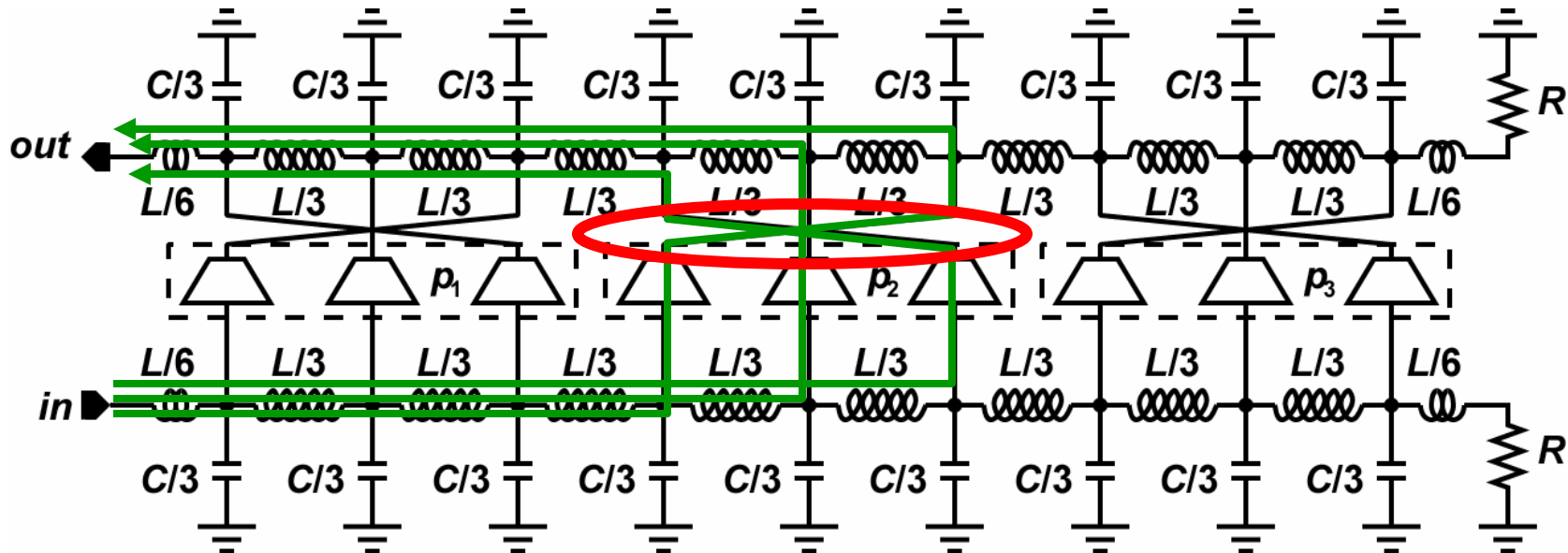
$$\text{Delay Line Bandwidth : } f_{3\text{dB}} = \frac{2}{\pi\sqrt{LC}} = \frac{4}{\pi\tau}$$

LC-delay line bandwidth

- The 6-section delay line has twice the bandwidth of the 3-section delay line for the same total delay

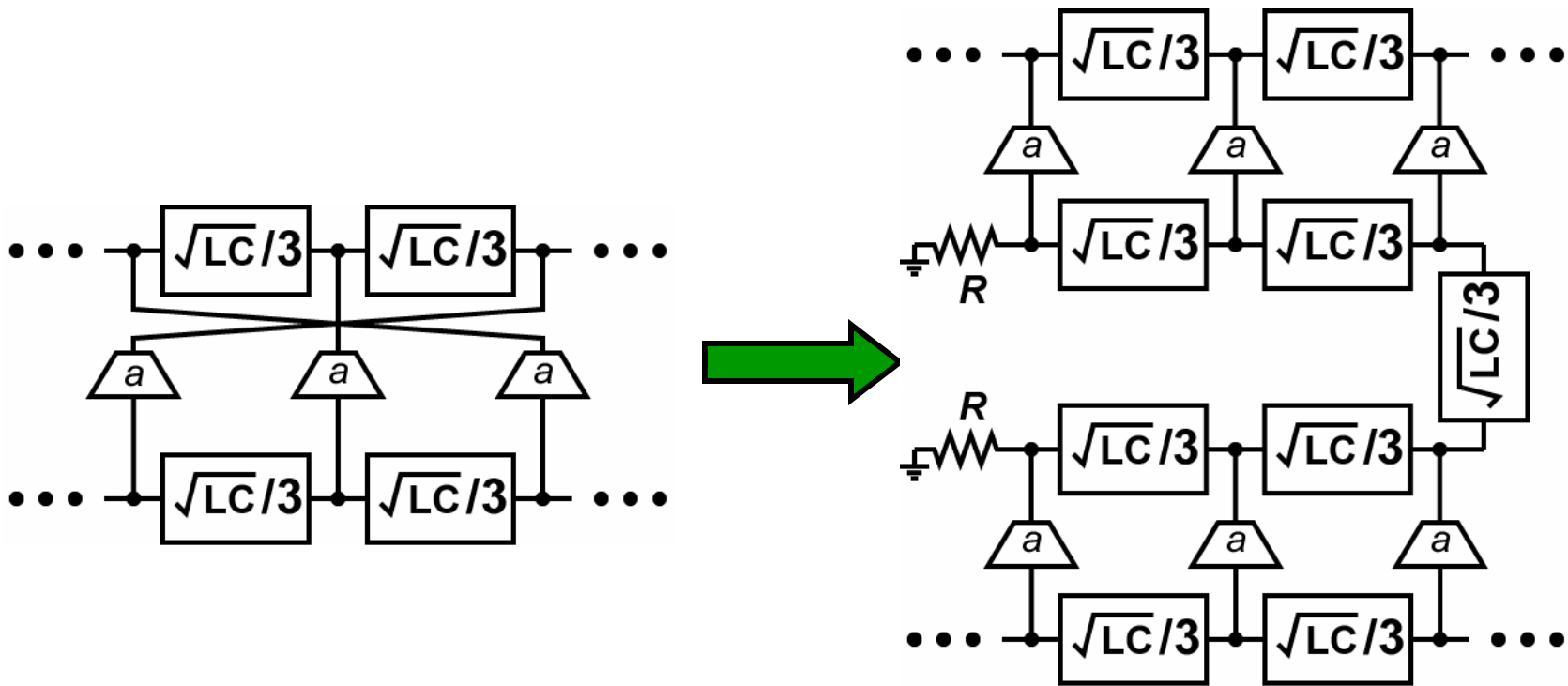


3-Tap Crossover TWF



- **Problem:** The crossover routing could introduce skew and crosstalk between paths that must be matched

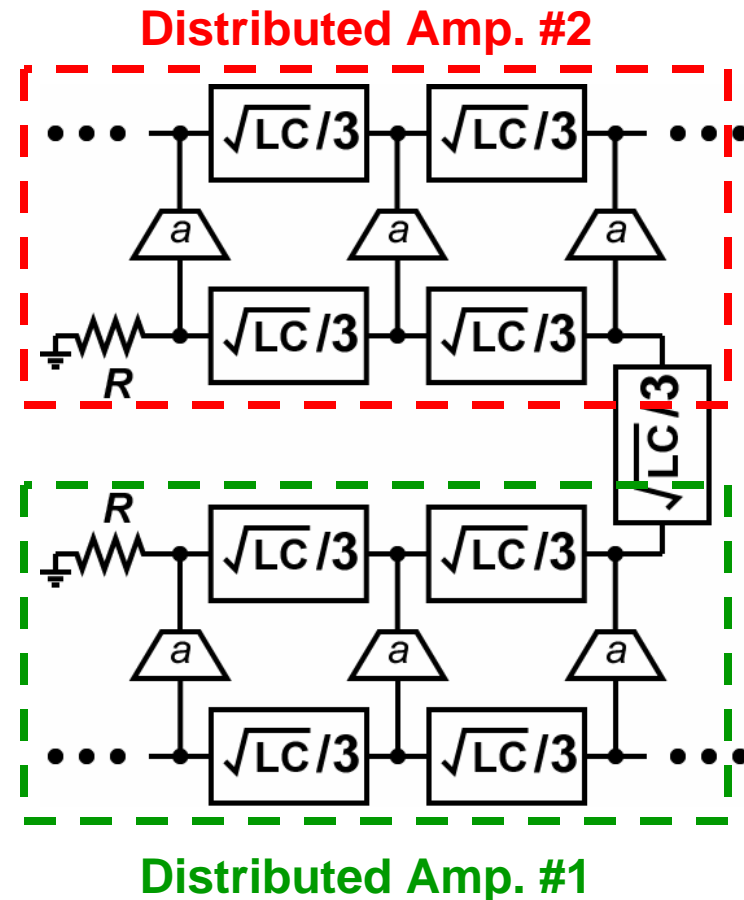
Folded-Cascade TWF



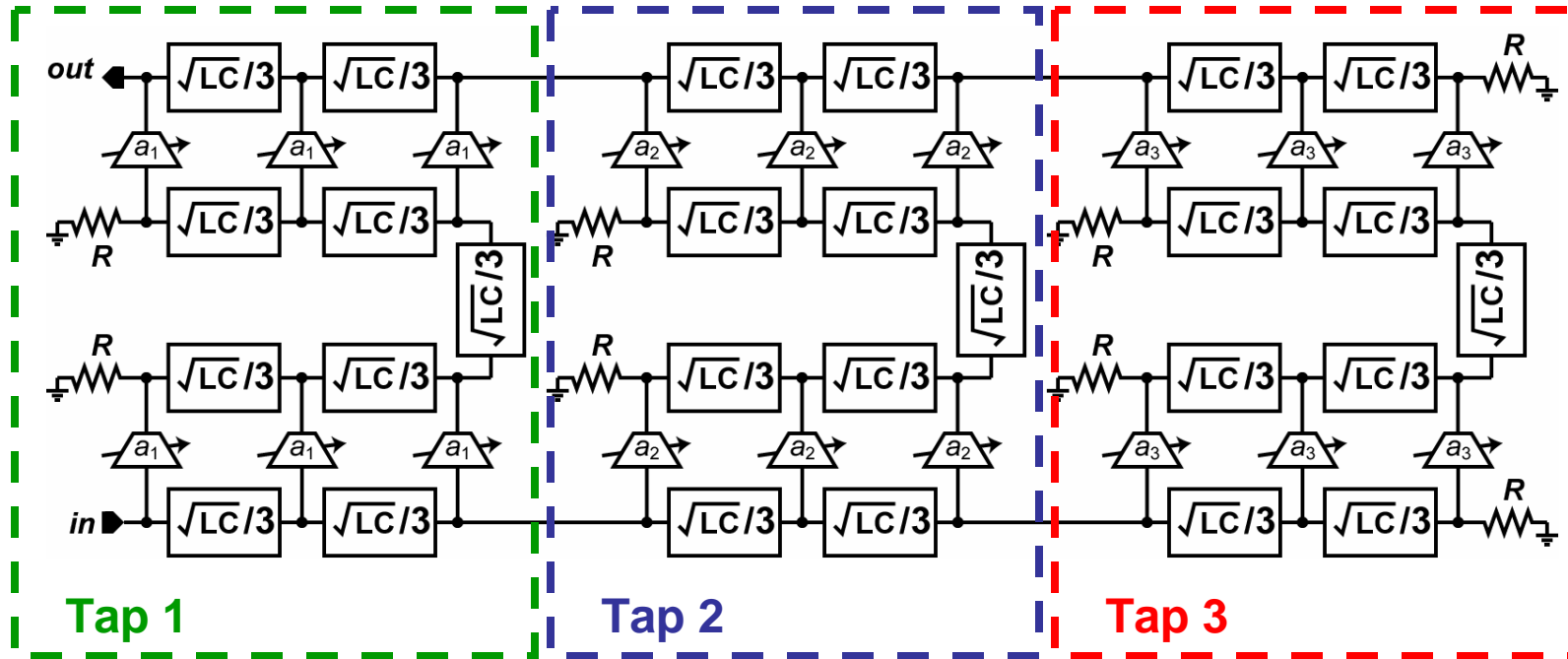
- **Solution:** Alleviate crossover routing by introducing an intermediate “folded” transmission line

Folded-Cascade TWF

- **Alternate interpretation:**
This is a cascade of 2 distributed amplifiers
- Each has a gain of $3a$ (assuming lossless delay elements)
- Total gain is $9a^2$



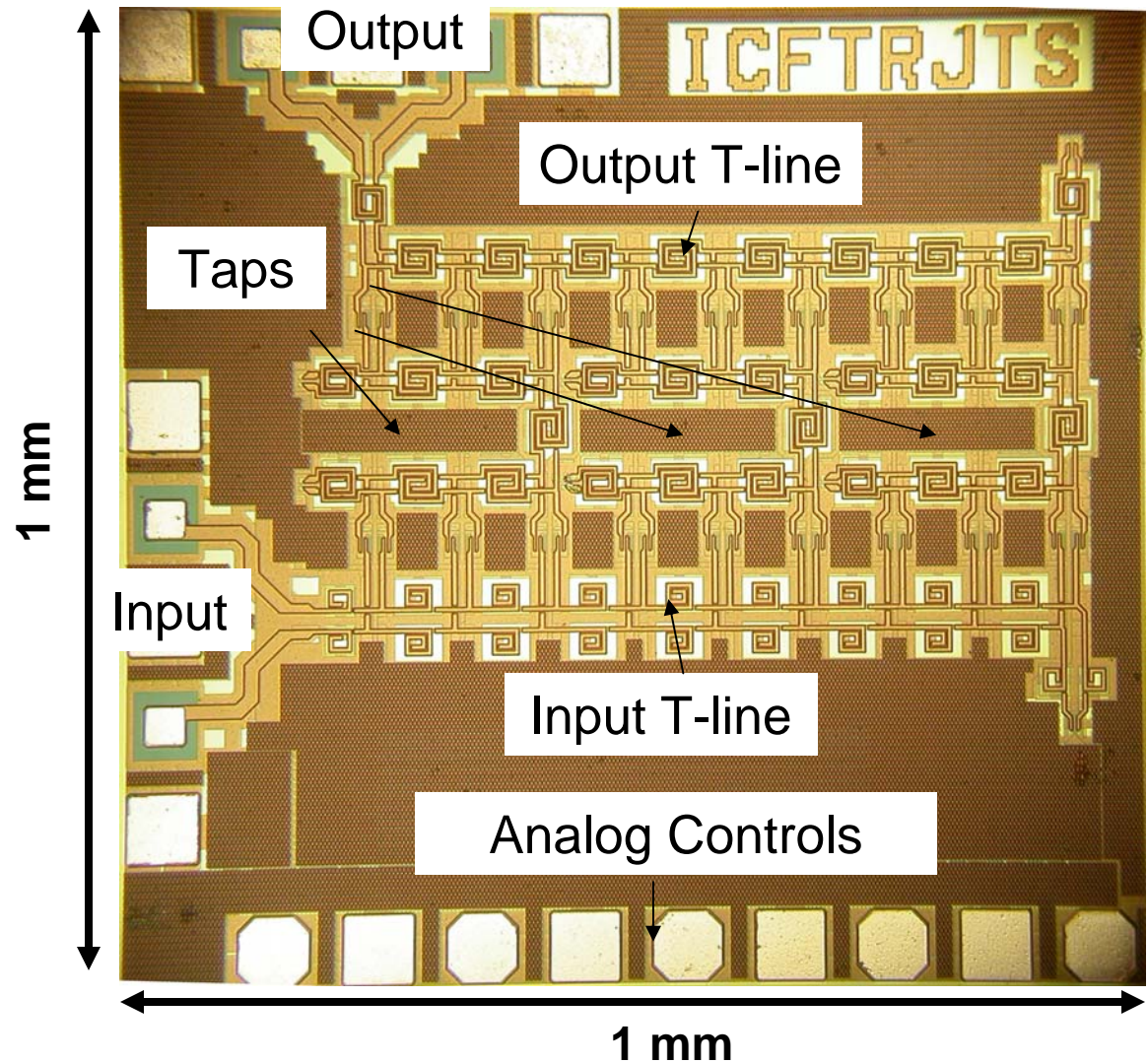
3-Tap Folded-Cascade TWF



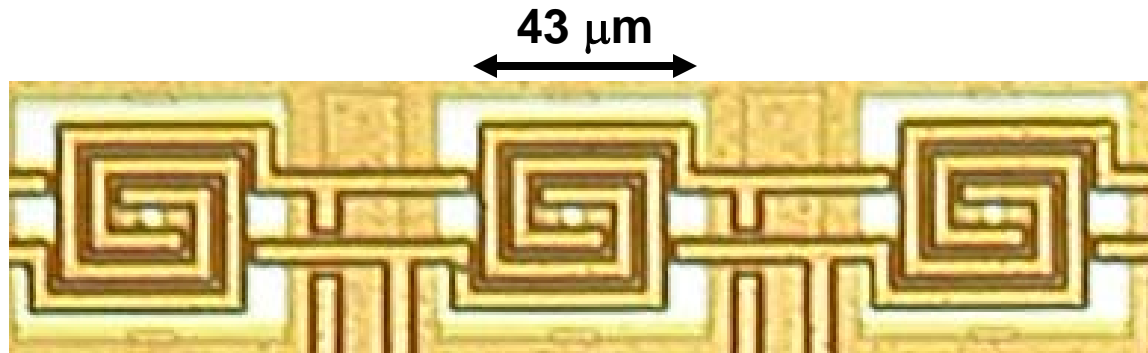
- Example: 3-tap FIR filter

3-Tap Folded-Cascade TWF

- 0.18 μm CMOS ($f_T = 45$ GHz)
- 3-tap filter
- Fully differential
- Analog control of tap weights
- 70 mW from a 1.8 V supply

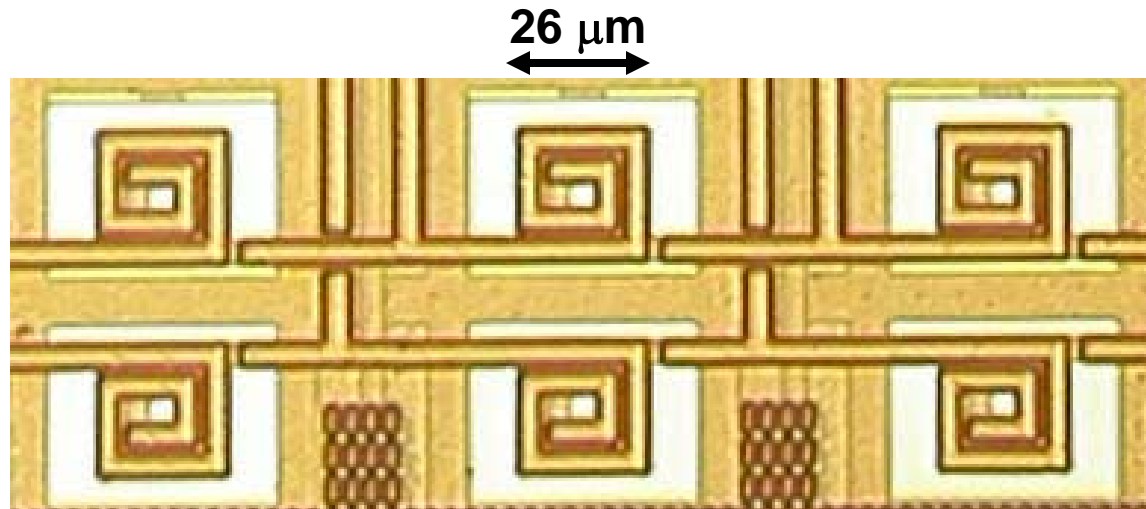


Passive Delay Line



- Differential spiral inductor, $L/3 \approx 210$ pH (per side)
- Capacitance, $C/3 \approx 80$ fF (per side), consisting of device and routing parasitic capacitances
 - Nominal tap spacing of 25 ps
 - Differential characteristic impedance, $Z_0 \approx 100$ Ohms
 - Terminated by two 50-Ohm resistors to V_{DD}

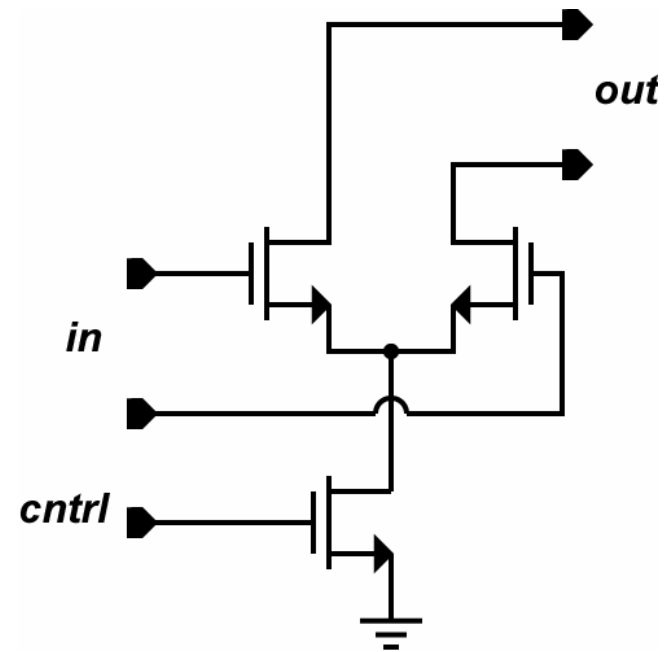
Input Delay Line



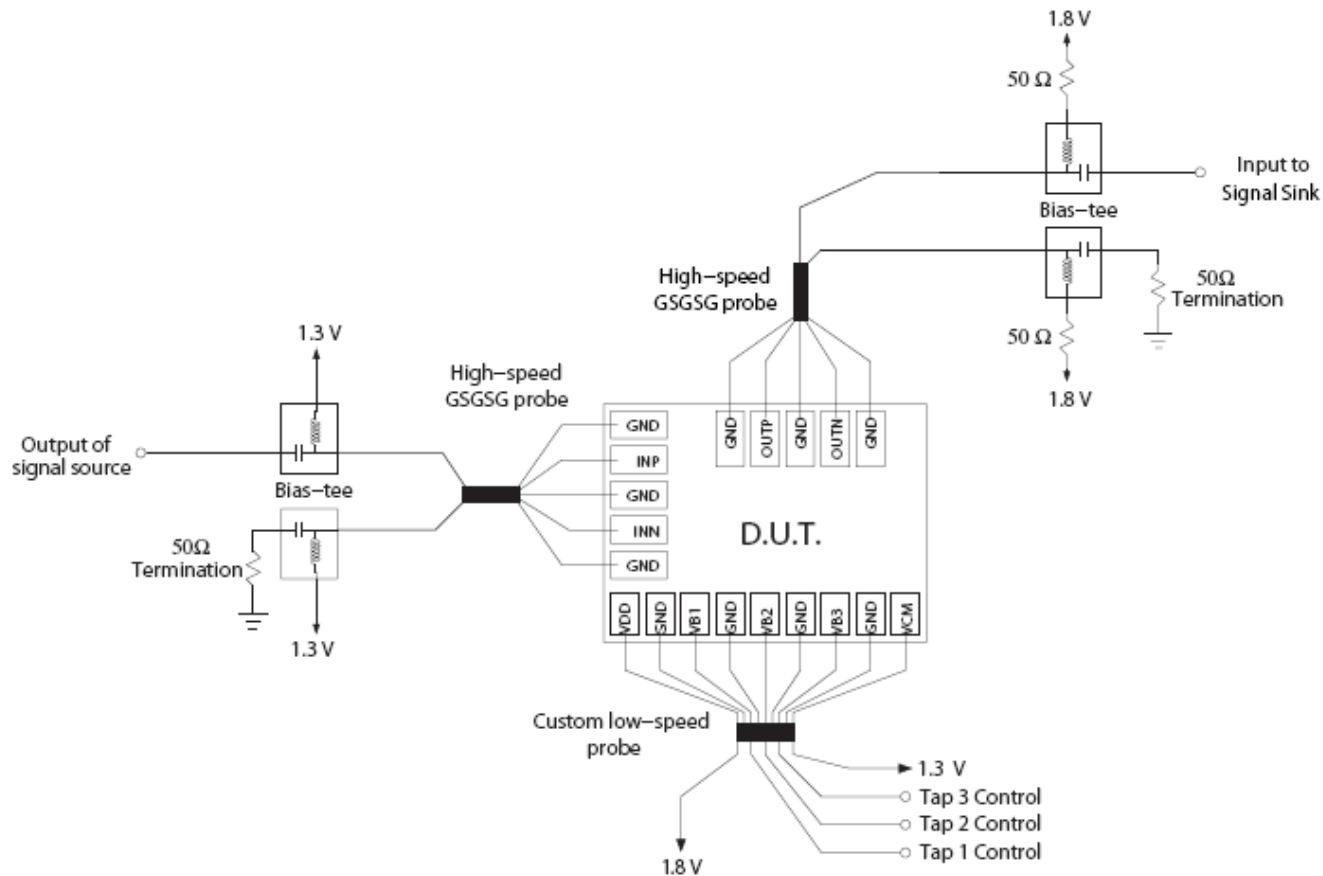
- The input delay line had to be compatible with single-ended testing
 - Two single-ended delay lines; no coupled spirals

Tap amplifiers

- Each tap amplifier is a simple differential pair
- The tail currents (hence, tap gains) are controlled by 3 external analog control voltages

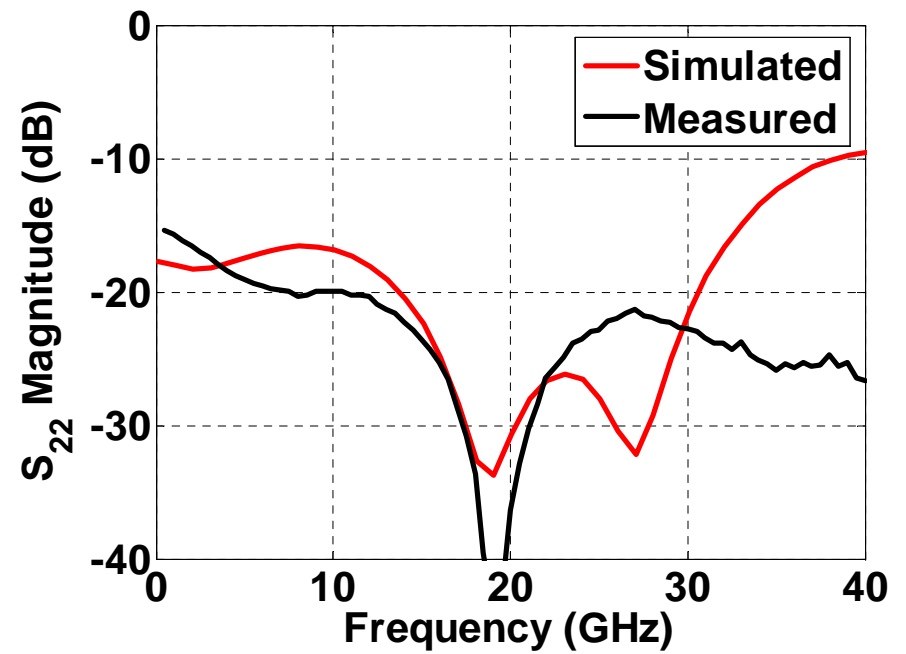
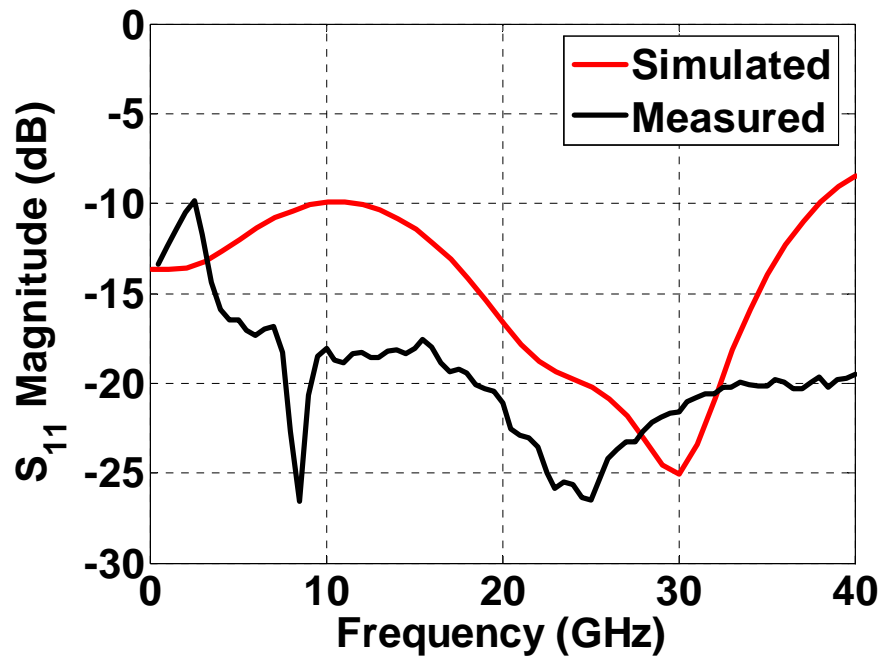


On-wafer Test Setup

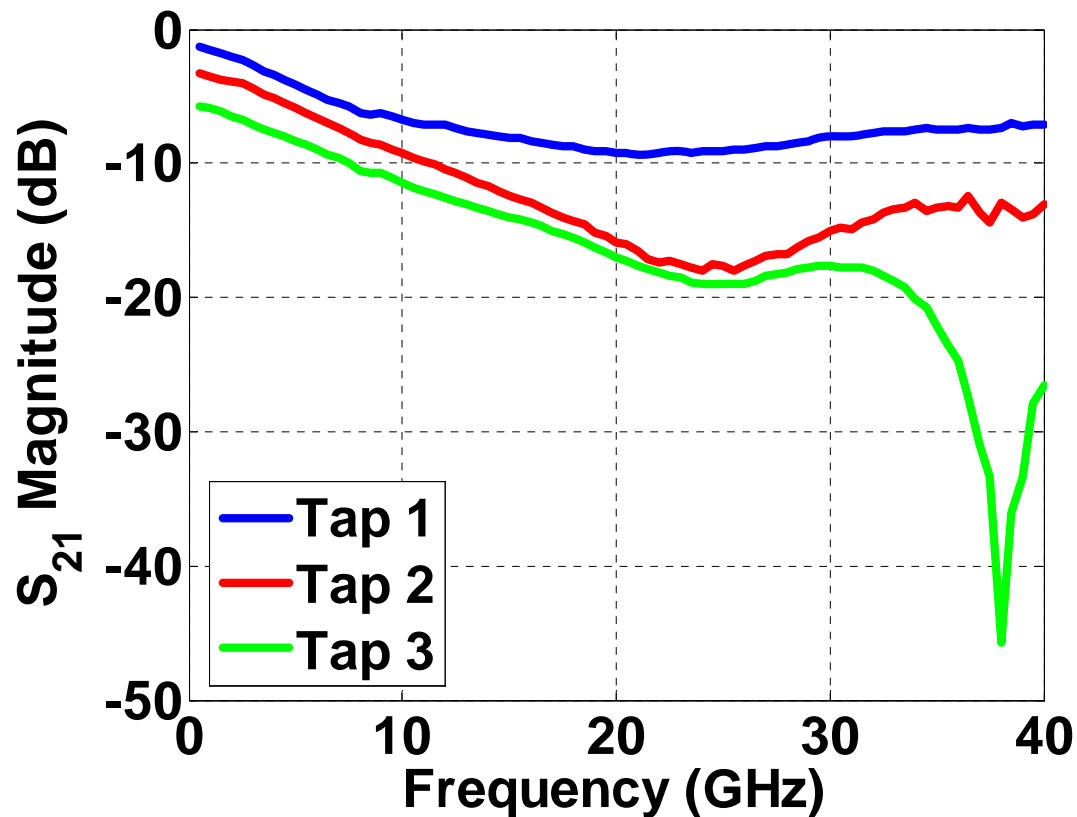


Note: 6 dB loss introduced due to single-ended testing

Input and Output Matching

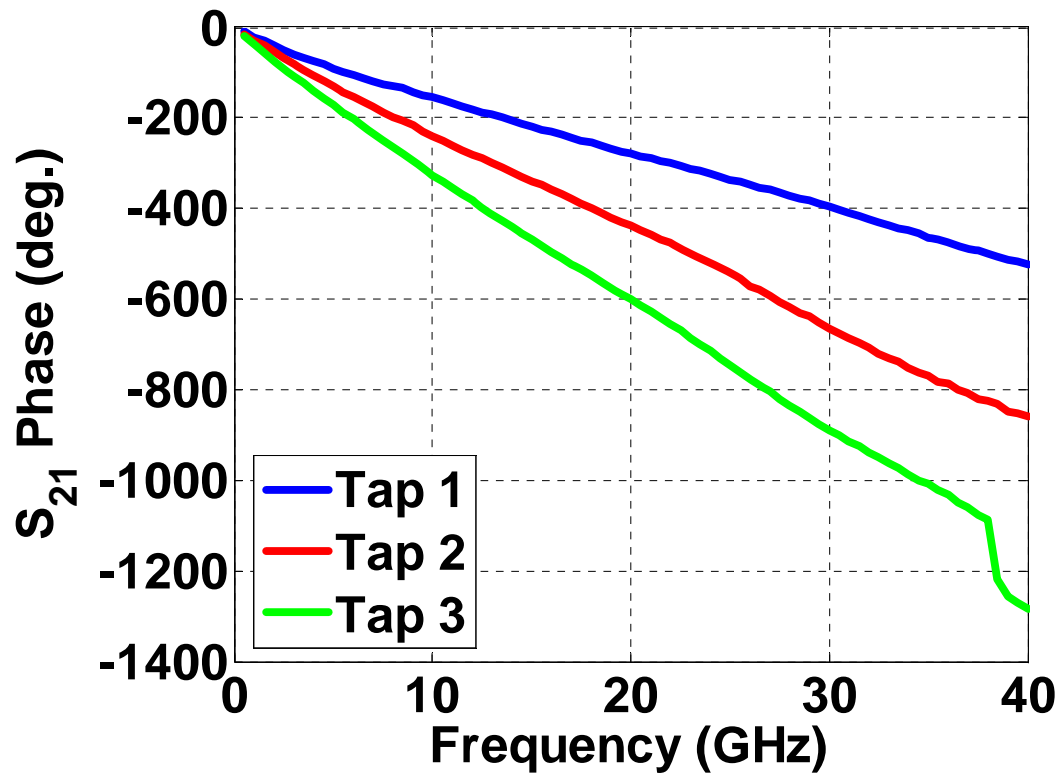


Tap Frequency Response



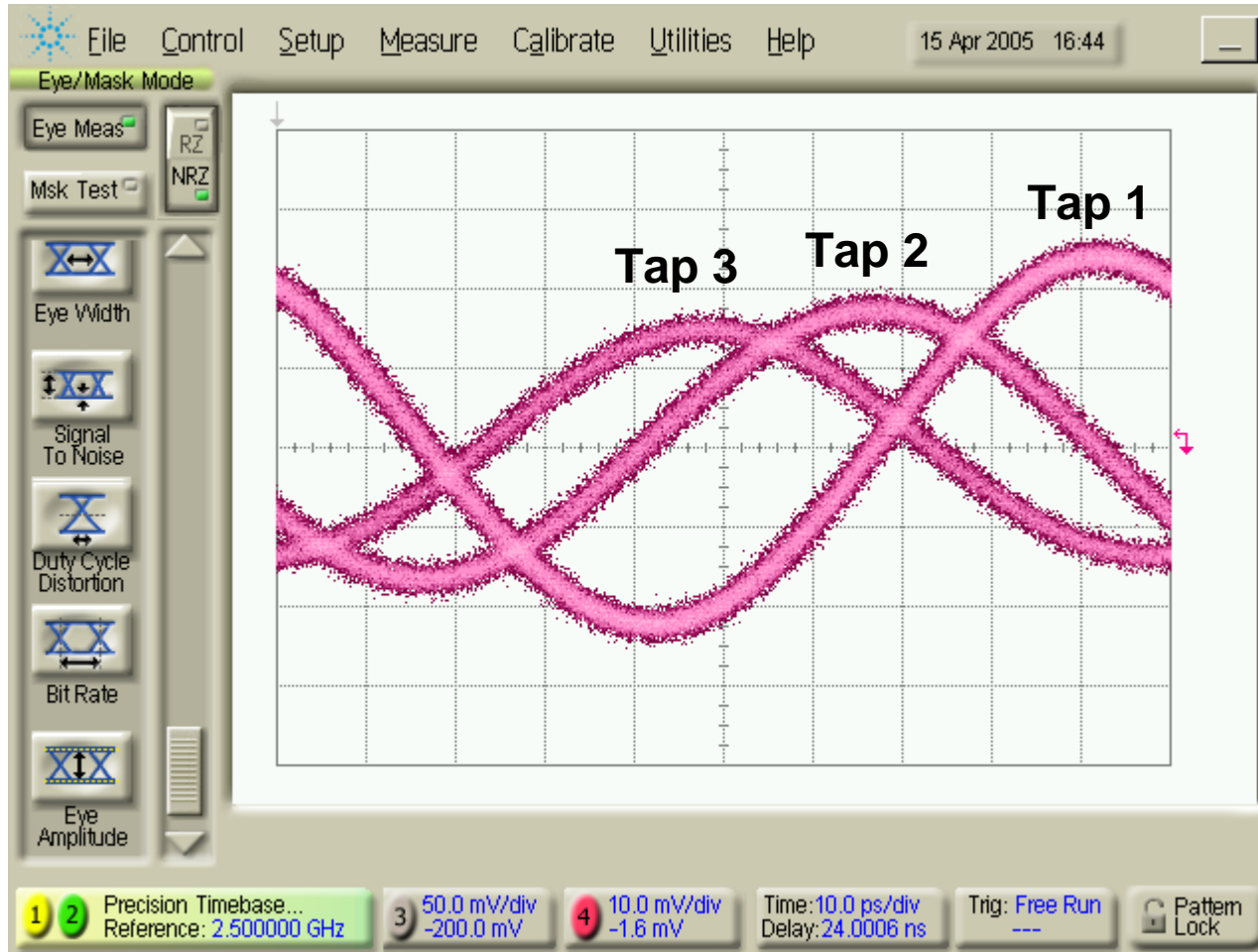
- Single ended measurements made with a 2-port network analyzer
- Differential measurements would be +6 dB greater

Tap Frequency Response



- The slope of the phase response corresponds to a tap spacing of approx. 25 ps

10 GHz Sinusoidal Response

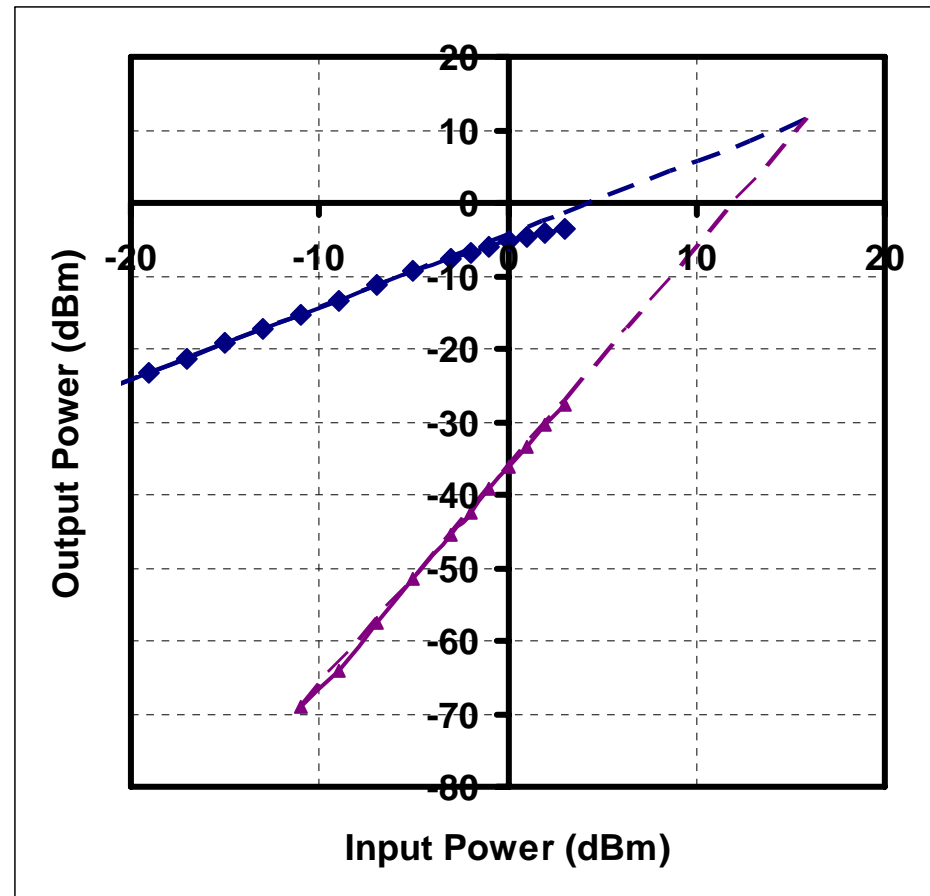


Delay per tap is approximately
 $25 \text{ ps} = 1 \text{ UI}$
at 40 Gb/s

Note: Polarity of tap 2 is always reversed with respect to taps 1 and 3

Linearity Measurements

- Example:
 - 2 GHz input sinusoid
 - Tap 1 only turned on with maximum gain
 - Single-ended testing
- Input 1 dB compression: 0 dBm
- IIP_3 : 15.8 dBm
- THD at 0 dBm input: -31.1 dB

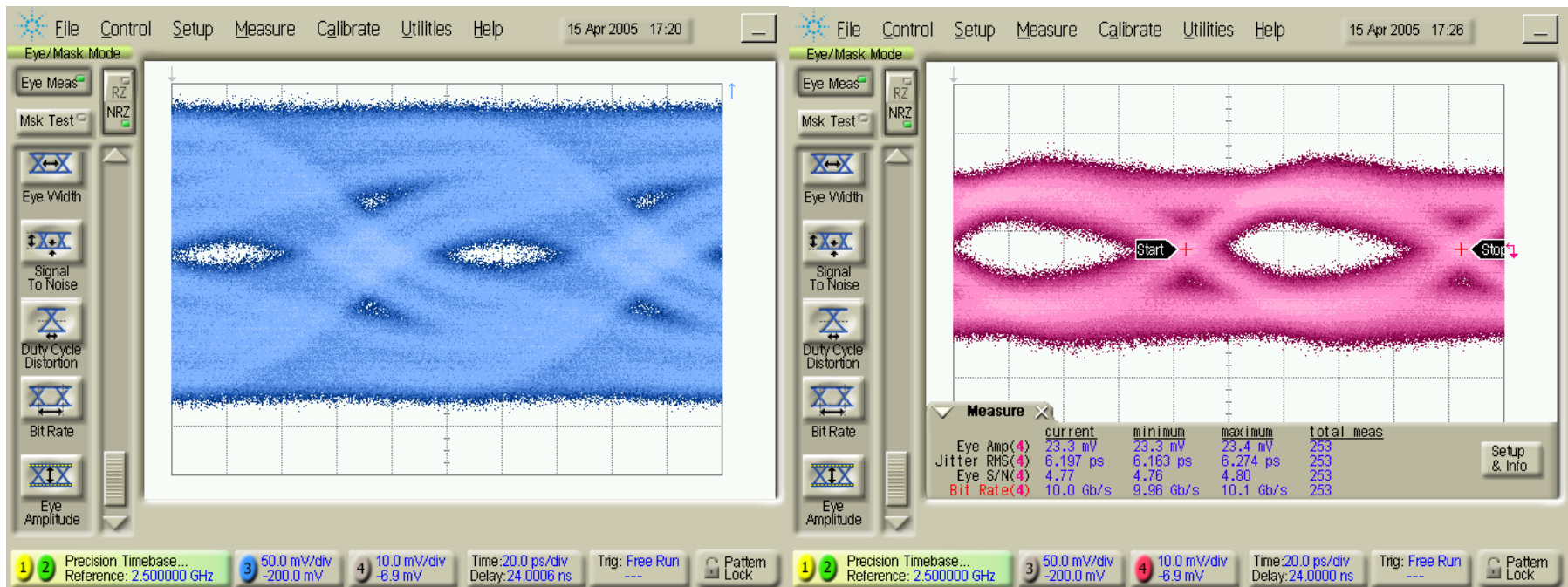


Linearity Measurements: Summary

All measurements at 2 GHz input frequency:

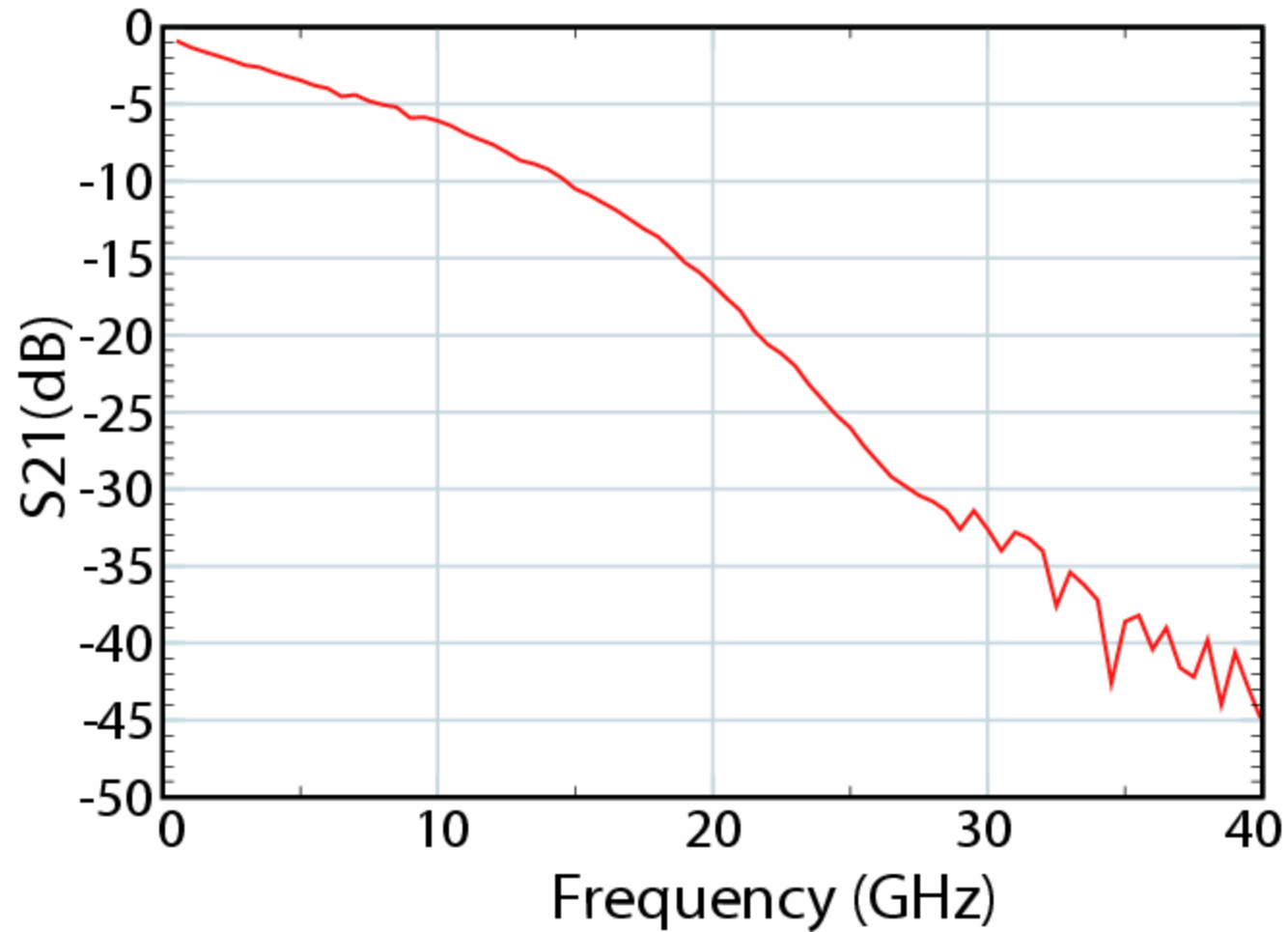
	Tap 1	Tap 2	Tap 3
Input 1 dB Compression	0.0 dBm	1.5 dBm	2.5 dBm
IIP ₃	15.8 dBm	17.0 dBm	18.3 dBm
THD at 0 dBm input power	-31.1 dB	-30.5 dB	-34.9 dB

10 Gb/s Measurements

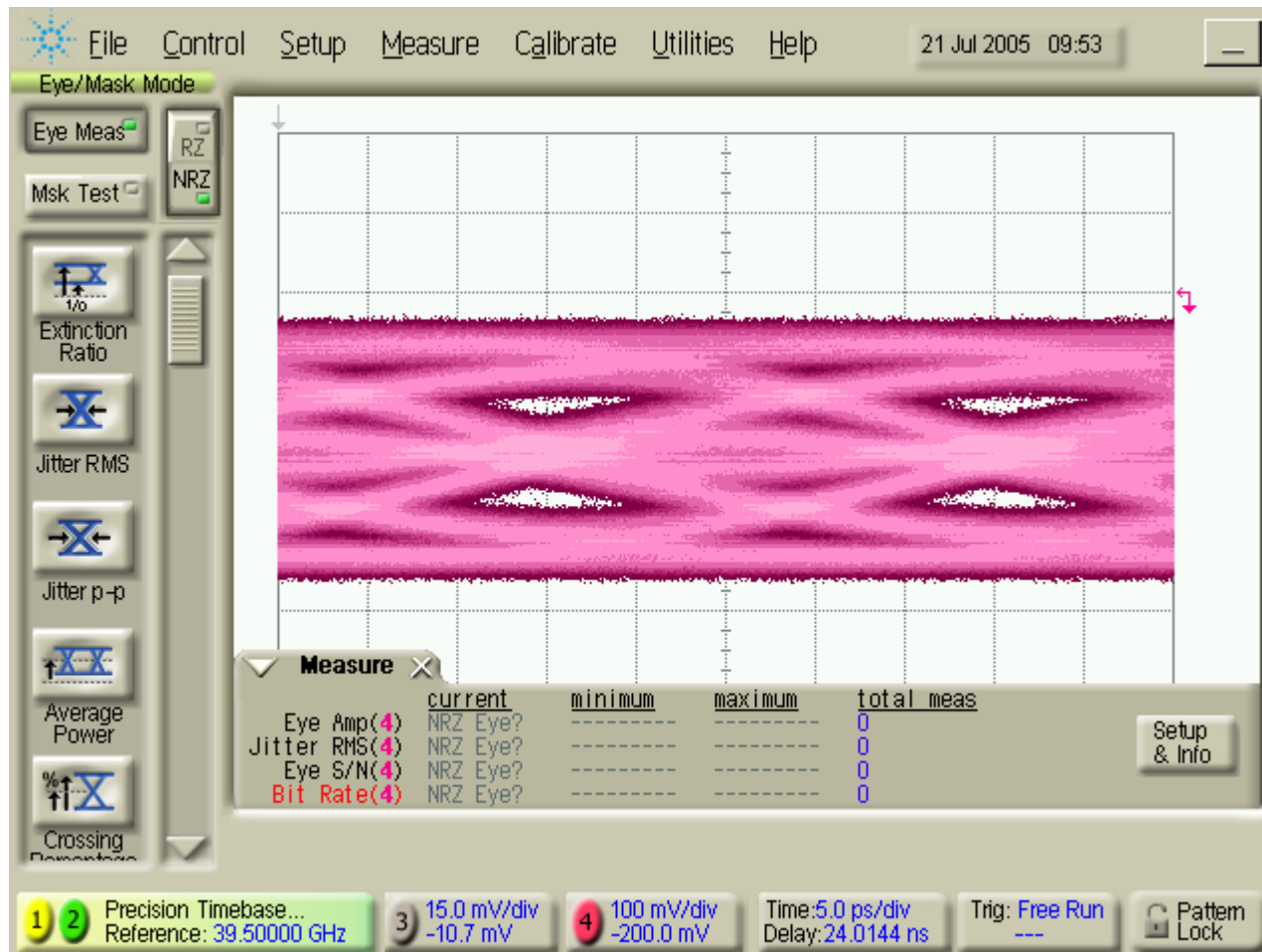


- Equalization over 5 meters of coaxial cable (8 dB loss at 5 GHz)

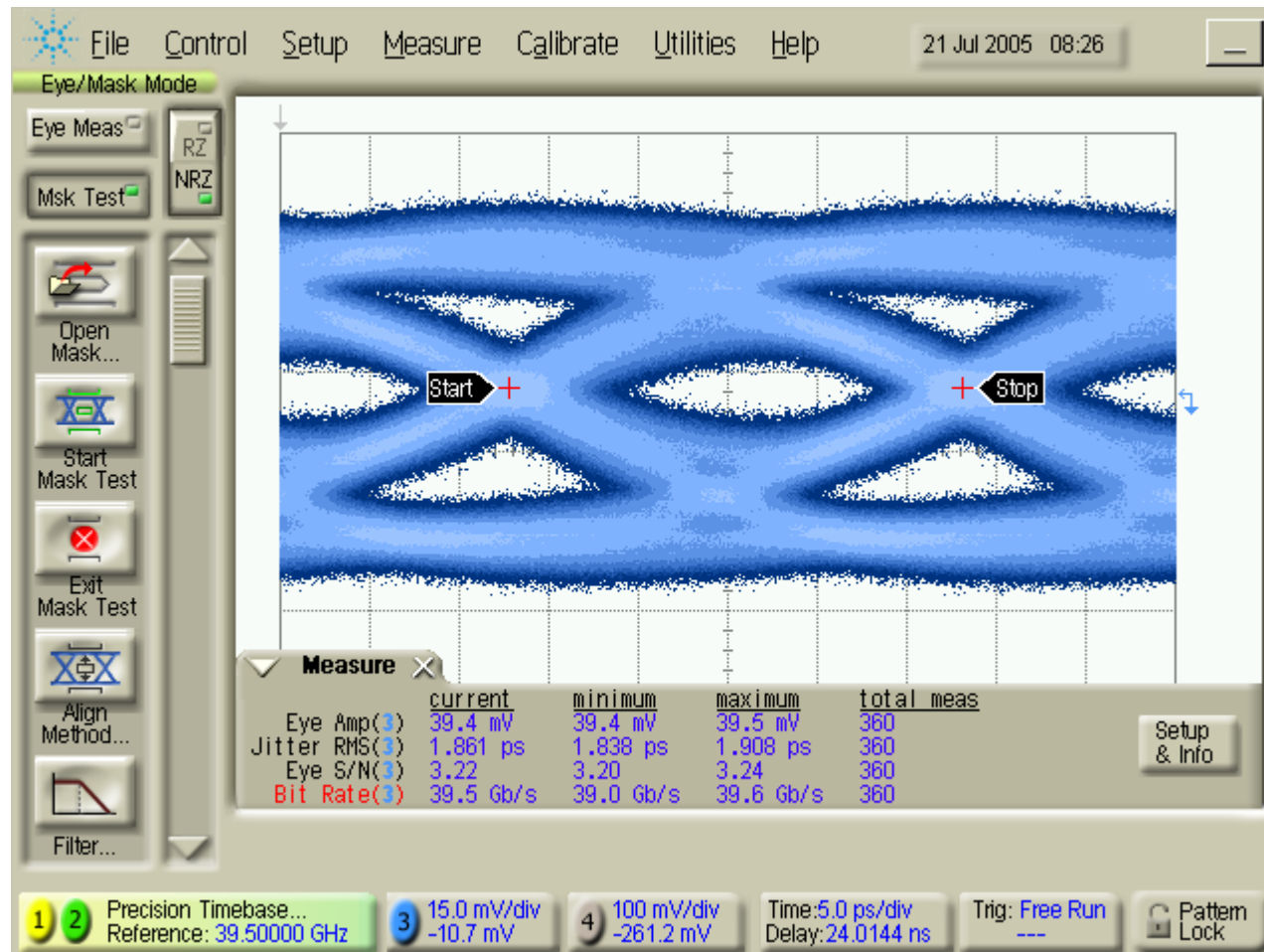
39.5 Gb/s Measurements: Channel response



39.5 Gb/s Measurements: Input Eye Diagram



39.5 Gb/s Measurements: Output Eye Diagram



Conclusions

- A folded-cascade traveling wave filter topology was introduced to increase the bandwidth of traditional traveling wave filters that use lumped-LC delay lines
- The passive LC-sections required to provide delay in the FIR filter are also used as part of distributed amplifiers
- The topology was demonstrated in a 3-tap 0.18 μm CMOS filter capable of equalization up to 40 Gb/s (the fastest known CMOS FIR filter to date)

Acknowledgements

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